Technologies of Cascaded H-Bridge Battery Energy Storage System

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Abstract

In recent years, the significant increase in the penetration of renewable energy sources, such as photovoltaic wind power, has challenged the safe and stable operation of the power grid. Therefore, a large number of Battery Energy Storage Systems (BESS) are connected to the power grid, mainly used to improve the grid's frequency regulation and voltage regulation capabilities.

The Cascaded H-bridge (CHB) topology of Power Conversion System (PCS) can connect low-voltage DC components directly to medium-voltage grid or even high-voltage grid, without a power transformer. Due to the high number of voltage levels in the cascaded topology, the equivalent switching frequency is high and thus the system output waveform is more satisfactory. In addition, CHB-PCS has the advantages of modularity and high scalability, so this topology scheme is very promising and has received widespread attention.

However, BESS based on CHB-PCS (CHB-BESS) faces the issue of inter-phase SOC imbalance. The conventional zero-sequence voltage injection strategy is inefficient when DC-side voltage is insufficient. To address this issue, an innovative self-adaptive inter-phase SOC balancing control strategy is proposed. In this strategy, injecting a three-phase common-mode max-min average signal significantly reduces the modulation voltage magnitude by 13.4%, thereby allowing for a remarkable increase in the injected zero-sequence voltage magnitude. This strategy dynamically adjusts the injected zero-sequence voltage amplitude and phase based on the real-time state of CHB-BESS. It optimally utilizes the DC-side voltage while avoiding overmodulation and remains effective even when conventional strategies are inefficient. To validate the effectiveness of this strategy, a 10kV 5MW/11.2MWh BESS was designed, and simulation was conducted using Matlab/Simulink for various operating conditions within its power capability. The results indicate that this strategy does not affect the

output power quality of the BESS. Moreover, it maintains satisfactory balancing efficiency even when the DC-side voltage is not abundant.

Moreover, due to the large number of sub-modules and thus the increased probability of sub-module failures, CHB-BESS needs to have a certain degree of fault-tolerance to improve system reliability. this research proposes an innovative fault-tolerance strategy for CHB-BESS to operate under fault conditions with power balance among all submodules and without voltage overmodulation. Theoretical analyses show that the modulation voltage amplitude of the new strategy is significantly lower than that of the conventional strategy when coping with the same fault and exhibits a wider range of applicability. Simulation results based on 6kV 2MW/6.72MWh CHB-BESS and a 10kV 5.5MW/11.2MWh CHB-BESS in Matlab/Simulink confirm that, under various operating conditions, the proposed solution exhibits negligible differences in output power quality compared to the conventional method. Compared with the conventional approach, the new strategy has significantly enhanced sub-module power equalization capability, demonstrating superior efficiency and applicability.

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List of Abbreviations

AC	Alternative Current
AEM	Area Equalization Modulation
AGC	Automatic Generation Control
ASAM	Asymmetric Switching Angle Modulation
AVC	Automatic Voltage Control
BESS	Battery Energy Storage System
BMS	Battery Management System
CHB-BESS	Cascaded H-Bridge BESS
CHB-PCS	Cascaded H-Bridge PCS
CHB-SVG	Cascaded H-Bridge Static Var Generator
DC	Direct Current
DSP	Digital Signal Processor
EMS	Energy Management System
FCS-MPC	Finite Control Set Model Predictive Control
FD	Freewheeling Diode
FDCT	Flexible DC Transmission
FFM	Fundamental Frequency Modulation
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
INLM	Improved Nearest Level Modulation
LS-PWM	Carrier Level-Shifted Pulse Width Modulation
MMC-BESS	Modular Multilevel Converter BESS
MMC-PCS	Modular Multilevel Converter PCS
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVC	Modulation Voltage Clapping
NLM	Nearest Level Modulation
PCS	Power Conversion System
PLL	Phase Locking Loop

PS-MPC	Sequential Phase-Shifted Model Predictive Control
PS-PWM	Phase-Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
SHE-PWM	Selective Harmonic Elimination Pulse Width Modulation
SOC	State of Charge
SOH	State of Health
SSAM	Symmetric Switching Angle Modulation
SVG	Static Var Generator
SV-PWM	Space Vector Pulse Width Modulation
S-WM	Staircase Wave Modulation
THD	Total Harmonic Distortion

Attestation

‘I hereby declare that this submission is my work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for qualification of any other degree or diploma of a university or other institution of higher learning, except where due acknowledgement is made in the acknowledgements.’

Xiaobin Wang

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Chapter 1

Introduction

1.1 Background

In recent years, the Battery Energy Storage Systems (BESS) industry has gained widespread attention and is rapidly developing. Many BESSes are connected to the power grid and are mainly used to improve the grid's frequency and voltage regulation capabilities. Popular renewable energy sources, such as wind and photovoltaic power plants, have significantly reduced carbon emissions in the power production process. However, the power grid's power and voltage regulation capabilities have been weakened. This is mainly due to the intermittent and fluctuating nature of the output of photovoltaic and wind power, and thus, it is impractical to control their output to match the real-time demand of loads. In addition, variations in the output of such renewable energy sources cause voltage fluctuations in the grid, affecting power quality. Accordingly, a sufficient scale of energy storage systems should be integrated into power grids to tackle these problems. Compared with traditional pumped storage, BESS has gained wide application because of its easy siting, short construction period and fast corresponding speed.

Nowadays, BESS has received widespread attention as an important means to break through the bottleneck of new energy applications, and its application scenarios involve nearly all aspects of power generation, transmission, distribution and consumption. Specifically, in the electricity power industry, BESS mainly has the following application scenarios [1]:

- Constructed with a photovoltaic power station or wind power station to smooth the new energy output and reduce wind and radiation rejection, provide inertia response and suppress low-frequency oscillation, and respond to the commands

from Automatic Generation Control (AGC) system and Automatic Voltage Control (AVC) system.

- Traditional coal-fired frequency-regulation power plants are equipped with BESS to increase the speed and accuracy of response to frequency fluctuation and AGC commands and reduce life time loss of water vapor valves, boilers and other relevant mechanical components [2]. Figure 1.1 shows a 20MW/10MWh BESS constructed at a 600MW coal-fired power plant to improve frequency regulation quality.
- Constructed independently and connected to the grid to reduce frequency fluctuation, provide AGC and AVC services, and serve as a black start power supply[1].
- Constructed on the load side to take advantage of the peak and valley tariff difference to reduce the cost of electricity consumption or participate in demand-side response for profits.

Figure 1.1 Construction of a 20MW/10MWh BESS at a 600MW coal-fired power plant to improve frequency regulation quality.

[1] Black start is the ability of generation to restart parts of the power system to recover from a blackout.

Compared with lead acid and flow batteries, lithium batteries are predominately applied in BESS due to many advantages, such as high power density, long lifespan, fast charging and discharging, and high efficiency. Therefore, unless otherwise noted, BESS hereinafter refers exclusively to lithium battery-based systems.

Although this thesis does not focus on the design of BESS, a brief introduction to the system is necessary. A BESS mainly consists of battery stacks, a Battery Management System (BMS), a Power Conversion System (PCS), an Energy Management System (EMS) and a transformer, which can be seen in Figure 1.2. From the perspective of costs, the most essential part is battery stacks, as shown in Figure 1.3. Many battery cells are connected mainly in series to form a pack, and several packs constitute a battery cluster. BMS is mainly used to measure the voltages, currents and temperatures of batteries, calculate State of Charge (SOC) and balance the SOC of cells.

Sometimes, a power transformer connects a BESS to a power grid, boosting AC voltages and suppressing harmonics. PCS is the bridge between AC and DC circuits. Although the cost of PCS is decreasing with the development and application of power electronic components, from a technical point of view, it determines BESS's output power quality and characteristics. It primarily affects the service life and safety of the battery cells. Some auxiliary equipment, such as metal containers, fire detection and suppression systems, lighting systems, and air conditioning systems, are also indispensable.

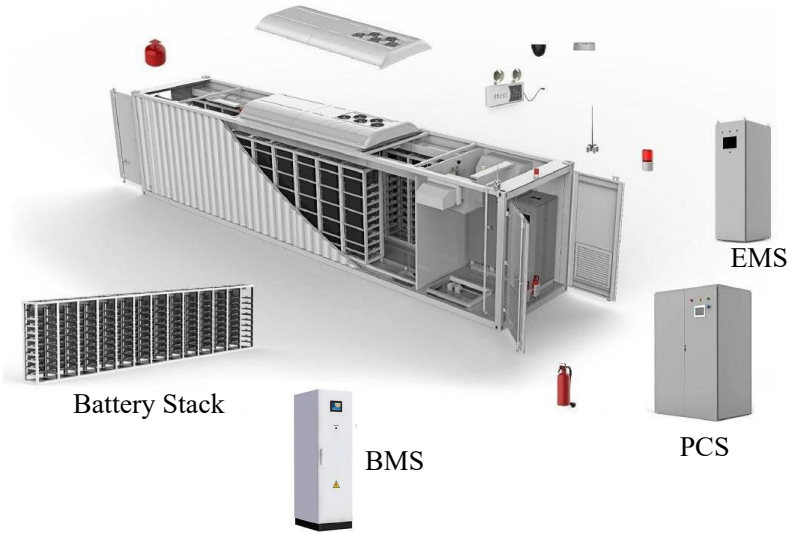


Figure 1.2 Schematic diagram of the key components of a BESS.

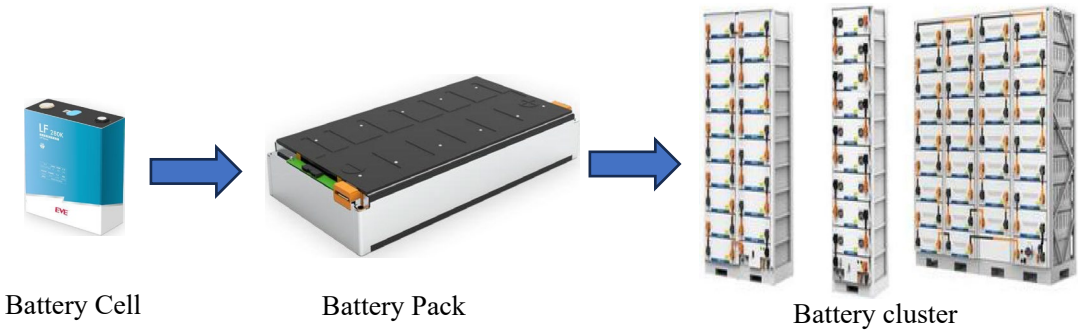


Figure 1.3 Relationship between battery cells, battery packs and battery clusters

PCS is the interface between battery stacks and AC power grids. Technically, it is the key item of equipment to control charging and discharging batteries on the DC side, as well as active and reactive powers on the AC side. According to the circuit topology of PCS, the types of BESS are generally divided into the power transformer-coupling and cascaded categories. Although the insulation level of Insulated Gate Bipolar Transistors (IGBT) even achieves 6500V, the insulation level of battery cells is usually less than 1500V, which determines the maximum number of battery cells connected in series. Moreover, as the State of Charge (SOC) of battery cells varies, the DC-side voltage of the corresponding battery cluster fluctuates below 1500V.

Consequently, two strategies are applied to connect a BESS to a medium-voltage power grid. The conventional and straightforward strategy is to utilize a power transformer

coupling the BESS and the grid. The other strategy is relatively complex, in which several low-voltage submodules are cascaded to achieve the desired high voltage. It should be noted that the complexity of the cascaded type lies not only in the topology and control strategy but also in the unique insulation design of the system.

Compared with the cascaded category, transformer-coupling BESS is technically and commercially mature. There are four main types of BESS in the category manufactured and applied commercially: (a) centralized type, (b) distributed type, (c) distributed-centralized type, and (d) string type. The topology drawings of the four types are shown in Figures 1.4, 1.5, 1.6 and 1.7, respectively.

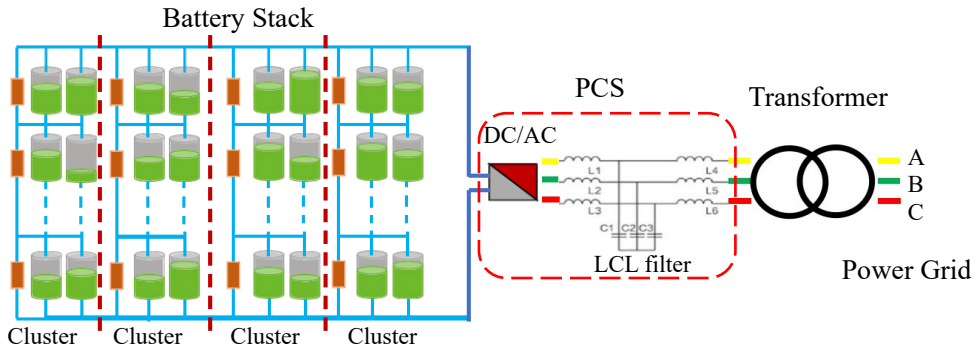


Figure 1.4 Circuit topology of transformer-coupling BESS of centralized type.

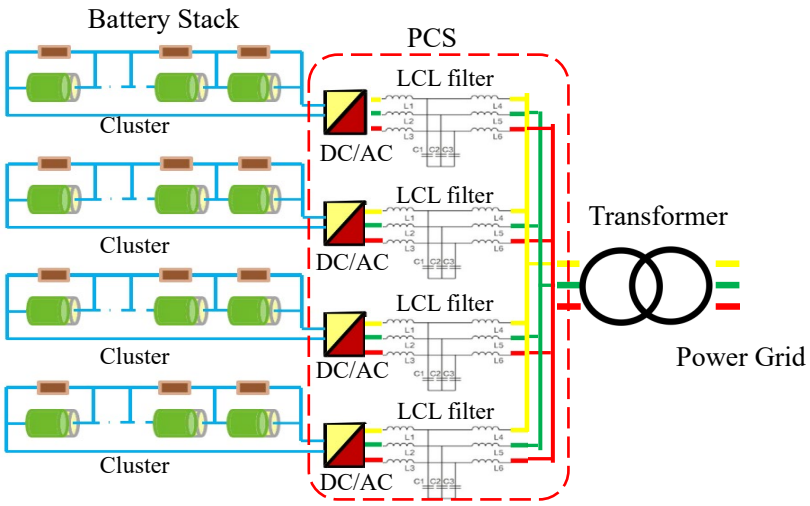


Figure 1.5 Circuit topology of transformer-coupling BESS of distributed type.

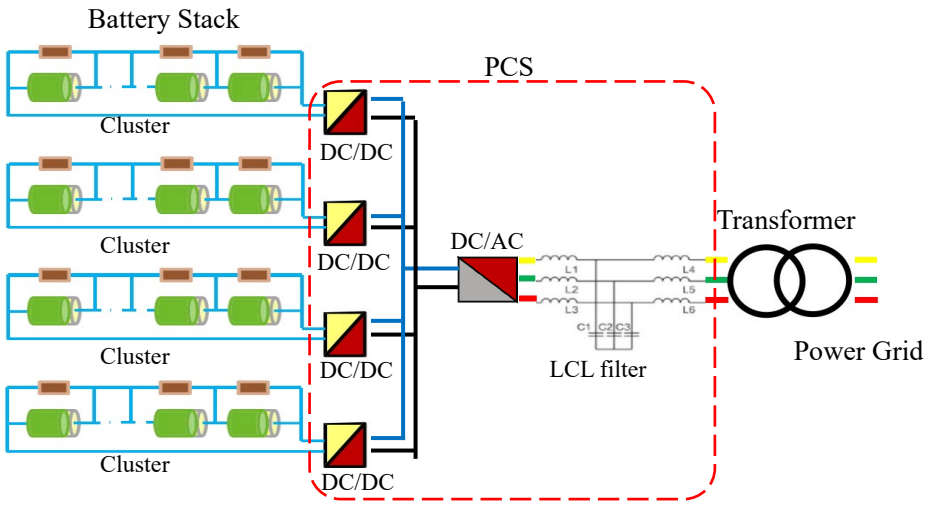


Figure 1.6 Circuit topology of transformer-coupling BESS of distributed-centralized type.

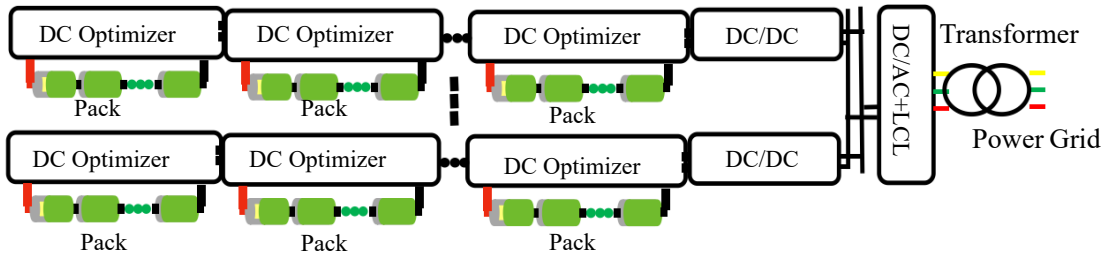


Figure 1.7 Circuit topology of transformer-coupling BESS of string type.

As seen in Figures 1.4, 1.5, 1.6 and 1.7, the structure of centralized type is the simplest of the four types and thus has relatively high conversion efficiency. However, due to the large number of cells connected in parallel is large, its disadvantages are also obvious:

- The coupling between battery cells is strong. One abnormal cell can lead to many normal cells being out of service.
- The dispersed degree of SOC of battery cells is high, and thus, the utilization rate of battery capacity is low. After the State of Health (SOH) between battery clusters is discrete, the 'short board effect' will be prominent, and the available capacity of the battery system will decay quickly.
- Due to the unavoidable differences in the internal resistance characteristics of battery cells, a loop current is generated between the cells connected in parallel during normal operation, resulting in power loss.

- When a single cell has a short-circuit fault, it causes an imbalance in voltage, which leads to the parallel cell discharging energy to the faulty cell, resulting in a chain of counter-failures.

The other three types of transformer-coupling BESS have been developed mainly to tackle the abovementioned drawbacks of the centralized type. The basic principle of the three types is decoupling battery clusters from each other to reduce the parallel number of battery cells through separate DC/AC or DC/DC converters, as seen in Figures 1.5, 1.6, and 1.7. This strategy employs more energy conversion components, which will inevitably reduce conversion efficiency and increase the costs of the whole system.

In contrast, cascaded BESS adopts an entirely different topological scheme. Generally, a battery cluster and a semiconductor switch (in many cases, a full or half bridge switch) are integrated into a submodule, and several submodules are cascaded in series to achieve the desired medium or even high voltage. The main advantages of BESS of the cascaded category are summarized as follows:

- The PCS of this category can connect low-voltage DC components directly to a medium-voltage grid or even a high-voltage grid without a step-up transformer. This means that the power transformer's load and no-load losses are eliminated, increasing power conversion efficiency and decreasing the system's footprint.
- Due to the high voltage levels in the cascaded topology, the equivalent switching frequency is high, and thus, the system output waveform is much more satisfactory. Furthermore, the LCL passive power filters of low voltage and large current are unnecessary and, therefore, replaced by a simple L filter for high and small currents.
- Battery clusters are naturally decoupled from each other, so the drawbacks of centralized type BESS are avoided.
- It has modular components and a higher scalability, redundancy, and fault-tolerant capability.

The topological schemes of the cascaded category are very promising and have received widespread attention because of the abovementioned strengths. Currently, two types of BESS in this category are the most popular, i.e. Cascaded H-Bridge BESS (CHB-BESS) and Modular Multilevel Converter BESS (MMC-BESS). Cascaded H-Bridge topology and Modular Multilevel topology are well-established topologies of power conversation systems (PCS), which have been used in high-voltage chained Static Var Generator (SVG) and Flexible DC Transmission (FDCT), respectively.

In 2007, Maharjan et al. [3,4] proposed the first application of Cascaded H-Bridge PCS (CHB-PCS) to a supercapacitor energy storage system, which enabled the energy storage system to be directly connected to the medium voltage grid without the need for a power transformer. Bragard et al. [5] investigated the charging and discharging strategy, an optimal number of voltage levels and modulation technique of BESS based on CHB-PCS connected to the medium voltage grid to improve efficiency further. Figure 1.8 shows the topology of three-phase CHB-BESS.

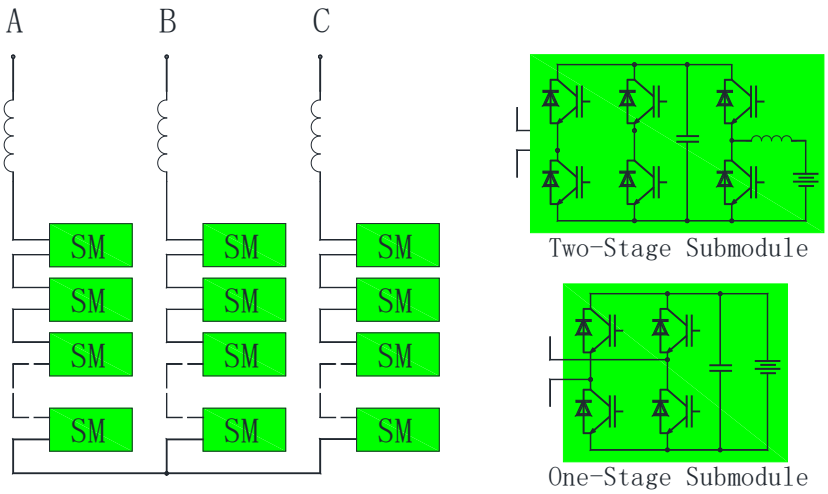


Figure 1.8 Configuration of the three-phase CHB-PCS.

In 2011, Teodorescu's team [6] first integrated BESS into the MMC-PCS. Compared with the CHB structure, the MMC topology has a common DC bus, which can realize the power interaction between the BESS, the AC grid and the DC grid, equivalent to a three-port converter. In MMC-BESS, the power transfer between AC grid, DC grid and

storage battery can also be decoupled and controlled [7]. However, MMC-BESS is still mainly focused on laboratory research and has not yet been applied in practical engineering. Figure 1.9 shows the topology of three-phase MMC-BESS.

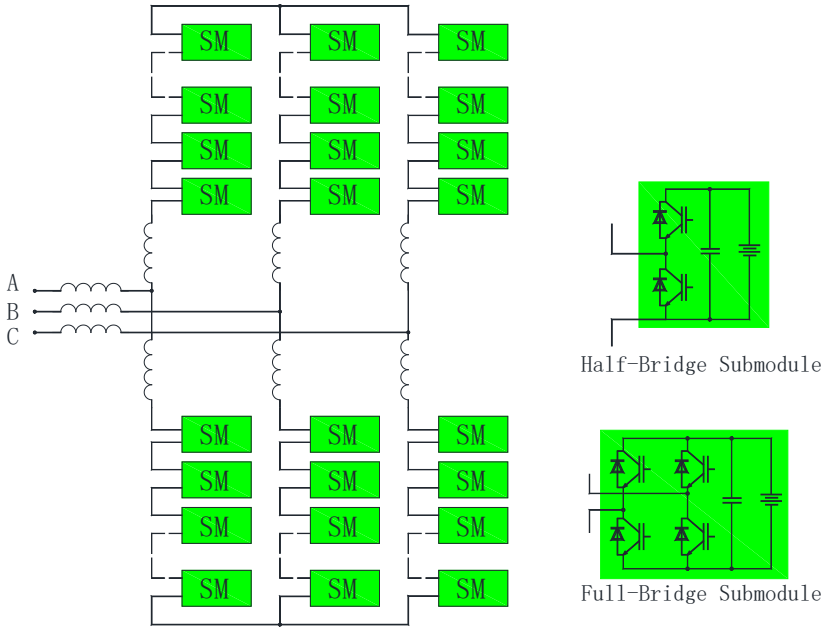


Figure 1.9 Configuration of the three-phase MMC-PCS.

1.2 Cascaded H-Bridge Power Conversion System

MMC and CHB cascaded topologies are considered the most promising. Still, ironically, they suffer from problems such as the presence of second harmonic currents in submodule batteries, inter-phase and inner-phase batteries SOC balancing and fault ride-through. Therefore, some research on novel cascade topologies mainly focuses on solving or improving these problems. Since this thesis does not focus on topologies, only three novel cascaded topologies are briefly described here.

Huang et al. [8] compared the power quality of one-stage and two-stage MMC-PCS and CHB-PCS. Through simulation analysis, they concluded that the one-stage MMC-PCS and CHB-PCS perform better in output voltage, current waveforms, and inter-phase circulating currents. They pointed out that the one-stage scheme has lower THD

performance due to the smaller fluctuation of the submodules' DC side voltage than the two-stage scheme. In contrast, the two-stage scheme eliminates the second harmonic current of the battery and makes better use of the battery capacity.

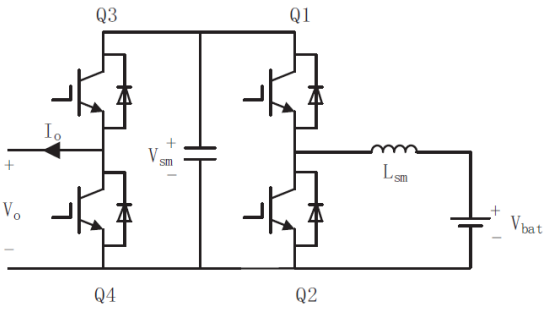


Figure 1.10 Two-stage submodule topology [6].

Alaas et al. [9] proposed a novel cascaded PCS topology capable of achieving battery cell level SOC balancing, in which each cell is connected in series to form a cluster via a half-bridge to achieve DC/DC conversion and then a full-bridge to achieve DC/AC conversion. Unlike the traditional cascaded PCS topology, which can only achieve SOC balancing at the battery cluster level, this new topology achieves cell or pack level balancing via PCS, which is currently achieved via a BMS system. However, this scheme is a two-stage topology with the inherent disadvantages of high system cost and low conversion rate.

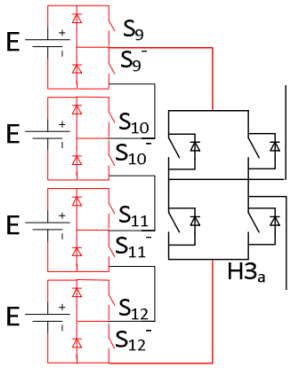


Figure 1.11 New submodule topology [7].

A cascaded PCS topology at the battery cell level is proposed by Nataraj et al. [10], in which a bi-directional H-bridge DC/DC converter is set up for each cell, and a high-

frequency transformer links the fully controlled H-bridges on both sides. They give the power control algorithm and cell SOC balancing control algorithm for this new topology. This scheme achieves the decoupling control of each cell's charging and discharging currents and thus achieves the SOC balancing of the cells more fundamentally. However, this scheme is essentially a multi-stage PCS with too many conversion links, affecting the conversion efficiency. Adding numerous power switching components and high-frequency transformers is bound to increase the per watt cost of PCS significantly.

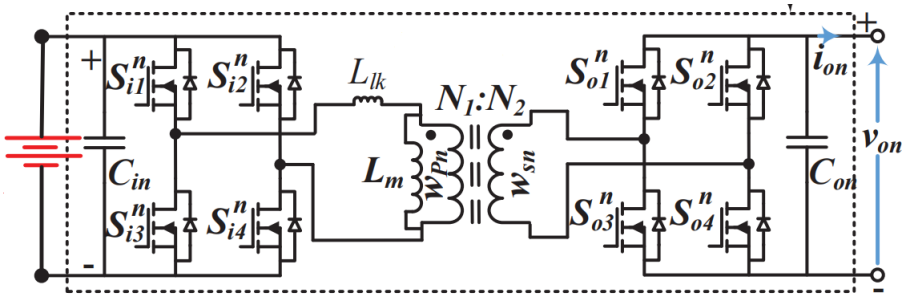


Figure 1.12 New submodule topology [8].

Although there are a variety of topologies for cascaded BESS, as mentioned above, MMC- and CHB-BESS are the most popular ones investigated. Soong et al. [11] compared the CHB-PCS, the MMC-PCS with centralized access to the batteries on the DC side and the MMC-PCS with distributed access to the batteries on the DC side. They showed that the MMC-PCS with distributed access to the batteries on the DC side requires the largest number of semiconductor switches to achieve the same AC voltage level but has better system redundancy due to the excess of submodules over the other schemes and has an optimal system conversion efficiency by simulation. The paper does not explain the high efficiency of the MMC-PCS with distributed access to the batteries on the DC side. At the same time, it is obvious that the submodules of the scheme adopt a half-bridge topology instead of a full-bridge topology. The submodules only need to conduct one semiconductor switch in each state, so the system switching loss and conduction loss are lower.

Compared with MMC-BESS, the SOC balancing control of CHB-BESS is simple. The SOC balancing control of CHB-MMC is divided into inter-phase equalization, inter-arm equalization of the same phase and inner-leg equalization, and loop current within the arms is injected to achieve inter-phase and inter-arm equalization, which is not only complex to control, but also occupies the capacity of the components. On the other hand, CHB-BESS only requires inter-phase and inner-phase equalization, which can be achieved using the zero-sequence voltage injection method. In addition, CHB-BESS does not require bridge-arm loop current suppression and bridge-arm inductances.

It is worth noting that the MMC topology scheme can be used as a three-port energy converter connecting AC grid, DC grid and BESS. In contrast, CHB-PCS can only be used to connect to an AC grid, which is the widest application scenario for BESS. Furthermore, CHB-BESS has been commercially applied in recent years. Also, the inter-phase SOC balancing and submodule fault-tolerant control strategies proposed in this thesis can be easily adapted into other cascaded topologies. Hence, the investigations involved in this thesis predominantly focus on CHB-BESS.

1.3 Literature Review on Recent Development

There are a range of research directions in cascaded BESS, each of which has been explored in a large body of literature. This section presents a literature review of only those research directions that are closely related to this research, which have been published mainly within the last decade.

1.3.1 Overview

The current research on Cascaded PCS mainly focuses on modulation strategies, State of Charge (SOC) balancing strategies, submodule DC ripple current suppression, cascaded topologies, submodule fault-tolerant control, power control and common-mode current suppression methods, etc. This thesis focuses on SOC balancing and submodule fault-tolerance control strategies, which inevitably involve modulation and

power control strategies, so this section discusses the recent developments in these aspects.

1.3.2 Output Power Control

The power control strategy is the basis of cascaded PCS, mainly including traditional decoupling control, amplitude-phase control, predictive control, direct power control, no differential beat control, etc. Decoupling control is one of the most common and reliable methods to achieve converter control objectives, such as power, voltage, frequency, etc., by effectively controlling the dq-axis current on the grid side.

Zhang et al. [12] investigated the output power control strategy of CHB-PCS under grid voltage unbalanced conditions. They derived the positive-sequence and zero-sequence reference values in a two-phase stationary frame reference and achieved current tracking by PR control. In addition, under the grid voltage unbalance condition, they achieved inter-phase SOC balancing by zero-sequence voltage injection method and inner-phase SOC balancing by output voltage superposition method.

Since the existing literature mainly focuses on the study of control algorithms for cascaded PCS with transformerless access at medium voltage such as 10kV, Zhu et al. [13] gave the calculation of the parameters of the main electrical components such as switching elements, filter capacitance and reactance for cascaded PCS with transformerless access at 35kV high voltage and the power decoupling control algorithm for this PCS. The paper does not innovate in the control algorithm but extends the study of cascaded PCS to high voltage.

Neira et al. [14] proposed using the Sequential Phase-Shifted Model Predictive Control (PS-MPC) in a multilevel BESS implementation using three-port full-bridge modules. In the three-port full-bridge modules, two inductors are added to the positive node of the submodule's battery pack and the topology of the submodules is changed so that the

coupling of the PCS output power to the submodule's DC-side capacitor voltage and battery current is reduced through the addition of state variables and thus made controllable. They improved the Finite Control Set Model Predictive Control (FCS-MPC) control algorithm based on the technical characteristics of Phase-Shifted Pulse Width Modulation (PS-PWM), which reduces the size of the control set and thus greatly reduces the computational amount. The simulation verified that the algorithm can simultaneously achieve multi-objective control of output power tracking, capacitor voltage, elimination of battery ripple current, and SOC equalization of submodule battery packs.

1.3.3 Battery State of Charge Balancing Control

For cascaded PCS, as the BESS charging and discharging, due to each battery's production process and self-discharging characteristics, it will lead to differences in the State of Charge (SOC) between the batteries, which may be amplified over time. Because of the equal flow of current through the power modules, it is easy to trigger the phenomenon of overcharging and over-discharging batteries, affecting the system's reliability. Therefore, SOC balancing is an important guarantee for the normal operation of the BESS based on cascaded PCS and avoiding overcharging and over-discharging batteries. In this view, a large number of SOC balancing studies have been carried out on different cascaded PCS structures.

The SOC balancing strategy in CHB-PCS can be divided into inter-phase and inner-phase balancing. The purpose of the inter-phase balancing control strategy is to make the average SOC of all the submodules in each phase equal to the average SOC value of all the submodules in the system, which is mainly divided into two major categories of zero-sequence voltage injection and negative-sequence current injection methods. The in-phase balancing control aims to make the SOC value of the battery rack in each submodule equal to the average SOC value of all submodule battery racks in the phase where it is located.

The zero-sequence voltage injection method calculates the corresponding zero-sequence voltage based on the amplitude of the phase balancing power and superimposes it on the reference voltage [15-18]. The zero-sequence voltage does not affect the output line voltage or output power, and it is easy to calculate. The negative sequence current injection method injects a small amount of negative sequence current into the reference current to adjust the power distribution among the three phases [19]. This method does not affect the total output power; a negative sequence current is injected into the grid.

Zhang et al. [20] proposed a zero-sequence voltage injection balancing strategy based on a self-adaptive balancing control strategy, which can adjust the balance coefficient during the balancing process and accelerate the balancing process without causing over-modulation.

Hu et al. [21] improved the traditional zero-sequence voltage injection method for inter-phase balancing, i.e., by calculating the maximum zero-sequence voltage injection proportional coefficient in case of no overmodulation of the normal phase to speed up the phase-to-phase balancing. In addition, they also improved the traditional in-phase balancing algorithm to ensure the three-phase output voltage balancing while avoiding submodule overmodulation.

In the field of inner-phase balancing research, the cascaded carrier rotation method based on CHB-PCS needs to rotate the carrier signals in different carrier cycles to make the battery racks with high SOC more discharging and less charging, and those with low SOC less discharging and more charging, to achieve the SOC balancing among the submodules [22,23].

In the sorting selection method [24-26], the SOCs of all the submodule battery racks are sorted so that the battery racks with higher SOC values are discharged more or charged less. This method is straightforward, but the sorting time is extended when the

number of submodules is large.

Chatzinikolaou and Rogers [27] measured the pseudo-open-circuit voltage of their battery pack every 3 seconds by bypassing a submodule ranked the pseudo-open-circuit voltages of all the submodules, and then combined the results of the ranking with a nearest level approximation algorithm for SOC balancing.

Jang et al. [28] used a sequencing selection method to perform SOC balancing within each phase by selecting appropriate states in the voltage space vector.

Some researchers have controlled the active power transfer between submodules by directly modifying the modulation reference wave of each submodule, i.e., superimposing a fundamental-frequency voltage component, whose amplitude is calculated by a PI controller according to the SOC imbalance [29,30]. This strategy is straightforward, but directly adjusting the reference waveform of each submodule will inevitably affect the output power quality, especially when the SOC differences between battery racks are large.

Liang et al. [31] analyzed and compared the SOC balancing capabilities of PI-Based and Sorting-Based State of Charge Balancing Methods in Cascaded H-Bridge Converters and provided a guide to choose the appropriate method according to the system specifications. They stated that considering the modulation index of grid-connected CHB converters is typically high, the sorting-based method should be the prior option for more satisfactory performance.

By taking advantage of the intrinsic voltage vector redundancy characteristic of three-phase CHB converters, Pirooz et al. [32] proposed an algorithm for phase-to-phase and in-phase simultaneously balancing based on a finite-set model-predictive current control (FSMPC) technique.

Markus Herzog et al. [33] gave a detailed procedure for the SOC balancing of the inner-phase submodules of CHB-PCS by using the sorting order method in Carrier Level-Shifted Pulse Width Modulation (LS-PWM) based on the academic results of previous researchers. In addition, they gave the formulae for the voltage amplitude and phase for inter-phase SOC balancing and fault ride-through while using the zero-sequence voltage injection method. To avoid overmodulation while simultaneously achieving fault ride-through and inter-phase SOC balancing, they further gave the upper limit of the injected zero-sequence voltage.

Alaas et al. [34] proposed a novel topology for inter-phase SOC balancing, in which an energy storage capacitor is connected to the neutral point through a three-phase half-bridge circuit. Based on the PS-PWM modulation method, they gave this novel topology's voltage output and in-phase SOC balancing strategy. Unlike the traditionally used zero-sequence voltage injection method, this paper transfers energy between different phases by controlling the charging and discharging of this capacitor. Compared to the zero-sequence voltage injection method, this method adds some hardware, significantly increasing the system cost. In addition, the output phase voltage needs to consider the influence of the charging capacitor voltage, and thus the control algorithm is complex.

1.3.4 Fault-Tolerance Control

Cascaded PCS of BESS contains a significant number of power-switching semiconductors. Each power element is a potential point of failure, which reduces the system's reliability and stability. Therefore, ensuring the effective output of the system by adopting fault-tolerant control without system downtime is a critical issue. Currently, the fault-tolerant control of cascaded PCS is mainly divided into adding a cold standby[2]

[2] Cold standby is a disaster recovery technique used in system design where you have a redundant system that acts as a backup for your primary system.

redundancy module [35] and a hot standby[3] redundancy module [36].

The cold standby redundancy module strategy, also known as the hardware redundancy method, refers to when the Cascaded PCS works normally, the redundant submodules are bypassed. When the working module fails, the working SM will be bypassed. The redundant submodule will be used to carry out the work instead [35]. The principle of this strategy is relatively simple and can reduce the conduction loss. However, in most cases, the cascaded PCS operates in a no-fault state, which means setting cold standby redundancy modules will cause a certain degree of resource waste, thus increasing the system's cost. In addition, the state of the batteries connected to the cold standby submodule put into operation may differ significantly from that connected to the operating submodules, and there is a transient switching process, which affects the output power quality.

In this regard, Liang et al. [37] proposed a setup of cold standby redundant modules without batteries, which reduces the system cost. The redundant module of this scheme is only discharged briefly to maintain the peak voltage. It charges the DC side capacitor at other times to maintain the DC voltage, so a corresponding voltage balancing algorithm is required.

The hot standby redundancy module strategy is also known as the software redundancy method. In this strategy, the redundant submodules are also operated when the system runs normally. The submodules are removed when they fail, and corresponding control methods are adopted to ensure the system's normal operation. In this method, submodule utilization is high, and the state consistency between submodules is better. Currently, there are more studies on hot standby fault-tolerant control strategies for CHB-BESS and MMC-BESS, which can be classified into symmetric resection

[3] Hot Standby refers to a redundancy strategy in system design where a backup system or component is continuously operational and synchronized with the primary system.

strategy and asymmetric resection strategy according to the treatment of faulty submodules.

The symmetrical resection strategy bypasses the same number of submodules in the other phases while bypassing the faulty submodules to ensure the three-phase symmetry of the system. This strategy has a simple control algorithm, but reducing the same number of submodules in each phase simultaneously reduces the capacity and the number of levels of the energy storage system [38].

The second strategy is the method of only removing the faulty submodules, which can also be called the asymmetric removal strategy. This method removes only the faulty submodules, leaving the other phases unchanged. Although this method is more complex, it provides greater redundancy and fully utilizes the capacity of the BESS.

Hu et al. [39] applied the asymmetric resection strategy to MMC-PCS, where redundant submodules are set up on each bridge arm of the three phases, and all the modules are involved in the normal operation. In the event of failure of a submodule, the proposed strategy bypasses that submodule, the standard module of the corresponding bridge arm, and the missing voltage level is redistributed to the remaining modules. In contrast, the modules of the other phases are maintained unchanged.

Some researchers have also proposed the zero-sequence voltage injection method to reduce the faulty phase's phase voltage and increase the non-faulty phase's phase voltage without affecting the line voltages [40]. In this strategy, all the remaining normal operation submodules evenly share the output voltage to reduce the impact of the faulty submodules on the CHB-BESS.

For MMC-BESS, Hillers and Biela [41] proposed a loop current control method to solve the problem of unbalanced power distribution among bridge arms when only the

faulty submodule is bypassed.

Gu et al. [42] achieved MMC-BESS submodule fault traversal by redistributing PWM pulses from the faulty submodule to other normal submodules, and the normal output of the system can be fully restored within a specific modulation depth range.

Li et al. [43] proposed using a sliding selection box to select each submodule for operation in each cycle. When a submodule fails, it is removed from the alternative queue of the sliding selection box. In this method, each submodule will take turns participating in normal operation, and the number of submodules put into operation after a failure remains unchanged, so the transient switching performance is better than the traditional hot standby method.

An algorithm based on phase-shifted pulse width modulation (PS-PWM) is given in the paper [44] to achieve power element fault tolerance for CHB-BESS. The method utilises the normal submodules to take on the voltage level lost by the faulty submodule. Still, it does not require modification of the output voltage reference and carrier phase-shift angle, resulting in better transient stability, verified by simulation and experiment.

Mhiesan et al. [45] proposed a hybrid cascaded H-bridge topology to improve the fault-tolerant ability of the system, in which an X-CHB submodule is connected in series in each phase. A flying capacitor is added to this submodule to double the DC side voltage of the submodule. After bypassing a fault submodule (e.g., a battery fault or a semiconductor switch short-circuit or open-circuit fault), this X-CHB capacitor compensates for the missing voltage level by using this flying capacitor. This thesis gives simulations and experiments to this novel topology, where LS-PWM modulation strategy is employed, and the results demonstrate the effectiveness of this topology in CHB-BESS fault tolerance.

D. Patel et al. [46] proposed a fault-tolerant structure using relays based on a three-

phase, seven-level CHB-BESS. When a semiconductor switch has a short or open circuit fault, the relay will act on a contactor to bypass the corresponding submodule and connect the corresponding battery cluster to the DC side of the normal submodule through the cooperation of several other contactors. It can be seen that this scheme does not cause the DC side voltage to decrease due to the bypass of the faulty submodule, thus ensuring the symmetry of the three phases of the system after the fault. However, although the DC side voltage remains the same before and after the fault, the number of voltage levels decreases, so the control scheme of the post-fault system needs to be further explored. In addition, the fault-tolerant structure can be very complex when the number of cascaded submodules is large, significantly increasing the system cost.

For three-phase seven-level CHB-BESS, Rahman et al. [47] proposed a new Fault-Tolerant Control Strategy, which differs from the conventional zero-sequence voltage injection method. In this strategy, the relative phases of the three-phase voltages are modulated to keep the three-phase line voltages symmetrical after the faulty submodule fault is bypassed. The essence of this scheme is still the zero-sequence voltage injection method, and how to adjust the reference voltage of each phase when the reference line voltage changes should be further researched.

Mhiesan et al. [48] summarized the problems and scope of applying fault-tolerant strategies. In particular, they pointed out that the fault reconfiguration strategy of connecting the batteries of the faulty submodule to the DC side of another normally operating submodule causes problems such as semiconductor switching overvoltages and difficulties in balancing the SOC of the batteries and requires a large number of high-voltage circuit breakers, and therefore is not suitable for medium- and high-voltage application scenarios. They proposed a reconfiguration scheme for CHB-BESS to achieve standby by connecting some controllable switches across the semiconductor switches. They gave simulation and experimental results in the case of an open-circuit fault in the semiconductor switch but did not analyze how to cope with a short-circuit fault. In addition, this reconfiguration scheme requires four additional semiconductor

switches per submodule, which significantly increases the system cost and control difficulty.

For the three-phase, five-level CHB-BESS, Sornsadaeng et al. [49] proposed a fault-tolerant strategy based on Space Vector Modulation (SVM), in which the fault types are classified into five modes according to the number of failed submodules. Corresponding to each mode, the symmetric space voltage vectors and corresponding submodule state tables are set up. Then, a sequence of appropriate space voltage vectors is selected from the corresponding state table according to the specific faults occurring. Unlike the zero-sequence voltage injection method, this scheme does not need to calculate the phase and amplitude of the zero-sequence voltage to be injected. However, with the increase in voltage levels, the number of space voltage vectors will grow exponentially, so this scheme only applies to CHB-BESS with a few levels.

To improve the applicability of Selective Harmonic Elimination Modulation (SHE) in the fault-tolerant operation of CHB-BESS, a modification of SHE was made by Aleenejad et al. [50]. Taking the 7-level three-phase CHB-BESS as the object of study, the method not only calculates the submodule switching angles under normal and faulty states in advance but also calculates the phase angle shift of the output phase voltages under the submodule faults in advance and stores it so that it can be recalled according to the actual state during the system operation. However, with the increase in voltage levels, the method needs to calculate the submodule switching angle and three-phase voltage phase angle shift under numerous system states in advance, so the technique lacks flexibility.

1.3.5 Modulation Strategy

As the key to the Cascaded BESS, the modulation strategy can directly affect the PCS's output voltage waveform quality and switching loss. Different multilevel BESS topologies have different performance requirements according to their own needs. Still,

there are two main control objectives: one is high output waveform quality, and the other is low switching frequency. The modulation strategies of cascaded PCS mainly include Staircase Wave Modulation (S-WM), Carrier Phase-shifted Pulse Width Modulation (PS-PWM), Carrier Level-Shifted Pulse Width Modulation (LS-PWM), Space Vector Pulse Width Modulation (SV-PWM), Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM), etc. [51].

SHE-PWM can eliminate low harmonics at specific frequencies and has low switching losses. However, in practical applications, its real-time calculation is complicated, and closed-loop control is difficult, so it is still difficult to successfully apply to Cascaded PCS. PS-PWM and LS-PWM are simple to implement and have good output characteristics. In PS-PWM, the H-bridge submodules adopt unipolar modulation. When PS-PWM is adopted, the submodules in one phase usually have the same voltage modulation waveform, and there is only a phase difference between the carrier waveforms of different H-bridge submodules. In this modulation mode, as the number of H-bridge submodules increases, the harmonic content of the output voltage on the AC side decreases, and the harmonic frequency increases, making it easier to filter out. Therefore, PS-PWM has been widely used in Cascaded PCS [52]. The basic principle of LS-PWM is shown in Figure 1.13.

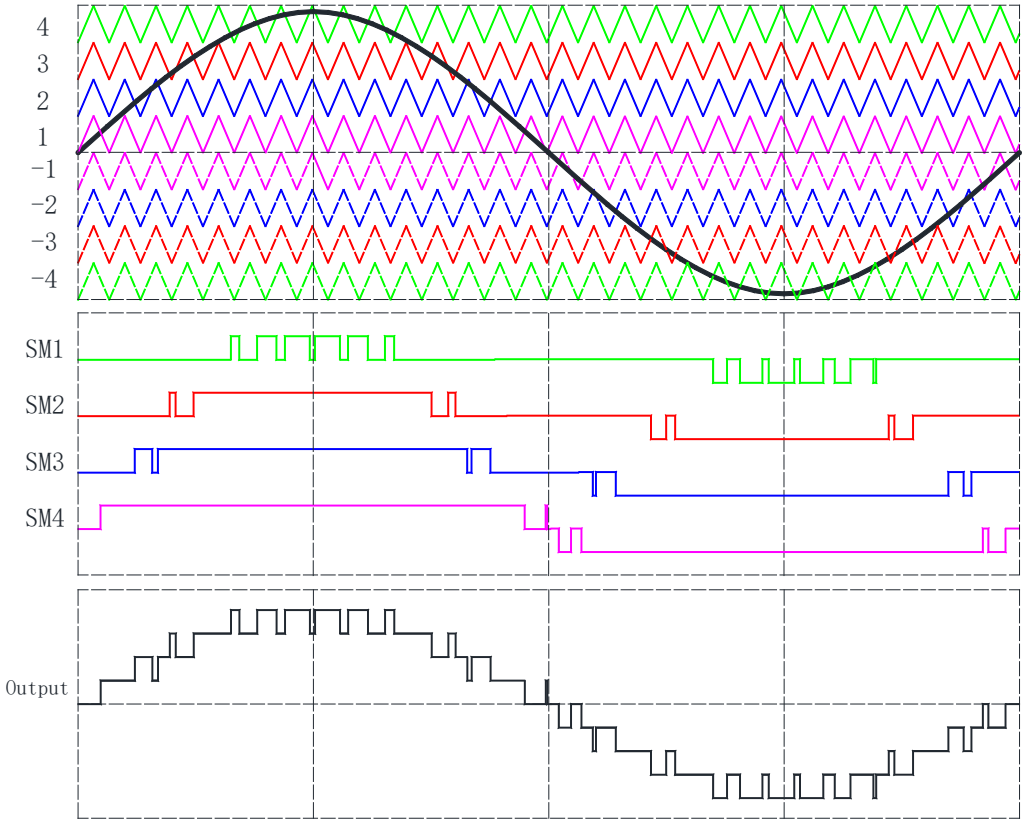


Figure 1.13 Principle of LS-PWM.

Some researchers have compared some modulation strategies and pointed out that modulation strategies such as Sinusoidal PWM, SVPWM and Graphical Method are more suitable for PCS topologies with fewer voltage levels, whereas in structures with a higher number of voltage levels, fundamental frequency modulation (FFM) in the form of Quantizer, Round Control and SV control are more advantageous due to lower switching loss [53].

Karmakar et al. [54] proposed a fundamental switched Area Equalization Modulation strategy (AEM). The switching angles are computed by equalizing the area under the reference voltage and carrier signals. Since the modulation method is based on fundamental frequency modulation (FFM) rather than pulse width modulation (PWM) control, the modulation method has a lower switching loss.

Wang [55] suggested an Asymmetric Switching Angle Modulation (ASAM). Unlike the conventional Symmetric Switching Angle Modulation (SSAM), the switching elements

have asymmetric turn-on and turn-off angles in this modulation method. The turn-on and turn-off angles of the switching elements are calculated by Fourier transform, which enables the cascaded PCS to compensate for both grid harmonics and reactive power. This modulation scheme is more flexible but computationally intensive than the conventional selective harmonic elimination (SHE) techniques with symmetric turn-on and turn-off angles.

Since SV-PWM has the feature of high utilization of the DC voltage, the application of SVPWM and convenience in cascaded multilevel structures has become the research of many scholars. To take advantage of the SV-PWM's better utilization of the DC-link voltage and to solve the problem of complex calculation and high switching frequency of this modulation method in CHB-PCS control, Xu Fan et al. [56] proposed a Hybrid SVPWM strategy, in which the reference vector is decomposed into a power vector and a high-frequency vector. Experiments proved the effectiveness of the method with desirable output waveform quality.

For a Hybrid 15-level topology, Sang et al. [57] compared three modulation methods, i.e., conventional PWM modulation, step-wave modulation and Nearest Level Modulation (NLM). Unlike the traditional topology, where each submodule is connected to the same number of battery cells, this topology connects the cells in a 1:2:4 ratio, doubling the output voltage levels and reducing the switching losses. The NLM modulation method has an advantage in switching loss and output waveform in this topology through simulation and comparison. Nevertheless, this topology lacks flexibility and requires further research to achieve SOC balancing and fault ride-through.

1.4 Objectives and Methodology

This research mainly consists of two topics. One topic is focused on the inter-phase State of Charge (SOC) balancing control of CHB-BESS, and one self-adaptive inter-

phase SOC control strategy is proposed. The objectives of this topic are as follows:

- Brief introduction of conventional inter-phase balancing control method by zero-sequence voltage injection.
- Further investigation of the method improves DC-Side voltage utilization by injecting a Max-Min average signal and presenting a new self-adaptive inter-phase SOC control strategy.
- Quantitative comparison between the conventional and new strategies, confirming the effectiveness of the new approach on a theoretical basis.
- Further validation of the effectiveness of the new strategy is done through modelling, simulation, and analysis based on Matlab/Simulink.

The other topic is focused on fault-tolerance control for CHB-BESS, and one fault-tolerance control strategy is proposed. The objectives of this topic are summarized as follows:

- Further investigation of conventional fault-tolerance control strategy for CHB-BESS and presentation of a new strategy.
- Quantitative comparison between the conventional and new strategies, confirming the effectiveness of the new strategy on a theoretical basis.
- Integrating the conventional and new strategies with the modulation voltage clapping (MVC) method used in motor driving and static var generators (SVG) facilitates the application of the two techniques.
- Further validation of the effectiveness of the new strategy is done through modelling, simulation, and analysis based on Matlab/Simulink.

As mentioned above, this research mainly focuses on inter-phase SOC balancing and submodule fault-tolerant control strategies. However, in order to conduct in-depth research on the two topics, modulation and power control strategies of CHB-BESS are inevitably involved. Active and reactive power decoupling control is one of the most common and reliable methods to achieve control objectives such as power, voltage, frequency, etc., by effectively controlling the dq-axis current on the grid side.

Accordingly, this power control strategy is applied to two research topics. Similarly, although there is a wide variety of modulation methods for CHB-BESS, PS-PWM is utilized in this research due to its maturity and satisfactory performance.

Therefore, apart from the general background, literature review, and aims of this research, as described in Chapter 1, the following chapters are structured accordingly in compliance with the objectives. Chapter 2, Principles of Cascade H-Bridge Battery Energy Storage System, describes the basic principles of CHB-BESS from physical and mathematical perspectives. This chapter also explains active and reactive power decoupling control based on rotating reference of frame and PS-PWM, which are involved in this research. Chapter 3, Inter-Phase State of Charge Balancing Control for Cascaded H-Bridge Battery Energy Storage System, covers the introduction of conventional inter-phase balancing control method by zero-sequence voltage injection, presentation of a new self-adaptive inter-phase SOC control strategy, and verification of the effectiveness of the new strategy on both theoretical analysis and Matlab/Simulink simulation. Chapter 4, Fault-Tolerance Control for Cascade H-Bridge Battery Energy Storage System, describes further investigation of conventional fault-tolerance control strategy, presentation of a new strategy, and verification of the effectiveness of the new strategy on both theoretical analysis and Matlab/Simulink simulation. Chapter 5, Discussion and Conclusion, discusses the pros and cons of the results and techniques from chapters 3 and 4, along with the conclusions and recommendations for future work in this field of research.

Chapter 2

Principles of Cascade H-Bridge Battery Energy Storage System

2.1 Basic Components of Battery Energy Storage System

Although the research does not focus on the design of a CHB-BESS, a brief description of the primary circuit is necessary to gain insight into the principles of CHB-BESS. The primary part of a CHB-BESS consists of an AC circuit breaker, a series reactor, and several submodules connected in series, as shown in Figure 2.1. The AC circuit breaker is generally employed to clear short-circuit faults at the BESS side. The series reactor, in many cases, iron-cored, is applied to suppress high-frequency harmonics of voltages generated by submodules. Three groups of series submodules that can be equated to a controllable three-phase voltage source are the key parts of the CHB-BESS. The basic principle of power control of the BESS is regulating the controllable source to achieve desired active and reactive power flows between the power grid and the BESS.

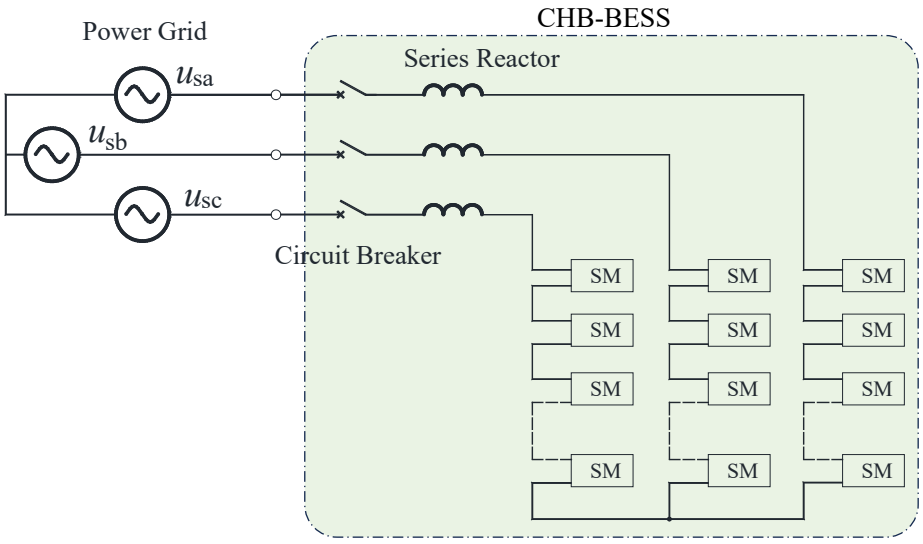


Figure 2.1 Sketch of the primary circuit of CHB-BESS

It should be noted that all the submodules have the same one-stage topology in the context of this thesis, as shown in Figure 2.2. The four IGBTs (or MOSFETs), each commonly incorporating a Freewheeling Diode (FD), form an H-bridge stationary switch, which will be covered in detail in the next section of this chapter. The inductor and capacitor are employed to suppress the ripple current in batteries, which can extend their lifespan. The two contactors and the resistor make up the start-up circuit. Contractor No.1 will be closed first to charge the capacitor in case of start-up, and the current will be limited to a desired value by the resistor. After a short time, the contactor No.2 will be closed to bypass the resistor, marking the completion of the start-up phase and entry into normal operation. The DC circuit breaker is used to clear faults in the battery cluster.

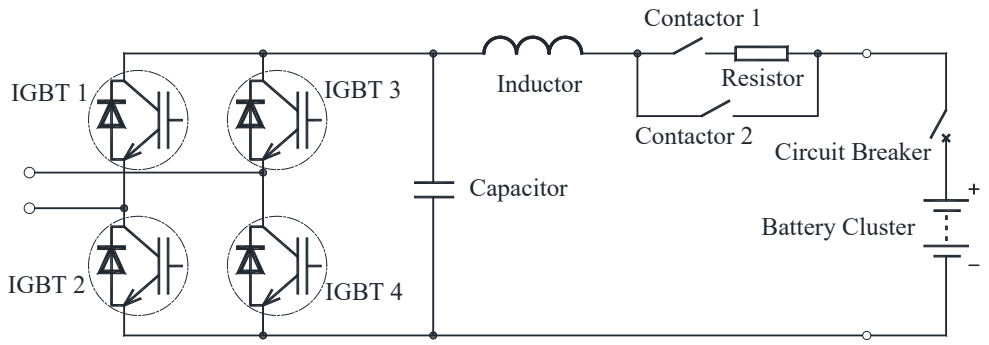


Figure 2.2 Sketch of the primary circuit of a CHB submodule.

2.2 PI Decoupling Power Control Strategy

During the normal operation of the BESS shown in Figure 2.1, the equivalent circuit diagram of the system can be represented in Figure 2.3. The voltages of the power grid, u_{sa}, u_{sb} and u_{sc}, can be expressed by Equation (2.1).

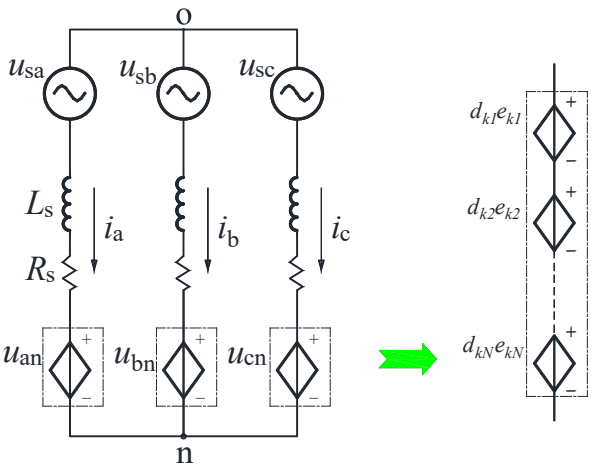


Figure 2.3 Equivalent circuit diagram of a CHB-BESS

$$\begin{cases} u_{\mathrm{sa}}(t) = U_{\mathrm{sk}}\cos(\omega t) \\ u_{\mathrm{sb}}(t) = U_{\mathrm{sk}}(\omega t - \dfrac{2\pi}{3}) \\ u_{\mathrm{sc}}(t) = U_{\mathrm{sk}}(\omega t + \dfrac{2\pi}{3}) \end{cases} \tag{2.1}$$

where U_{sk} is for the magnitude of power grid voltages, and ω represents the angular frequency of the power grid.

From Kirchhoff's law and grid current-voltage symmetry, the BESS output voltage and grid current-voltage relationship can be obtained, as shown in Equation (2.2).

$$\begin{cases} L_{\mathrm{s}}\dfrac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{a}} \\ i_{\mathrm{b}} \\ i_{\mathrm{c}} \end{bmatrix} = -R_{\mathrm{s}}\begin{bmatrix} i_{\mathrm{a}} \\ i_{\mathrm{b}} \\ i_{\mathrm{c}} \end{bmatrix} + \begin{bmatrix} u_{\mathrm{sa}} \\ u_{\mathrm{sb}} \\ u_{\mathrm{sc}} \end{bmatrix} - \begin{bmatrix} u_{\mathrm{ao}} \\ u_{\mathrm{bo}} \\ u_{\mathrm{co}} \end{bmatrix} \\ \begin{bmatrix} u_{\mathrm{ao}} \\ u_{\mathrm{bo}} \\ u_{\mathrm{co}} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{an}} \\ u_{\mathrm{bn}} \\ u_{\mathrm{cn}} \end{bmatrix} + u_{\mathrm{no}} \\ u_{\mathrm{no}} = -\dfrac{1}{3}(u_{\mathrm{an}} + u_{\mathrm{bn}} + u_{\mathrm{cn}}) \end{cases} \tag{2.2}$$

where L_{s} denotes the inductance of the series reactor, and R_{s} denotes the resistance of the circuit.

Since R_{s} is significantly small compared with ωL_{s}, if we ignore it, we can derive from the top row of Equation (2.2) that the active and reactive power exchanged between the grid and the BESS can be expressed by equation (2.3).

$$\begin{cases} P = -\dfrac{3U_{\mathrm{ko}}U_{\mathrm{sk}}\sin\varphi}{\omega L_{\mathrm{s}}} \\ Q = \dfrac{3U_{\mathrm{ko}}(U_{\mathrm{sk}}\cos\varphi - U_{\mathrm{ko}})}{\omega L_{\mathrm{s}}} \end{cases} \tag{2.3}$$

where P is for active power from the power grid to BESS, Q is for reactive power from the power grid to BESS, U_{ko} is for the magnitude of u_{ao}, u_{bo} and u_{co}, and φ represents the phase angle u_{ao} of exceeding u_{sa}.

As shown in Equation (2.3), we can regulate the magnitude and phase angle of the controllable voltage source to achieve the desired active and reactive powers. In the case of $\varphi>0$, then $P<0$, the BESS operates in the inverting state and thus generates active power into the grid. Conversely, in the case of $\varphi<0$, then $P>0$, the BESS operates in the rectifying state, thus absorbing active power from the grid. Similarly, when φ keeps constant, the BESS generates reactive power in the case of $U_{\mathrm{ko}}>U_{\mathrm{sk}}\cos\varphi$ while absorbing reactive power in the case of $U_{\mathrm{ko}}<U_{\mathrm{sk}}\cos\varphi$. Accordingly, the vector relationship of the BESS operating in a steady state is summarized in Figure 2.4.

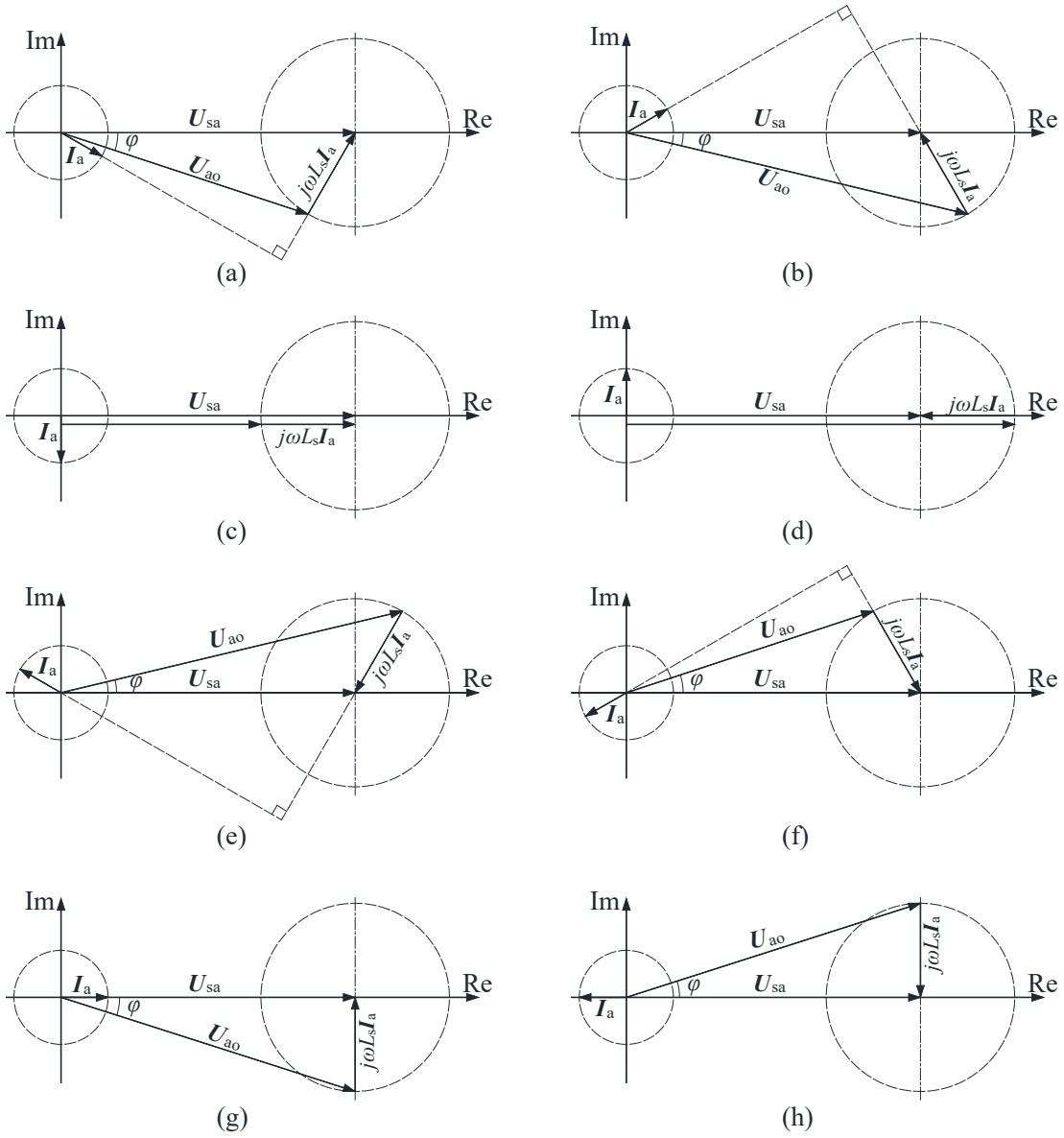


Figure 2.4 Vector relationship of the BESS operating in a steady state.
(a) state of BESS absorbing active and reactive powers. (b) state of BESS absorbing active power and generating reactive powers. (c) state of BESS absorbing reactive powers. (d) state of BESS generating reactive powers. (e) state of BESS generating active and reactive powers. (f) state of BESS generating active power and absorbing active powers. (g) state of BESS absorbing reactive powers. (h) state of BESS generating active powers.

Based on the reference value of P and Q from either AGC/AVC or EMS and the measured value of U_{sk}, the reference values of U_{ko} and φ can be easily derived from Equation (2.3). Then, u_{ao}, u_{bo} and u_{co} are generated through the controllable voltage source, and consequently the desired power flow between the grid and BESS is obtained. However, this is only theoretically correct, and only differential control can be achieved. Errors are widespread in component parameters, measurements and output links. The

impedance of the circuit cannot be obtained precisely and is not constant. For example, the resistance value is affected by temperature, while the reactance is affected by the current due to the saturation characteristics. Also, IGBTs have a deadband, leading to a difference between the reference voltage and the actual output value.

It is known that a PI controller is applied to perform difference-free tracking of signals with a non-time-varying steady state. Equation (2.2) represents the mathematical model of CHB-BESS in a three-phase stationary frame of reference. The physical meaning of the model is clear, and the system description is intuitive. However, the variables in the equation are time variables, which is not conducive to the application of the PI controller. The model should be transformed into one in the dq rotating frame of reference to facilitate the controller's application.

We can use the transforming array $\boldsymbol{T}_{\text{abc-dq}}$ shown in Equation (2.4) and array $\boldsymbol{T}_{\text{dq-abc}}$ shown in Equation (2.5) to transform a variable from the three-phase stationary frame of reference to the dq rotating frame of reference in which d axis coincides with u_{sa}, and conversely transform the variable.

$$\boldsymbol{T}_{\text{abc-dq}} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.4}$$

$$\boldsymbol{T}_{\text{dq-abc}} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.5}$$

Based on Equation (2.4) and (2.5), Equation (2.6) and then Equation (2.7) can be derived.

$$\boldsymbol{T}_{\text{abc-dq}} \frac{\mathrm{d}\boldsymbol{T}_{\text{abc-dq}}^{-1}}{\mathrm{d}t} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \tag{2.6}$$

$$\boldsymbol{T}_{\text{abc-dq}} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\text{a}} \\ i_{\text{b}} \\ i_{\text{c}} \end{bmatrix} = \boldsymbol{T}_{\text{abc-dq}} \frac{\mathrm{d}}{\mathrm{d}t}\left(\boldsymbol{T}_{\text{abc-dq}}^{-1}\boldsymbol{T}_{\text{abc-dq}}\begin{bmatrix} i_{\text{a}} \\ i_{\text{b}} \\ i_{\text{c}} \end{bmatrix}\right)$$

$$= \boldsymbol{T}_{\mathrm{abc-dq}} \frac{\mathrm{d}\boldsymbol{T}_{\mathrm{abc-dq}}^{-1}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} + \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} + \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} \tag{2.7}$$

Where i_{d} and i_{q} are in the dq reference frame corresponding to i_{a}, i_{b} and i_{c}.

When $\boldsymbol{T}_{\mathrm{abc\text{-}dq}}$ is applied at both sides of Equation (2.2), the mathematical model of the BESS in the dq rotating frame of reference is obtained as Equation (2.8).

$$\begin{cases} L_{\mathrm{s}} \dfrac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} = -R_{\mathrm{s}} i_{\mathrm{d}} + \omega L_{\mathrm{s}} i_{\mathrm{q}} + u_{\mathrm{sd}} - u_{\mathrm{do}} \\ L_{\mathrm{s}} \dfrac{\mathrm{d}i_{\mathrm{q}}}{\mathrm{d}t} = -R_{\mathrm{s}} i_{\mathrm{q}} - \omega L_{\mathrm{s}} i_{\mathrm{d}} - u_{\mathrm{qo}} \end{cases} \tag{2.8}$$

Where u_{sd} and u_{sq} are in the dq reference frame corresponding to u_{sa}, u_{sb} and u_{sc}. u_{do} and u_{qo} are in the dq reference frame corresponding to u_{ao}, u_{bo} and u_{co}.

The Laplace transform of Equation (2.8) gives Equation (2.9).

$$\begin{cases} i_{\mathrm{d}} = \dfrac{1}{R_{\mathrm{s}} + sL_{\mathrm{s}}} (\omega L_{\mathrm{s}} i_{\mathrm{q}} + u_{\mathrm{sd}} - u_{\mathrm{do}}) \\ i_{\mathrm{q}} = \dfrac{1}{R_{\mathrm{s}} + sL_{\mathrm{s}}} (-\omega L_{\mathrm{s}} i_{\mathrm{d}} - u_{\mathrm{qo}}) \end{cases} \tag{2.9}$$

It can be seen that there are coupling terms of $\omega L_{\mathrm{s}} i_{\mathrm{q}}$ and $-\omega L_{\mathrm{s}} i_{\mathrm{d}}$ for i_{d} and i_{q}, respectively in Equation (2.9). Therefore, PI controllers are applied to decouple i_{d} and i_{q} as shown in Equation (2.10).

$$\begin{cases} (R_{\mathrm{s}} + sL_{\mathrm{s}}) i_{\mathrm{d}} = \left(K_{\mathrm{d}}^{\mathrm{P}} + \dfrac{K_{\mathrm{d}}^{\mathrm{I}}}{s} \right) \left(i_{\mathrm{d}}^{\mathrm{ref}} - i_{\mathrm{d}} \right) \\ (R_{\mathrm{s}} + sL_{\mathrm{s}}) i_{\mathrm{q}} = \left(K_{\mathrm{q}}^{\mathrm{P}} + \dfrac{K_{\mathrm{q}}^{\mathrm{I}}}{s} \right) \left(i_{\mathrm{q}}^{\mathrm{ref}} - i_{\mathrm{q}} \right) \end{cases} \tag{2.10}$$

where $i_{\mathrm{d}}^{\mathrm{ref}}$ and $i_{\mathrm{q}}^{\mathrm{ref}}$ are reference values of i_{d} and i_{q}, respectively. $K_{\mathrm{d}}^{\mathrm{P}}$, $K_{\mathrm{d}}^{\mathrm{I}}$, $K_{\mathrm{q}}^{\mathrm{P}}$ and $K_{\mathrm{q}}^{\mathrm{I}}$ are gain constants of PI controllers.

After substituting Equation (2.10) into Equation (2.8), we can derive Equation (2.11).

$$\begin{cases} u_{\mathrm{do}}^{\mathrm{ref}} = -\left(K_{\mathrm{d}}^{\mathrm{P}} + \dfrac{K_{\mathrm{d}}^{\mathrm{I}}}{s} \right) \left(i_{\mathrm{d}}^{\mathrm{ref}} - i_{\mathrm{d}} \right) + \omega L_{\mathrm{s}} i_{\mathrm{q}} + u_{\mathrm{sd}} \\ u_{\mathrm{qo}}^{\mathrm{ref}} = -\left(K_{\mathrm{q}}^{\mathrm{P}} + \dfrac{K_{\mathrm{q}}^{\mathrm{I}}}{s} \right) \left(i_{\mathrm{q}}^{\mathrm{ref}} - i_{\mathrm{q}} \right) - \omega L_{\mathrm{s}} i_{\mathrm{d}} \end{cases} \tag{2.11}$$

where $u_{\mathrm{do}}^{\mathrm{ref}}$ and $u_{\mathrm{qo}}^{\mathrm{ref}}$ are reference values of u_{do} and u_{qo}, respectively.

Based on Equations (2.9) and (2.11), the block diagram of decoupling PI control and the mathematical model is depicted in Figure 2.5. In this figure, K_G is the gain factor of the controllable voltage source.

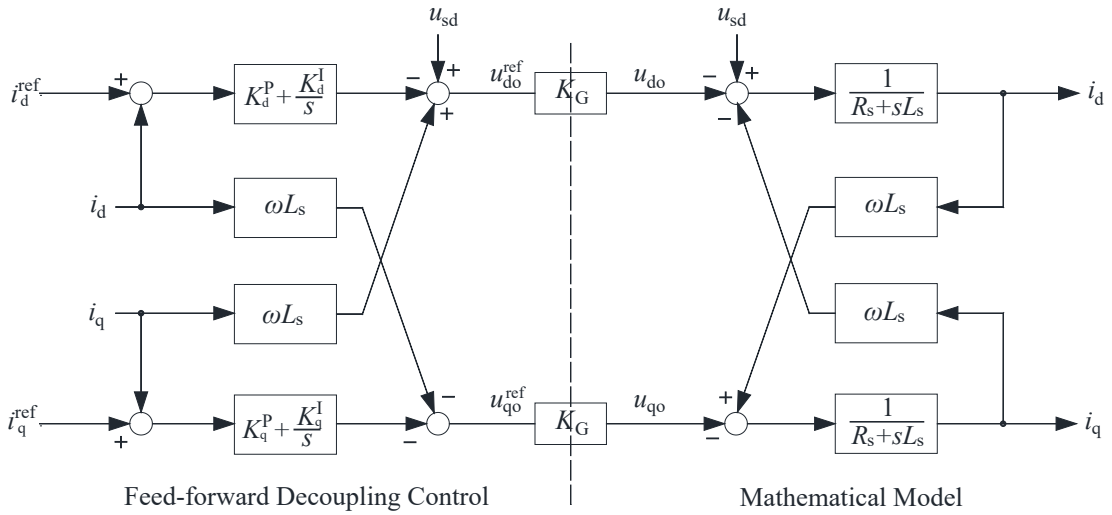


Figure 2.5 The block diagram of PI power decoupling control and the mathematical model.

According to the instantaneous power theory, the matrix expression for the active and reactive powers of the system in the dq rotating frame of reference is given by Equation (2.12).

$$\begin{bmatrix} P^{\mathrm{ref}} \\ Q^{\mathrm{ref}} \end{bmatrix} = \frac{3}{2}\begin{bmatrix} u_{\mathrm{sd}} & u_{\mathrm{sq}} \\ u_{\mathrm{sq}} & -u_{\mathrm{sd}} \end{bmatrix}\begin{bmatrix} i_{\mathrm{d}}^{\mathrm{ref}} \\ i_{\mathrm{q}}^{\mathrm{ref}} \end{bmatrix} \tag{2.12}$$

Where $P_{\mathrm{d}}^{\mathrm{ref}}$ and $Q_{\mathrm{q}}^{\mathrm{ref}}$ are reference values of P_{d} and Q_{q}, respectively.

As aforementioned, the vector $\boldsymbol{U}_{\mathrm{sa}}$ coincides with the d axis so that it can be derived that u_{sq}=0. Equation (2.13) can then be derived from Equation (2.12).

$$\begin{cases} i_{\mathrm{d}}^{\mathrm{ref}} = \dfrac{2P^{\mathrm{ref}}}{3u_{\mathrm{sd}}} \\ i_{\mathrm{q}}^{\mathrm{ref}} = -\dfrac{2Q^{\mathrm{ref}}}{3u_{\mathrm{sd}}} \end{cases} \tag{2.13}$$

Given P^{ref} and Q^{ref}, the reference currents $i_{\mathrm{d}}^{\mathrm{ref}}$ and $i_{\mathrm{q}}^{\mathrm{ref}}$ are found by Equation (2.13), and then the reference voltages $u_{\mathrm{do}}^{\mathrm{ref}}$ and $u_{\mathrm{qo}}^{\mathrm{ref}}$ are found by Equation (2.11). Finally, the reference voltages are used to drive the controllable voltage source after

transforming from dq rotating frame of reference to a three-phase stationary frame of reference. Based on the above analysis, the block diagram of the PI power decoupling control of CHB-BESS can be obtained, as shown in Figure 2.6. In the figure, PLL stands for Phase Locked Loop, while u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref} are reference values of u_{ao}, u_{bo} and u_{co}, respectively.

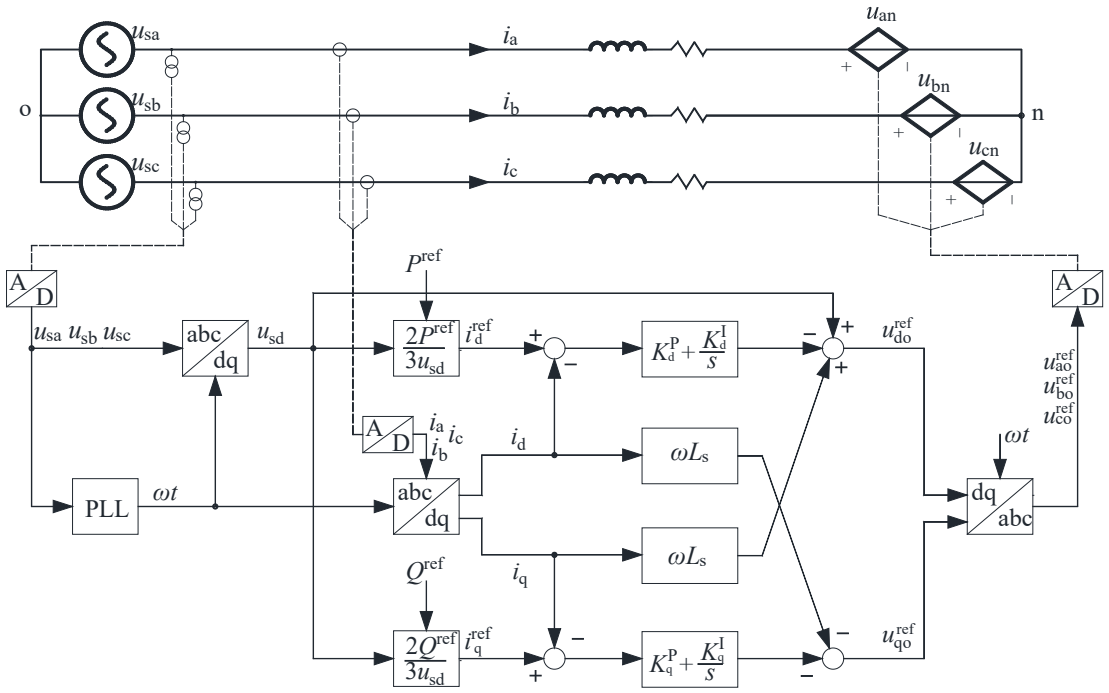


Figure 2.6 Block diagram of the PI power decoupling control of CHB-BESS.

As shown in Figure 2.6, normally u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref} are directly used to drive the controllable voltage source, which means that u_{no}^{ref}=0. However, this is not always the case. In some scenarios, such as inter-phase SOC balancing and fault-tolerance control, u_{no}^{ref} is not equal to 0 constantly, and thus the reference values u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} corresponding to u_{an}, u_{bn}, and u_{cn} should be derived from Equation (2.2). This is further investigated in Chapters 3 and 4.

As mentioned, the controllable voltage source consists of three groups of series H-bridge submodules. How to use the reference values u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} to determine the state of each submodule is exactly the problem solved by voltage modulation strategies, one of which is covered in detail in the next section.

2.3 Carrier Phase-Shifted Pulse Width Modulation

As shown in Figure 2.2, one H-bridge submodule consists of four semiconductor switches. The states of the four switches are ordered as S_1, S_2, S_3, and S_4, defining their values as 0 when the switch is off and 1 when it is on. The two switches of the same bridge arm in the submodule complement each other to avoid short and open circuits of the battery cluster. Thus, four operating states of the submodule are obtained. The correspondence between the submodule states and the states of its switches is given in Table 2.1. In the table, U_C denotes the capacitor voltage. Submodule states 1, -1, and 0 indicate the forward conduction, reverse conduction, and bypass of the submodule, respectively. Both '0' states are useful and can be used interchangeably to distribute each switch's burden evenly. For example, in the submodule state sequence '1010 → 1100 → 1010 → 0011 → 1010', each switch undergoes one open-close cycle, whereas in '1010 → 1100 → 1010 → 1100 → 1010 → 1010', switches 1 and 4 have no action, while switches 2 and 3 undergo two open-close cycles.

Table 2.1 Correspondence between the state of the submodule and the state of its four switches

States of Switches				Output Voltage u_{out}	Submodule State	Corresponding Circuits
S_1	S_2	S_3	S_4			
1	0	1	0	U_c	1	2.6 (a)
0	1	0	1	$-U_c$	-1	2.6 (b)
1	1	0	0	0	0	2.6 (c)
0	0	1	1	0	0	2.6 (d)

Figure 2.7 gives the conduction circuits of the submodule in the four states. It can be seen that each state corresponds to two circuits, and whether the current flows through the IGBT or the FD of a particular switch is determined by the direction of the current.

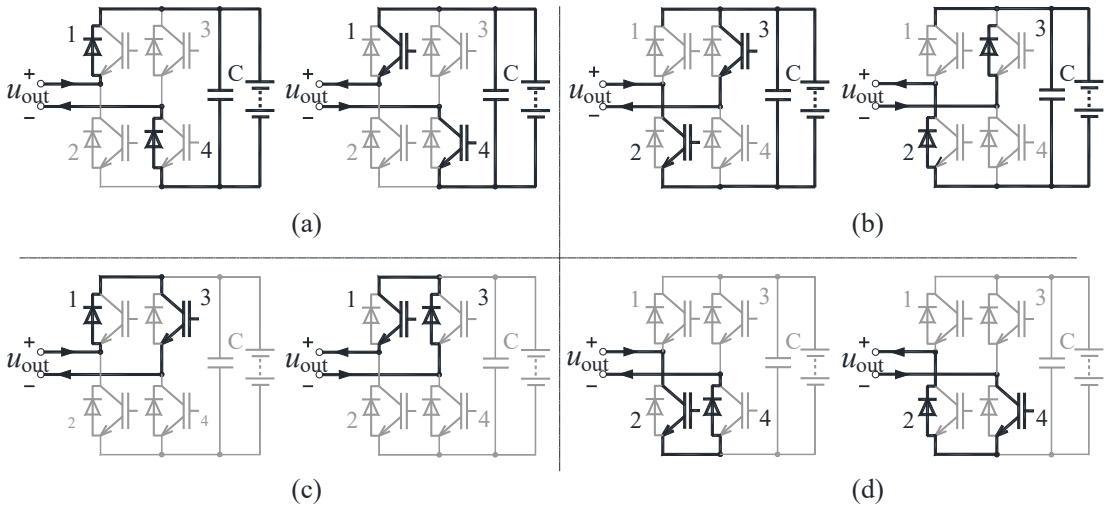


Figure 2.7 Conducted circuits of a submodule in a certain state.
(a) Forward conducting state. (b) Reverse conducting state. (c) One bypassed state. (d) The other bypassed state.

According to the above analysis, for a CHB-BESS with a cascaded number *N*, its output voltages can be expressed as Equation (2.14).

$$\begin{cases} u_{\mathrm{an}} = \sum_{i=1}^{N} S_{\mathrm{a}i} U_{ai}^{\mathrm{cap}} \\ u_{\mathrm{bn}} = \sum_{i=1}^{N} S_{\mathrm{b}i} U_{\mathrm{b}i}^{\mathrm{cap}} \\ u_{\mathrm{cn}} = \sum_{i=1}^{N} S_{\mathrm{c}i} U_{ci}^{\mathrm{cap}} \end{cases} \tag{2.14}$$

Where $S_{\mathrm{a}i}$, $S_{\mathrm{b}i}$ and $S_{\mathrm{c}i}$ are for the state of *i*-th submodule in the A, B and C phases, respectively, while U_{ai}^{cap}, $U_{\mathrm{b}i}^{\mathrm{cap}}$and U_{ci}^{cap} separately stand for the capacitor voltage of *i*-th submodule in the A, B and C phases.

In most cases, it is impossible to use reference values of u_{an}, u_{bn} and u_{cn} along with Equation (2.14) to solve for submodule states. However, we can even derive values of submodule states in a short time. These values are continuous between -1 and 1 and are the so-called duty cycles of the submodules. There are countless groups of values of submodule duty cycles for certain reference values of u_{an}, u_{bn} and u_{cn}. The voltage modulation strategies solve the problem of selecting exactly one group of values.

As introduced in Section 1.3.6, there are many voltage modulation strategies for CHB-BESS. Among them, the carrier phase-shift pulse-width modulation (PS-PWM) is simple, has superior performance, reliable operation, and can output higher switching frequency under the premise of lower switching frequency of the system, so it is almost only one commercially applied for CHB-BESS. Because unipolar PS-PWM is exclusively adopted for CHB-BESS in this research, this section describes it in detail. Thus, from here on in this thesis, PS-PWM refers specifically to unipolar one unless otherwise noted.

When PS-PWM is adopted, all the H-bridge submodules in one phase normally have the same voltage modulation waveform, and there is only a phase difference between the carrier waveforms of different submodules. The phase difference can be either $2\pi/N$ or π/N depending on how the carrier cluster is set, but they give the same result. Firstly, we need to normalize. $u_{\mathrm{an}}^{\mathrm{ref}}$, $u_{\mathrm{bn}}^{\mathrm{ref}}$ and $u_{\mathrm{cn}}^{\mathrm{ref}}$ to get modulation voltages based on the sum of the capacitor voltages of the sub-modules in each phase according to equation (2.15).

$$\begin{cases} u_{\mathrm{an}}^{\mathrm{mod}} = \dfrac{u_{\mathrm{an}}^{\mathrm{ref}}}{\sum_{i=1}^{N} U_{\mathrm{a}i}^{\mathrm{cap}}} \\ u_{\mathrm{bn}}^{\mathrm{mod}} = \dfrac{u_{\mathrm{bn}}^{\mathrm{ref}}}{\sum_{i=1}^{N} U_{\mathrm{c}i}^{\mathrm{cap}}} \\ u_{\mathrm{cn}}^{\mathrm{mod}} = \dfrac{u_{\mathrm{bn}}^{\mathrm{ref}}}{\sum_{i=1}^{N} U_{\mathrm{c}i}^{\mathrm{cap}}} \end{cases} \tag{2.14}$$

Where $u_{\mathrm{an}}^{\mathrm{mod}}$, $u_{\mathrm{bn}}^{\mathrm{mod}}$ and $u_{\mathrm{cn}}^{\mathrm{mod}}$ are modulation voltages.

The triangular wave function with a magnitude equal to 1 can be expressed by Equation (2.15).

$$\mathrm{tri}(\omega_{\mathrm{c}}t) = \begin{cases} -1 + \dfrac{2}{\pi}(\omega_{\mathrm{c}}t - 2k\pi) & \omega_{\mathrm{c}}t \in [2k\pi, (2k+1)\pi) \\ 3 - \dfrac{2}{\pi}(\omega_{\mathrm{c}}t - 2k\pi) & \omega_{\mathrm{c}}t \in [(2k+1)\pi, 2(k+1)\pi) \end{cases} \tag{2.15}$$

Where ω_{c} is for the angle frequency of the function and k is an integer not less than 0.

Based on the concept of PS-PWM, we can take tri($\omega_c t$-2π(i-1)/N) as the bipolar carriers of the i-th submodule in phases A, B or C. Then, we unipolar shift the bipolar carriers to obtain a group of unipolar carriers shown in Equation (2.16).

$$\mathrm{uni}\left(\omega_c t-\frac{2\pi(i-1)}{N}\right)=\frac{1+\mathrm{tri}\left(\omega_c t-\frac{2\pi(i-1)}{N}\right)}{2} \tag{2.16}$$

The state of the i-th submodule in phase A at the moment t can be derived from Equation (2.17). And $S_{bi}(t)$ and $S_{ci}(t)$ can be obtained when u_{an}^{mod} is replaced by u_{bn}^{mod} and u_{cn}^{mod} respectively.

$$S_{ai}(t)=\begin{cases}1 & u_{an}^{mod}(t)>\mathrm{uni}\left(\omega_c t-\frac{2\pi(i-1)}{N}\right)\\ -1 & u_{an}^{mod}(t)<-\mathrm{uni}\left(\omega_c t-\frac{2\pi(i-1)}{N}\right)\\ 0 & \text{else}\end{cases} \tag{2.17}$$

It is worth noting that in most cases, $S_{ai}(t)$, $S_{bi}(t)$, and $S_{ci}(t)$ derived from Equation (2.17) do not make u_{an}, u_{bn} and u_{cn} from Equation (2.14) separately equal to u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref}. However, the average values of u_{an}, u_{bn} and u_{cn} during several carrier cycle times are essentially equal to u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref}. Also, this is easy to prove mathematically, but it will not be discussed further here.

Figure 2.8 provides a relatively intuitive illustration of the basic principle of PS-PWM. In this figure, N=4 and thus, the phase shift between carriers is π/2. In practice, the carrier frequency is much higher than the power frequency in units often of kHz. Therefore, the modulation voltages vary little during a carrier cycle.

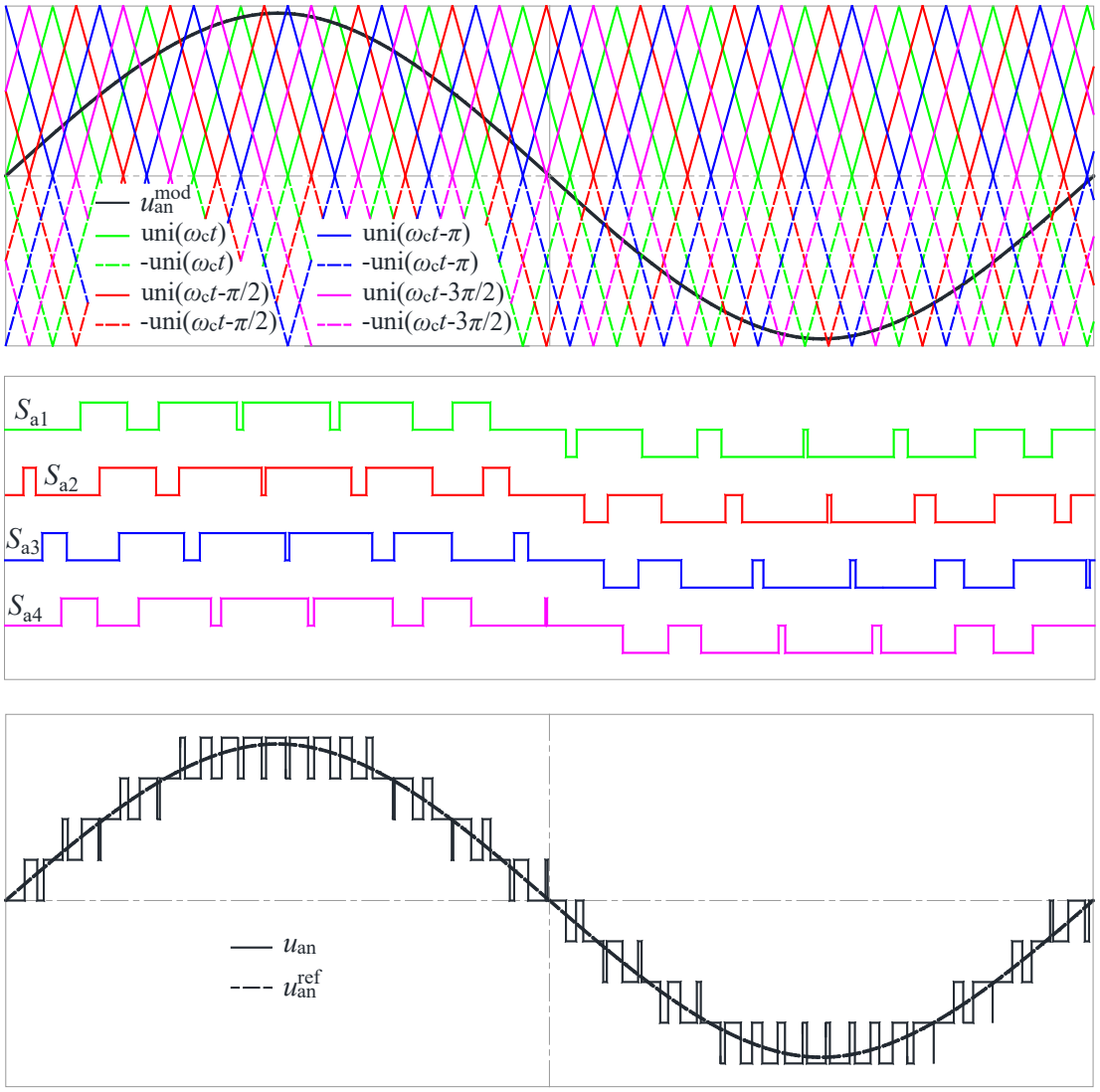


Figure 2. 8 Schematic diagram of PS-PWM basic principle

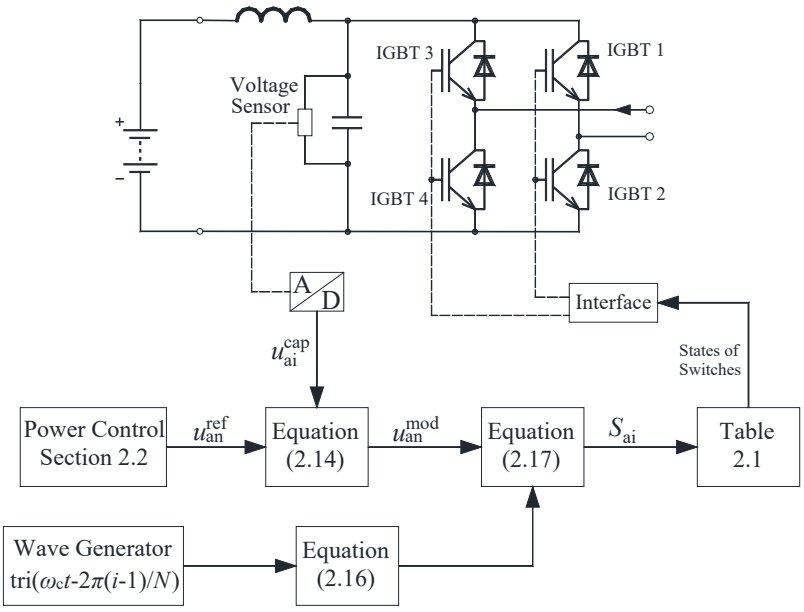


Figure 2.9 Implementation flow of PS-PWM

To summarize this section, the implementation flow of PS-PWM is shown in Figure 2.9.

PS-PWM is one of the voltage modulation strategies based on carriers, which means that analogue circuitries are commonly required to perform their function correctly. Another class of modulation strategies is not based on carrier signals and can, therefore, be implemented by microprocessors. Typical is Nearest Level Modulation (NLM) and its improved strategy. The basic principle of the NLM is straightforward - it outputs the value closest to the modulating voltage every sample cycle. Therefore, the switching frequency is very low, but the harmonic content is also relatively high. An improved NLM strategy (INLM) is based on minimizing the cumulative difference between the output voltage and the modulating voltage. This improved strategy increases the equivalent switching frequency and significantly reduces the harmonic content.

This research does not focus on modulation strategies, so only simulation results for the three modulation strategies are given here. And there is no quantitative comparison of the results because they have different applicable scenarios. A set of three-phase sinusoidal voltage signals is modulated using three separate methods. The main

parameters of the controllable voltage source and the modulating voltage are shown in Table 2.2, while the main parameters of the three modulation strategies are given in Table 2.3.

Table 2.2 Main Parameters of System Used for Comparison between Modulation Strategies.

Item	Value
Modulation Voltage Amplitude	9000 V
Frequency	50Hz
Cascaded Number of DC sources	9
Voltage of each DC source	1100V

Table 2.3 Main Parameters of the three Modulation Strategies.

Modulation Strategy	Carriers	Frequency
NLM	No	10kHz (Sampling)
INLM	No	10kHz (Sampling)
PS-PWM	Yes	1.5kHz (Carriers)

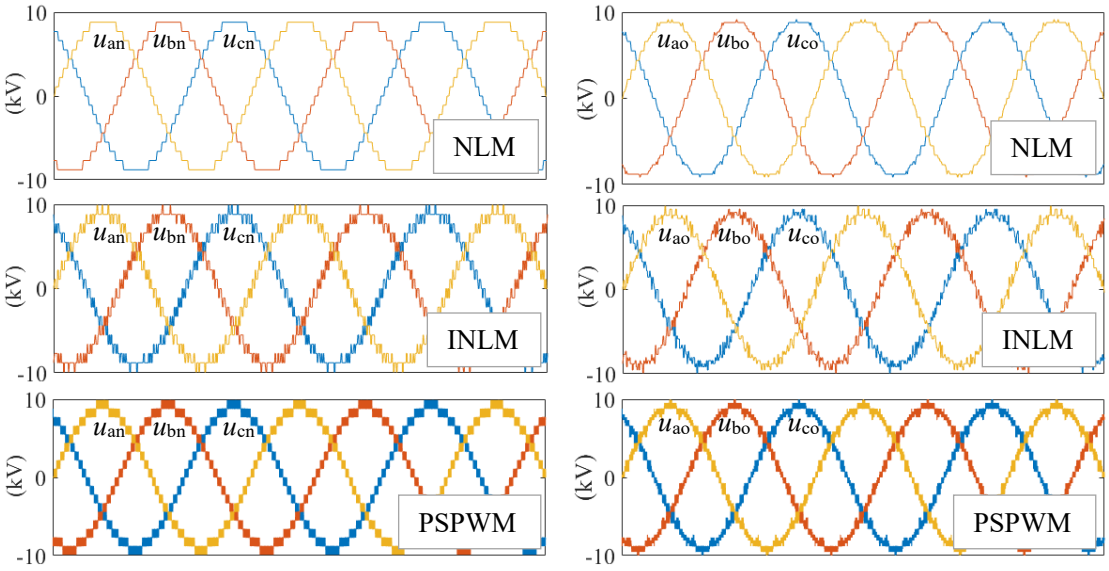


Figure 2.10 Output voltages of the controllable voltage source applied with the three modulation strategies, respectively.

Figures 2.10 and 2.11 show output voltages u_{an}, u_{bn}, u_{cn} and u_{ao}, u_{bo}, and u_{co} of the

controllable voltage source applied with NLM, INLM and PS-PWM respectively. Although the carrier frequency is only 1.5kHz, when PS-PWM is used for voltage modulation, the system presents the highest frequency and the harmonic voltages are easily filtered out, which can be inferred that the current quality will be more satisfactory. In the application of NLM, the switching frequency is the lowest, and the advantage of NLM will be more obvious as the number of controlled voltage source submodule cascades increases.

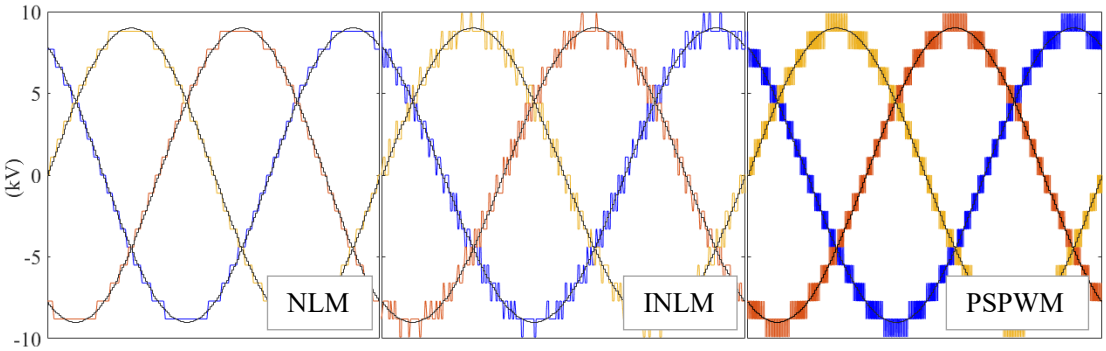


Figure 2.11 Comparison between modulation voltages and output voltages with the three modulation strategies, respectively.

Figure 2.12 shows the variation of cumulative error modulation voltages and output voltages when using INLM.

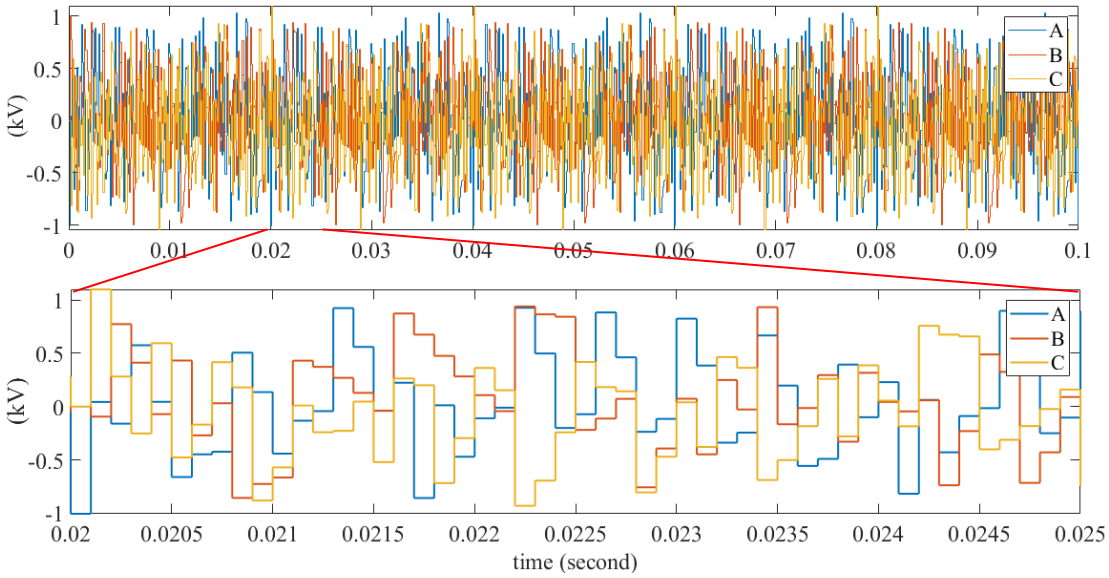


Figure 2.12 Cumulative errors modulation voltages and output voltages.

Chapter 3

Inter-Phase State of Charge Balancing Control for Cascaded H-Bridge Battery Energy Storage System

3.1 Introduction

Currently, renewable energy sources such as wind and solar energy are connected to the grid in large quantities, which increases the complexity of grid control and the risk of grid operation due to the uncertainty of their output. Battery storage systems (BESS) are widely used to solve these problems due to their easy siting, fast construction and regulation. The cascaded H-bridge (CHB) topology of the power conversion system (PCS) can directly connect low-voltage DC battery components to a medium-voltage or high-voltage grid without a step-up transformer. Furthermore, the equivalent switching frequency is high due to the high voltage levels in the cascaded topology. Thus, the system output waveform is more satisfactory, so this topology scheme is very promising and has received widespread attention.

Nevertheless, the topology of multiple submodules cascaded also complicates the control of CHB-PCS. Due to the inconsistencies caused by the battery production process and operation, CHB-PCS needs to keep the inter-phase SOC balanced during the control of the charging and discharging process to utilize the capacity of the batteries fully. To tackle this problem, the SOC balancing method by zero-sequence voltage injection has been widely researched because it does not affect the output inter-phase voltages or output power and is easy to calculate. However, in this method, to avoid overmodulation, the zero-sequence voltage amplitude is small or even zero when the DC-side voltage adequacy is low. Hence, the conventional zero-sequence voltage injection method is significantly influenced by the operational conditions of BESS,

leading to poor adaptability.

The conventional zero-sequence voltage injection method is prone to one-phase or two-phase voltage overmodulation, illustrated in Figure 3.1. When the inter-phase SOC is balanced, the modulation voltage vectors of the CHB-PCS are symmetrical as $\boldsymbol{U}_{ao}$, $\boldsymbol{U}_{bo}$, and $\boldsymbol{U}_{co}$. When the SOCs of the three phases are unbalanced and thus the zero-sequence voltage $\boldsymbol{U}_{no}$ is injected, the modulation voltage vectors are $\boldsymbol{U}_{an}$, $\boldsymbol{U}_{bn}$, and $\boldsymbol{U}_{cn}$. It can be seen that before and after the injection of zero-sequence voltage, the output three-phase voltages $\boldsymbol{U}_{ao}$, $\boldsymbol{U}_{bo}$, and $\boldsymbol{U}_{co}$ of the BESS remain unchanged and symmetrical. However, the real-part amplitude of modulation voltage $\boldsymbol{U}_{an}$ is significantly larger than that of previous modulation voltage $\boldsymbol{U}_{ao}$, which may exceed the DC side voltage, i.e., there is a risk of overmodulation. In the BESS design, the number of sub-modules cascaded in the PCS considers the effects of the minimum allowable batteries' voltage, system voltage fluctuation, and system voltage unbalance. Suppose further consideration is given to meet the need for inter-SOC balancing. In that case, it will inevitably increase the number of cascaded sub-modules and the cost of the whole system, so in practice, it is not considered to meet this condition. This means that when the system voltage reaches the maximum positive deviation, and the voltage of batteries is low, the zero-sequence voltage injection method can easily cause one- or two-phase voltage overmodulation. Through the above analysis, it can be seen that it is of practical significance to make full use of the DC side voltage to avoid voltage overmodulation during inter-phase SOC balancing.

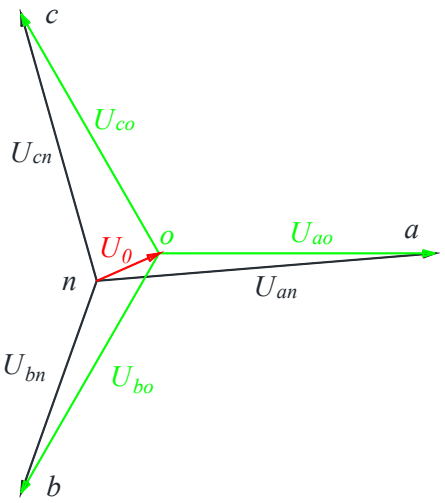


Figure 3.1 Vector diagram of conventional zero-sequence voltage injection method.

Maharjan et al. [16] applied the zero-sequence voltage injection method to inter-phase SOC balancing of BESS in 2009. This method has also been detailed in literature such as [17] and [58]. However, these studies maintain a fixed value for the proportional gain of the zero-sequence voltage amplitude, leading to the risk of overmodulation and underutilization of the DC-side voltage. An adaptive gain that adjusts to the BESS state is proposed in [20], but it lacks quantitative analysis and relies on empirical observations. Methods for calculating the maximum amplitude of the zero-sequence voltage are presented in [18] and [21], which can effectively avoid overmodulation. Nevertheless, the value is small when the adequacy of the DC-side voltage is low. Alaas et al. [34] introduced a method to achieve inter-phase SOC balancing by connecting energy storage capacitors to the neutral point through a three-phase half-bridge circuit. This approach maintains high efficiency even when the DC-side adequacy is low. However, it introduces additional hardware, increasing system costs.

Voltage Space Vector Modulation (SVM) can fully utilize the DC-side voltage compared to other modulation methods. Still, SVM is unsuitable for CHB-PCS because the number of voltage vectors in the CHB-PCS state is cubic to the number of levels [59]. The methods of injecting three-phase common-mode harmonics to achieve the equivalent DC-side voltage utilization as SVM in motor control have been widely

studied [60-63]. Among them, injecting a common-mode max-min average signal is straightforward, and the algorithm is simple. However, no literature has been found on BESS control using these methods.

In this chapter, one innovative self-adaptive inter-phase SOC control strategy for CHB-PCS is proposed, which applies to various modulation methods, such as carriers layer shift PMW (LS-PWM), carriers phase shift PWM (PS-PWM) and nearest level modulation (NLM). As well as not changing the inter-phase voltage and output power, this strategy can make inter-phase SOC equalization efficient even when the DC-side voltage is low.

The rest of the chapter is organized as follows. Section 3.2 investigates a modulation voltage calculation method based on injecting a max-min average signal, which can fully use the DC-side voltage. Section 3.3 briefly introduces the conventional inter-phase SOC balancing control strategy, namely the zero-sequence voltage injection method. This section elaborates on the principles of the proposed adaptive inter-phase SOC balancing strategy, analyzes its performance, and presents a detailed block diagram for its implementation. Simulation results are provided in Section 3.4 to validate the effectiveness of the proposed strategy. Finally, Section 3.5 concludes this chapter.

3.2 Further Investigation of the Method Improving DC-Side Voltage Utilization by Injecting Max-Min Average Signal

The three-phase equivalent circuit diagram of CHB-BESS is shown in Figure 2.3. The output voltage of each phase of the BESS is obtained by superposition of the output voltages of the sub-modules of that phase, as shown in Section 2.3. Equation (2.2) gives the mathematical model of CHB-BESS connected to the power grid in a three-phase stationary frame of reference.

It can be seen from Equations (2.2) and (2.14) that voltages u_{ao}, u_{bo} and u_{co} output from the CHB-BESS are synthesized by u_{no} with u_{an}, u_{bn} and u_{cn} respectively, while the amplitudes of u_{an}^{mod}, u_{bn}^{mod} and u_{cn}^{mod} determine the modulation ratio of each phase. Therefore, reasonable control of u_{no}^{ref} (variables marked with a superscript 'ref' denote the reference values of the original variables) to reduce the amplitude of u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} is a basic strategy to use the DC-side voltage fully and thus avoid overmodulation. It is worth noting that. u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} are not necessarily sinusoidally symmetrical, which is different from u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref}.

If u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref} are directly used as the modulation voltages, the DC-side voltage of the CHB-BESS is not effectively utilized. This is because the amplitude of line-to-line voltages is $\sqrt{3}$ times that of the line-to-ground voltages. This means that when the modulation voltage of one phase reaches its amplitude, the modulation voltages of the other two phases are less than their amplitude. Therefore, u_{no}^{ref} can be set reasonably so that the amplitude of u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} can be significantly reduced. The desired u_{no}^{ref} can be derived from Equation (3.1).

$$u_{no}^{ref} = \frac{\max\left(u_{ao}^{ref}, u_{bo}^{ref}, u_{co}^{ref}\right) + \min\left(u_{ao}^{ref}, u_{bo}^{ref}, u_{co}^{ref}\right)}{2} \tag{3.1}$$

After substituting the expressions of u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref}, u_{no}^{ref} can be obtained as (3.2), where U_{ko} is the amplitude of u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref}, ω is the power angle frequency, φ is the phase angle of u_{ao}^{ref} exceeding the grid voltage u_{sa} and i is 0 or a positive integer.

$$u_{no}^{ref} = \begin{cases} -\frac{U_{ko}}{2}\cos\left(\omega t + \varphi - \frac{2(1+i)\pi}{3}\right) & \frac{2i\pi}{3} \le \omega t + \varphi < \frac{(2i+1)\pi}{3} \\ -\frac{U_{ko}}{2}\cos\left(\omega t + \varphi - \frac{2i\pi}{3}\right) & \frac{(2i+1)\pi}{3} \le \omega t + \varphi < \frac{2(i+1)\pi}{3} \end{cases} \tag{3.2}$$

The expressions of u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} can be derived by the second row of Equation (2.2) substituted in Equation (3.2), and thus $U_{kn}=\sqrt{3}U_{ko}/2$ (U_{kn} is the amplitude of u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref}) can be easily obtained.

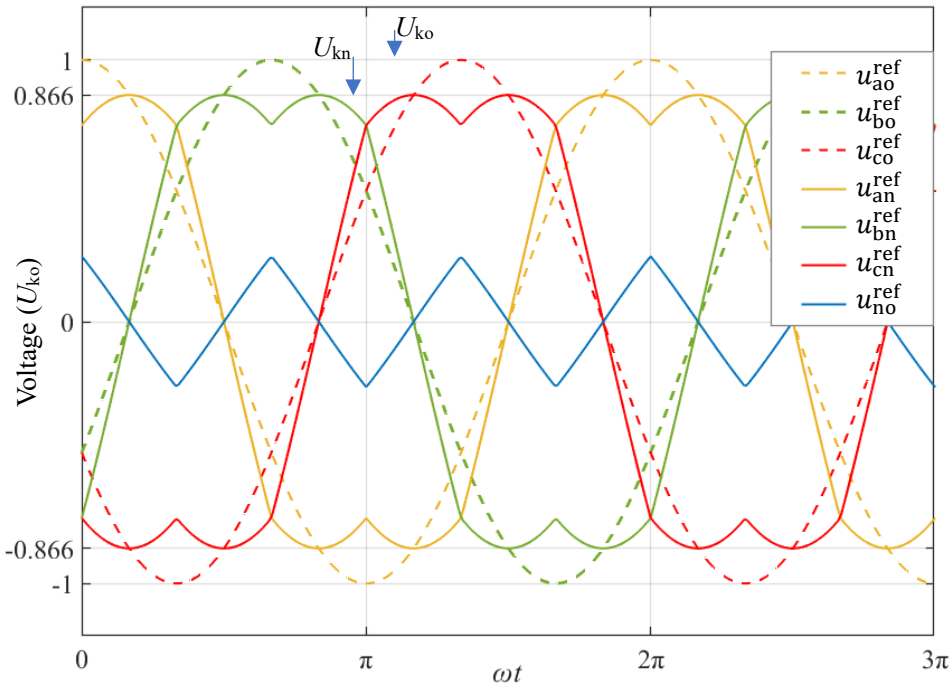


Figure 3. 2 Time-domain curves of voltages u_{ao}^{ref}, u_{bo}^{ref}, u_{co}^{ref}, u_{an}^{ref}, u_{bn}^{ref} and u_{cn}^{ref} after voltage injection at the neutral point, according to Equation (3.1).

Figure 3.2 shows the waveforms of relevant voltages. For ease of analysis, the voltage values in the figure are the normalized values of U_{ko} as the reference. It can be seen that compared to sinusoidal, u_{ao}^{ref}, u_{bo}^{ref} and u_{co}^{ref} as the modulation voltages, after setting the neutral voltage according to Equation (3.1), the DC-side voltage sufficiency of the BESS increases by 13.4% U_{ko}. It can be managed and used for inter-phase SOC equalization or submodule fault-tolerance control without voltage overmodulation.

To facilitate comparison, the variations of voltage vectors $\boldsymbol{U}_{ao}^{ref}$ and $\boldsymbol{U}_{a}^{ref}$ during an angle period of 4π are depicted in Figure 3.3, while Figure 3.4 shows the relationship of relevant voltage vectors in four angle periods after the neutral point is injected with voltage according to Equation (3.1). As shown in the two figures, the real part magnitude of $\boldsymbol{U}_{an}^{ref}$, $\boldsymbol{U}_{bn}^{ref}$ and $\boldsymbol{U}_{cn}^{ref}$ are significantly smaller than that of $\boldsymbol{U}_{ao}^{ref}$, $\boldsymbol{U}_{bo}^{ref}$ and $\boldsymbol{U}_{co}^{ref}$.

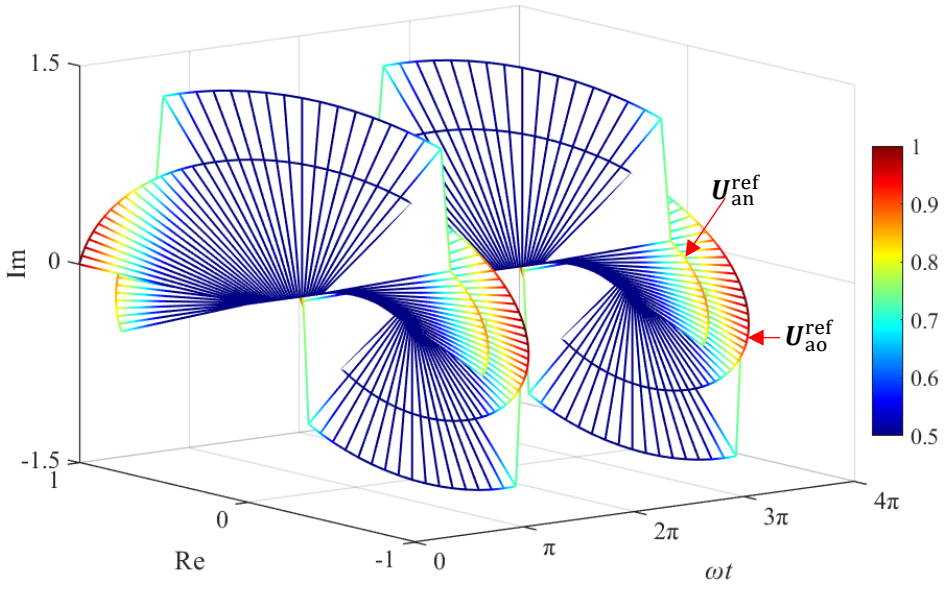


Figure 3.3 Variation of voltage vectors $\boldsymbol{U}_{ao}^{ref}$ and $\boldsymbol{U}_{an}^{ref}$ during an angle period of 4π after the neutral point is injected with voltage, according to Equation (3.1).

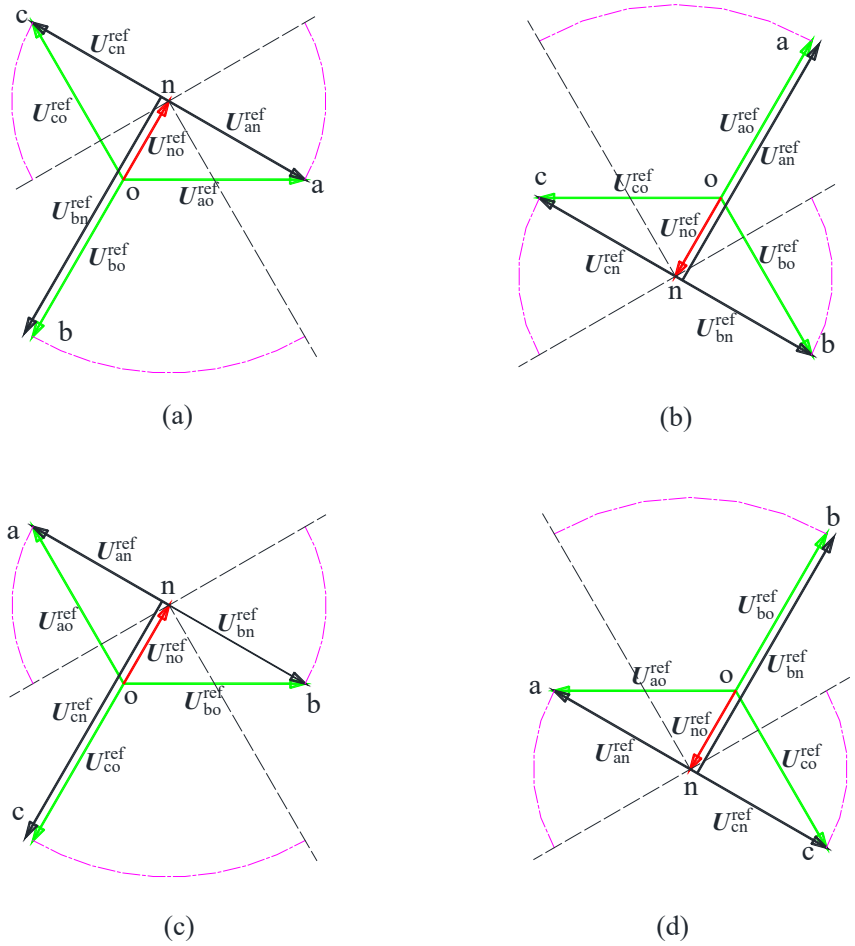


Figure 3. 4 The relationship of the relevant voltage vectors in four angle periods after the neutral point is injected with voltage according to Equation (3.1).

(a) $0\leq\omega t<\pi/3$. (b) $\pi/3\leq\omega t<2\pi/3$. (c) $2\pi/3\leq\omega t<\pi$. (d) $\pi\leq\omega t<4\pi/3$.

3.3 Inter-Phase SOC Balancing Control Strategy

This section first introduces the classical conventional inter-phase SOC balancing strategy in subsection 3.3.1, and then in subsection 3.3.2 a new balancing strategy is proposed and theoretically compared with the conventional strategy.

3.3.1 Conventional Inter-phase Balancing Control Method by Zero-Sequence Voltage Injection

The existing literature on inter-phase SOC equalization mainly focuses on the zero-sequence voltage injection method. The zero-sequence voltage injection method has clear ideas and simple algorithms, and most importantly, it does not change the external output characteristics of CHB-BESS.

A detailed description of the conventional zero-sequence voltage algorithm can be found in [1]-[3]. The SOC of each phase and SOC of BESS can be separately calculated through Equation (3.3) and (3.4). In the two equations, SOC_{ai}, SOC_{bi} and SOC_{ci} represent SOC of the i-th submodule in phases A, B and C, respectively, and BMS directly provides them. SOC_a, SOC_b and SOC_c are for SOC of phases A, B and C, respectively, while SOC_s are SOC of BESS.

$$\begin{cases} \mathrm{SOC_a} = \dfrac{\sum_{i=1}^{N} \mathrm{SOC_{a}}i}{N} \\ \mathrm{SOC_b} = \dfrac{\sum_{i=1}^{N} \mathrm{SOC_{b}}i}{N} \\ \mathrm{SOC_c} = \dfrac{\sum_{i=1}^{N} \mathrm{SOC_{c}}i}{N} \end{cases} \tag{3.3}$$

$$\mathrm{SOC_s} = \frac{\mathrm{SOC_a} + \mathrm{SOC_b} + \mathrm{SOC_c}}{3} \tag{3.4}$$

The magnitude and phase angle of injected zero-sequence voltage is shown in Equations (3.5), (3.6) and (3.7). In these equations, $\triangle SOC_a$, $\triangle SOC_b$ and $\triangle SOC_c$ are calculated through Equation (3.8), $\triangle SOC_m$ reacts to the dispersion degree of the SOC values of the three phases, δ is the phase angle of the A-phase current exceeds u_{sa}, v_0^{ref} denotes the zero-sequence voltage that needs to be injected, θ is the angle exceeding

u_{sa}, and K_0 is proportional gain.

$$\triangle \mathrm{SOC_m} = \sqrt{\triangle \mathrm{SOC_a^2} + \triangle \mathrm{SOC_b^2} + \triangle \mathrm{SOC_c^2}} \tag{3.5}$$

$$\theta = \begin{cases} \delta + \arctan \dfrac{\triangle \mathrm{SOC_b} - \triangle \mathrm{SOC_c}}{\sqrt{3} \triangle \mathrm{SOC_a}} & \triangle \mathrm{SOC_a} \neq 0 \\ \delta + \dfrac{\pi}{2} & \triangle \mathrm{SOC_a} = 0 \text{ and } \triangle \mathrm{SOC_b} > \triangle \mathrm{SOC_c} \\ \delta - \dfrac{\pi}{2} & \triangle \mathrm{SOC_a} = 0 \text{ and } \triangle \mathrm{SOC_b} < \triangle \mathrm{SOC_c} \end{cases} \tag{3.6}$$

$$v_0^{\mathrm{ref}} = K_0 \bullet \triangle \mathrm{SOC_m} \cos(\omega t + \theta) \tag{3.7}$$

$$\begin{cases} \triangle \mathrm{SOC_a} = \mathrm{SOC_s} - \mathrm{SOC_a} \\ \triangle \mathrm{SOC_b} = \mathrm{SOC_s} - \mathrm{SOC_b} \\ \triangle \mathrm{SOC_b} = \mathrm{SOC_s} - \mathrm{SOC_c} \end{cases} \tag{3.8}$$

The value of K_0 directly affects the inter-phase SOC balancing efficiency, which means a larger value can shorten the balancing time, but it tends to cause voltage overmodulation. If K_0 is too small, the balancing time will grow, and when the PCS output current is small, the effect will further deteriorate. It can be seen that the value of K_0 is limited by the maximum amplitude of the zero-sequence voltage that can be injected.

Quantitative research on the maximum zero-sequence voltage magnitude of the conventional zero-sequence injection method has been conducted in [5, 6]. However, no straightforward calculation method was proposed. This thesis gives a straight formula to calculate the value shown in Equation (3.9). Where $V_{0\max}^{(1)}$ denotes the maximum zero-sequence voltage magnitude of the conventional zero-sequence injection method, $U_{\mathrm{a}}^{\mathrm{cap}}$, $U_{\mathrm{b}}^{\mathrm{cap}}$ and $U_{\mathrm{c}}^{\mathrm{cap}}$ separately are calculated through Equation (3.10), denoting the DC-side voltages of phases A, B and C, R_{m} is the permissible maximum modulation ratio, and γ is the angle at which v_0^{ref} exceeds $u_{\mathrm{ao}}^{\mathrm{ref}}$.

$$V_{0\max}^{(1)} = \min\left(\begin{array}{c} \sqrt{\left(R_{\mathrm{m}}U_{\mathrm{a}}^{\mathrm{cap}}\right)^2 - U_{\mathrm{ko}}^2\sin^2\gamma} - U_{\mathrm{m}}\cos\gamma \\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{b}}^{\mathrm{cap}})^2 - U_{\mathrm{ko}}^2\sin^2\left(\gamma+\frac{2\pi}{3}\right)} - U_{\mathrm{m}}\cos\left(\gamma+\frac{2\pi}{3}\right) \\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{c}}^{\mathrm{cap}})^2 - U_{\mathrm{ko}}^2\sin^2\left(\gamma-\frac{2\pi}{3}\right)} - U_{\mathrm{m}}\cos\left(\gamma-\frac{2\pi}{3}\right) \end{array}\right) \tag{3.9}$$

$$\begin{cases} U_{\mathrm{a}}^{\mathrm{cap}} = \sum_{i=1}^{N} U_{ai}^{\mathrm{cap}} \\ U_{\mathrm{b}}^{\mathrm{cap}} = \sum_{i=1}^{N} U_{\mathrm{b}i}^{\mathrm{cap}} \\ U_{\mathrm{c}}^{\mathrm{cap}} = \sum_{i=1}^{N} U_{ci}^{\mathrm{cap}} \end{cases} \tag{3.10}$$

3.3.2 Innovative Self-Adaptive Inter-Phase State-of-Charge Balancing Control Strategy

The inter-phase SOC balancing control strategy proposed in this thesis is based on the injection of voltage at the neutral point according to Equation (3.2), followed by the injection of the zero-sequence voltage, the phase of which can be obtained from Equation (3.6). The maximum magnitude $V_{0\max}^{(2)}$ of the zero-sequence voltage is shown in Equation (3.11).

$$V_{0\max}^{(2)}=\min\left(\begin{array}{l}\sqrt{(R_{\mathrm{m}}U_{\mathrm{a}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma+\frac{\pi}{6}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma+\frac{\pi}{6}\right)\\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{a}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma-\frac{\pi}{6}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma-\frac{\pi}{6}\right)\\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{b}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma+\frac{5\pi}{6}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma+\frac{5\pi}{6}\right)\\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{b}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma+\frac{\pi}{2}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma+\frac{\pi}{2}\right)\\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{c}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma-\frac{\pi}{2}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma-\frac{\pi}{2}\right)\\ \sqrt{(R_{\mathrm{m}}U_{\mathrm{c}}^{\mathrm{cap}})^2-\frac{3}{4}U_{\mathrm{ko}}^2\sin^2\left(\gamma-\frac{5\pi}{6}\right)}-\frac{\sqrt{3}}{2}U_{\mathrm{ko}}\cos\left(\gamma-\frac{5\pi}{6}\right)\end{array}\right) \tag{3.11}$$

It can be seen from Equation (3.9) and (3.10) that the maximum zero-sequence voltage magnitudes that the two methods can inject are affected by $U_{\mathrm{a}}^{\mathrm{cap}}$, $U_{\mathrm{b}}^{\mathrm{cap}}$, $U_{\mathrm{c}}^{\mathrm{cap}}$, U_{ko} and the phase angle γ. To facilitate the analysis, we can set R_{m}=0.95, $U_{\mathrm{a}}^{\mathrm{cap}}$=$U_{\mathrm{b}}^{\mathrm{cap}}$=$U_{\mathrm{c}}^{\mathrm{cap}}$=$E$ and normalize the voltage quantities in the two equations by E. Figures 3.5, 3.6, 3.7 and 3.8 clearly and quantitatively show the advantages of the new strategy proposed in this paper over the conventional one. The curves in Figures 3.5 and 3.6 reflect the variation in the values of $V_{0\max}^{(1)}$ and $V_{0\max}^{(2)}$ with the angle γ and U_{ko}.

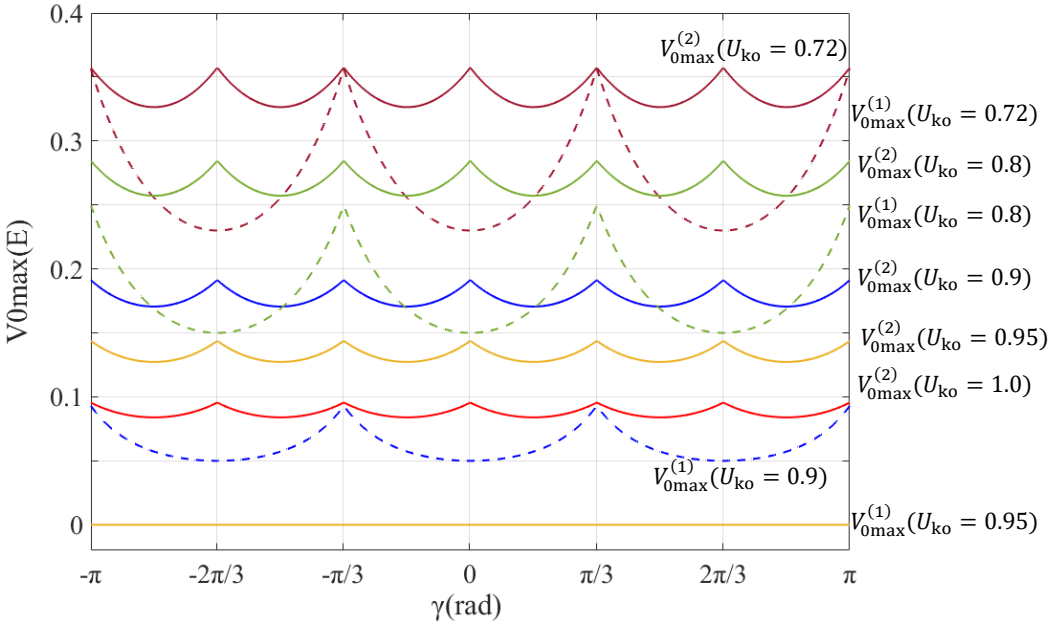


Figure 3.5 Values of $V_{0\max}^{(1)}$ and $V_{0\max}^{(2)}$ versus angle γ for U_{ko}=0.72, 0.8, 0.9, 0.95 and 1,

respectively.

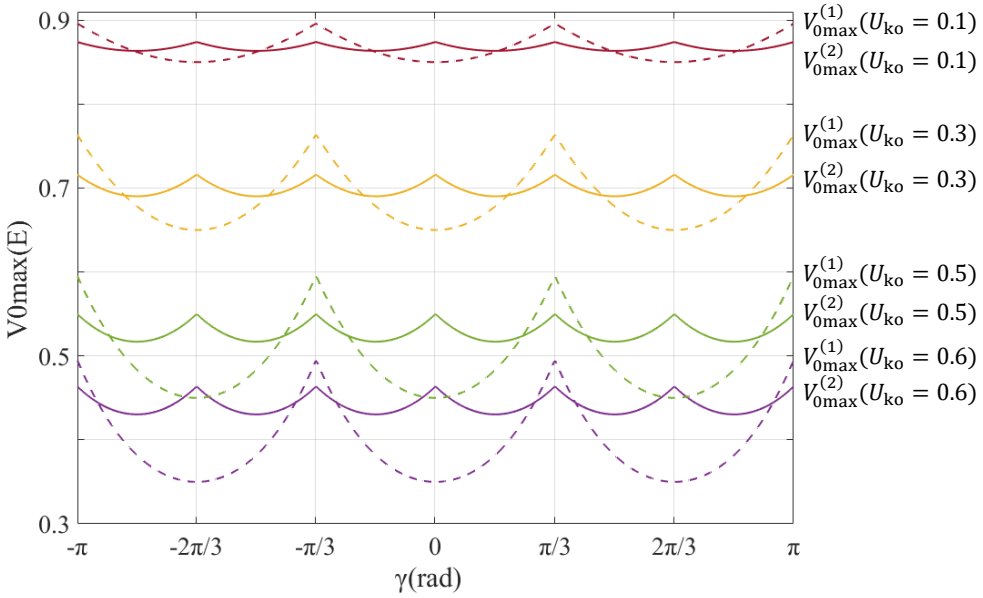


Figure 3. 6 Values of $V_{0max}^{(1)}$ and $V_{0max}^{(2)}$ versus angle γ for U_{ko}=0.1, 0.3, 0. 5 and 0.6, respectively.

From Figures 3.5 and 3.7, it can be seen that When U_{ko} is between 0.72E and 1E, $V_{0max}^{(2)}$ is significantly larger than $V_{0max}^{(1)}$ in the full range of values of the phase angle. When U_{ko}=0.8, $V_{0max}^{(2)}$ is about 1.5 times as large as $V_{0max}^{(1)}$; when Um = 0.9, $V_{0max}^{(1)}$ is only 0.05 at the lowest point, which means if the BESS is in low power operation, the balancing speed of the conventional method will be very slow, and even the equalization target cannot be achieved; when Um=0.95, $V_{0max}^{(1)}$=0, i.e., the conventional method fails, while $V_{0max}^{(2)}$ is about 0.134, so the new method is still able to carry out the inter-phase SOC balancing. It is worth noting that $V_{0max}^{(1)}$ takes relatively large values at γ = -π/3, π/3 and π. However, a practical algorithm should be universally adaptable and robust, so these points are not representative.

In comparison, when Um is between 0.1E and 0.6E, $V_{0max}^{(1)}$ is greater than $V_{0max}^{(2)}$ in the local range of γ, as evident from Figures 3.6 and 3.8. However, even in this case, when U_{ko}≥0.5E, $V_{0max}^{(2)}$ is still greater than $V_{0max}^{(1)}$ in most of the range of γ, it indicates that the new strategy still has certain advantages over the conventional approach. It is worth noting that in practical BESS scenarios, U_{ko} <0.5E is relatively uncommon.

The above analysis shows that the new strategy has a significant advantage over the conventional approach when the DC-side voltage is low. Even when the DC-side voltage is high, the new plan still has advantages over the conventional one.

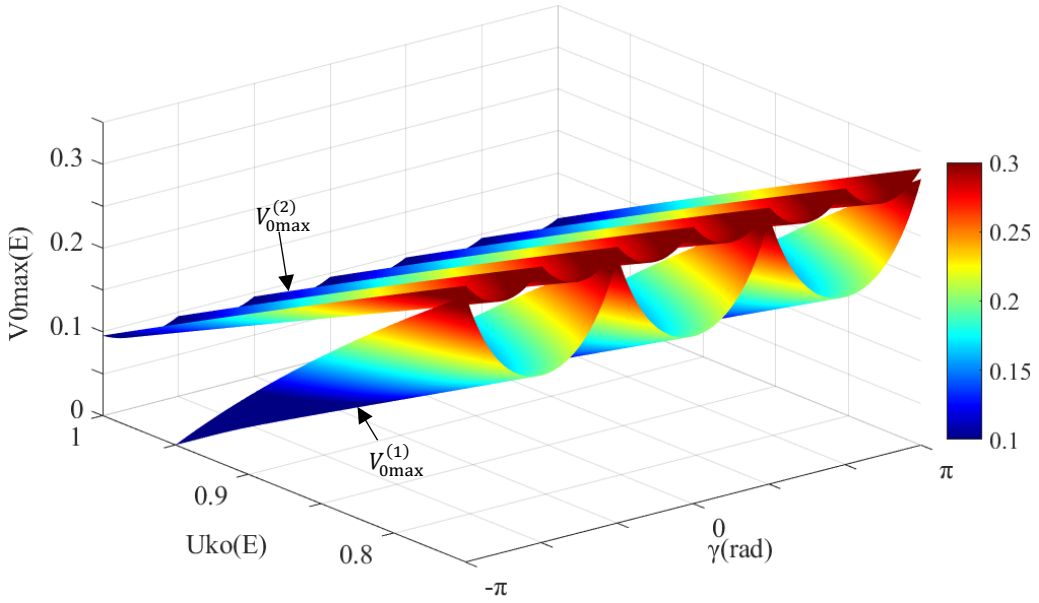


Figure 3.7 3D plots of $V_{0max}^{(1)}$ versus $V_{0max}^{(2)}$ values in the range $-\pi < \gamma \leq \pi$ and $0.72 \leq U_{ko} \leq 1$.

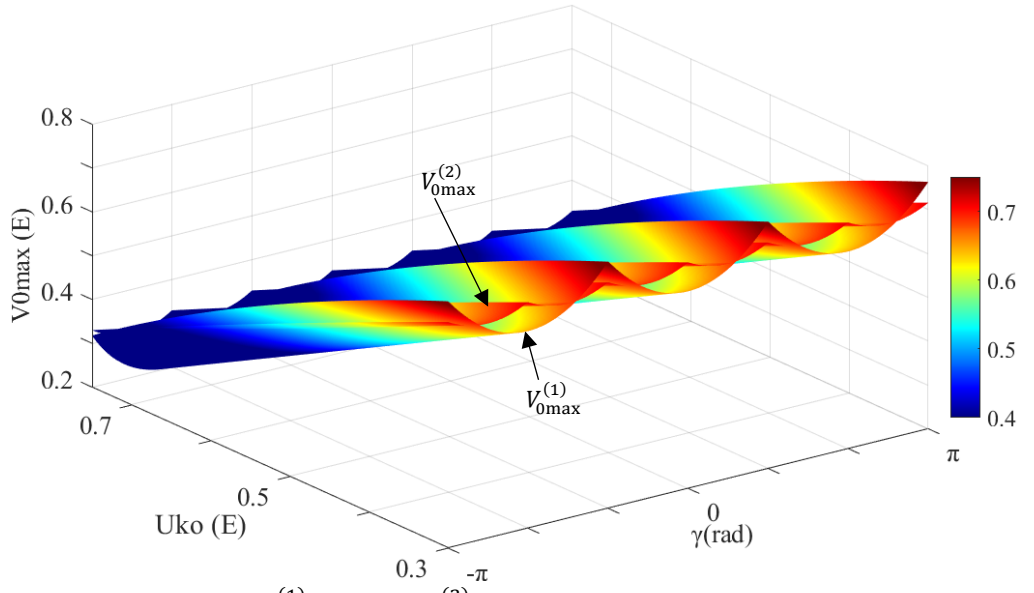


Figure 3. 8 3D plots of $V_{0max}^{(1)}$ versus $V_{0max}^{(2)}$ values in the range $-\pi < \gamma \leq \pi$ and $0.3 \leq U_{ko} \leq 0.72$.

Equation (3.11) also avoids overmodulation caused by blind selection of one more considerable K_0 value or low equalization efficiency caused by a zero-sequence voltage magnitude that is too small. Through Equation (3.9) and (3.11), it is possible to calculate the zero-sequence voltage amplitude according to U_a^{cap}, U_b^{cap}, U_c^{cap}, U_{ko} and γ in real-time and adapt to various operating conditions for inter-phase SOC balancing control

instead of setting a fixed proportional gain K_0. Compared with the fixed proportional gain K_0, this strategy is more adaptable and flexible. Therefore, this paper proposes to use Equation (3.12) instead of Equation (3.7) to calculate v_0^{ref}. It can be seen that when $\triangle \mathrm{SOCm} \geq 0.002$, it is calculated in real-time according to the actual state of the BESS to make full use of the DC-side voltage for SOC equalization. When $\triangle \mathrm{SOC_m} < 0.002$, the amplitude of v_0^{ref} decreases with $\triangle \mathrm{SOC_m}$ to achieve a soft landing of SOC balancing control.

$$v_0^{\mathrm{ref}} = \begin{cases} V_{0\max}\cos(\omega t + \theta) & \triangle \mathrm{SOC_m} > 0.002 \\ 500 \triangle \mathrm{SOC_m} V_{0\max}\cos(\omega t + \theta) & \triangle \mathrm{SOC_m} \leq 0.002 \end{cases} \tag{3.12}$$

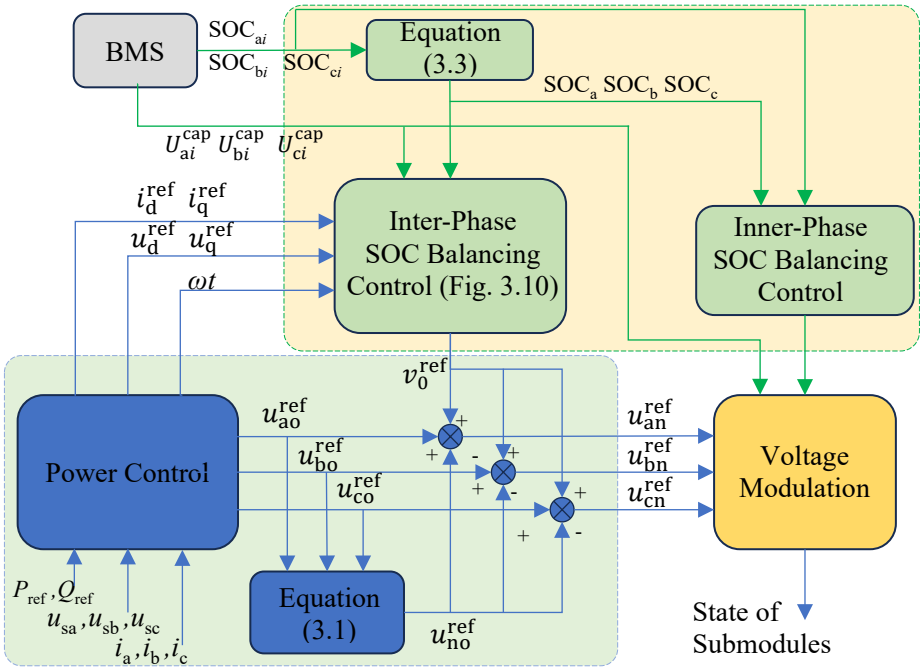


Figure 3. 9 The whole control block diagram for CHB-BESS with the proposed inter-phase SOC balancing control strategy.

Figure 3.9 illustrates the overall control strategy of CHB-PCS based on the inter-phase SOC control strategy proposed in this chapter. In the figure, N is the number of sub-modules cascaded in each phase, U_{ai}^{cap}, U_{bi}^{cap} and U_{ci}^{cap} (i=1,2...N) are the capacitor voltages of sub-modules within the A, B and C phases, respectively. The subscript 'ref' indicates the reference value. It can be seen that the whole control system is mainly divided into three parts: the power control subsystem, the SOC balance control

subsystem, and the modulation subsystem. Since the battery SOC changes relatively slowly, the SOC balance control subsystem can use a lower sampling frequency to reduce the computational burden of the microcontroller.

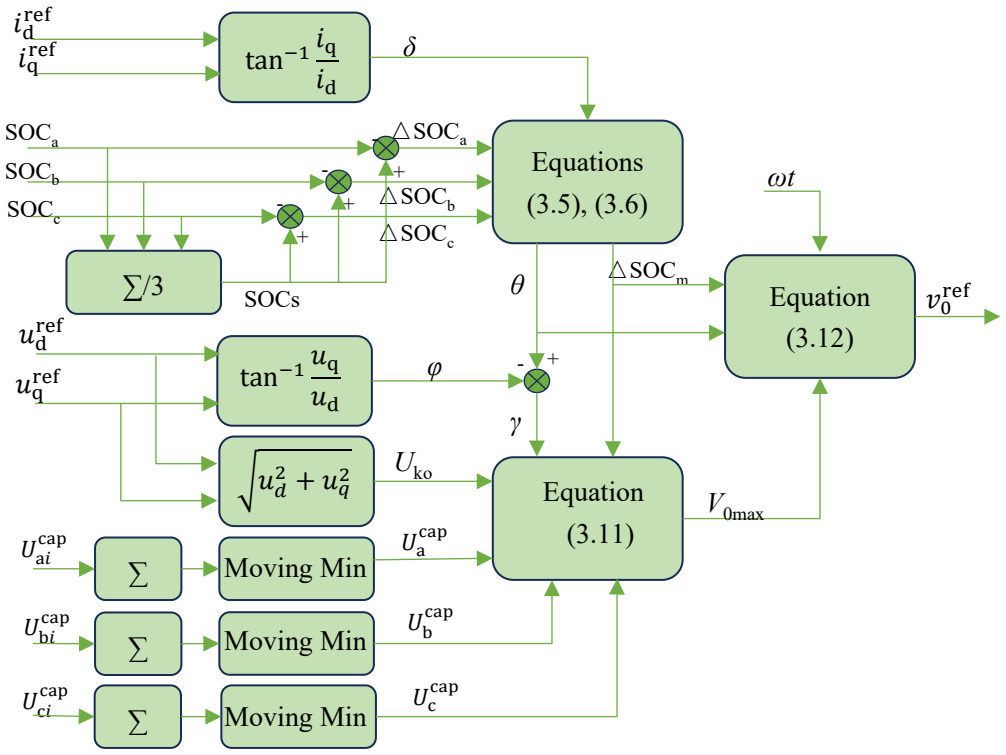


Figure 3. 10 Detailed block diagram of the proposed Inter-phase SOC balancing control strategy.

The detailed block diagram of the inter-phase SOC balancing control strategy proposed in this paper is given in Figure 3.10. Similarly, the sampling frequency of different regions can be further subdivided, e.g., zone ① should be the same as the sampling frequency of the power control subsystem, zone ② can have half of the sampling frequency of the power control subsystem, and zone ③ can have an even lower sampling frequency. This is further demonstrated in the simulation part of this chapter.

In addition, the voltages of sub-module capacitors fluctuate even during normal operation, so if the voltages are used as the basis of DC-side Voltages, V_{0max} has to be recalculated every sampling cycle. Replacing the real-time capacitance voltages with the sliding minima, U_a^{cap}, U_b^{cap}, U_c^{cap} and V_{0max} do not need to be recalculated every sampling cycle during the stable operation of the BESS, which can further reduce the

computational burden of the microcontroller.

3.4 Simulation Verification

In this section, the new inter-phase SOC balancing strategy proposed in section 3.3 is validated from simulation using Matlab/simulink. Subsection 3.4.1 describes the main parameters of the BESS system used for the simulation, while subsections 3.4.2 and 3.4.3 validate the effectiveness of the new strategy in terms of both power quality and equalisation efficiency, respectively.

3.4.1 Overview of the BESS Designed for Simulation

To verify the effectiveness of the control strategy proposed in this chapter, a 5MW/11.2MWh BESS connected to the 10kV grid is designed, and a model is built with Matlab/Simulink for simulation and calculation. The relevant parameters of the system are shown in Table 3.1. The system employs 280Ah Li-FePO4 battery cells with an insulation level of 1.5kV. The number of battery cells connected in series in each sub-module is 416, and the battery cluster voltage of each submodule is 1.04kV and 1.52kV for SOC of 0 and 1, respectively. In addition, the system can operate within the limits of the power capability chart in IEC 62933-1[63].

Table 3.1 Parameters of the BESS Designed

Parameter Name	Value
Grid Voltage (phase-to-phase, rms)	10kV
Fundamental Frequency	50Hz
Short-Circuit Capacity	200MVA
Capacity of Battery Cell (Lithium-Iron)	280Ah
Number of SMs per phase, N	10
Number of Battery Packs per SM	8
Number of Cells per Battery Pack	52
AC Coupling Inductor	15mH
Capacitor of SMs	10mF
Carrier Frequency	1.5kHz
Sampling Frequency of Power Control	10kHz
Sampling Frequency of Fig. 8 zone ①	10kHz
Sampling Frequency of Fig. 8 zone ②	5kHz
Sampling Frequency of Fig. 8 zone ③	1Hz

The technologically mature PI power decoupling control strategy in [4] is used for the Power Control part of the BESS. PS-PWM in [65] is adopted for the Modulation part, which is also discussed in detail in Chapter 2.

3.4.2 Waveform Quality of the Proposed Strategy

To verify the effectiveness of the method proposed in Section 3.3.2, the PCS output voltage and current quality are compared with that of the conventional method. For reliable conclusions, 80 power points spreading over four quadrants are selected within the power capability of the BESS. They are further classified into 160 comparison cases based on whether or not a zero-sequence voltage is injected. The chosen power points are shown in Figure 3.11.

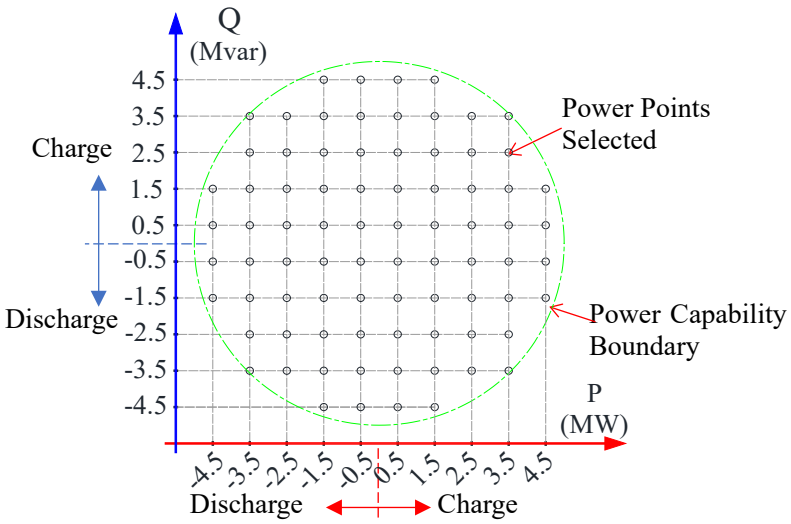
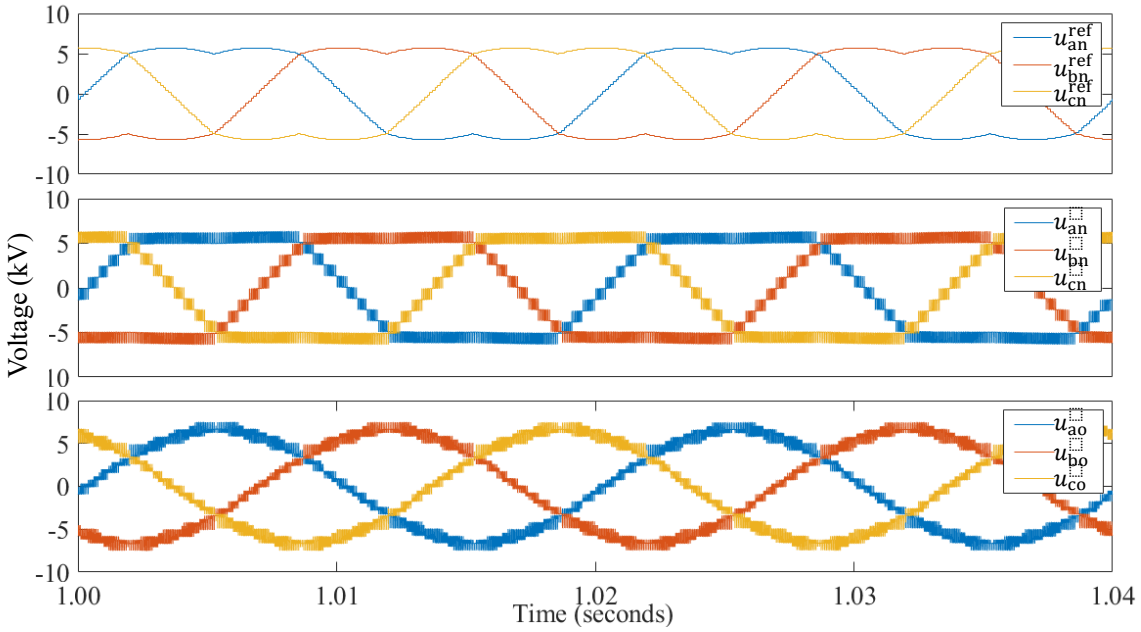


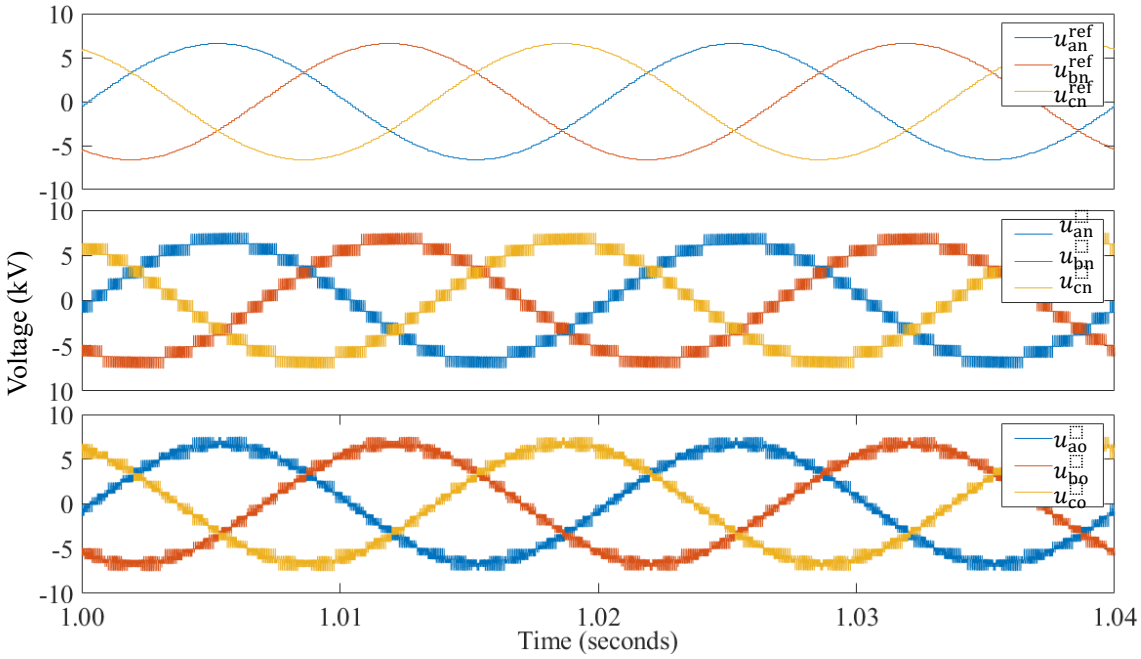
Figure 3.11 Power points were selected to compare the proposed strategy with the conventional one.

In Figure 3.11, the positive number represents the grid generating power, and the negative number represents the grid absorbing power. For comparison, the same zero-sequence voltage, with amplitude V_{0m}=2000V and phase $\varphi=\pi/6$, is injected in both strategies.

Figure 3.12 shows waveforms of u_{an}^{ref}, u_{bn}^{ref}, u_{cn}^{ref}, u_{an}, u_{bn}, u_{cn}, u_{ao}, u_{bo} and u_{co} without specified zero-sequence voltage injection when P=2.5MW and Q=3.5Mvar, while Figure 3.13 depicts waveforms of these voltages with specified zero-sequence voltage injection when P=2.5MW and Q=3.5Mvar.

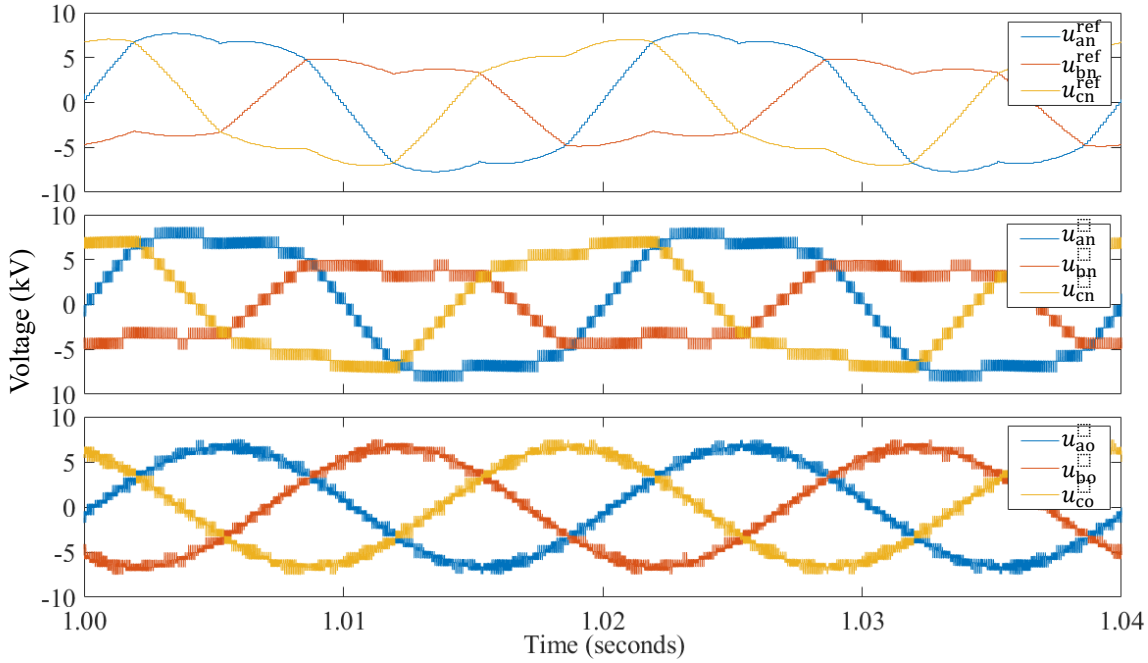


(a)

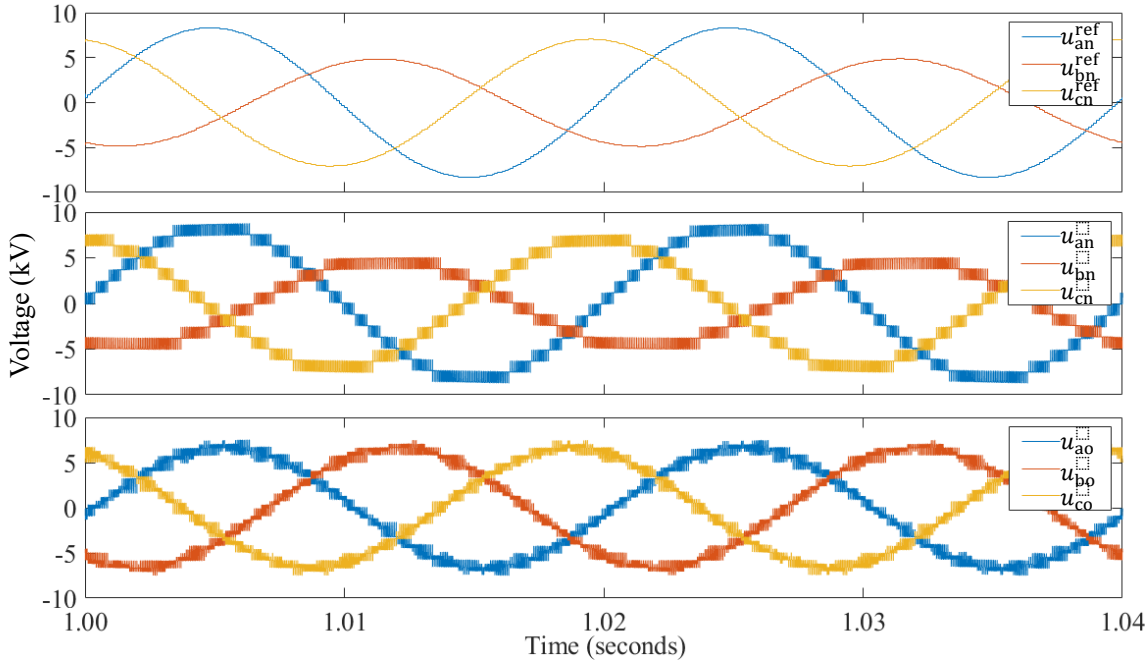


(b)

Figure 3.12 Waveforms of relevant voltages without zero-sequence voltage injection when P=2.5MW and Q=3.5Mvar.
(a) New strategy. (b) Conventional strategy.



(a)



(b)

Figure 3.13 Waveforms of relevant voltages with zero-sequence voltage injection when P=2.5MW and Q=3.5Mvar.
(a) New strategy. (b) Conventional strategy.

Figures 3.14 and 3.15 show the Total Harmonic Distortion (THD) distribution patterns of output voltage and current of the BESS in the two strategies. These figures show that the difference in current and voltage THD between the two schemes is negligible and

exhibits similar distribution patterns. The THD of the output current increases rapidly as the output current decreases. Regardless of the injection of zero-sequence voltage components, except for the four smallest comparison cases (P=±0.5MW, Q=±0.5Mvar), all output current THD values are less than 0.4%. Simultaneously, the THD values of all output voltages are between 5% and 10%, and overall, they significantly increase with the increase in Q. This is because the increase in Q leads to a decrease in modulation voltage, thereby reducing the voltage levels utilized in the output.

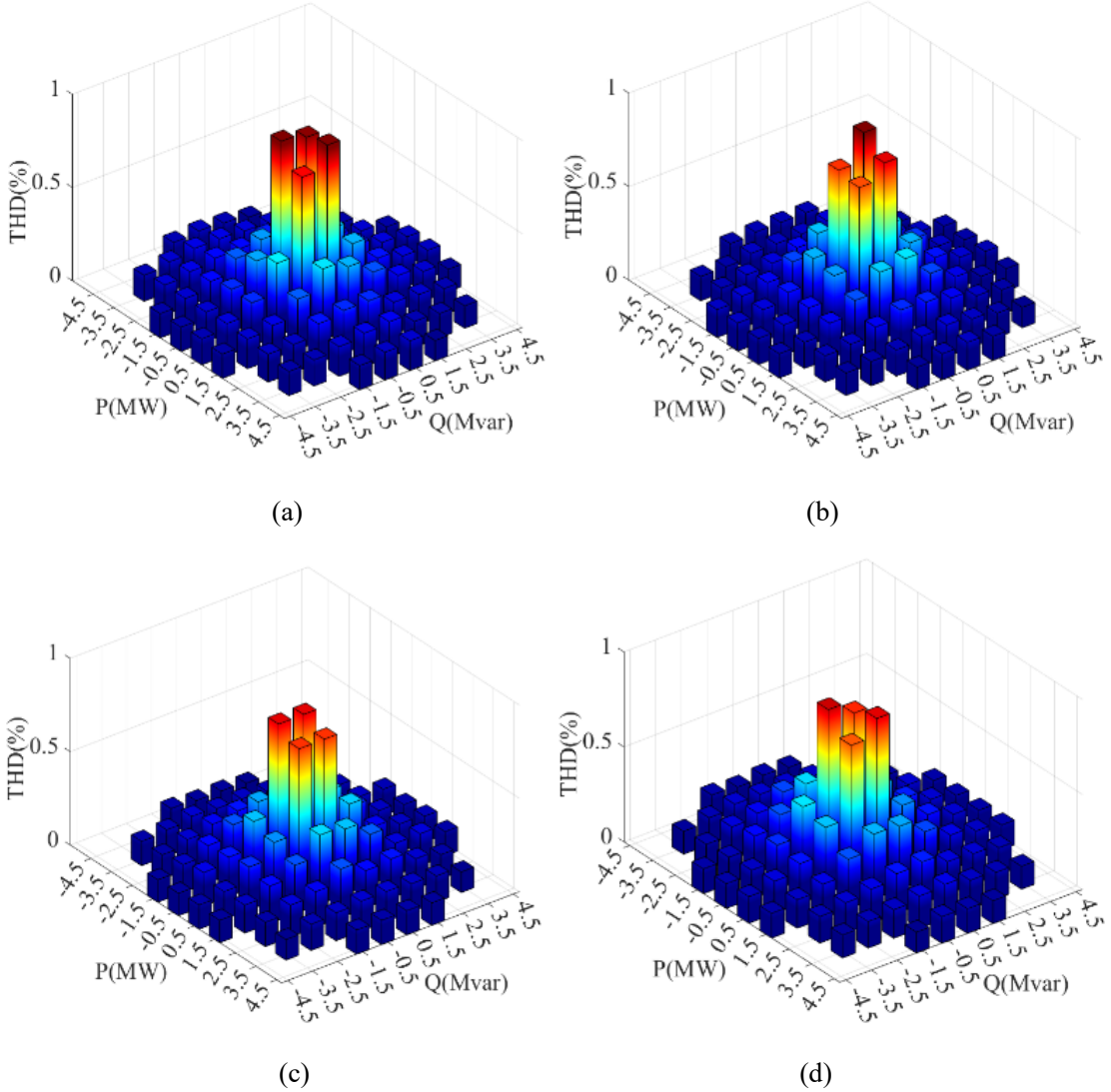


Figure 3. 14 THD distribution plot of the output current.
(a) New strategy without zero-sequence voltage injection. (b) Conventional strategy without zero-sequence voltage injection. (c) New strategy with zero-sequence voltage injection. (d) Conventional strategy with zero-sequence voltage injection.

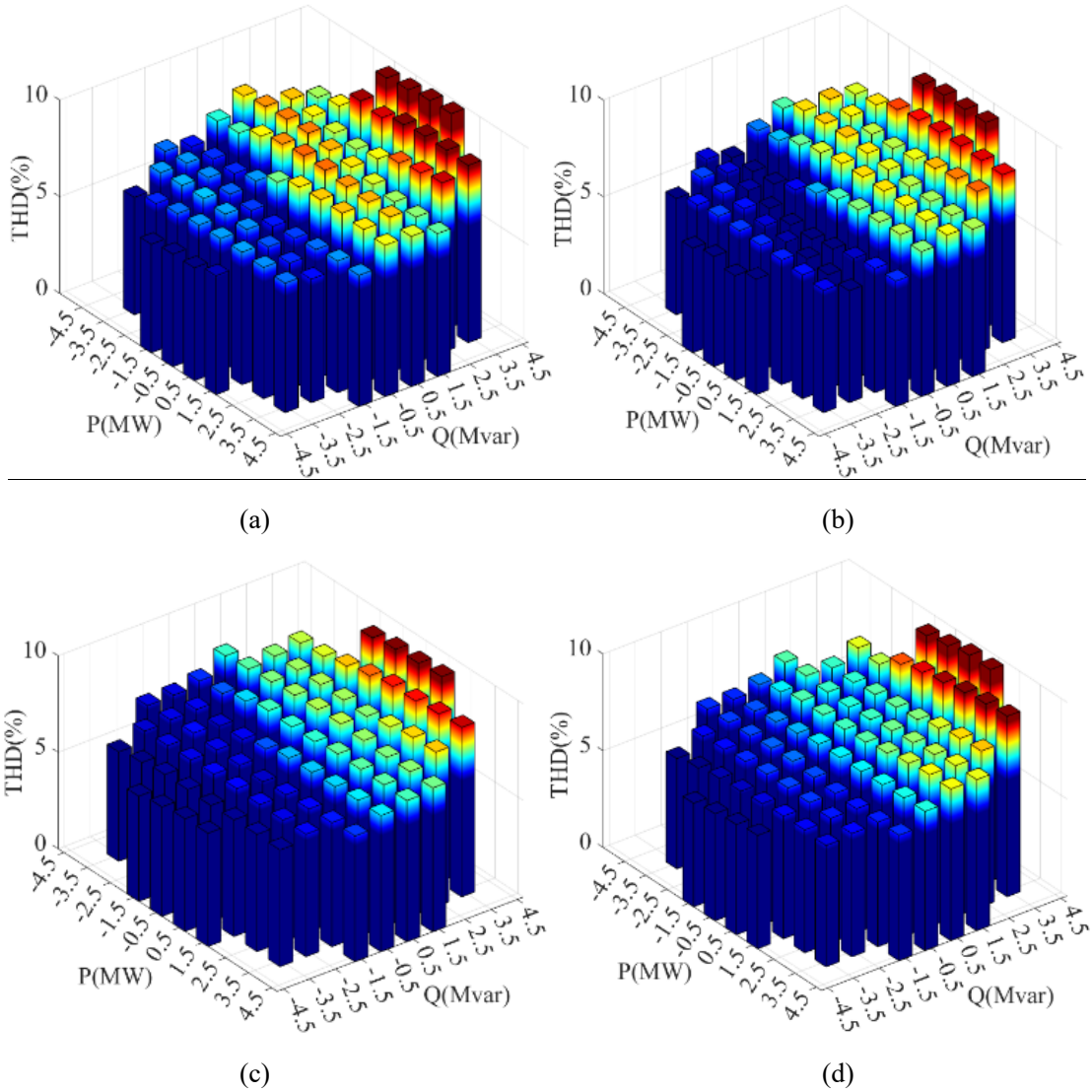


Figure 3.15 THD distribution plot of the output voltage.
(a) New strategy without zero-sequence voltage injection. (b) Conventional strategy without zero-sequence voltage injection. (c) New strategy with zero-sequence voltage injection. (d) Conventional strategy with zero-sequence voltage injection.

Table 3.2 provides the average output current and voltage THD values for all power points under the proposed and conventional strategies.

Table 3.2 Average Values of Output Current and Voltage THD

Item Name	Average THD of Currents	Average THD of Voltages
Proposed Strategy without Zero-Sequence Voltage Injection	0.224% Figure 3.14(a)	7.49% Figure 3.15(a)
Conventional Strategy without Zero-Sequence Voltage Injection	0.214% Figure 3.14(b)	7.19% Figure 3.15 (b)
Proposed Strategy with Zero-Sequence Voltage Injection	0.211% Figure 3.14(c)	7.03% Figure 3.15 (c)
Conventional Strategy with Zero-Sequence Voltage Injection	0.212% Figure 3.14(d)	7.21% Figure 3.15 (d)

3.4.3 Effectiveness of the Proposed Strategy

To validate the newly proposed inter-phase State of Charge (SOC) balancing strategy in Section 3.3.2, two scenarios of BESS operation were established and compared with the conventional scheme mentioned in Section 3.3.1. For a comprehensive comparison between the two approaches, the initial SOC of the BESS is relatively large in Scenario I. Conversely, in Scenario II, the initial SOC of the BESS system is relatively small. The maximum voltage modulation ratio allowed for both scenarios is set at 0.95, and the BESS systems operate for 15 minutes, with active and reactive reference values following the pattern shown in Figure 3.16. The main settings for the two scenarios are summarized in Table 3.3.

Table 3.3 Key Setting for the Two Scenarios

Scenario No.	I	II
Reference Values of P, Q	Performed as Fig. 13	
Maximum Modulation Ratio Mm	0.95	0.95
Initial Value of SOCa	48%	5%
Initial Value of SOCb	45%	7%
Initial Value of SOCc	40%	10%

To validate the applicability of the new strategy under various operating conditions, the reference values for active and reactive power change every 2 minutes, totalling seven different situations. These situations encompass various charging and discharging conditions for active and reactive power.

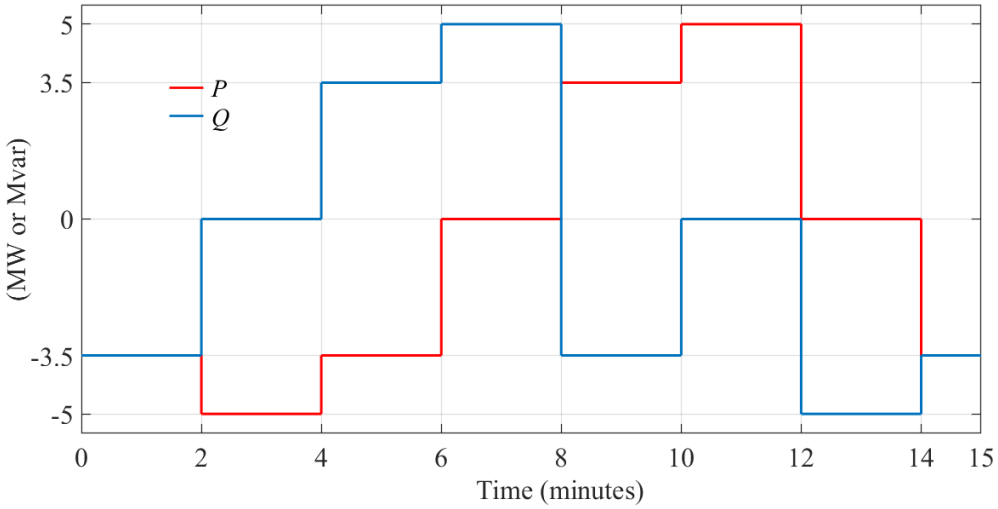


Figure 3.16 Reference values of exchanged active and reactive power between BESS and the grid for the two scenarios

Figures 3.17 and 3.18 illustrate the amplitude of injected zero-sequence voltage, changes in three-phase SOC, and imbalance magnitude $\triangle SOC_m$ for the two strategies under two operating scenarios. It can be observed that, in both scenarios, the new strategy proposed in this paper is more efficient than the conventional approach. In Scenario I, the efficiency advantage of the new strategy is insignificant, achieving the balancing goal at 10.8 minutes, while the conventional strategy accomplishes it at 11.9 minutes. In contrast, in Scenario II, the new strategy achieves the balancing goal at 8.1 minutes, while the conventional approach fails to do so within the 15-minute timeframe. The new strategy has a significant advantage over the conventional approach when the SOC is low, as the system's DC-side voltage adequacy is smaller at lower SOC. It is worth noting that, in Scenario II, the conventional approach becomes completely ineffective during the 0-2 and 12-15-minute intervals due to zero-sequence voltage amplitude being 0. Therefore, the effectiveness of the new strategy is less affected by SOC and operating conditions compared to the conventional approach, demonstrating

greater adaptability.

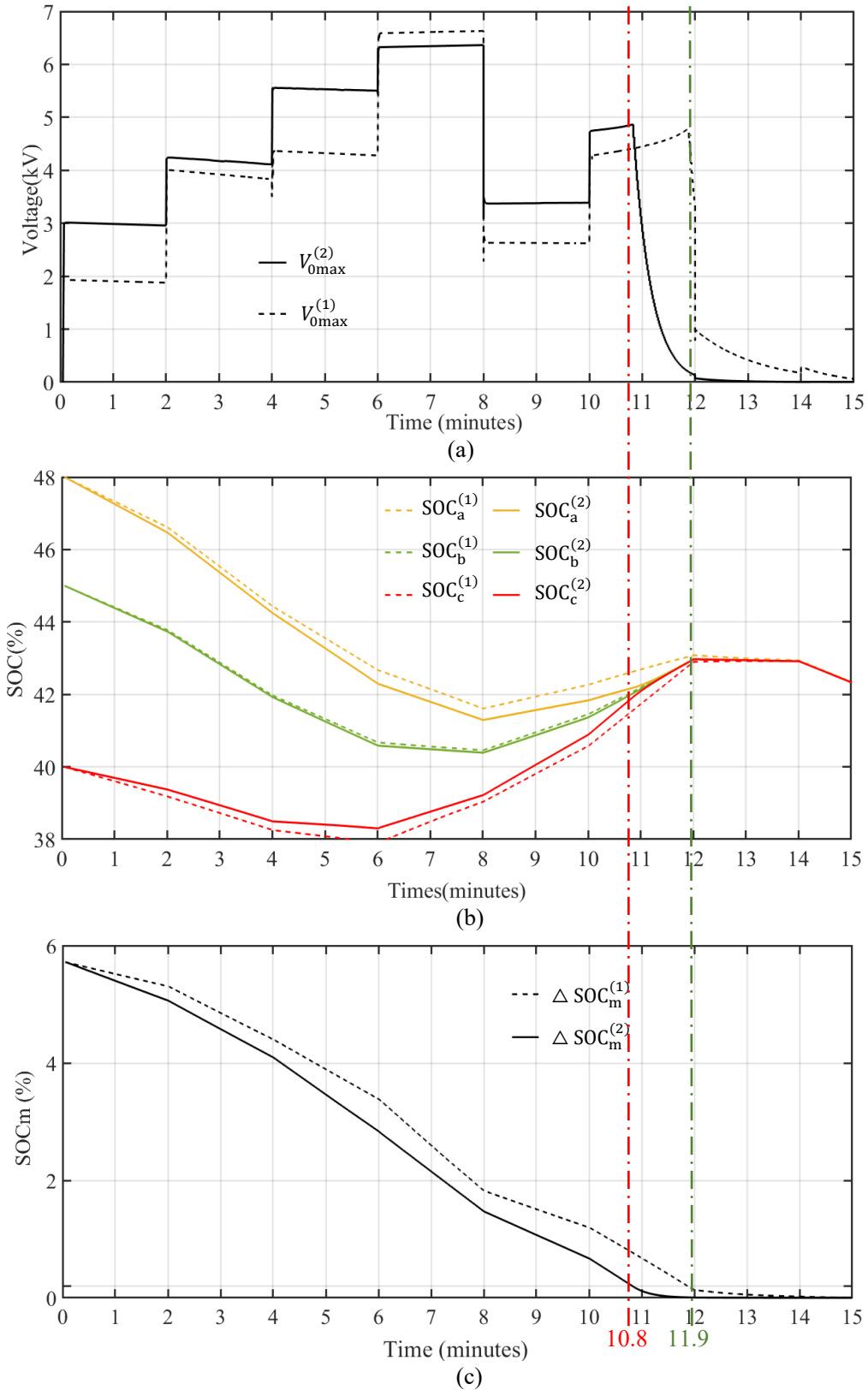


Figure 3.17 Curves of the two strategies in Scenario I.

(a) Magnitudes of injected zero-sequence voltage. (b) Three-phase SOC. (c) Three-phase SOC imbalance magnitudes.

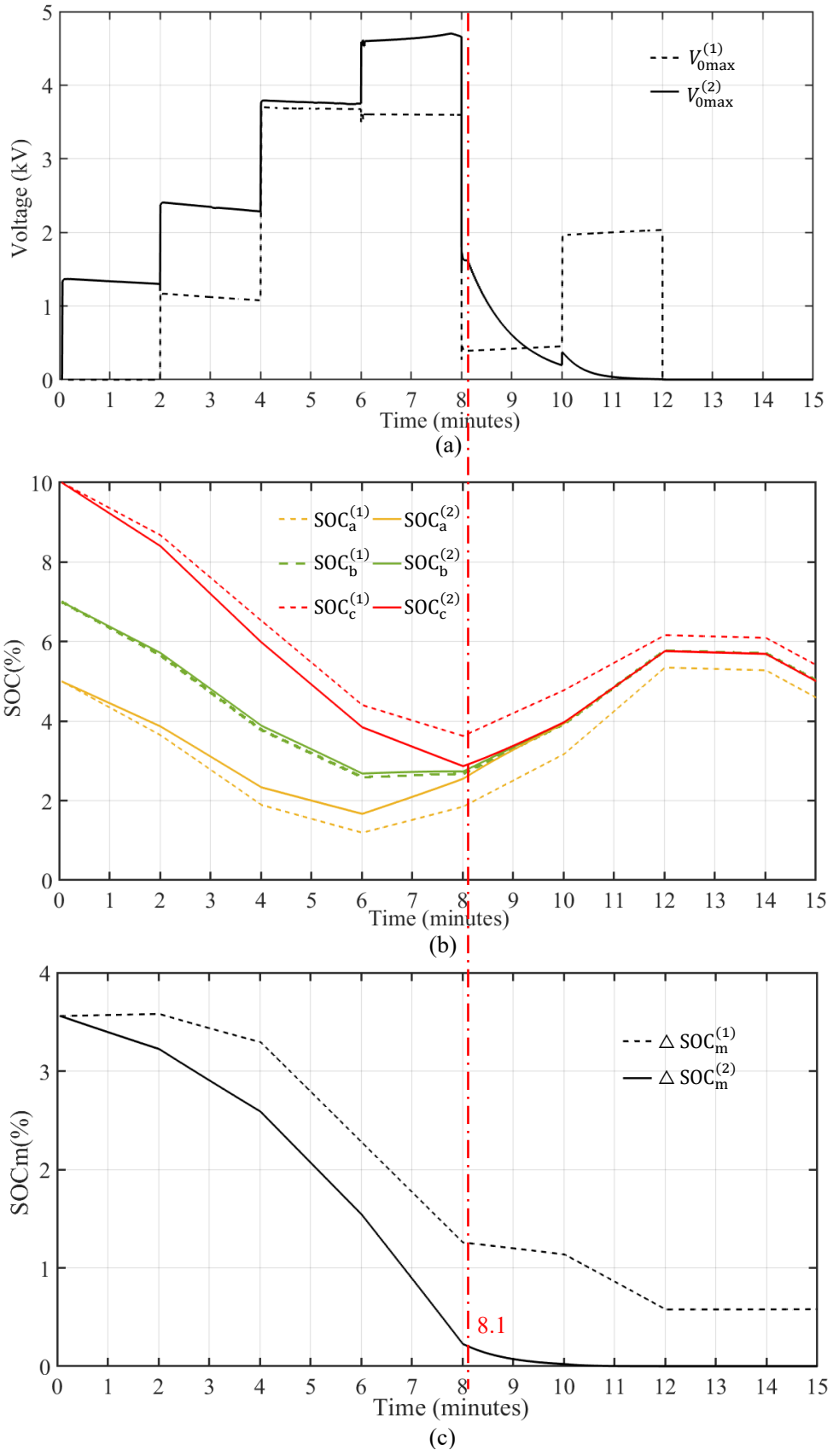
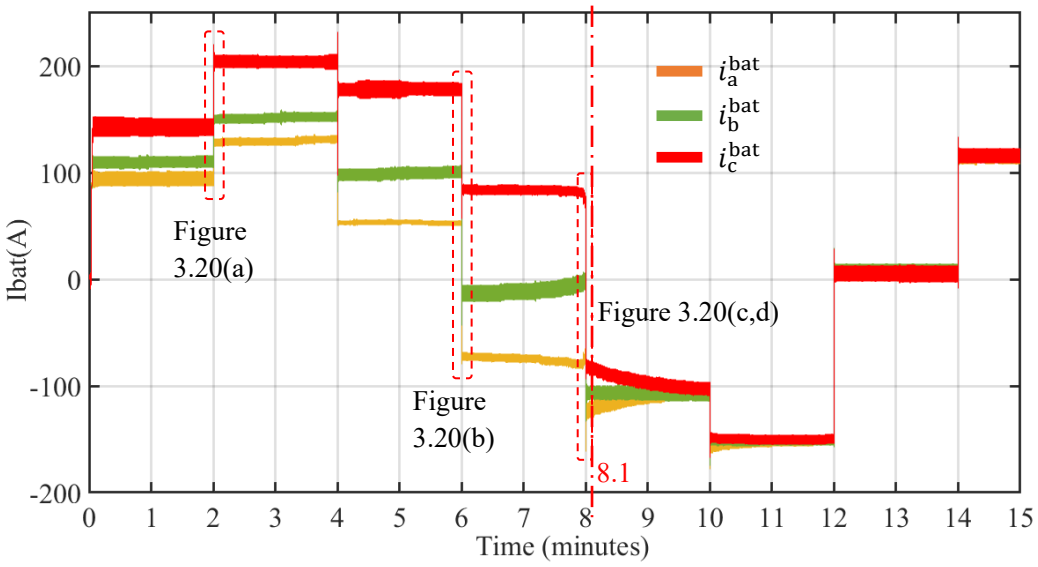
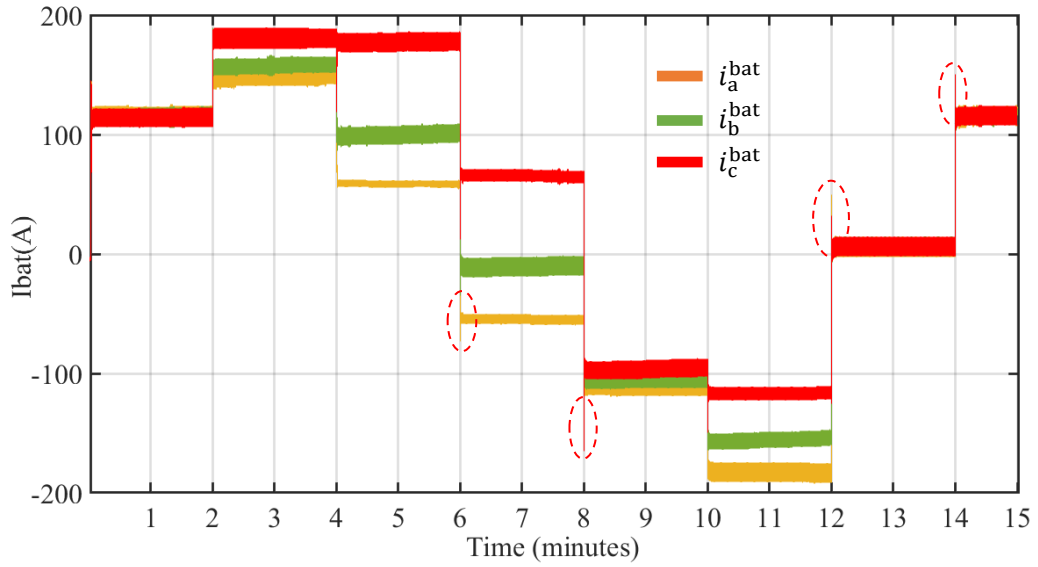


Figure 3.18 Curves of the two strategies in Scenario II.

(a) Magnitudes of injected zero-sequence voltage. (b) Three-phase SOC. (c) Three-phase SOC imbalance magnitudes.



(a)



(b)

Figure 3.19 The battery current curves of the first submodules for the two strategies in Scenario II. (a) The proposed strategy. (b) Conventional strategy.

Figure 3.19 shows the battery current curves of the first submodules for the two strategies in Scenario II. i_a^{bat}, i_a^{bat} and i_a^{bat} are for A-, B- and C-phase battery currents, respectively. It can be observed that before 8.1 minutes, the proposed strategy has more dispersed phase currents, resulting in higher efficiency. To avoid exacerbating the transient processes of battery current and capacitor voltage during power transitions, the amplitude of injected zero-sequence voltage gradually increases to its maximum, increasing the dispersion of the three-phase battery currents as shown in Figure 3.20(a)

and (b). Due to the sampling frequency of zone ③ being 1 Hz, after achieving the balance objective, the zero-sequence voltage amplitude gradually decreases with the decrease of SOC at 1 Hz. This causes subtle fluctuations in the battery currents, as shown in Figure 3.20(d).

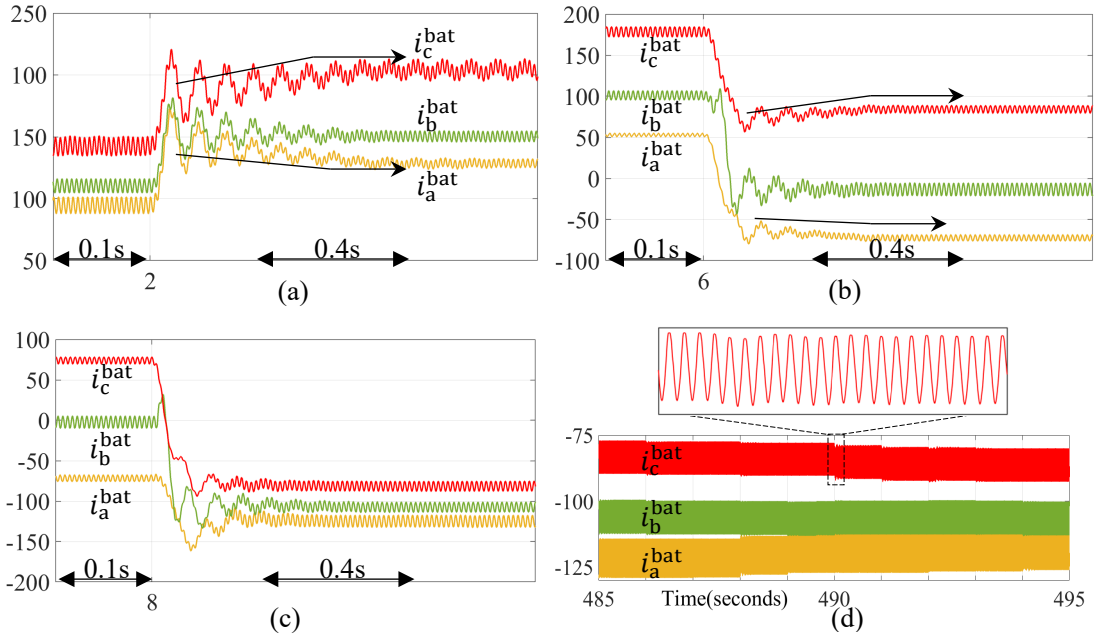


Figure 3.20 The segments from Figure 3.19.

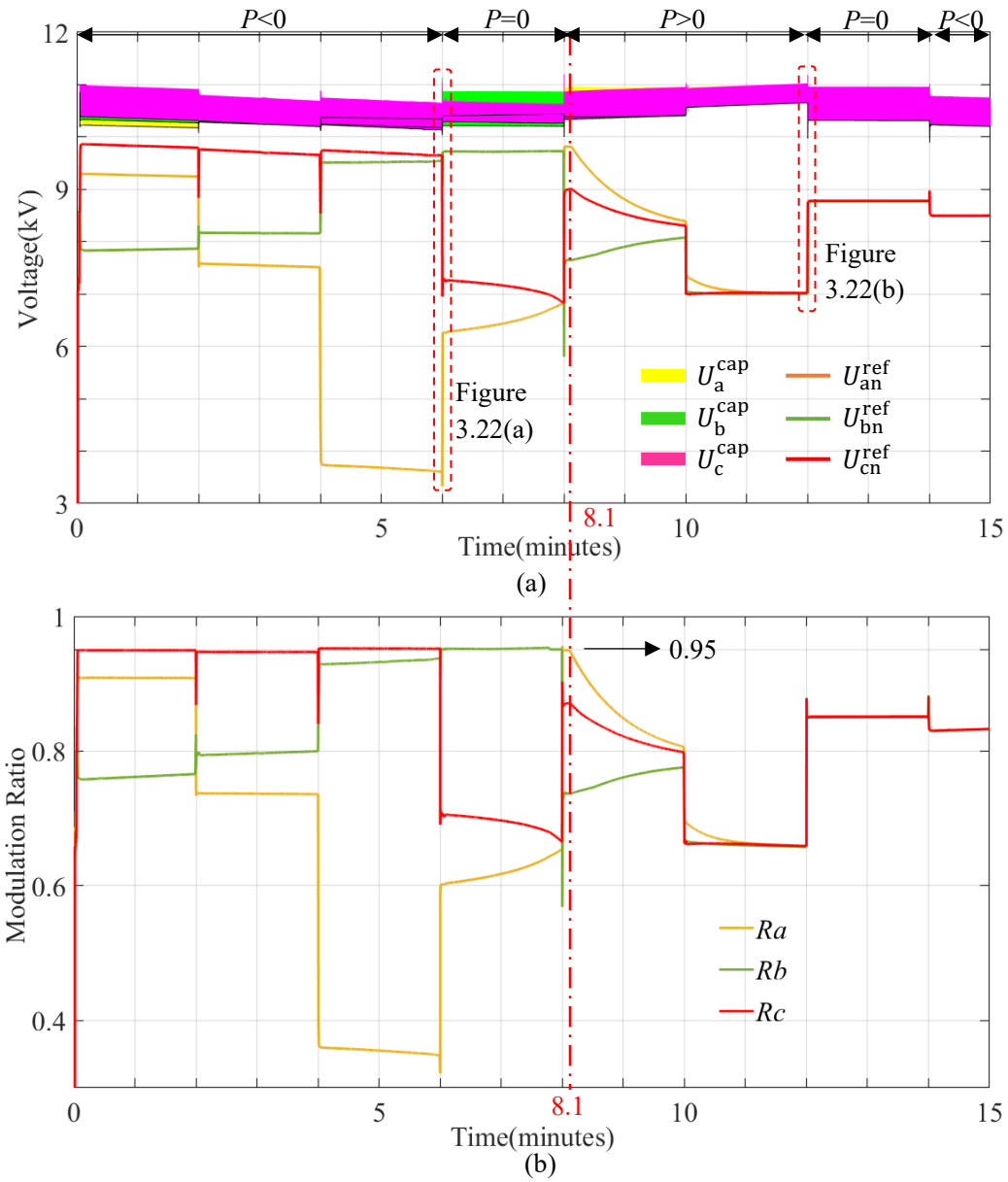


Figure 3.21 Curves of relevant voltages for the proposed strategy in Scenario II.
(a) Amplitudes of modulation voltages and DC-side voltages. (b) Three-phase modulation ratios.

Figure 3.21 shows curves of modulation voltage amplitudes, DC-side voltages and modulation ratios for the proposed strategy in Scenario II. It can be seen that before achieving the balance objective, the maximum modulation ratio remains around 0.95 (0.947~0.955) as preset. Therefore, the DC-side voltage of the system is fully utilized, and overmodulation is avoided, further demonstrating the effectiveness of the inter-phase SOC balancing strategy proposed in this chapter.

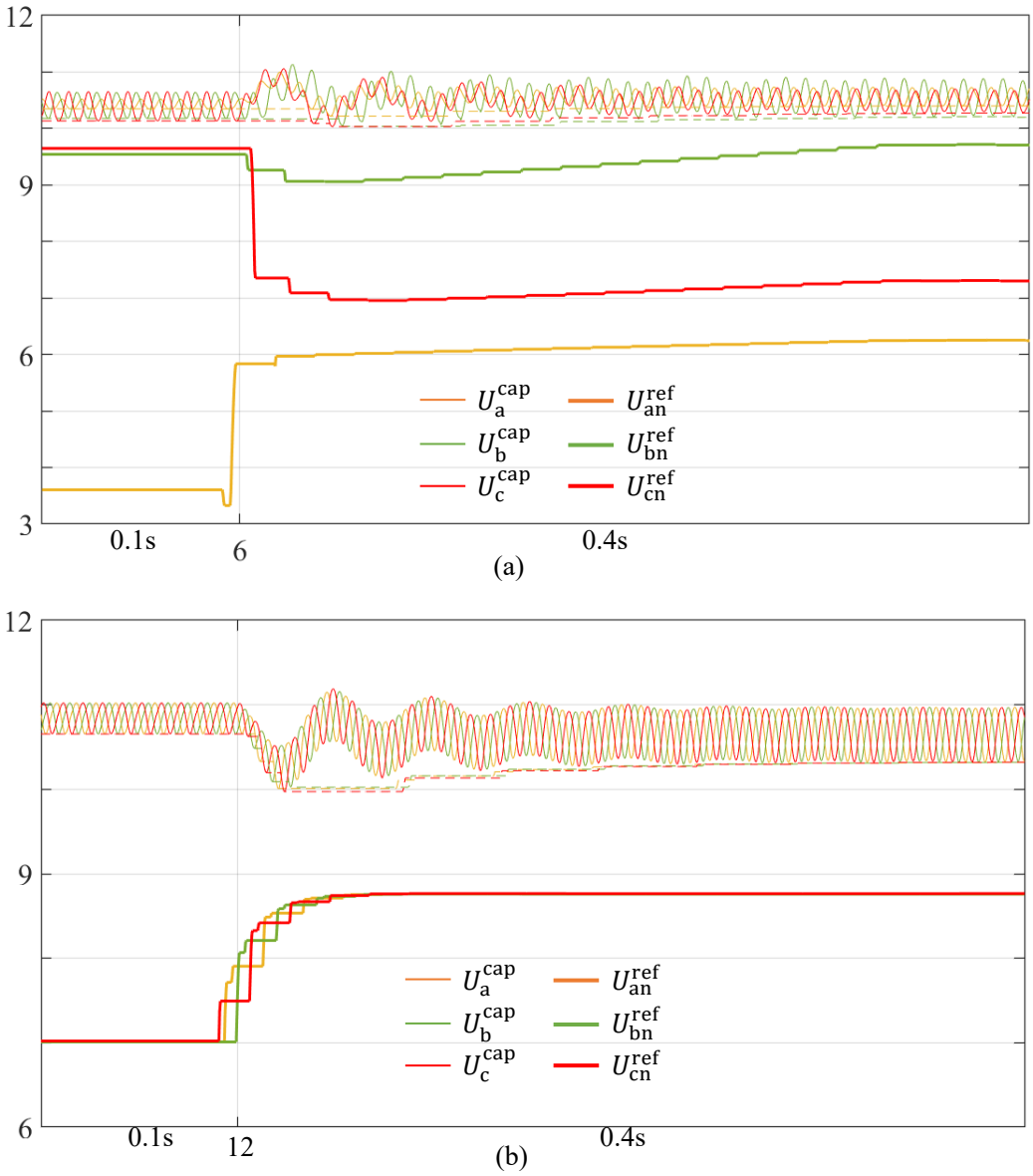


Figure 3.22 The segments from Figure 3.21.

3.5 Conclusion

This chapter proposes an innovative balancing strategy to enhance the efficiency of inter-phase SOC balancing in CHB-BESS under scenarios with insufficient DC voltage. This strategy maximizes the utilization of DC voltage, allowing for the injection of a larger amplitude of zero-sequence voltage without overmodulation compared to the conventional approach. Simulation results based on a 10kV 5MW/11.2MWh CHB-BESS in Matlab/Simulink confirm that, under various operating conditions and whether

zero-sequence voltage is injected or not, the proposed solution exhibits negligible differences in output power quality compared to the conventional method. Moreover, the effectiveness of this strategy is significantly less affected by BESS SOC and power states than the conventional approach, demonstrating superior efficiency and applicability.

Chapter 4

Fault-Tolerance Control for Cascaded H-Bridge Battery Energy Storage System

4.1 Introduction

CHB-PCS can connect low-voltage DC components directly to medium-voltage or high-voltage grids without a power transformer. Because of the high voltage levels in the cascaded topology, the equivalent switching frequency is high, and thus, the system output waveform is more satisfactory. In addition, CHB-BESS has the advantages of modularity and high scalability, so this topology scheme is very promising and has received widespread attention.

However, because CHB-BESS comprises a significant number of power-switching semiconductors, each power element is a potential point of failure, which reduces the system's reliability and stability. Therefore, ensuring the effective output of the system by adopting fault-tolerant control without system downtime is a critical issue. Currently, the fault-tolerance control strategies of CHB-BESS are mainly categorized into the addition of a cold standby redundancy submodule and a hot standby redundancy submodule.

The cold standby redundancy submodule strategy, also known as the hardware redundancy method, refers to when the CHB-PCS works normally, the redundant submodules are bypassed. When the working module fails, the failed submodule will be bypassed. The redundant submodule will be used to perform the work instead. The principle of this strategy is relatively simple and can reduce the conduction loss. However, in most cases, the CHB-PCS operates in a no-fault state, which means setting

cold standby redundancy modules will cause a certain degree of resource waste, thus increasing the system's cost. In addition, the state of the batteries connected to the cold standby submodule put into operation may differ greatly from that connected to the operating submodules, and there is a transient switching process, which affects the output power quality.

The hot standby redundancy module strategy is also known as the software redundancy method. In this strategy, the redundant submodules are also operated when the system runs normally. The submodules are removed when they fail, and corresponding control methods are employed to ensure the system's normal operation. In this method, submodule utilization is high, and the state consistency between submodules is better. Currently, there are more studies on hot standby fault-tolerant control strategies for CHB-PCS and Modular Multilevel Converter PCS (MMC-PCS), which can be mainly classified into type of symmetric resection strategies and type of asymmetric resection strategies according to the treatment of faulty submodules.

The symmetrical resection type of strategy bypasses the same number of submodules in the other phases while bypassing the faulty submodules to ensure the three-phase symmetry of the system. This type has a simple control algorithm, but reducing the same number of submodules in each phase simultaneously reduces the BESS's capacity and number of levels.

Removing the faulty submodules is the second type of strategy, also called the asymmetric removal type. This type removes only the faulty submodules, leaving the other phases unchanged. Although this type is more complex, it provides greater redundancy and fully utilizes the capacity of the BESS. The basic principle of this type of strategy is fully utilizing the DC-side voltages of the operating submodules to keep the AC-side characteristics of the system unchanged while maintaining the power balance between these submodules as much as possible. The typical conventional strategy of this type is injecting predetermined zero-sequence voltage to offset the

system neutral point, aiming to limit the modulation voltage of the faulty phase and equalize power among all remaining submodules. However, in many cases, the two goals are challenging to meet simultaneously. The conventional strategy is introduced in detail in Section 4.2.

Software-based asymmetric fault-tolerance control strategies have been widely studied in the CHB converters of medium-voltage variable speed drives [66-68]. However, all these works focus only on the balance of submodule modulation voltages due to the characteristics of the research object. It is, therefore, not practical to directly apply the results of these studies to fault-tolerance control of CHB-BESS.

The modulation voltage clapping (MVC) proposed in [69,70] can maximize the utilization of DC voltage to promote fault-tolerance capability. However, in the case of BESS, voltages and power balancing between submodules are of concern to us. In other words, when a submodule of a BESS fails, it will be bypassed, and the system should continue operating under the condition that all submodules have the same power without voltage overmodulation. When an MVC method is adopted, it isn't easy to analyze and control the power distribution of submodules in real time because the waveforms of modulation voltages vary unpredictably.

In this chapter, one innovative fault-tolerance control strategy for CHB-BESS is proposed. In addition to not changing the inter-phase voltage and output power, hybridizing with MVC, this strategy can navigate several common faults with submodule power balancing without overmodulation. It is worth noting that this strategy is applicable for fault tolerance and improving the situation where submodules are not fully charged or discharged simultaneously. For example, when BESS operates in discharging condition, it is typical for the battery cluster of one submodule to be fully discharged first and thus out of service. Employing the proposed strategy, the BESS can continue to operate normally with several submodules bypassed in sequence due to SOC reaching zero, enlarging its energy capacity.

The rest of the chapter is organized as follows. Section 4.2 investigates a typical conventional fault-tolerance strategy based on injecting zero-sequence voltage. Section 4.3 proposes a new fault-tolerance strategy. This section elaborates on the principles of the proposed new strategy, analyzes its performance compared to the conventional strategy, and presents a detailed block diagram for its implementation. Simulation results are provided in Section 4.4 to validate the effectiveness of the proposed strategy. Finally, Section 4.5 concludes this chapter.

4.2 Further Investigation of Conventional Strategy

With the conventional method of superimposing zero-sequence voltage, when one submodule in phase A fails, the modulation voltages of each submodule can be expressed by Equation (4.1).

$$\begin{cases} v_{\mathrm{an}}^{\mathrm{I}(100)} = \dfrac{1}{N-1}\left(U_{\mathrm{ko}}\cos\omega t - V_0^{(100)}\cos\left(\omega t + \varphi_0^{(100)}\right)\right) \\ v_{\mathrm{bn}}^{\mathrm{I}(100)} = \dfrac{1}{N}\left(U_{\mathrm{ko}}\cos\left(\omega t - \dfrac{2\pi}{3}\right) - V_0^{(100)}\cos\left(\omega t + \varphi_0^{(100)}\right)\right) \\ v_{\mathrm{cn}}^{\mathrm{I}(100)} = \dfrac{1}{N}\left(U_{\mathrm{ko}}\cos\left(\omega t + \dfrac{2\pi}{3}\right) - V_0^{(100)}\cos\left(\omega t + \varphi_0^{(100)}\right)\right) \end{cases} \tag{4.1}$$

Where $v_{\mathrm{an}}^{\mathrm{I}(100)}$, $v_{\mathrm{bn}}^{\mathrm{I}(100)}$ and $v_{\mathrm{cn}}^{\mathrm{I}(100)}$ are the modulation voltages of submodules in phases A, B and C, respectively, so they are just reference values instead of real ones. N is the number of submodules in a series under normal conditions. U_{ko} is the magnitude of u_{ao}, u_{bo} and u_{co}. $V_0^{(100)}$ and $\varphi_0^{(100)}$ are the magnitude and phase angle exceeding u_{ao} of superimposed zero-sequence voltage, respectively. ω and t are the power angular velocity and time, respectively. The superscripts 'I' and '(100)' represent the conventional method and single-submodule fault at phase A, respectively.

To balance the powers of submodules, the power of each submodule is set equal, i.e. $P_{\mathrm{an}}=P_{\mathrm{bn}}=P_{\mathrm{cn}}=P/(3N\text{-}1)$, which can be further expressed as Equation (4.2) when Equation (4.1) is substituted.

$$\begin{aligned}&\frac{1}{N-1}I_{\mathrm{sk}}\left(U_{\mathrm{ko}}\cos\delta-V_0^{(100)}\cos\left(\delta-\varphi_0^{(100)}\right)\right)\\&=\frac{1}{N}I_{\mathrm{sk}}\left(U_{\mathrm{ko}}\cos\delta-V_0^{(100)}\cos\left(\delta-\frac{2\pi}{3}-\varphi_0^{(100)}\right)\right)\\&=\frac{1}{N}I_{\mathrm{sk}}\left(U_{\mathrm{ko}}\cos\delta-V_0^{(100)}\cos\left(\delta+\frac{2\pi}{3}-\varphi_0^{(100)}\right)\right)\\&=\frac{3}{3N-1}I_{\mathrm{sk}}U_{\mathrm{ko}}\cos\delta\end{aligned}\tag{4.2}$$

Where δ is the phase angle of i_{sa} exceeding u_{ao} and I_{sk} is for the magnitude of i_{sa}, i_{sb} and i_{sc}.

Then, $V_0^{(100)}$ and $\varphi_0^{(100)}$ can be derived as Equation (4.3) from Equation (4.2), and the superimposed zero-sequence voltage $v_0^{(100)}$ can be expressed as Equation (4.4).

$$\begin{cases}V_0^{(100)}=\dfrac{2}{3N-1}U_{\mathrm{ko}}\cos\delta\\ \varphi_0^{(100)}=\delta\end{cases}\tag{4.3}$$

$$v_0^{(100)}=\frac{2}{3N-1}U_{\mathrm{ko}}\cos\delta\cos(\omega t+\delta)\tag{4.4}$$

Where δ is the phase angle of i_{sa} exceeding u_{ao}.

To facilitate the investigation of the voltage modulation ratio after the zero-sequence voltage is superimposed, the expressions of the magnitudes of $v_{\mathrm{an}}^{\mathrm{I}(100)}$, $v_{\mathrm{bn}}^{\mathrm{I}(100)}$ and $v_{\mathrm{cn}}^{\mathrm{I}(100)}$ should be derived. After substituting Equation (4.4) to (4.1), $V_{\mathrm{an}}^{\mathrm{I}(100)}$, $V_{\mathrm{bn}}^{\mathrm{I}(100)}$ and $V_{\mathrm{cn}}^{\mathrm{I}(100)}$, the magnitudes of $v_{\mathrm{an}}^{\mathrm{I}(100)}$, $v_{\mathrm{bn}}^{\mathrm{I}(100)}$ and $v_{\mathrm{cn}}^{\mathrm{I}(100)}$ respectively, can be obtained as Equation (4.5). It can be concluded that modulation ratios of submodules would change according to N and δ after the conventional method is taken to go through a single-submodule fault.

$$\begin{cases}V_{\mathrm{an}}^{\mathrm{I}(100)}=\dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{1+\dfrac{(8-12N)\cos^2\delta}{(3N-1)^2}}\\ V_{\mathrm{bn}}^{\mathrm{I}(100)}=\dfrac{U_{\mathrm{ko}}}{N}\sqrt{1+\dfrac{(6N+2)\cos^2\delta}{(3N-1)^2}+\dfrac{\sqrt{3}\sin\delta\cos\delta}{3N-1}}\\ V_{\mathrm{cn}}^{\mathrm{I}(100)}=\dfrac{U_{\mathrm{ko}}}{N}\sqrt{1+\dfrac{(6N+2)\cos^2\delta}{(3N-1)^2}-\dfrac{\sqrt{3}\sin\delta\cos\delta}{3N-1}}\end{cases}\tag{4.5}$$

Similarly, when both A and B phases have one fault submodule bypassed, the modulation voltages of each submodule can be expressed by Equation (4.6).

$$\begin{cases} v_{\mathrm{an}}^{\mathrm{I}(110)} = \dfrac{1}{N-1}\left(U_{\mathrm{ko}}\cos\omega t - V_0^{(110)}\cos\left(\omega t + \varphi_0^{(110)}\right)\right) \\ v_{\mathrm{bn}}^{\mathrm{I}(110)} = \dfrac{1}{N-1}\left(U_{\mathrm{ko}}\cos\left(\omega t - \dfrac{2\pi}{3}\right) - V_0^{(110)}\cos\left(\omega t + \varphi_0^{(110)}\right)\right) \\ v_{\mathrm{cn}}^{\mathrm{I}(110)} = \dfrac{1}{N}\left(U_{\mathrm{ko}}\cos\left(\omega t + \dfrac{2\pi}{3}\right) - V_0^{(110)}\cos\left(\omega t + \varphi_0^{(110)}\right)\right) \end{cases} \tag{4.6}$$

Where superscript '(110)' represents a double-submodule fault, with one failure at phase A and the other at phase B.

The power of each submodule is set equal, i.e. P_{an}=P_{bn}=P_{cn}=P/(3N-2), and after substituting Equation (4.6) into the equation, the corresponding superimposed zero-sequence voltage $v_0^{(110)}$ can be expressed as Equation (4.7). Furthermore, $V_{\mathrm{an}}^{\mathrm{I}(110)}$, $V_{\mathrm{bn}}^{\mathrm{I}(110)}$ and $V_{\mathrm{cn}}^{\mathrm{I}(110)}$ the magnitudes of the modulation voltages of submodules in phases A, B, and C can be derived as Equation (4.8).

$$v_0^{(110)} = \frac{2}{3N-2}U_{\mathrm{ko}}\cos\delta\cos\left(\omega t + \delta - \frac{\pi}{3}\right) \tag{4.7}$$

$$\begin{cases} V_{\mathrm{an}}^{\mathrm{I}(110)} = \dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{1 + \dfrac{4\cos^2\delta}{(3N-2)^2} - \dfrac{4\cos\delta\cos\left(\delta - \frac{\pi}{3}\right)}{3N-2}} \\ V_{\mathrm{bn}}^{\mathrm{I}(110)} = \dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{1 + \dfrac{4\cos^2\delta}{(3N-2)^2} - \dfrac{4\cos\delta\cos\left(\delta + \frac{\pi}{3}\right)}{3N-2}} \\ V_{\mathrm{cn}}^{\mathrm{I}(110)} = \dfrac{U_{\mathrm{ko}}}{N}\sqrt{1 + \dfrac{4(3N-1)\cos^2\delta}{(3N-2)^2}} \end{cases} \tag{4.8}$$

Based on the same principle, the expressions of zero-sequence voltages superimposed to navigate other faults can be derived. Table 4.1 gives the equations of zero-sequence voltages in correspondence with a series of common faults. This thesis provides the magnitudes of submodule modulation voltages under fault conditions of '100' and '110', as shown in Equations (4.5) and (4.8), respectively, for theoretically investigating the strategy's performance.

Table 4.1 Zero-sequence voltages in correspondence of a series of common faults

Fault Type	Magnitude, V_0	Phase (in reference to u_{ao}), φ_0
100	$\frac{2}{3N-1}U_{ko}\cos\delta$	δ
110	$\frac{2}{3N-2}U_{ko}\cos\delta$	$\delta-\frac{\pi}{3}$
200	$\frac{4}{3N-2}U_{ko}\cos\delta$	δ
210	$\frac{2\sqrt{3}}{3N-3}U_{ko}\cos\delta$	$\delta-\frac{\pi}{6}$
300	$\frac{2}{N-1}U_{ko}\cos\delta$	δ
211	$\frac{2}{3N-4}U_{ko}\cos\delta$	δ

4.3 New fault-tolerance Strategy

As shown in Equation (4.9), a common-mode voltage can be injected into the neutral point to utilise the DC-side voltage fully. Then (4.1) is rewritten as (4.10).

$$u_{no}=\frac{\max(u_{ao},u_{bo},u_{co})+\min(u_{ao},u_{bo},u_{co})}{2} \tag{4.9}$$

$$\begin{cases} v_{an}^{II(100)}=\frac{1}{N-1}\left(U_{ko}\cos\omega t-u_{no}-V_0^{(100)}\cos(\omega t+\varphi_0)\right) \\ v_{bn}^{II(100)}=\frac{1}{N}\left(U_{ko}\cos\left(\omega t-\frac{2\pi}{3}\right)-u_{no}-V_0^{(100)}\cos(\omega t+\varphi_0)\right) \\ v_{cn}^{II(100)}=\frac{1}{N}\left(U_{ko}\cos\left(\omega t+\frac{2\pi}{3}\right)-u_{no}-V_0^{(100)}\cos(\omega t+\varphi_0)\right) \end{cases} \tag{4.10}$$

Where $v_{an}^{II(100)}$, $v_{bn}^{II(100)}$ and $v_{cn}^{II(100)}$ are the modulation voltages of submodules in phases A, B and C, respectively. The superscript 'II' represents the proposed strategy.

It can be seen from Equation (3.2) u_{no} has a period of 2π/3, and thus, the three average values of powers obtained from u_{no} with i_{sa}, i_{sb}, i_{sc} are all equal to 0, so when the powers of each submodule are set equal, i.e. $P_{an}=P_{bn}=P_{cn}=P/(3N\text{-}1)$, from Equation (4.10), $V_0^{(100)}$ and $\varphi_0^{(100)}$ can be derived the same as Equation (4.3), and the superimposed zero-sequence voltage $v_0^{(100)}$ can still be expressed as Equation (4.4).

Nevertheless, this has a different effect on the modulation ratios. After substituting Equation (4.3) and (4.9) to (4.10), $V_{\mathrm{an}}^{\mathrm{II}(100)}$, $V_{\mathrm{bn}}^{\mathrm{II}(100)}$ and $V_{\mathrm{cn}}^{\mathrm{II}(100)}$, the magnitudes of $v_{\mathrm{an}}^{\mathrm{II}(100)}$, $v_{\mathrm{bn}}^{\mathrm{II}(100)}$ and $v_{\mathrm{cn}}^{\mathrm{II}(100)}$ respectively, can be obtained as Equation (4.11).

$$\begin{cases} V_{\mathrm{an}}^{\mathrm{II}(100)} = \dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{\dfrac{3}{4}+\dfrac{(7-9N)\cos^2\delta}{(3N-1)^2}+\dfrac{\sqrt{3}|\sin\delta\cos\delta|}{(3N-1)}} \\ V_{\mathrm{bn}}^{\mathrm{II}(100)} = \dfrac{U_{\mathrm{ko}}}{N}\sqrt{\dfrac{3}{4}+\dfrac{4\cos^2\delta}{(3N-1)^2}-\dfrac{2\sqrt{3}\min\left(\cos\delta\cos\left(\delta+\frac{5\pi}{6}\right),-\cos\delta\sin\delta\right)}{(3N-1)}} \\ V_{\mathrm{cn}}^{\mathrm{II}(100)} = \dfrac{U_{\mathrm{ko}}}{N}\sqrt{\dfrac{3}{4}+\dfrac{4\cos^2\delta}{(3N-1)^2}-\dfrac{2\sqrt{3}\min\left(\cos\delta\cos\left(\delta-\frac{5\pi}{6}\right),\cos\delta\sin\delta\right)}{(3N-1)}} \end{cases} \tag{4.11}$$

Similarly, when both A and B phases have one fault submodule bypassed, the corresponding superimposed zero-sequence voltage $v_0^{(110)}$ can still be expressed as Equation (4.7). Furthermore, $V_{\mathrm{an}}^{\mathrm{II}(110)}$, $V_{\mathrm{bn}}^{\mathrm{II}(110)}$ and $V_{\mathrm{cn}}^{\mathrm{II}(110)}$ The magnitudes of the modulation voltages of submodules in phases A, B, and C can be derived as Equation (4.12).

$$\begin{cases} V_{\mathrm{an}}^{\mathrm{II}(110)} = \dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{\dfrac{3}{4}+\dfrac{4\cos^2\delta}{(3N-2)^2}-\dfrac{4\min\left(\cos\delta\cos\left(\delta-\frac{\pi}{6}\right),\cos\delta\sin\delta\right)}{(3N-2)}} \\ V_{\mathrm{bn}}^{\mathrm{II}(110)} = \dfrac{U_{\mathrm{ko}}}{N-1}\sqrt{\dfrac{3}{4}+\dfrac{4\cos^2\delta}{(3N-2)^2}-\dfrac{4\min\left(\cos\delta\cos\left(\delta+\frac{\pi}{6}\right),-\cos\delta\sin\delta\right)}{(3N-2)}} \\ V_{\mathrm{cn}}^{\mathrm{II}(110)} = \dfrac{U_{\mathrm{ko}}}{N}\sqrt{\dfrac{3}{4}+\dfrac{4\cos^2\delta}{(3N-2)^2}+\dfrac{4\max\left(\cos\delta\cos\left(\delta-\frac{\pi}{6}\right),\cos\delta\cos\left(\delta+\frac{\pi}{6}\right)\right)}{(3N-2)}} \end{cases} \tag{4.12}$$

We know U_{ko} is the function of I_{sk}, the magnitude of i_{sk}, and δ. Regardless of the resistance in the circuit, the value of U_{ko} peaks nearly as $\delta=\pi/2$ and I_{sk} peaks, so the minimum value of DC-side voltage (commonly, SOC=0) should not be less than the maximum value of U_{ko}, i.e. $E^{\min} \geq U_{\mathrm{ko}}^{\max}$. Therefore, a satisfactory fault-tolerance strategy should not cause voltage overmodulation when the BESS generates full reactive power. To facilitate the theoretical comparison between the proposed strategy

and the conventional one, the maximum magnitude of voltage drop on the AC coupling inductor is reasonably assumed to be $20\%U_{\mathrm{ko}}^{\max}$, then U_{ko} can be expressed as Equation (4.13). Further, based on $U_{\mathrm{ko}}^{\max}$, the maximum modulation ratio $R_x^{y(z)}$ of phase x with strategy y under the fault condition z can be derived by substituting Equation (4.5), (4.8), (4.11) or (4.12) into (4.14). It can be seen that $R_x^{y(z)}$ is the function with just two variables, N and δ.

$$U_{\mathrm{ko}} = U_{\mathrm{ko}}^{\max}\max\left(0.8, 0.2\left(\sin\delta + \sqrt{\sin^2\delta + 15}\right)\right) \tag{4.13}$$

$$R_x^{y(z)} = N\frac{V_{x\mathrm{n}}^{y(z)}}{U_{\mathrm{ko}}^{\max}} \quad x \in \{\mathrm{a};\ \mathrm{b};\ \mathrm{c}\}, y \in \{\mathrm{I};\ \mathrm{II}\}, z \in \{100, 110\} \tag{4.14}$$

Figures 4.1 and 4.2 show the curves of maximum modulation ratios versus N from 3 to 12 and δ from $-\pi$ to π, separately by proposed and conventional strategies. It can be seen that with the proposed strategy, no voltage overmodulation occurs in the two fault-free phases. Also, when $N \geq 8$, voltage overmodulation disappears in the single-fault phase. This means the proposed strategy can operate effectively with SOC balancing and without overmodulation when the number of cascaded submodules in one phase is greater than 8. In contrast, voltage overmodulation cannot be entirely avoided regardless of N with the conventional method, especially when the BESS generates large-scale reactive power.

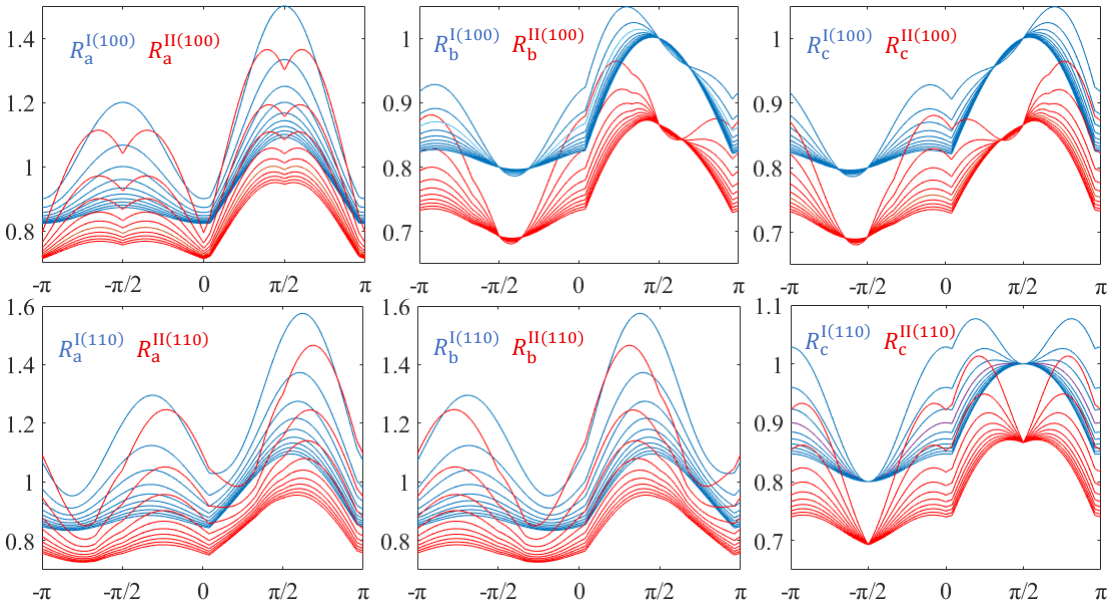


Figure 4.1 Curves of maximum modulation ratios versus N and δ, separately by proposed and conventional strategies.

The plots in the first row are under the condition of a single-submodule fault, while the second row gives the images under the condition of a double-submodule fault. In each bundle of curves, from top to bottom, N increases in sequence from 3 to 12.

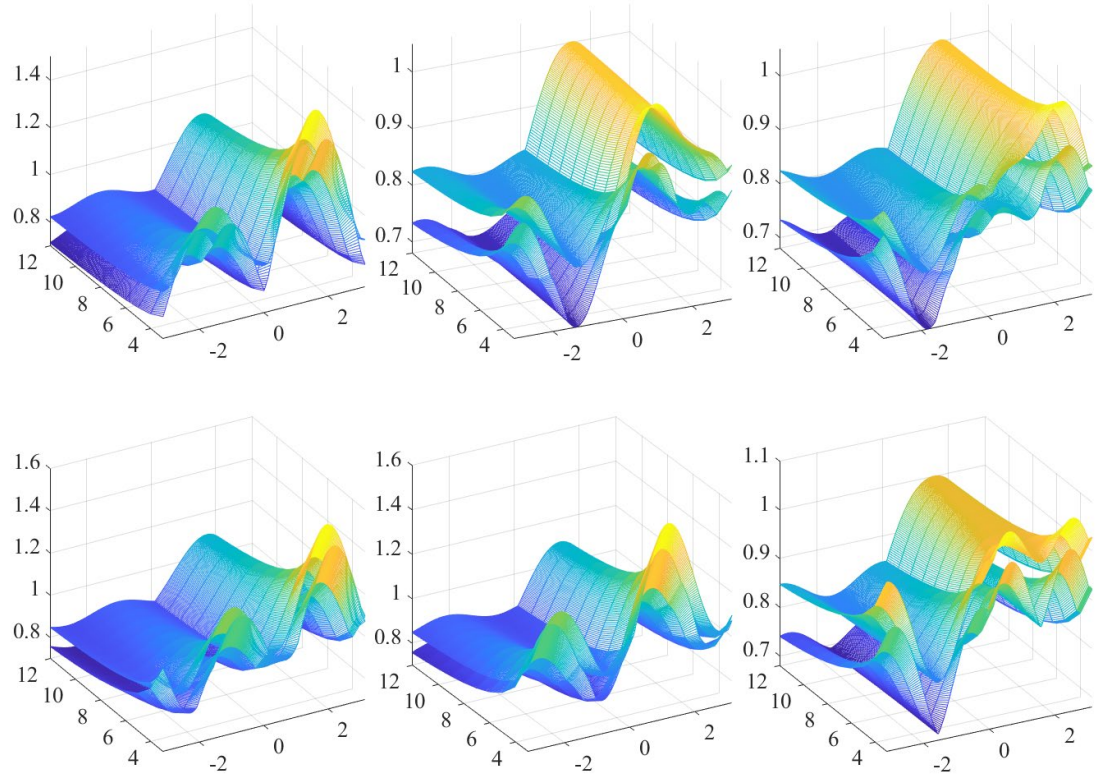


Figure 4.2 3D plots of maximum modulation ratios versus N and δ, separately by proposed and conventional strategies.
The photos in the first row are under the condition of a single-submodule fault, while the second row gives the images under the condition of a double-submodule fault.

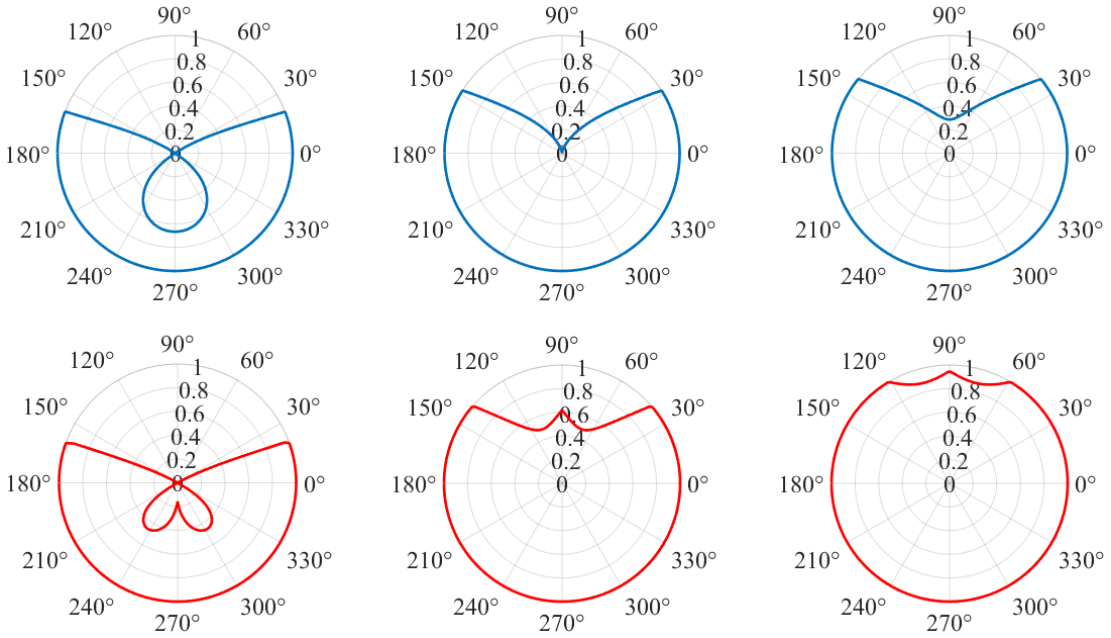


Figure 4.3 Current limits of the two strategies under conditions of single-submodule fault. Blue and red curves correspondingly represent the current limits of conventional and proposed strategies. From left to right, each column refers to N equal to 3, 5 and 7, respectively. In each polar plot, the radius is for the value of I_{m}, based on the magnitude of the rated normal current of BESS, while the angle is for the value of δ.

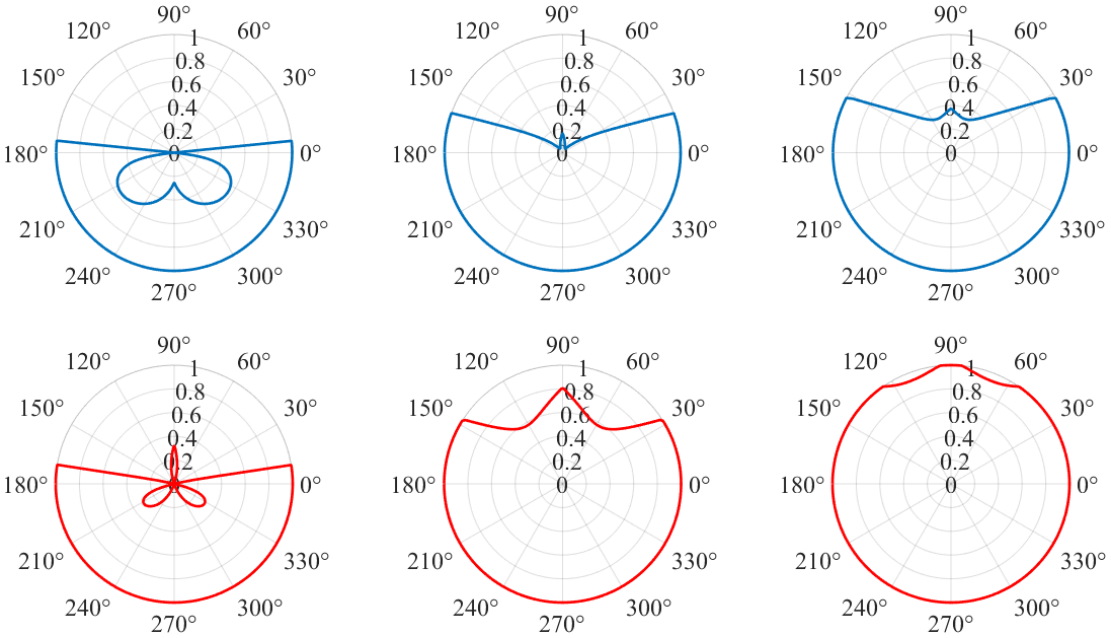


Figure 4.4 Current limits of the two strategies under conditions of single-submodule fault. Blue and red curves correspondingly represent the current limits of conventional and proposed strategies. From left to right, each column refers to N equal to 4, 6 and 8, respectively. In each polar plot, the radius is for the value of I_{m}, based on the magnitude of the rated normal current of BESS, while the angle is for the value of δ.

Figures 4.3 and 4.4 show the current limits of the two strategies under single-submodule fault (at A phase) and double-submodule fault (separately at A and B phases). Figure 4.3 gives three cases of cascaded number *N* equal to 3, 5 and 7 separately, while Figure 4.4 gives three cases of cascaded number *N* equal to 4, 6 and 8, respectively. It can be seen that the proposed strategy can significantly broaden the power capability of a BESS under submodule fault conditions.

It is possible to satisfy Equation (2.2) by keeping the difference between the values of $u_{\mathrm{an}}^{\mathrm{ref}}$, $u_{\mathrm{an}}^{\mathrm{ref}}$ and $u_{\mathrm{an}}^{\mathrm{ref}}$ constant at all times while adjusting them. MVC is based on this principle to limit the modulation voltage and thus avoid overmodulation. MVC is easy to implement through a computer program, and the flow of its programmed implementation is given in Figure 4.5.

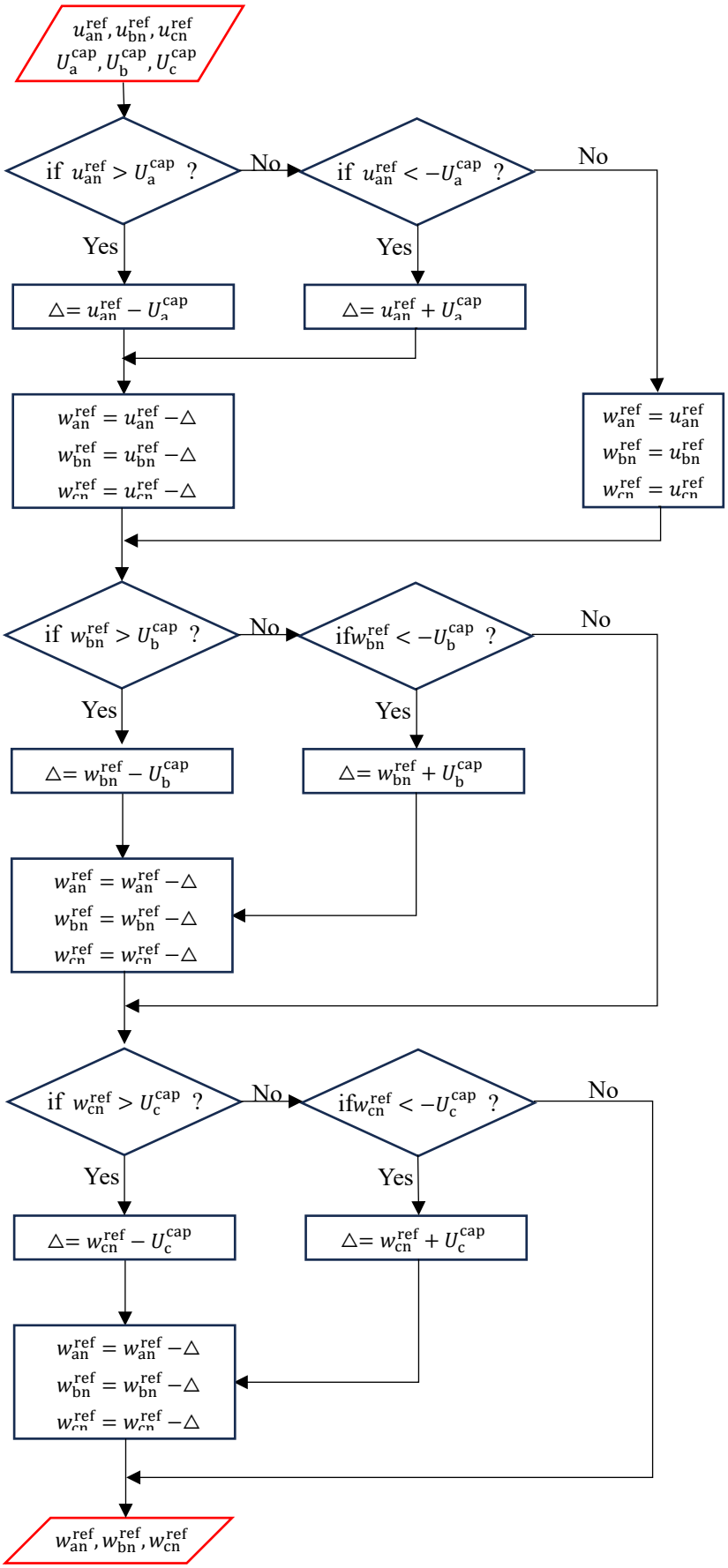


Figure 4. 5 Program flow of MVC

When only an MVC method is utilized to navigate through submodule fault conditions for a CHB-BESS, voltage overmodulation can be effectively avoided. Still, inter-phase SOC balancing is nearly impossible to perform. However, MVC methods can be used as a supplement if the proposed method still leads to overmodulation. For example, when N is equal to 6, there is a small portion of the operating zone beyond the current limit while going through a double-submodule fault, as is shown in the photo at the bottom middle of Figure 4.4. Within the current limit, just utilizing the proposed strategy (Method II) can make the BESS operate without voltage overmodulation and with inter-phase SOC balancing. When exceeding the current limit, the approach of Method II + MVC can be taken to avoid overmodulation. Although the hybrid approach cannot strictly ensure inter-phase SOC balancing, it can significantly reduce the power difference among submodules and thus prolong the operating duration time compared to only using MVC. Figure 4. 6 shows the basic principle of MVC, Method I + MVC and Method II + MVC, while the overall control block diagram of BESS with Method II + MVC is shown in Figure 4.7.

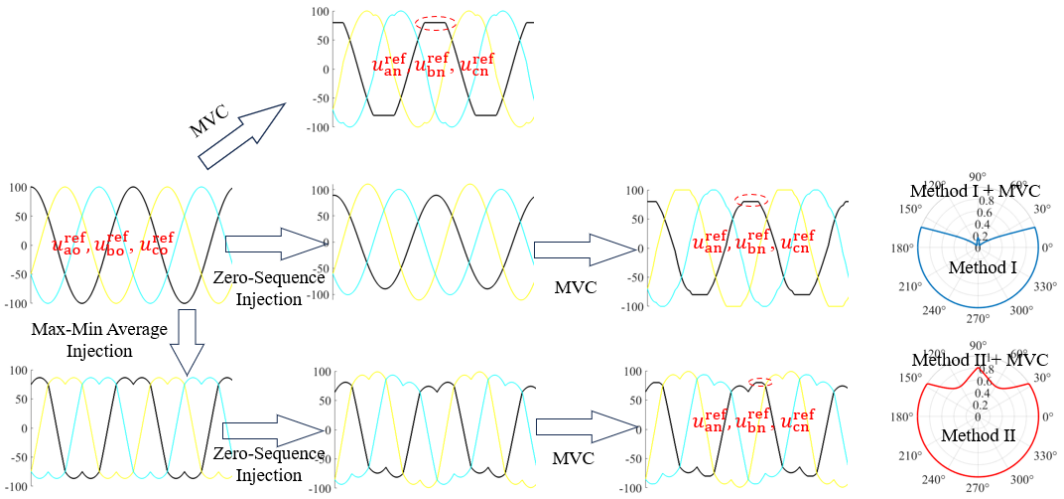


Figure 4. 6 Basic principle of MVC, Method I+ MVC and Method II.

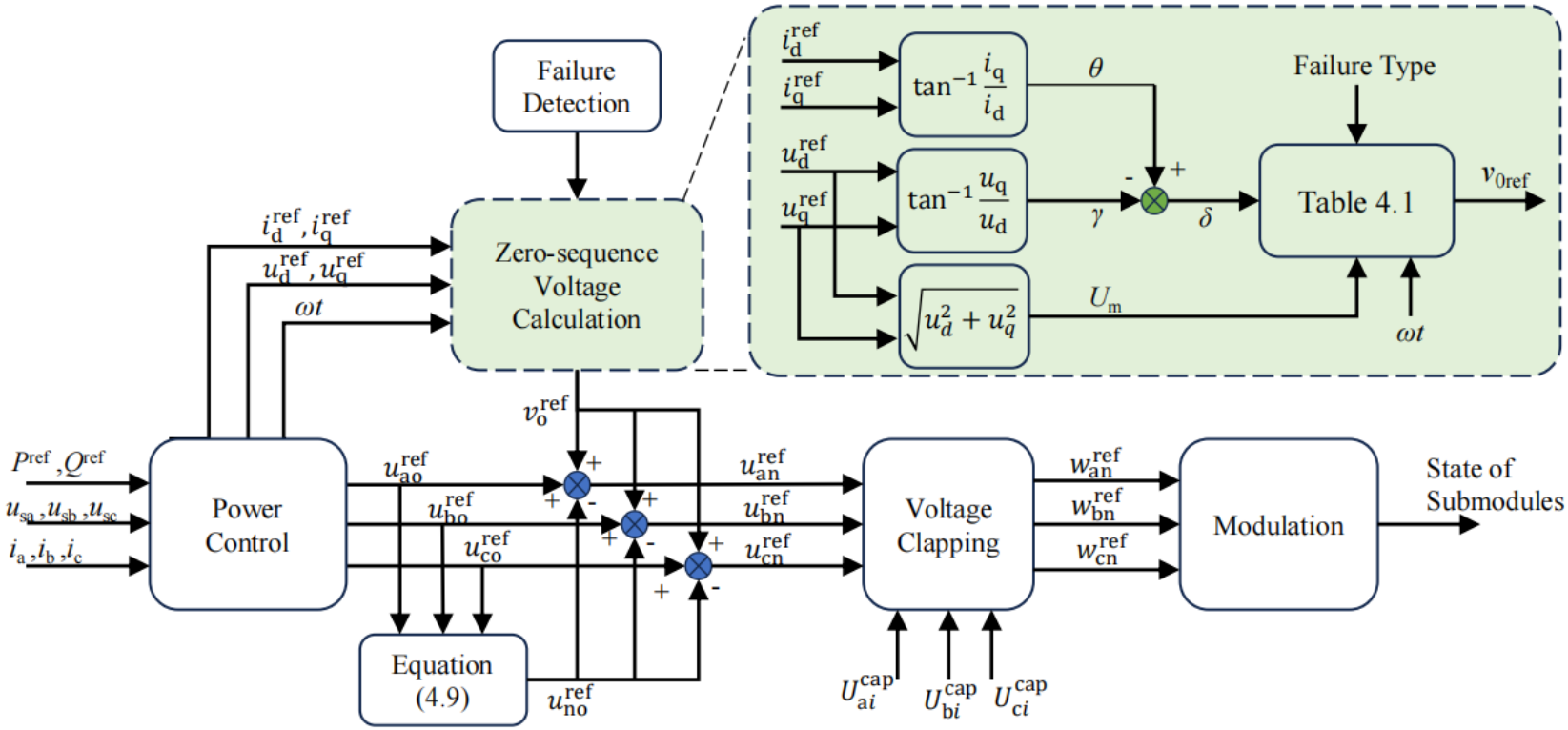


Figure 4.7 Overall control block diagram for CHB-PCS with the proposed fault-tolerance strategy.

4.4 Simulation Verification

In this section, the new fault-tolerance strategy proposed in section 4.3 is validated from simulation using Matlab/simulink. Subsection 4.4.1 describes the main parameters of two BESS systems used for the simulation, while subsections 4.4.2 and 4.4.3 validate the effectiveness of the new strategy based on the two systems, respectively.

4.4.1 Overview of the BESS Designed for Simulation

To verify the effectiveness of the fault-tolerance strategy proposed in this paper, a 2MW/6.72MWh BESS system (BESS No.1) and a 5MW/11.2MWh BESS system (BESS No.2), respectively connected to 6kV and 10kV grids are designed, and corresponding models are built with Matlab/Simulink for simulation and analysis. BESS No.1 and BESS No.2 share the same type of submodules, the main parameters of which are listed in Table 4.2. As shown in Table 1, Each submodule employes 416 pcs 280Ah Li-FePO4 battery cells with an insulation level of 1.5kV, and these battery cells are connected in series, establishing the DC-side voltage of each submodule with a minimum value of 1040V (SOC=0) and maximum value 1518.4V (SOC=100%). Table 4.3 gives the main parameters of both BESS systems and the relevant parameters of the power grids they are connected with.

Table 4.2 Main parameters of submodules

Item	Quantity
Capacity of Battery Cell (Lithium-Iron)	280Ah
Number of Battery Packs per SM	8
Number of Cells per Battery Pack	52
Number of Battery Cells per SM	416
Voltage Range per SM	1040V to 1518.4V

Table 4.3 Main parameters of the two BESS systems

BESS Name	BESS No.1	BESS No.2
Number of SMs per Phase, N	6	10
Rated Apparent Power	2MVA	5.5MVA
Rated Energy Capacity	6.72MWh	11.2MWh
Grid Voltage (phase-to-phase, RMS)	6kV	10kV
Short-Circuit Capacity of Grid	72MVA	200MVA
AC Coupling inductor	15mH	15mH
Carrier Frequency	1.5kHz	1.5kHz
Sampling Frequency	10kHz	10kHz

Based on the two BESS systems, the three fault-tolerance strategies, i.e. MVC, hybrid method of conventional strategy with MVC (I+MVC) and hybrid method of proposed strategy with MVC (II+MVC), are separately employed to ride through several particular submodule faults for comparison. To thoroughly compare the three strategies, 3 and 6 types of submodule faults are selected for BESS No.1 and BESS No.2, respectively, as shown in Table 4.4.

Table 4.4 Respective submodule faults of the two systems, selected for comparison between the three fault-tolerance strategies

BESS Name	BESS No.1	BESS No.2
Fault Type	100, 110, 200	100, 110, 200, 210, 300, 211

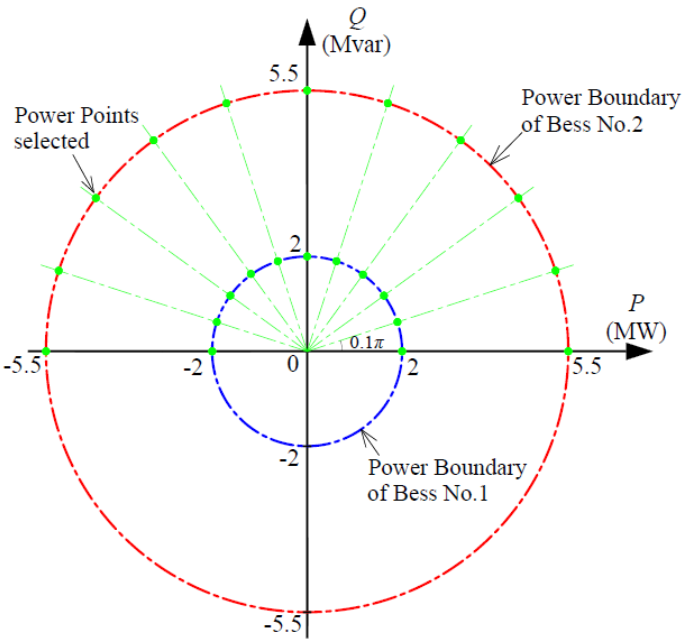


Figure 4. 8 The power boundaries of BESS No.1 and BESS No.2, in blue and red, respectively. Green points are the power points selected for comparison between MVC, I+MVC, and II+MVC.

Under normal conditions, both BESS systems can operate within the limits of the power capability chart in IEC 62933-1. This means they can operate at any point in the area cycled by their rated apparent power to exchange energy with power grids, as shown in Figure 4.8. It must be clarified that both Rated Apparent Powers of the two systems are predominantly determined with their minimum DC-side voltages, deliberately designed to facilitate verification of the proposed strategy. However, in engineering practice, the Rated Apparent Power of a BESS may also be constrained by battery cells' Rated Charge/Discharge Rate (RCDR) in addition to the minimum DC-side voltage. To avoid RCDRs constraining corresponding Rated Apparent Powers, for BESS No.1 and BESS No.2, we can determine the respective RCDRs of battery cells to be 1C and 1.5C.

As analyzed in section III, the scenario that δ, the phase angle of i_{sa} exceeding u_{ao} is between 0 and π, is significantly challenging for a BESS navigating through a fault, compared to δ between $-\pi$ and 0, mainly because the magnitude of u_{ko} is relatively large when the BESS injects reactive power into the power grid. Therefore, in this simulation section, the comparison between the three strategies is focused on this scenario. 11

power points on the power boundary of each BESS system, with θ, the phase angle of i_{sa} exceeding u_{sa} equal to 0, 0.1π, 0.2π, …, π respectively, are selected to compare the three strategies, as shown in Figure 4.8. Additionally, in all simulation cases, the initial SOC of each submodule is 2%, with a corresponding DC-side voltage of 1050V. It should be noted that although it is convenient to conduct theoretical analysis with the angle δ, it is not practical to use δ as an input variable in simulation or engineering practice. For this reason, we use θ instead, and the simulation results can still reflect the corresponding theoretical analysis in section III because of a small difference between the two angles.

To quantify the power balancing capability of the three strategies, the relative standard deviation in reference to the rated normal power of every submodule is utilized, as is given in Equation (4.15). It can be seen that *DEV* reflects the degree of power consistency of submodules in the three phases.

$$\begin{cases} P_{\mathrm{r}}^{\mathrm{SM}} = \dfrac{S_{\mathrm{r}}^{\mathrm{BESS}}}{3N} \\ P_{\mathrm{ave}}^{\mathrm{SM}} = \dfrac{P_{\mathrm{a}}^{\mathrm{SM}} + P_{\mathrm{b}}^{\mathrm{SM}} + P_{\mathrm{c}}^{\mathrm{SM}}}{3} \\ DEV = \dfrac{1}{P_{\mathrm{r}}^{\mathrm{SM}}} \sqrt{\dfrac{\left(P_{\mathrm{a}}^{\mathrm{SM}} - P_{\mathrm{ave}}^{\mathrm{SM}}\right)^2 + \left(P_{\mathrm{b}}^{\mathrm{SM}} - P_{\mathrm{ave}}^{\mathrm{SM}}\right)^2 + \left(P_{\mathrm{c}}^{\mathrm{SM}} - P_{\mathrm{ave}}^{\mathrm{SM}}\right)^2}{3}} \end{cases} \tag{4.15}$$

Where $P_{\mathrm{r}}^{\mathrm{SM}}$ represents the rated normal power of one submodule, $P_{\mathrm{a}}^{\mathrm{SM}}$, $P_{\mathrm{b}}^{\mathrm{SM}}$ and $P_{\mathrm{c}}^{\mathrm{SM}}$ refer to the operating powers of every submodule in phases A, B and C, respectively, and *DEV* is the relative standard deviation.

4.4.2 Simulation Results on BESS No.1

Figures 4.9, 4.10 and 4.11 show DEV's scatter diagrams when BESS No.1 rides through faults '100', '110' and '200' respectively, with the three strategies employed separately. All the points in the three figures correspond with the PowerPoints selected in Figure 4.8. These DEV points in blue, yellow and black are about the three strategies: MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively. The square points indicate MVC is operating, while the round ones indicate MVC is not.

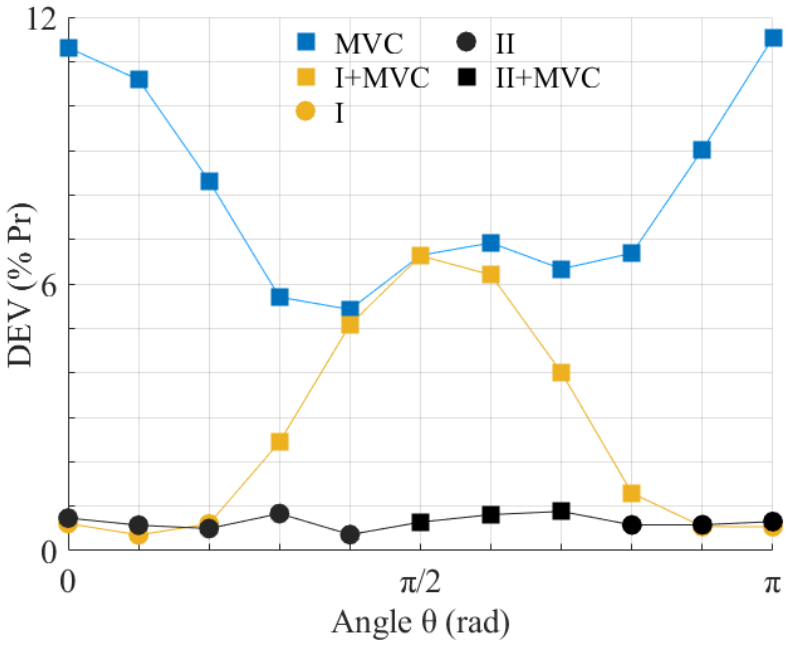


Figure 4.9 DEV scattering when BESS No.1 rides through fault '100', with the three strategies employed separately.

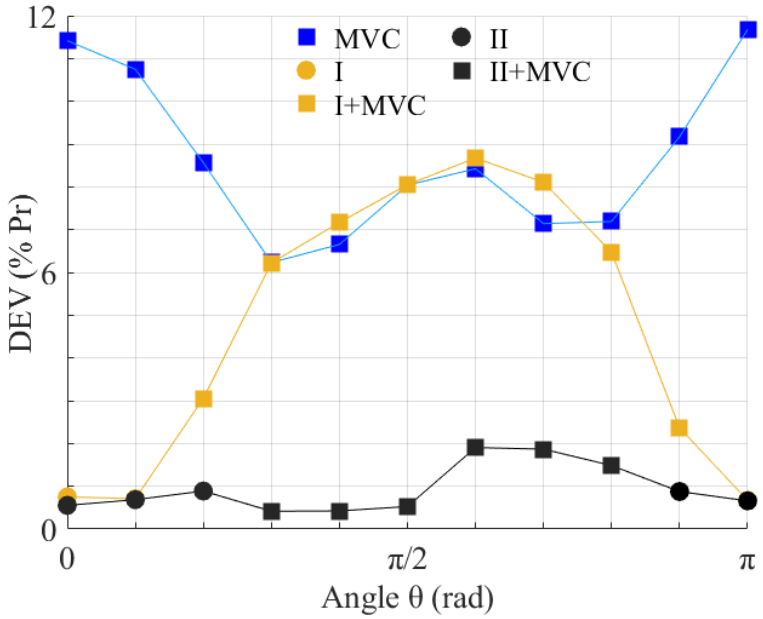


Figure 4. 10 DEV scattering when BESS No.1 rides through fault '110', with the three strategies employed separately.

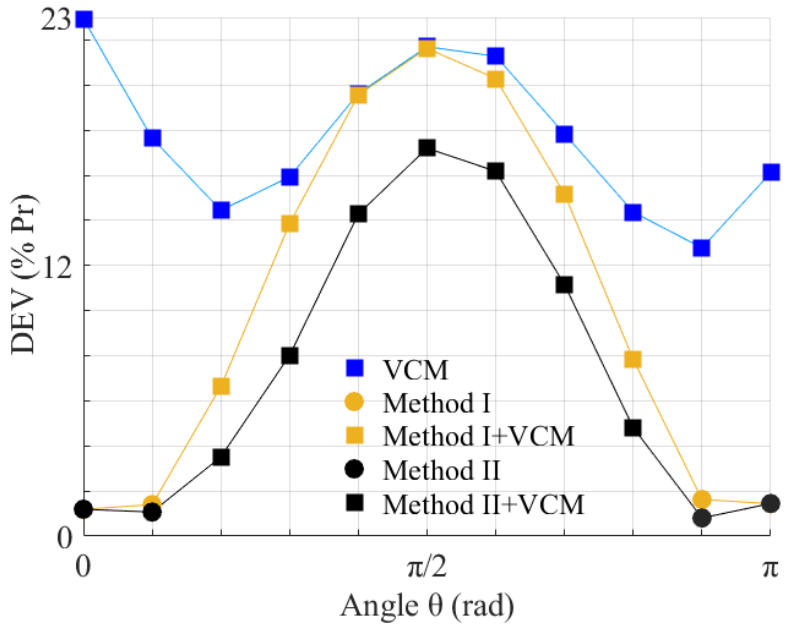


Figure 4.11 DEV scattering when BESS No.1 rides through fault '200', with the three strategies employed separately.

It can be seen from Figures 4.9, 4.10, and 4.11 that although the MVC method is applicable in cases of motor driving, it is less suitable in BESS due to the lack of capability for balancing power among submodules in different phases. The conventional method can equalize power among submodules in cases where the magnitudes of modulation voltages are relatively small, such as when θ is equal to 0, 0.1π or 0.2π in Figure 4.9. However, when the magnitudes of modulation voltages are greater than DC-side voltages, MVC has to act to limit the magnitudes of modulation voltages, dramatically weakening the power balancing capability of the method. In contrast, the proposed method has performed a significant ability to navigate through both faults of '100' and '110'. Although in some cases, such as cases of θ equal to 0.6π and 0.7π, MVC has operated to avoid voltage overmodulation, as shown in Fig. 8, the values of *DEV* increase slightly.

As shown in Figure 4.11, it is challenging for all strategies to balance power between submodules in different phases while operating under the fault '200', even though the hybrid strategy of the proposed method with MVC performs better than the other two strategies. In this scenario, because the DC-side voltage of phase A is significantly low

compared to fault '100' or '110', MVC has to act significantly to constrain the modulation voltage of phase A, causing power equalization impossible to perform effectively.

Figures 4.12, 4.13 and 4.14 depict the curves of some relevant voltages in one period of 0.02s, when the BESS navigated through the faults '100', '110' and '200', respectively, with θ equal to 0.7π. Each figure of the three left, middle and right columns shows curves of modulation voltages $u_{kn}^{ref}/w_{kn}^{ref}$, phase output voltages u_{kn} and BESS output voltages u_{ko}, separately, while rows from top to bottom refer to the employment of MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively. w_{kn}^{ref} are the modulation voltages derived from u_{kn}^{ref} reshaped by MVC. If MVC does not be triggered, u_{kn}^{ref} is directly used as modulation voltages.

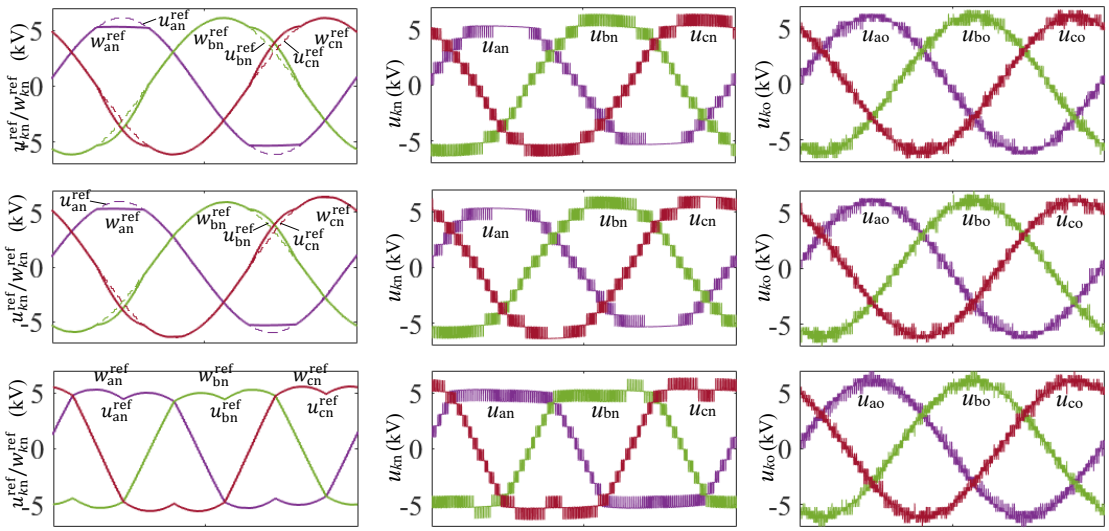


Figure 4.12 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '100' in case of θ equal to 0.7π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+MVC, respectively.

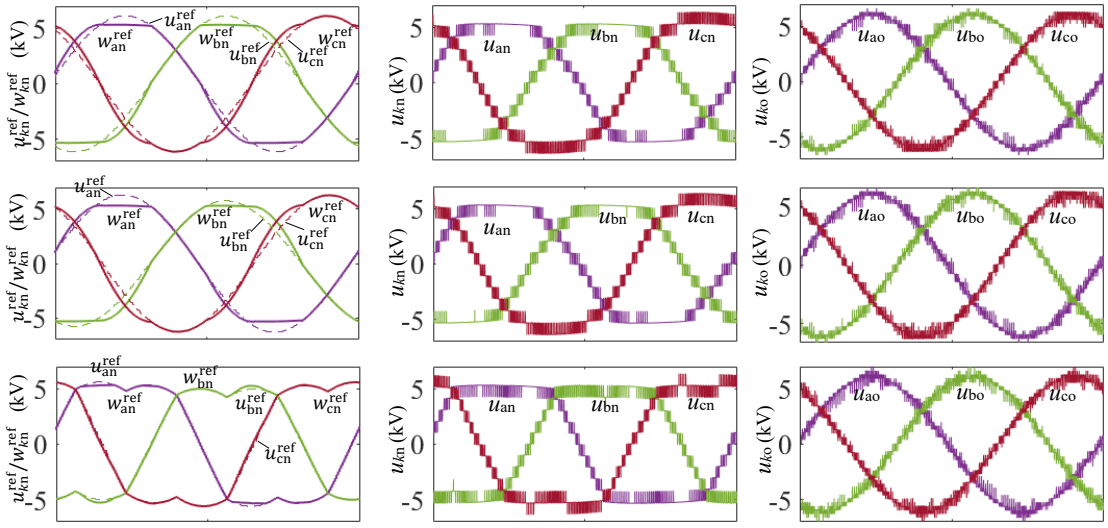


Figure 4.13 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '110' in case of θ equal to 0.7π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

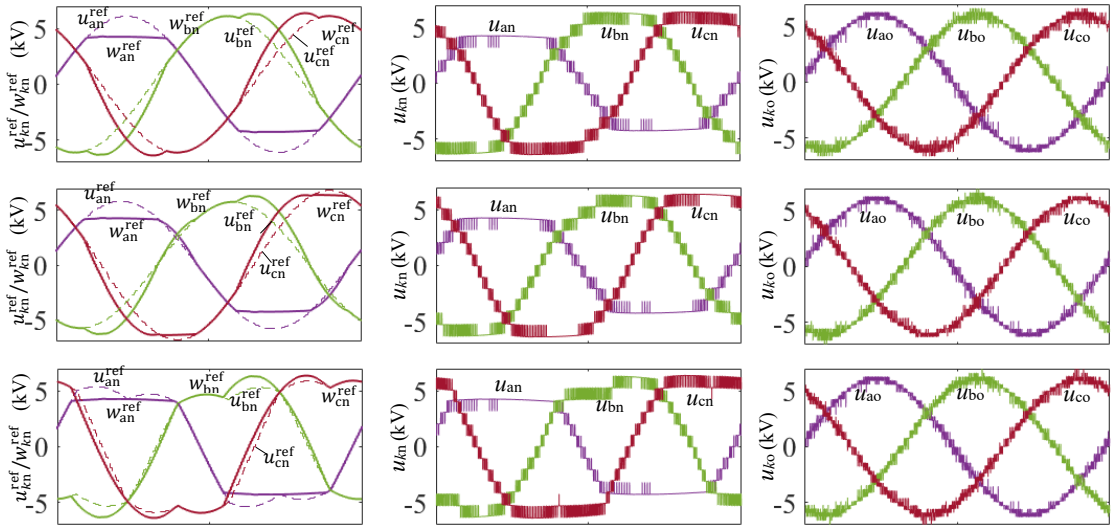


Figure 4.14 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '200' in case of θ equal to 0.7π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

We can see from Figure 4.12 that voltages u_{kn}^{ref} of the proposed method are almost directly utilized as modulation voltages without the interference of MVC, and Figure 4.13 shows that MVC just slightly reshapes u_{kn}^{ref} of the proposed method to modulation voltages w_{kn}^{ref}, so the hybrid method of II+ MVC performs a noticeable power balancing capability in fault conditions of either 100 or 110. In contrast, in either Figure 4.12 or

4.13, MVC significantly reshapes u_{kn}^{ref} of the conventional method to w_{kn}^{ref}, cause its power balancing capability weakened. As is shown in Figure 4.14, MVC greatly interferes with the voltage u_{kn}^{ref} of either the conventional or proposed method, degrading their power equalisation capability.

There is a small difference between δ and θ, as aforementioned. Also, resistances in the BESS system have been considered in the design and simulation, which has been neglected in the theoretical analysis above. However, Figures 4.12 and 4.13 fully confirm the theoretical analysis. For example, from the middle row of Figure 4.12, it can be seen that voltage overmodulation will occur at phase A without interference of MVC, and phase C is more susceptible to voltage over modulation than phase B, as depicted in Figure 4.1. Another example is only phase A suffers voltage overmodulation during navigating fault '110' with the proposed method in case of θ equal to 0.7π, as shown in Figure 4.1, and Figure 4.12 conforms to the conclusion.

Figures 4.15, 4.16 and 4.17 give the Total Hamonic Distortion (THD) of the output voltages u_{ko} and currents i_{sk}, in cases of the BESS riding through faults '100', '110' and '200', respectively. It can be seen from the three figures the THD difference of either voltages or currents between the three strategies is negligible.

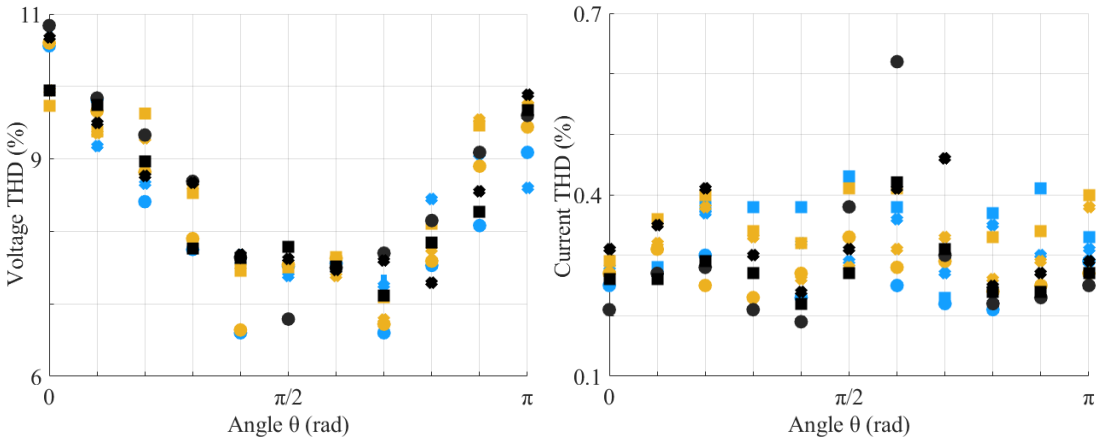


Figure 4.15 Total Hamonic Distortion (THD) scattering of output voltages and currents of the BESS under the fault condition of '100'.
Points in blue, yellow and black refer to MVC, hybrid method of I+MVC and hybrid method of II+

MVC, respectively. And the round, square and star points correspond to phases A, B, and C, respectively.

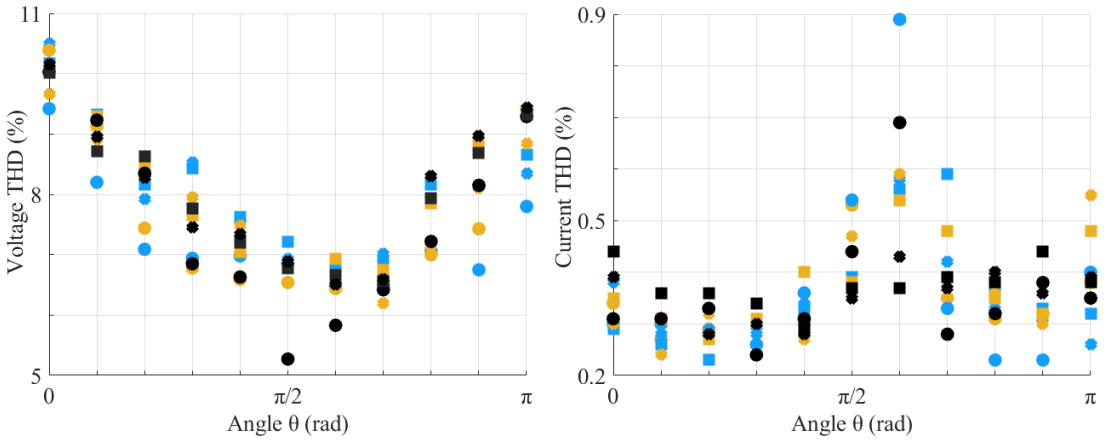


Figure 4.16 Total Hamonic Distortion (THD) scattering of output voltages and currents of the BESS under the fault condition of '110'.
Points in blue, yellow and black refer to MVC, hybrid method of I+MVC and hybrid method of II+MVC, respectively. And the round, square and star points correspond to phases A, B, and C, respectively.

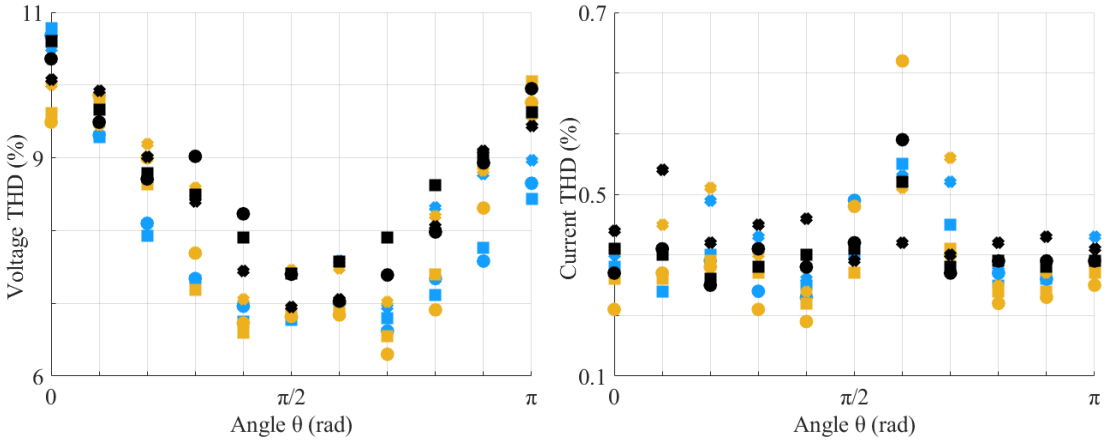


Figure 4.17 Total Hamonic Distortion (THD) scattering of output voltages and currents of the BESS under the fault condition of '200'.
Points in blue, yellow and black refer to MVC, hybrid method of I+MVC and hybrid method of II+MVC, respectively. And the round, square and star points correspond to phases A, B, and C, respectively.

When the BESS rides through a double-submodule fault, either '110' or '200', the occurrence of voltage overmodulation is difficult to completely avoid in some cases, such as the case of θ equal to 0.6π, regardless of fault-tolerance strategies employed, which is depicted in Figures 4.18 and 4.19. This is because the magnitudes of one or two of three required phase-to-phase voltages are greater than the sum of DC-side

voltages of the corresponding two phases, as expressed in Equations (4.16) and (4.17). After further investigation, it can be concluded that the maximum modulation ratio is around 1.03. However, the voltage modulation does not significantly affect waveforms of output voltages and currents, as shown in the relevant results mentioned above.

$$U_{\mathrm{ab}}^{\mathrm{ref}} > E_{\mathrm{a}} + E_{\mathrm{b}} \tag{4.16}$$

$$\begin{cases} U_{\mathrm{ab}}^{\mathrm{ref}} > E_{\mathrm{a}} + E_{\mathrm{b}} \\ U_{\mathrm{ca}}^{\mathrm{ref}} > E_{\mathrm{a}} + E_{\mathrm{c}} \end{cases} \tag{4.17}$$

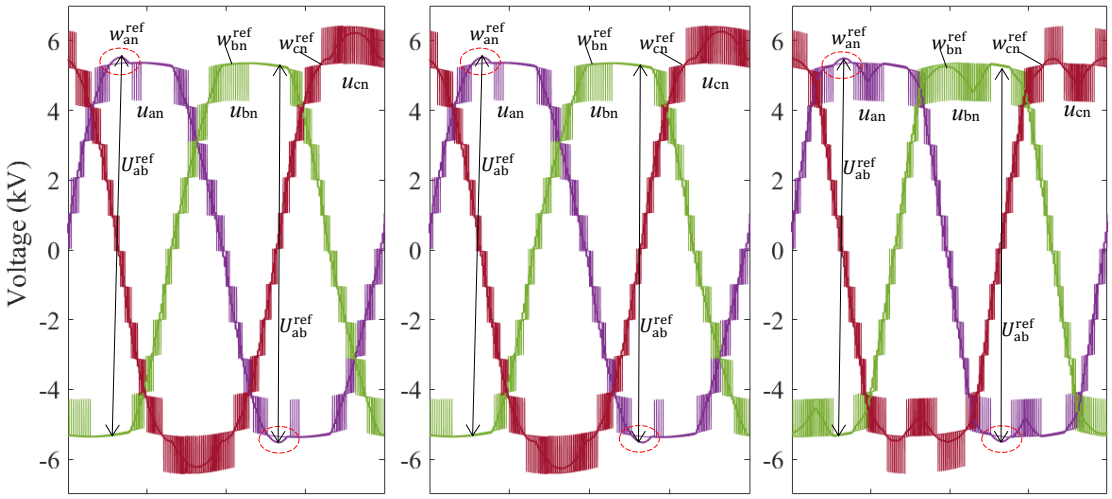


Figure 4. 18 Occurrence of voltage overmodulation when the BESS rides through fault '110'. Overmodulation parts are circled in red. The left, middle and right columns refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

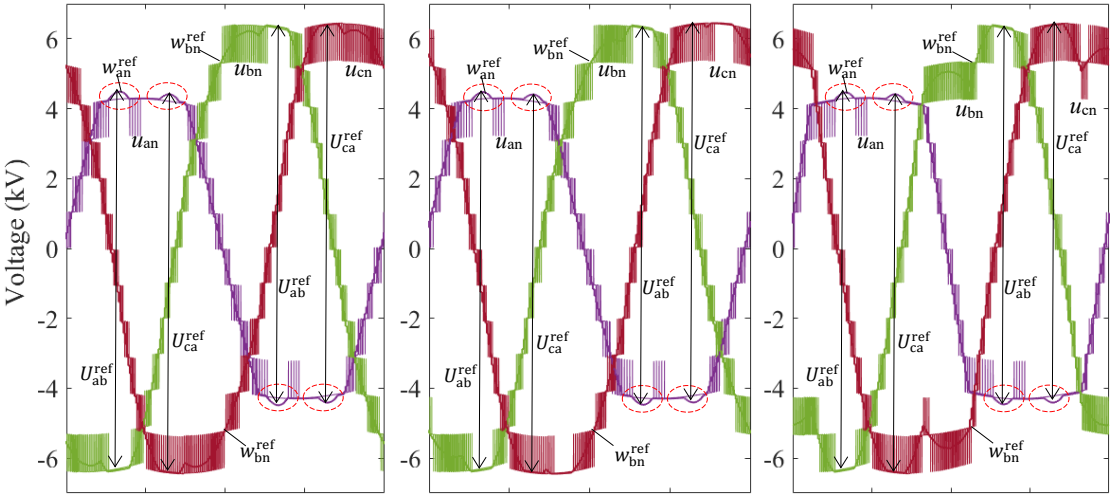


Figure 4. 19 Occurrence of voltage overmodulation when the BESS rides through fault '200'. Overmodulation parts are circled in red.
The left, middle and right columns refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

4.4.3 Simulation Results on BESS No.2

Figure 4.20 shows DEV scattering when BESS No.1 rides through several faults, with the three strategies employed separately. It can be seen that the conventional strategy can ride through single-submodule fault '100' with the achievement of power balancing (maximum value of DEV is around 2% at equal to θ equal to 0.5π) and DC-side voltage restraint. At the same time, it cannot meet the power balancing requirement in the cases of the other five faults. In contrast, the proposed strategy can achieve both the goals of power balancing and voltage overmodulation, avoiding simultaneously in the cases of faults '100', '110', '200', '210' and '211', presenting a significant applicability. When navigating through fault '300', although the performance of the proposed strategy is better than that of the conventional one, the ability to balance power has deteriorated noticeably due to the substantial interference of MVC.

It should be noted that the value of DEV is continuously greater than zero, keeping around 1%, even without the interference of MVC, which means the powers of submodules are not strictly equal. This is because these strategies are based on the reference value of $u_{k\mathrm{o}}$, which differs from the theoretical analysis above. If a tolerance-free balance is required, feedback control can be applied. However, this will not be investigated in this paper.

Figures 4.12, 4.13 and 4.14 depict the curves of some relevant voltages in one period time of 0.02s, when the BESS navigate through the faults '100', '200', '210' and '300', respectively, with θ equal to 0.7π. Similar conclusions to section 4.42 can be drawn.

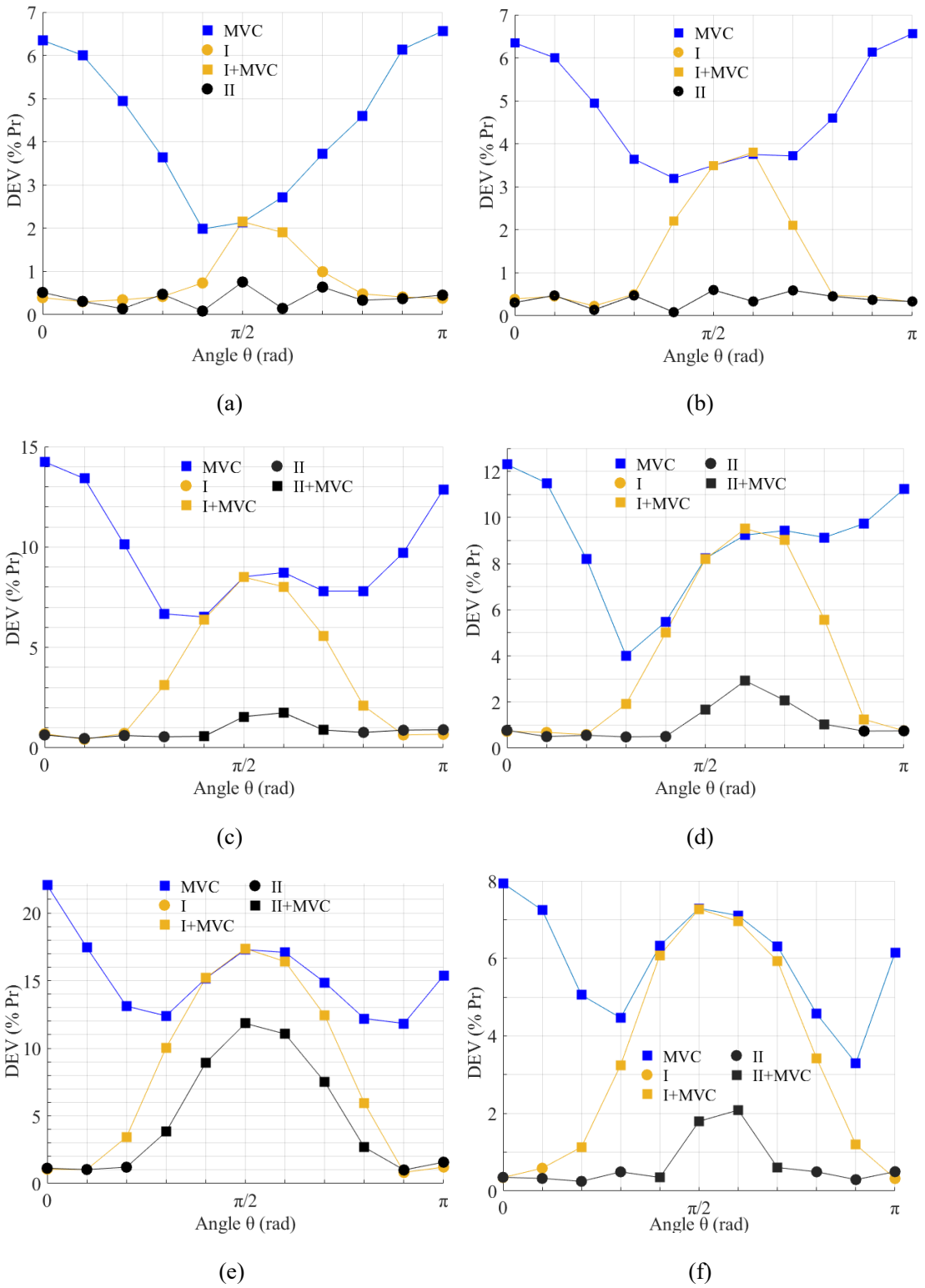


Figure 4.20 DEV scattering when BESS No.1 rides through several faults, with the three strategies employed separately.

(a) fault '100'. (b) fault '110'. (c) fault '200'. (d) fault '210'. (e) fault '300'. (f) fault '211'.

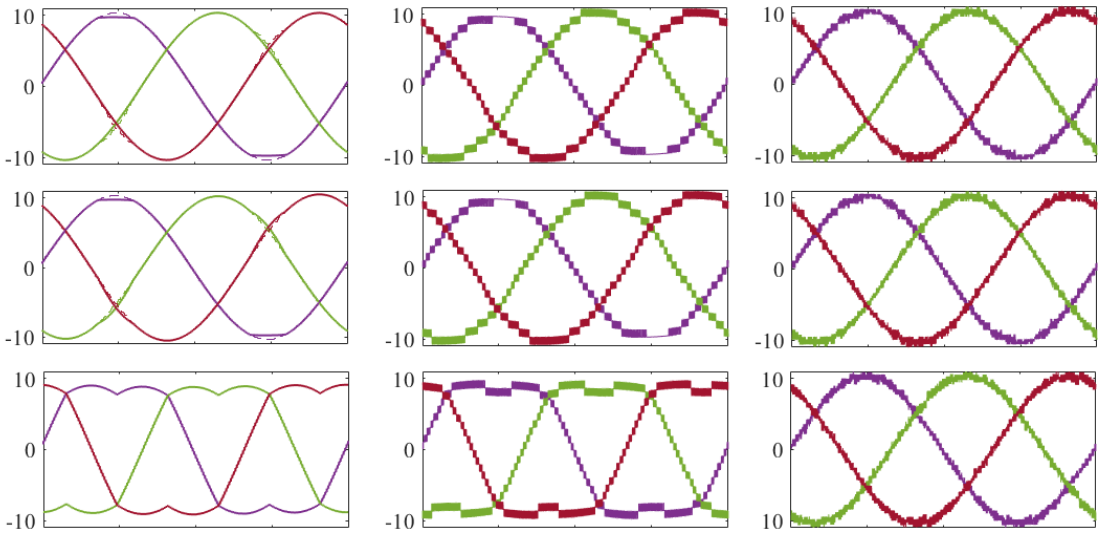


Figure 4.21 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '100' in case of θ equal to 0.6π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

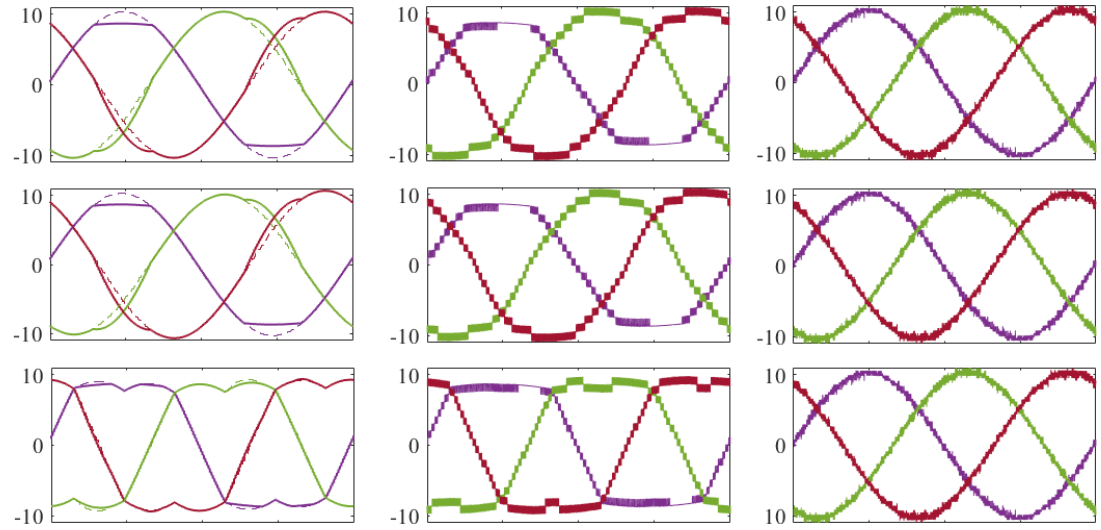


Figure 4.22 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '200' in case of θ equal to 0.6π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

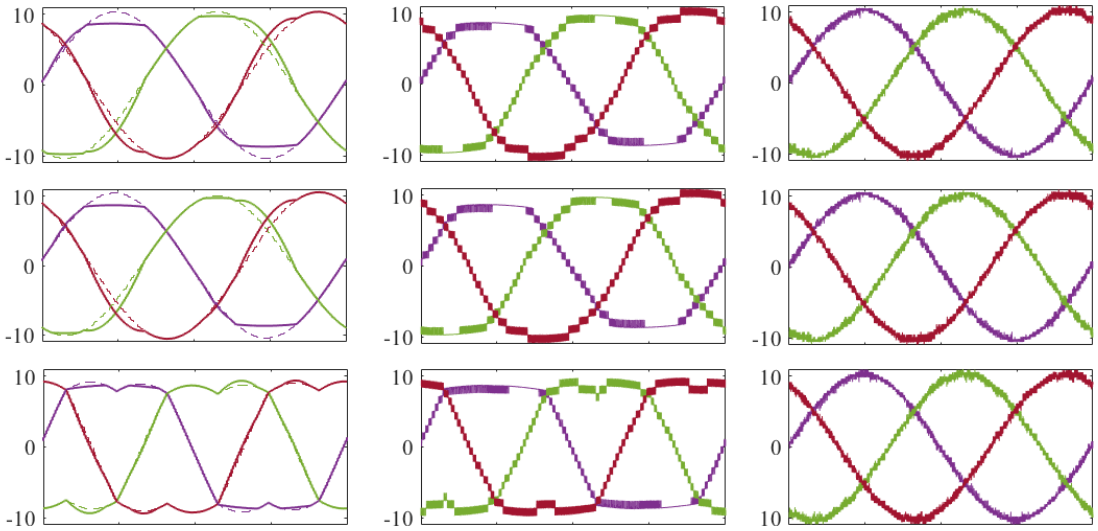


Figure 4.23 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '210' in case of θ equal to 0.6π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

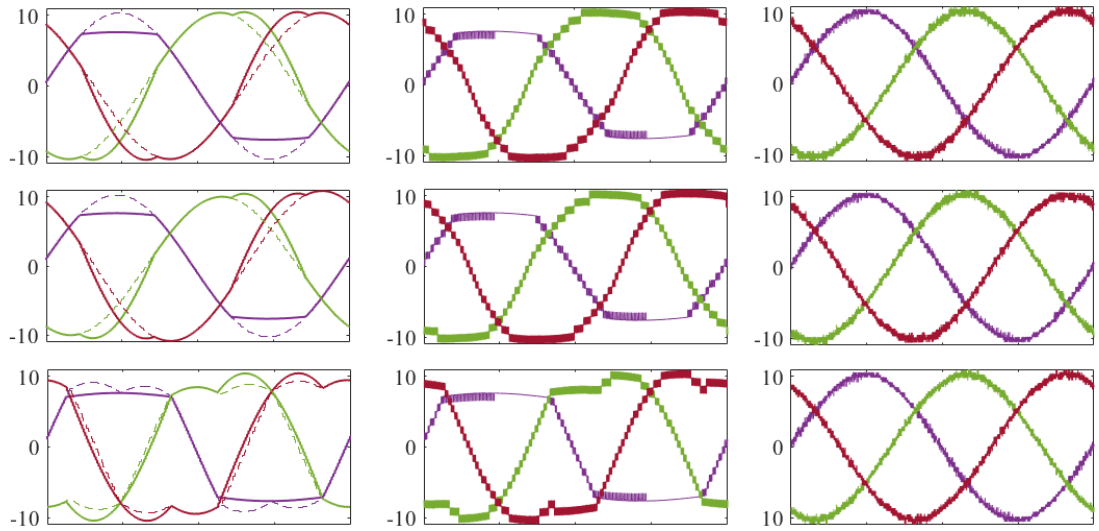


Figure 4.24 Curves of some relevant voltages in one period of 0.02s, when the BESS navigate through the faults '300' in case of θ equal to 0.6π, separately with the three strategies.
The top, middle and bottom rows refer to MVC, hybrid method of I+MVC and hybrid method of II+ MVC, respectively.

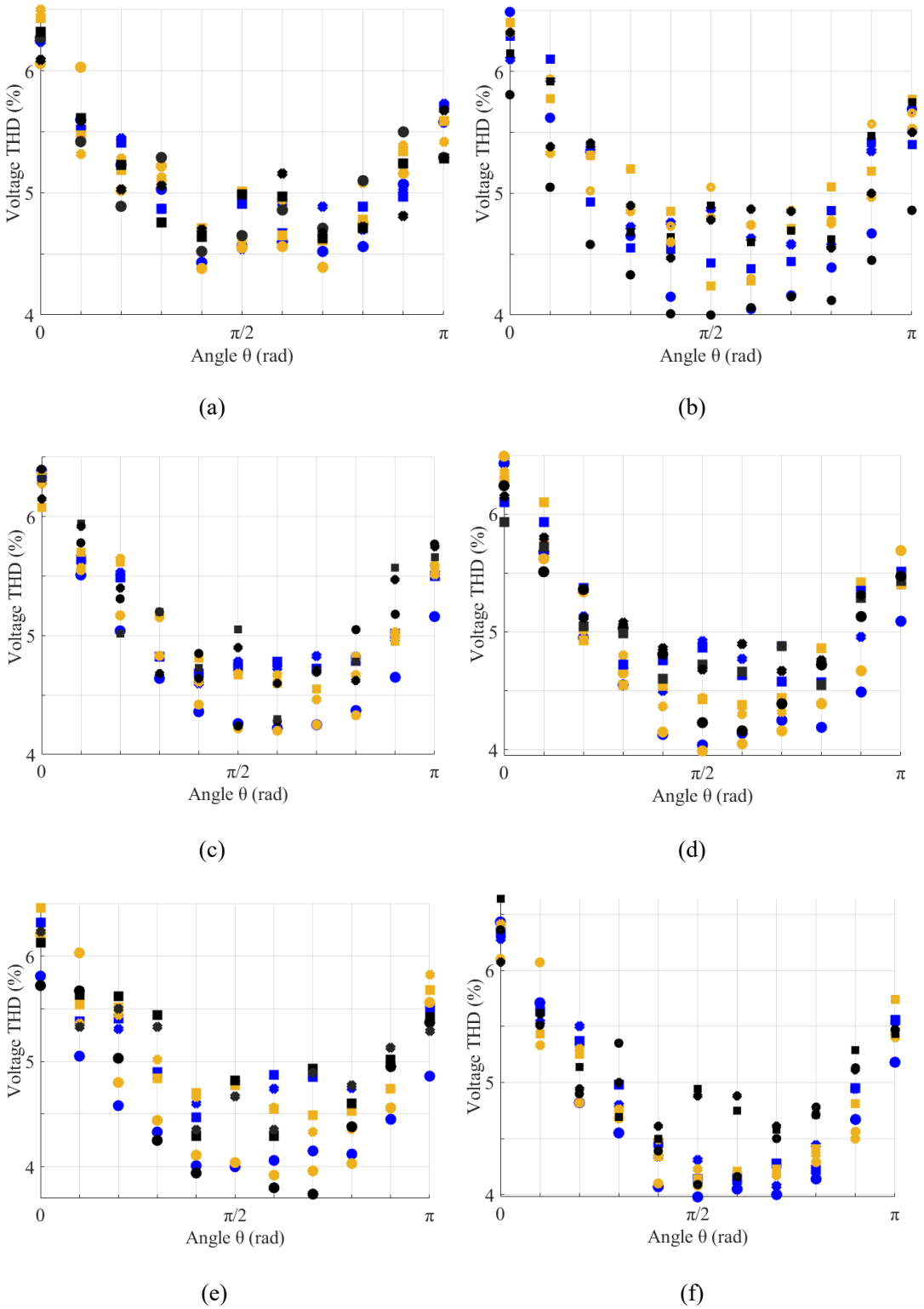


Figure 4.25 Total Hamonic Distortion (THD) scattering of output voltages of BESS No.2 under a series of fault conditions.

Points in blue, yellow and black refer to MVC, hybrid method of I+MVC and hybrid method of II+MVC, respectively. And the round, square and star points correspond to phases A, B, and C, respectively. (a) fault '100'. (b) fault '110'. (c) fault '200'. (d) fault '210'. (e) fault '300'. (f) fault '211'.

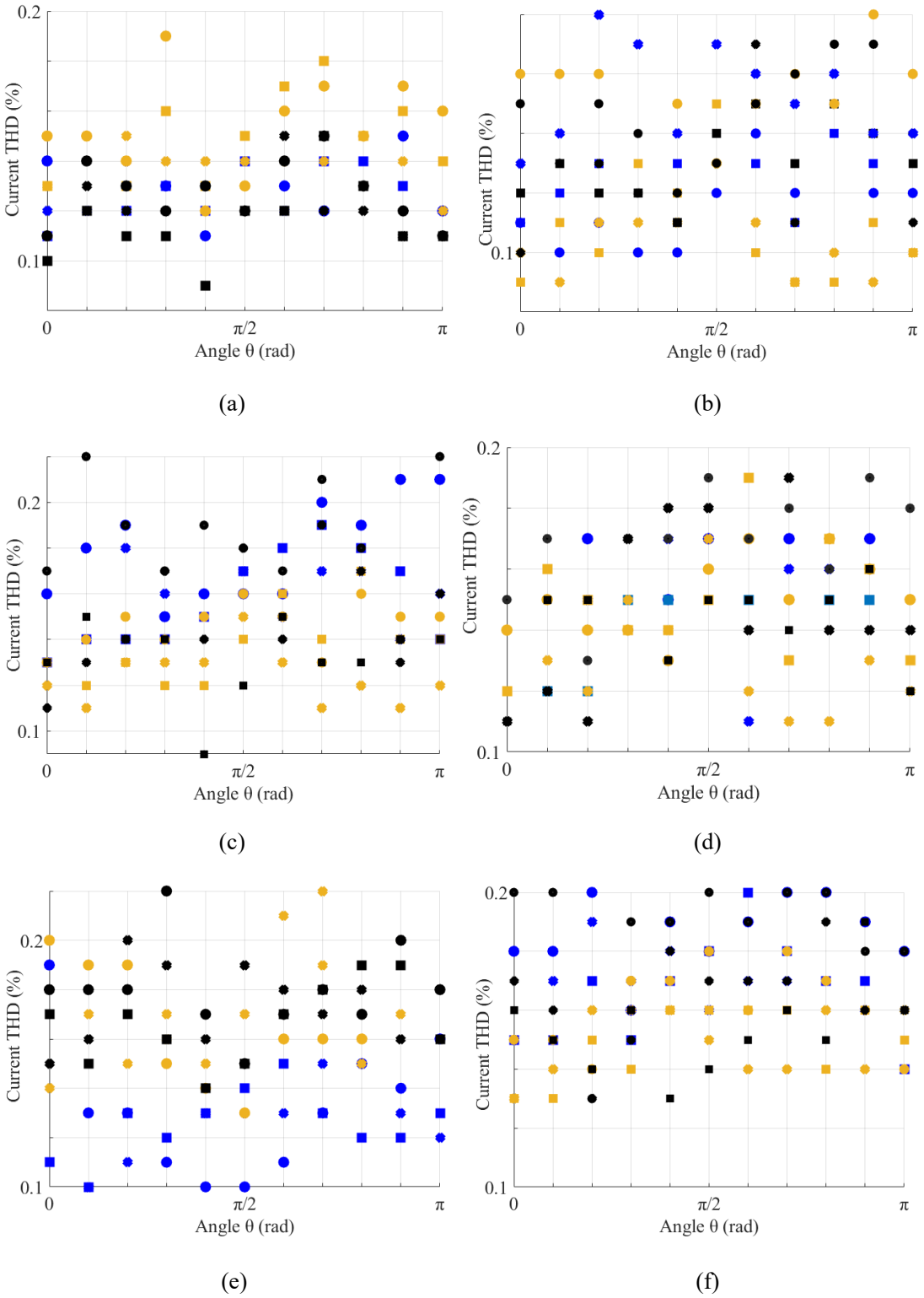


Figure 4. 26 Total Hamonic Distortion (THD) scattering of output currents of BESS No.2 under a series of fault conditions.

Points in blue, yellow and black refer to MVC, hybrid method of I+MVC and hybrid method of II+MVC, respectively. And the round, square and star points correspond to phases A, B, and C, respectively. (a) fault '100'. (b) fault '110'. (c) fault '200'. (d) fault '210'. (e) fault '300'. (f) fault '211'.

Figures 4.24 and 4.25 give the Total Hamonic Distortion (THD) of the output voltages u_{ko} and currents $i_{sk,}$ respectively, when BESS No.2 rides through a series of faults. It can be seen from the three figures the THD difference of either voltages or currents between the three strategies is negligible. The values of voltage THD are mainly between 4% and 6.5%, and they scatter in a 'V' shape. This is because as the magnitude of u_{ko} increases, the number of voltage levels employed grows, reducing the THD of u_{ko}. Current THD values are predominantly between 0.1% and 0.2%.

4.5 Conclusion

This chapter proposes an innovative fault-tolerance strategy for CHB-BESS to operate under fault conditions with power balance among all submodules and without voltage overmodulation. Theoretical analyses show that the modulation voltage a-mplitude of the new strategy is significantly lower than that of the conventional strategy when coping with the same fault and exhibits a wider range of applicability. Simulation results based on 6kV 2MW/6.72MWh CHB-BESS and a 10kV 5.5MW/11.2MWh CHB-BESS in Matlab/Simulink confirm that, under various operating conditions, the proposed solution exhibits negligible differences in output power quality compared to the conventional method. Moreover, the new strategy has significantly enhanced sub-module power equalization capability compared to the conventional approach, demonstrating superior efficiency and applicability.

Chapter 5

Discussion and Conclusions

5.1 Introduction

This chapter discusses all of the main stages of this research. The main stages of this research are a bibliography study, theoretical analysis, simulation development data collection, and signal pre-processing. These stages are layered on each other and make up this thesis. Some of the problems encountered or items for attention at each stage are described in this chapter. Also, the pros and cons of each stage are described, along with some potential work extensions that can be implemented for further research.

5.2 Bibliography Study

The research involves a large amount of bibliography study, mainly focusing on the existing papers on CHB-BESS and MMC-BESS, as well as on CHB converters of medium-voltage variable speed drives. While the CHB converter for BESS is a relatively new application of the technology, the CHB converter for frequency control of induction motors has a long history of research. Therefore, these papers often provide some inspiration for CHB-BESS research and avoid getting stuck in a mindset.

5.3 Theoretical analysis

Theoretical analysis is essential to an academic thesis, and mathematics is a fundamental tool for carrying out theoretical analysis. This thesis provides a detailed theoretical analysis of the proposed and traditional strategies and mathematically compares them as shown in Sections 3.2, 3.3, 4.2 and 4.3. Many of the analytical formulations are original and not available in the existing literature, such as Equation (3.9), (3.11), (4.11) and (4.12), among others. The software Matlab was mainly used in

this part of the research.

5.4 Simulation Development

The simulation software Matlab/Simulink is exclusively employed in the research. Simulink library has numerous predefined modules, including electrical elements and signal processing modules. Simulink predefines a significant portion of basic signal processing modules used in the research, such as the Phase Locking Loop (PLL) module, 'abc/dq0' and 'dq0/abc' transform modules, and Fast Fourier Transform (FFT) module. Therefore, building a desired simulation model for CHB-BESS is relatively straightforward. Nevertheless, there are some matters of concern.

Firstly, the functionality of PLL can implemented by either an analogue circuit or program, corresponding to continuous and discrete models in the Simulink library, respectively. In practice, the function can be realized by a Digital Signal Processor (DSP) of CHB-PCS, so the discrete PLL model is the better choice to facilitate converting the digital part of the model into a C++ program in case of subsequent experimenting.

Secondly, in some cases, utilizing preset elements to build a specified module is not that convenient, so customized modules based on Matlab language are an indispensable complement. For example, to realize Equations (3.9) and (3.11), a Matlab language-based modelling solution tends to be more flexible. This means that some degree of programming skills are necessary for this research.

Finally, PS-PWM is a triangular carrier-based modulation method realized by analogue components. This means zero crossing points between modulation signals and carriers are necessary at the sampling time, so in many cases, the continuous model should be set up for PS-PWM in consideration of simulation accuracy. Typical scenarios that require strict simulation accuracy are the validation of power control strategies and the analysis of current and voltage harmonic content (Section 3.4.2, 4.4.2 and 4.4.3).

Therefore, variable-step solvers are a more appropriate way to solve this model than fixed-step ones. However, the high-frequency characteristics presented by the model make the simulation consume a lot of time, especially when the goal of the simulation is to validate the efficiency of SOC balancing strategies (Section 3.4.3), where the simulation time scale is on the order of minutes, resulting in an unacceptable runtime for the simulation. In this case, a fixed solver is employed, and the model of the BESS is decomposed reasonably into several parts for multi-core CPUs to run the model in parallel.

The high number of submodule cascades, 120 semiconductor switching elements alone, results in a very high matrix order for the mathematical equations so that the solution of the analogue circuits consumes a significant portion of the computational resources. To address this issue, the primary circuit model is divided into four parts, as shown in Figure 5.1, and then these parts are assigned to four different cores of a computer.

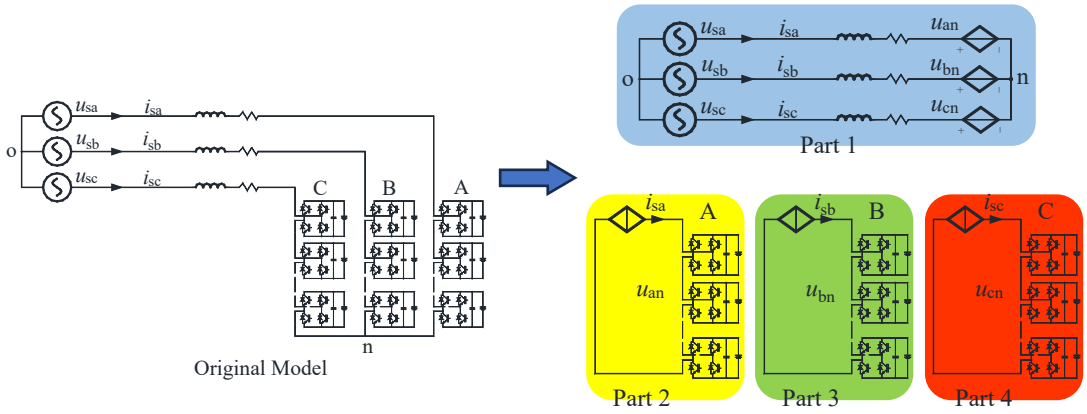


Figure 5. 1 The Primary circuit model is split into four parts, aiming to adapt to multicore computation.

In Figure 5.1, each sub-model is solved using data from the previous sampling moment of the other sub-models instead of the current sampling moment. For example, $i_{sa}(k)$ is derived from $u_{sa}(k)$ and $u_{an}(k\text{-}1)$ instead of $u_{an}(k)$. The four sub-models are mathematically separated rather than associative, significantly improving the speed of solving the whole model. This naturally reduces the simulation accuracy to some extent. However, it is sufficient to validate the effectiveness of the SOC balancing strategies.

Continuous sub-systems are assigned a smaller simulation step as shown in Table 5.1, to ensure that the simulation has a certain degree of accuracy. The BESS and PS-PWM are assigned the smallest simulation step due to their high-frequency characteristics at the 10kHz level. On the other hand, the discrete sub-systems are assigned simulation steps according to the actual sampling frequency. It should be noted that subsystems with different simulation steps should be assigned to other CPU cores.

Table 5.1 Simulation step of sub-systems in the parallel model for Section 3.4.3.

Sub-System	Nature of Sub-System	Simulation Step
Power Grid (Part 1 in Figure 5.1)	Continuous	0.02 ms
A Phase of BESS (Part 2 in Figure 5.1)	Continuous	0.01 ms
B Phase of BESS (Part 3 in Figure 5.1)	Continuous	0.01 ms
C Phase of BESS (Part 4 in Figure 5.1)	Continuous	0.01 ms
PS-PWM	Continuous	0.01 ms
Power Control	Digital	0.1 ms
Other	Digital	1s, 0.2ms, 0.1 ms

5.4 Data Collection and Signal Pre-processing

The important parameters of the BESS, as shown in Tables 3.4, 4.2 and 4.3, are derived from the currently popular commercially available products. In contrast, the distribution network parameters are selected based on the general situation of the distribution network of the corresponding voltage levels in China.

Due to the long simulation run time and the large amount of data, it is more realistic to use the ‘To File’ module than the ‘To Workspace’ module to obtain the data. In solving the variable-step model, the steps are often very short, on the order of microseconds, and therefore the amount of data generated is large. In solving the fixed-step model, the

data is also large because the simulation time is on the order of minutes. It should be noted that the frequency of data collection should be reasonable. For example, in the fixed-step model, since the simulation step of the BESS subsystem is 0.01ms, as shown in Table 5.1, setting the step of the voltage signal u_{kn} data interception to be the same as simulation step of the subsystem will result in a large amount of data, which may exceed the storage space of the computer. In the simulation, the 'To File' module's' Decimation' is set to 200, as shown in Figure 5.2. Similar operations are required for other data acquisition.

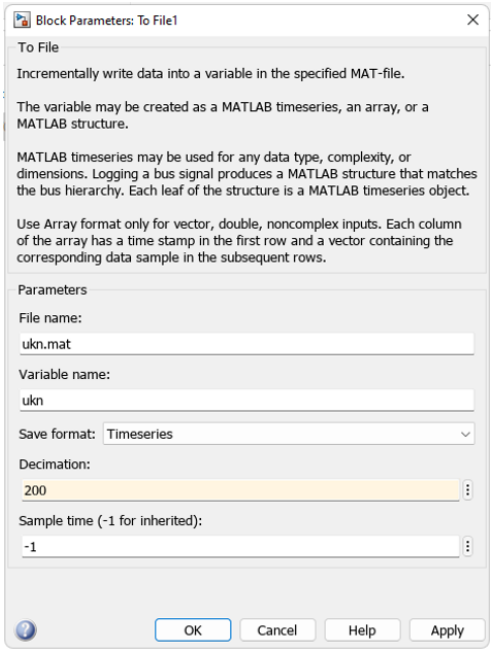


Figure 5.2 Parameter configuration window of module 'To File'.

FFT Analyzer of the module 'powergui' recognizes the signal format of 'Time structure', while the module 'To File' outputs signals with the format of 'Timeseries'. Therefore, voltage and current signals must be transformed from the format of 'Timeseries' to 'Time structure' with Matlab codes before conducting Fast Fourier Transform (FFT) analysis.

5.5 Conclusions

In summary, this research has investigated aspects of BESS's CHB-PCS. In addition to outlining the application scenarios of BESS and the main research directions of CHB-BESS, this thesis focuses on two directions, mainly related to PI decoupling power control, PS-PWM, SOC equalization and fault tolerance.

The areas which had been covered in this research included:

- Overview of BESS applications, typical topologies, and current research hotspots of CHB-BESS and literature review.
- Basic working principle and mathematical model of CHB-BESS, PI decoupling control strategy and PS-PWM mechanism of CHB-BESS.
- Further investigation of the conventional inter-phase SOC balancing strategy of CHB-BESS, presentation of one new strategy, and then theoretical and simulation comparison of the two strategies.
- Further investigation of the conventional fault-tolerance strategy of CHB-BESS, presentation of one new strategy, and the theoretical and simulation comparison of the two strategies are needed.

The main contributions of the research are summaried as following:

- Proposed a new self-adaptive inter-phase SOC balancing control strategy, reducing modulation voltage by 13.4% and enhancing zero-sequence voltage. This strategy dynamically adjusts based on real-time conditions, optimizing DC voltage usage and preventing overmodulation.
- Proposed an innovative fault-tolerance strategy to improve fault-tolerance capability of BESS during sub-module failures. It ensures balanced power among sub-modules and prevents overmodulation, offering better reliability than conventional methods.

This research achieved satisfactory results, and the proposed new strategy has some

advancement; therefore, it is promising for application and can be used to fully reach the upper limit of the intrinsic inter-phase SOC balancing and fault-tolerance capacity of CHB-BESS.

5.6 Recommendations

- Bibliography study

— more studies can focus on the existing academic papers on Cascaded H-Bridge Static Var Generator (CHB-SVG) and CHB converters of medium-voltage variable speed drives. Although CHB-BESS has a much wider range of operating states than CHB-SVG, CHB-SVG is more academically and commercially mature. Thus, there must be excellent academic results that can be adapted to BESS.

- Inter-phase SOC balancing strategy

— A common-mode square voltage can be injected instead of a common-mode sine voltage. A square wave has a fundamental amplitude of $4/\pi$ of its amplitude, so by injecting square voltage, the SOC balancing efficiency can still be improved when the DC-side voltage is low. It is necessary to derive the analytical equation of the corresponding V_{0max} to analyze its performance on a theoretical basis and avoid voltage overmodulation.

— The strategy of adaptive regulation of the neutral point voltage incorporating Modulation Voltage Clapping (MVC) methods to avoid overmodulation must be very promising. Thus, it can be studied in depth in the future. The strategies of injecting a common mode voltage of pre-determined waveform are mathematically analytical. Therefore, it is naturally challenging to reach the limits of the inter-phase SOC balancing potential of the BESS.

- Fault-tolerance Strategy

— A closed-loop control strategy can be investigated to make *DEV* equal to 0 without MVC intervention. The strategy presented in Chapter 4 is open-loop, and since the

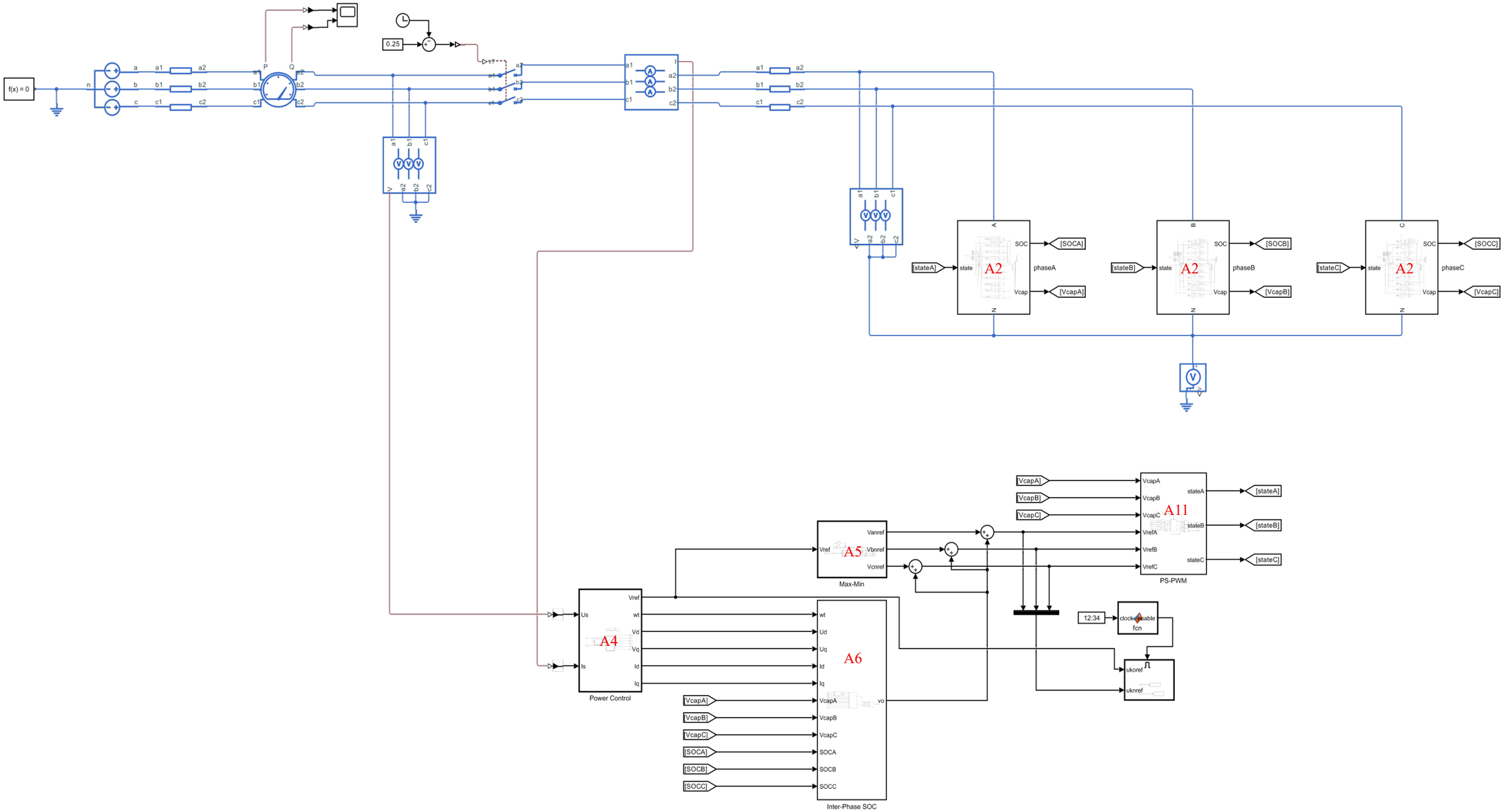
calculation of the zero-sequence voltage is based on the reference values of $i_{\mathrm{d}}^{\mathrm{ref}}$, $i_{\mathrm{q}}^{\mathrm{ref}}$, $u_{\mathrm{d}}^{\mathrm{ref}}$ and $u_{\mathrm{q}}^{\mathrm{ref}}$ rather than the actual values of i_{d}, i_{q}, u_{d} and u_{q}, as shown in Figure (3.6), coupled with system parameter errors, even if the MVC does not intervene, the *DEV* is still slightly greater than 0. Therefore, the closed-loop strategy can be investigated based on the actual power feedback from the submodules.

— The strategy of adaptive regulation of the neutral point voltage incorporating Modulation Voltage Clapping (MVC) methods to avoid overmodulation must be very promising. Thus, it can be studied in depth in the future. The strategies of injecting a common mode voltage pre-determined in Table 4.1 are not flexible enough, and it is naturally challenging to reach the limits of the inter-phase SOC balancing potential of the BESS as they are analytical methods.

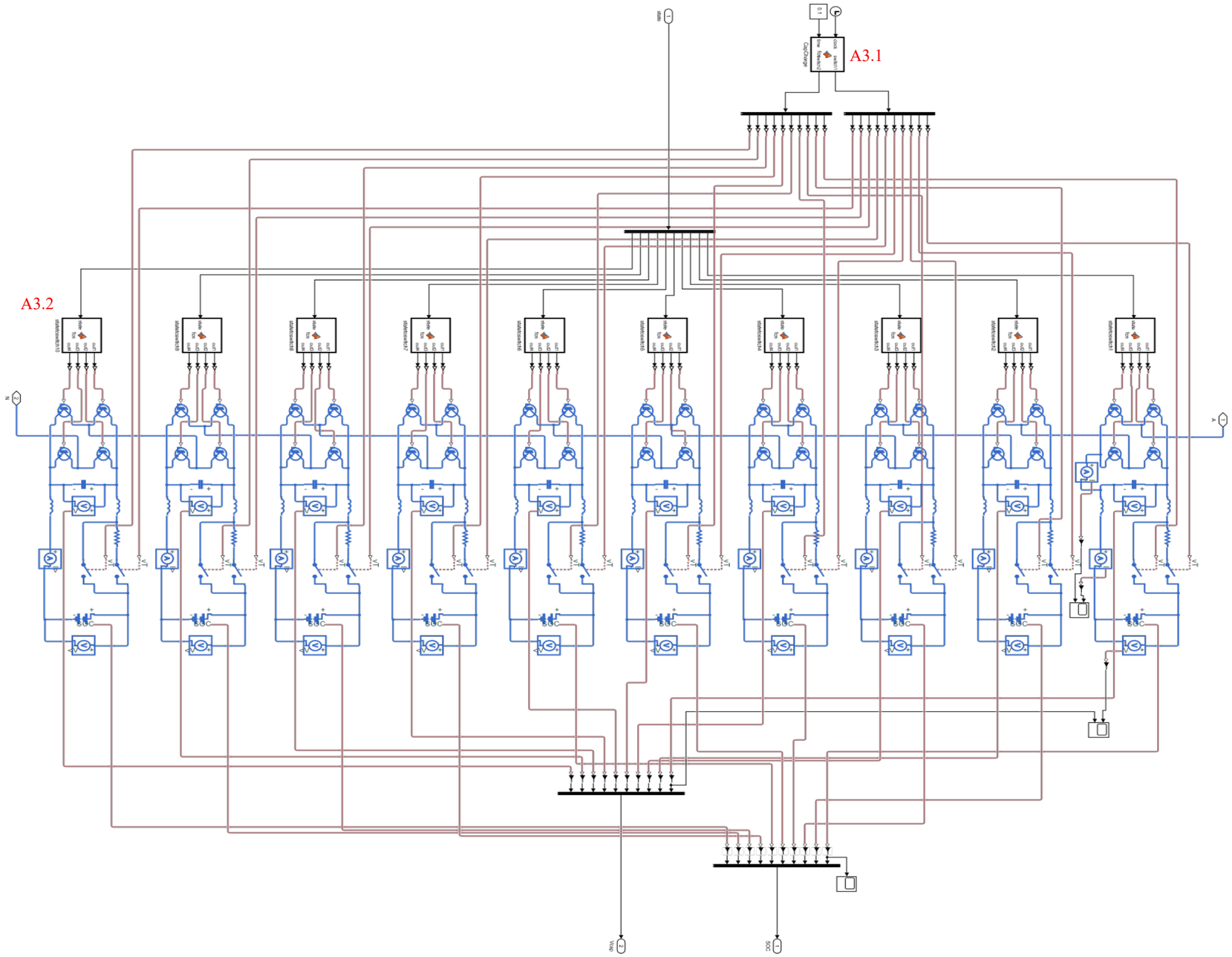
- Experiments

Experiments can be implemented to validate the new strategies proposed in this thesis further in the future. In this thesis, the effectiveness of the new strategies is not only discussed in depth in the theoretical analysis but also verified through a large number of simulations. However, due to time constraints, experiments were not implemented to validate the proposed strategies.

Appendix A1 Simulink Model of Inter-phase SOC balancing Control used for THD Calculation.



Appendix A2　Sub-Model of Cascaded H-Bridge Submodules (Phase A)



Appendix A3 Matlab Codes Involved in Appendix A2

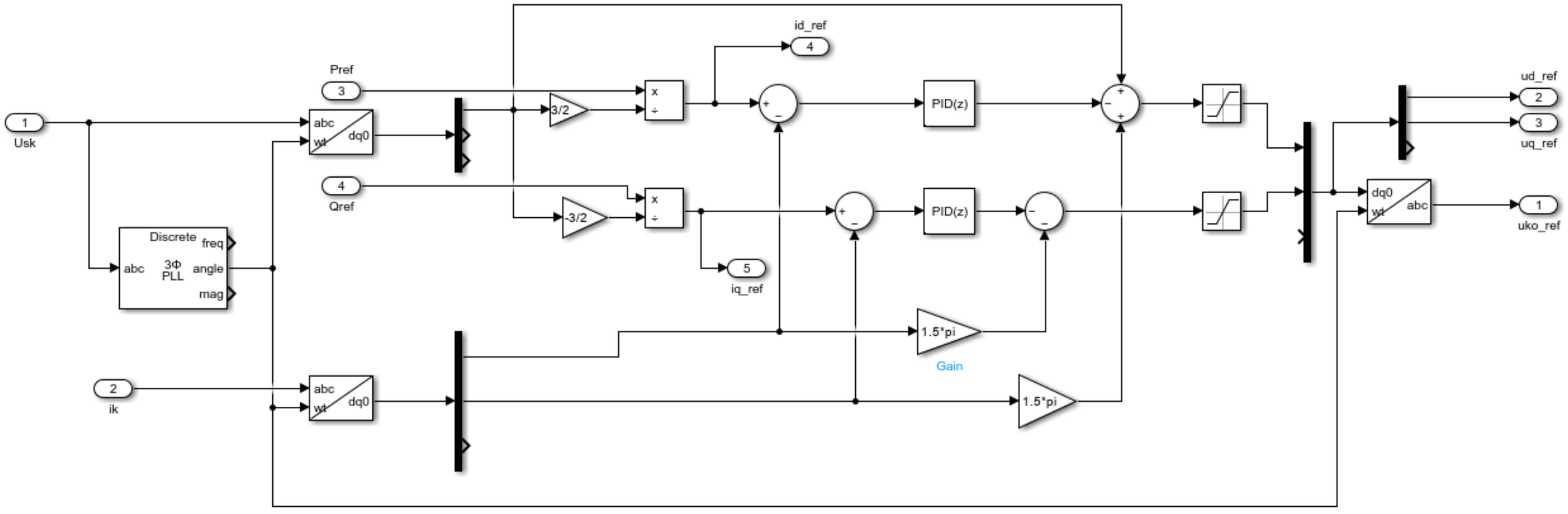
A3.1 Charging Capacitor

```
function [switch1,switch2] = fcn(clock,time)
switch1=[1,1,1,1,1,1,1,1,1,1];
switch2=[0,0,0,0,0,0,0,0,0,0];
if clock>time
    switch1=[0,0,0,0,0,0,0,0,0,0];
    switch2=[1,1,1,1,1,1,1,1,1,1];
end
end

```

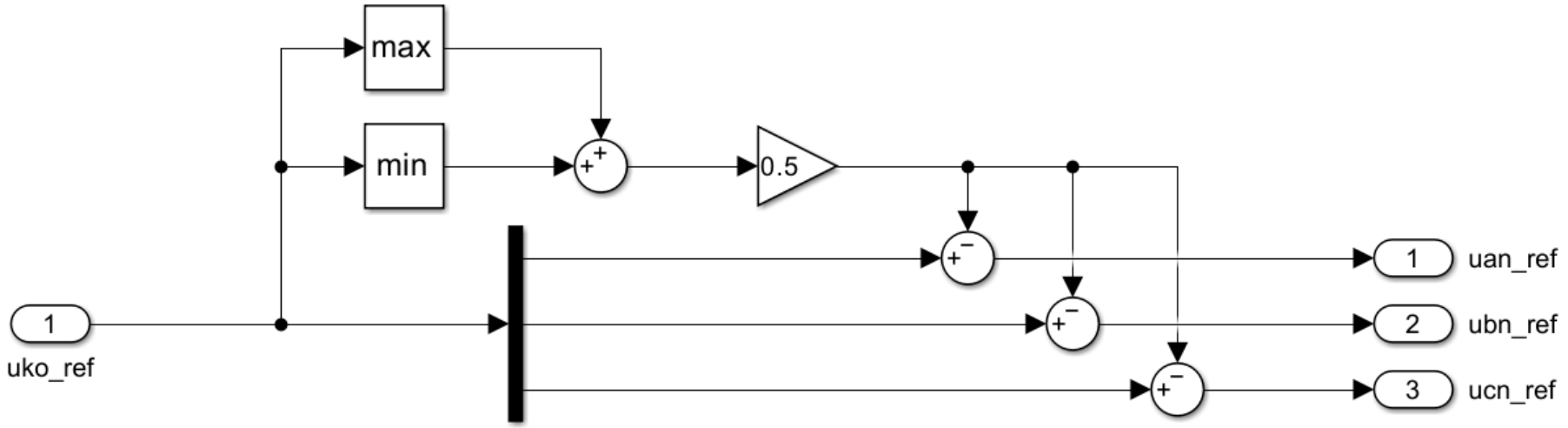
A3.2 Converting Submodule State into Gate Signals of IGBTs

```
function [out1,out2,out3,out4] = fcn(state)
global chaZeroStateA preZeroStateA;
if state==1
    out1=20;
    out3=20;
    out2=-20;
    out4=-20;
elseif state==-1
    out2=20;
    out4=20;
    out1=-20;
    out3=-20;
elseif state==0
    if preZeroStateA(1)~=0
        if chaZeroStateA(1)>0
            out1=-20;
            out2=-20;
            out3=20;
            out4=20;
            chaZeroStateA(1)=-1;
        else
            out1=20;
            out2=20;
            out3=-20;
            out4=-20;
            chaZeroStateA(1)=1;
        end
    else
        if chaZeroStateA(1)>0
            out1=20;
            out2=20;
            out3=-20;
            out4=-20;
        else
            out1=-20;
            out2=-20;
            out3=20;
            out4=20;
        end
    end
else
    out1=-20;
    out2=-20;
    out3=-20;
    out4=-20;
end
preZeroStateA(1)=state;
end
```

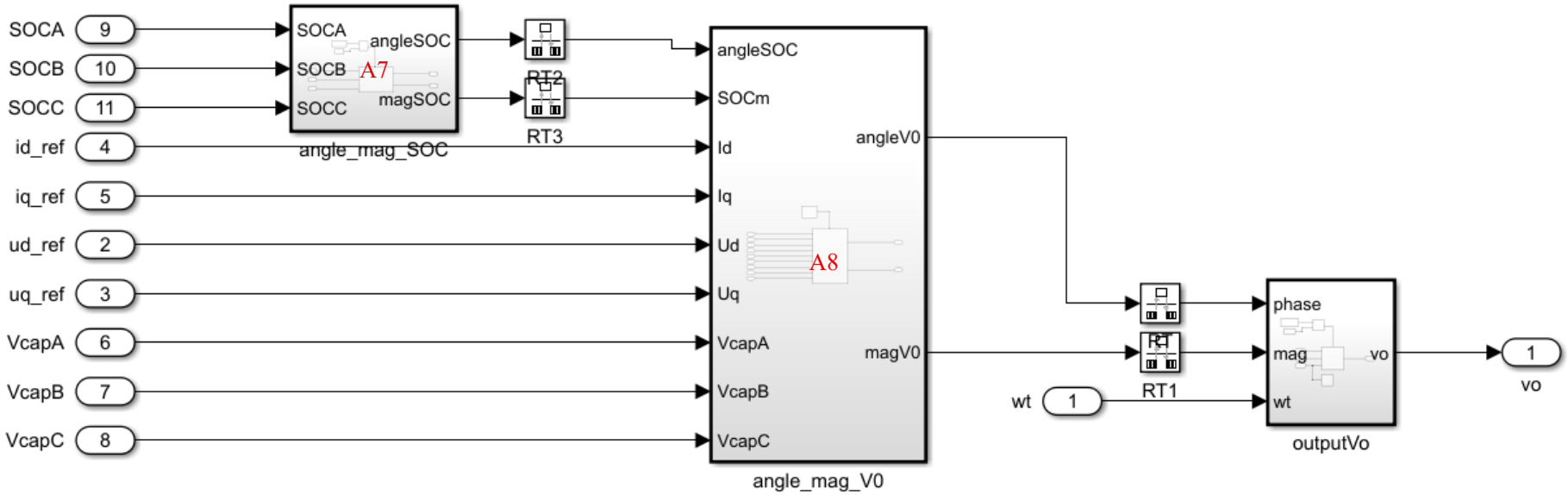
Appendix A4　PI Active and Reactive Decoupling Power Control Sub-model



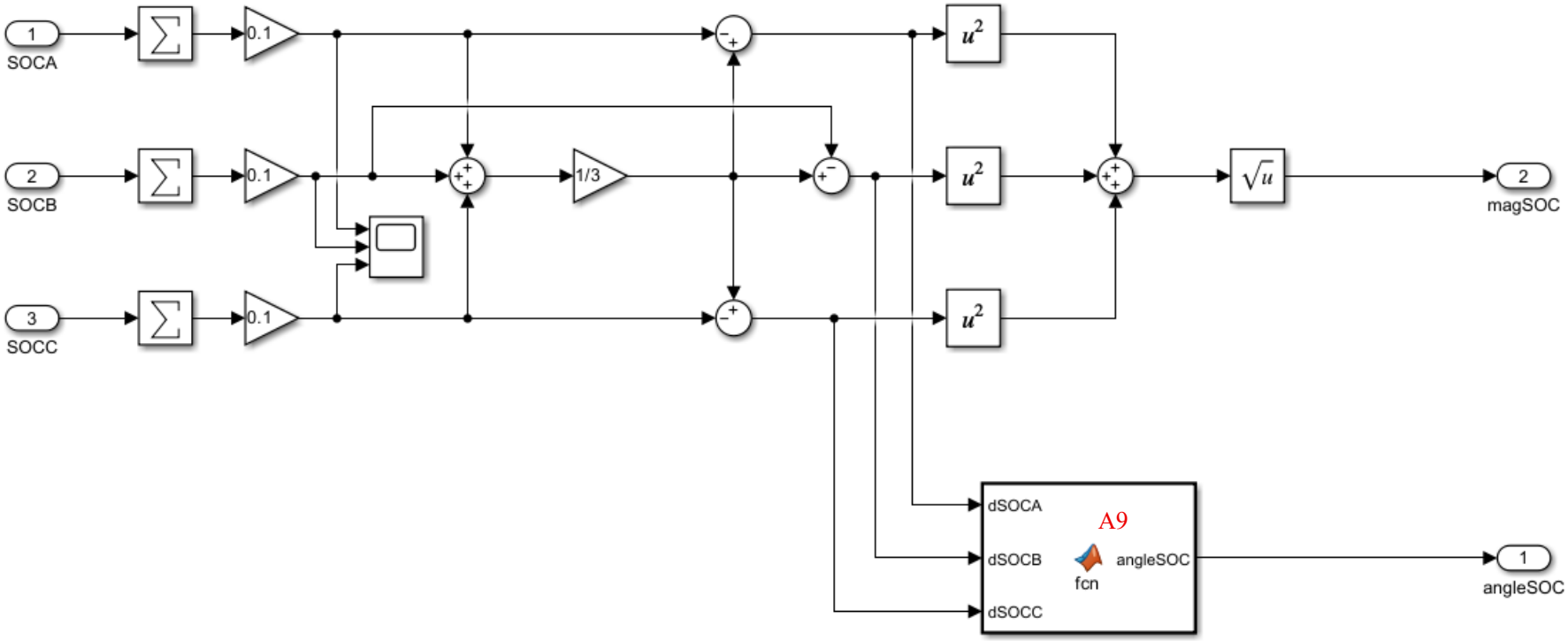
Appendix A5 Max-Min Common Voltage Generating Sub-model



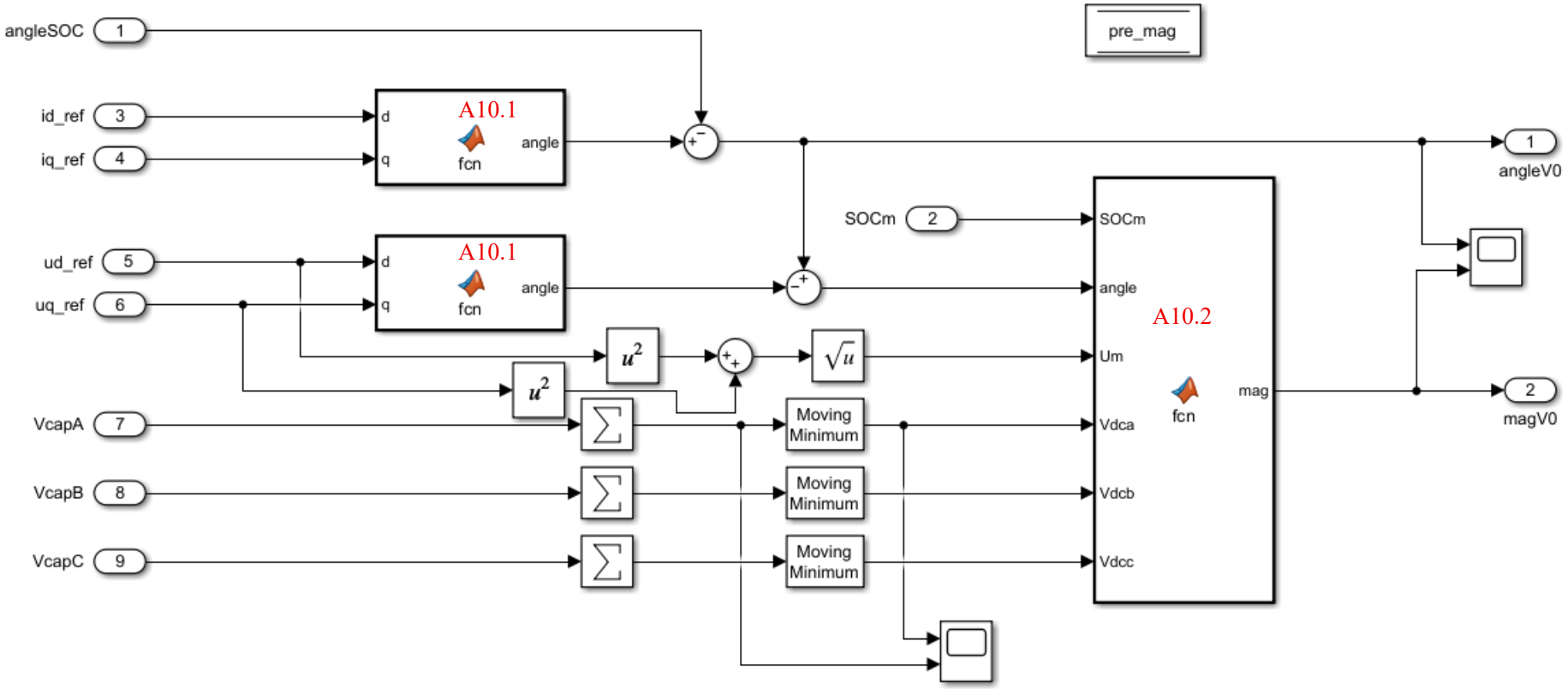
Appendix A6　Zero-sequence Voltage Generating Sub-model



Appendix A7　SOC Calculating Sub-model



Appendix A8　Zero-Sequence Voltage Calculating Sub-model



Appendix A9 Matlab Codes Involved in Appendix A7

```
function angleSOC = fcn(dSOCA,dSOCB,dSOCC)
if dSOCA==0
    if dSOCB>dSOCC
        angleSOC=pi/2;
    else
        angleSOC=-pi/2;
    end
else
    tanSOC=(dSOCB-dSOCC)/(sqrt(3)*dSOCA);
    if dSOCA>0
        angleSOC=atan(tanSOC);
    else
        angleSOC=atan(tanSOC)+pi;
    end
end
end
```

Appendix A10 Matlab Codes Involved in Appendix A8

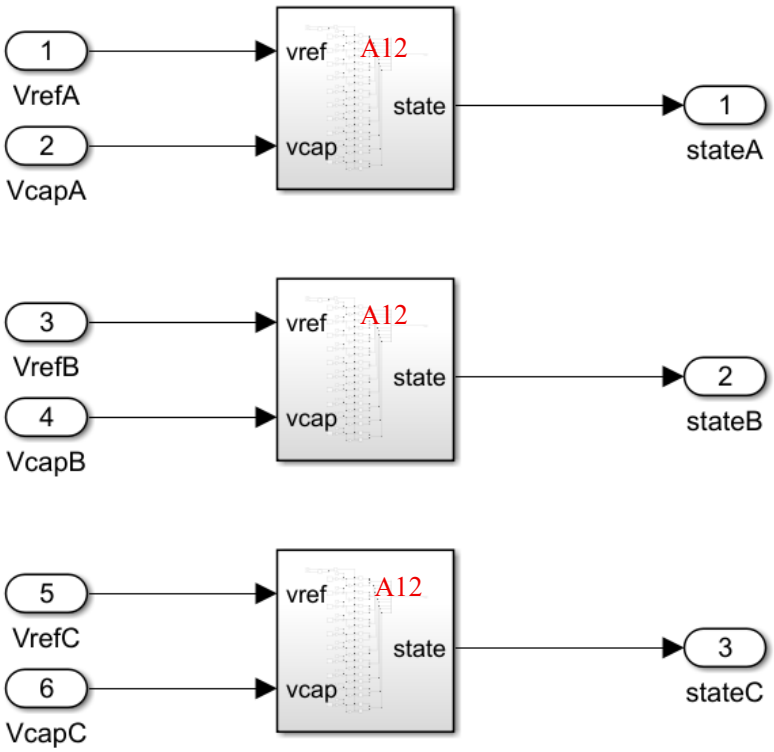
A10.1 Calculating the Angles of Voltages and Currents

```
function angle = fcn(d,q)
if d==0
    if q>0
        angle=pi/2;
    else
        angle=-pi/2;
    end
elseif d>0
    angle=atan(q/d);
else
    angle=atan(q/d)+pi;
end
end
```

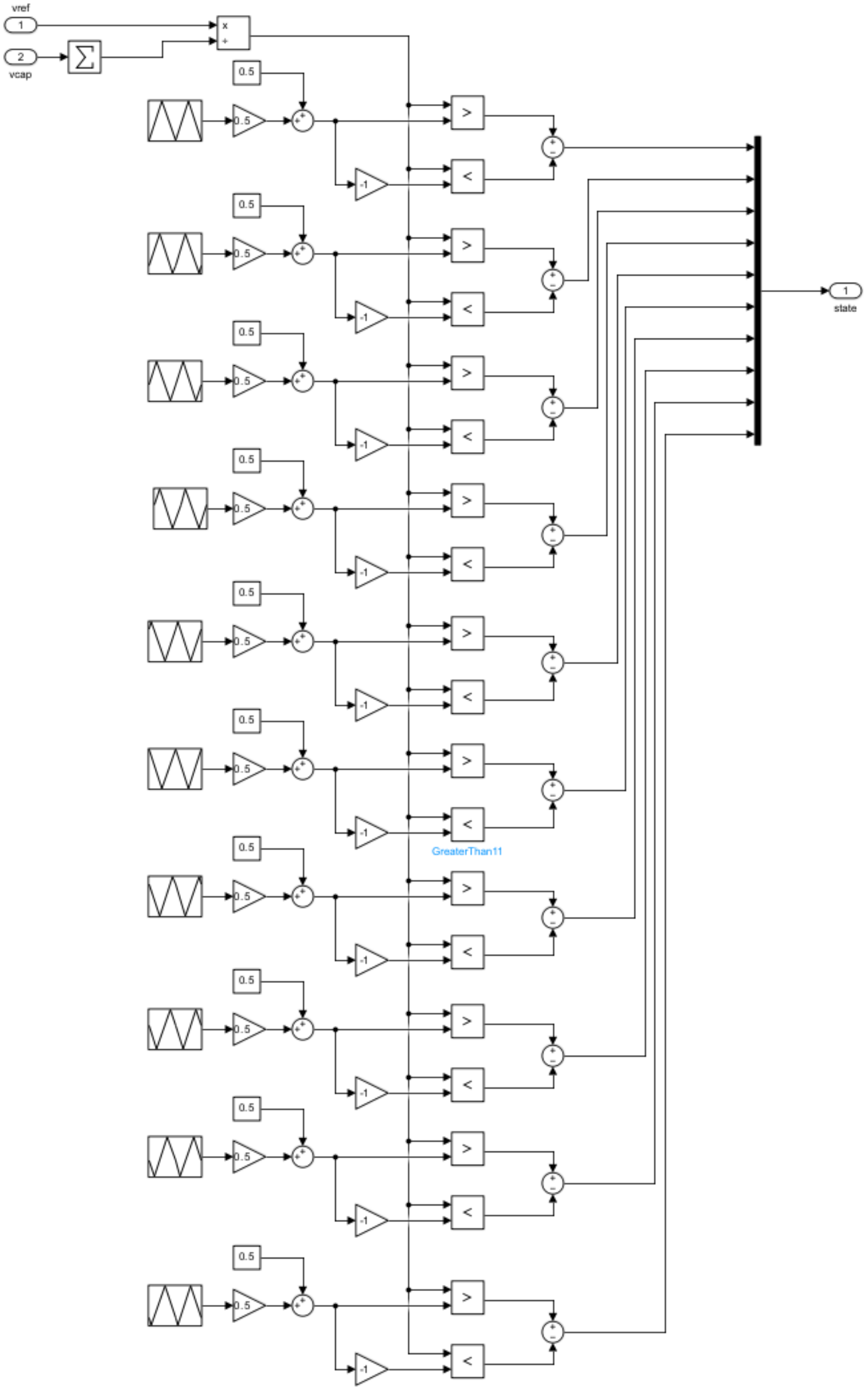
A10.2 Calculating the Magnitude of Zero-sequence Voltage

```
function mag = fcn(SOCm,angle,Um,Vdca,Vdcb,Vdcc)
global pre_mag;

if angle<=-pi
    angle=2*pi+angle;
elseif angle>pi
    angle=angle-2*pi;
end

if SOCm==0
    mag=0;
else
    if angle>0&&angle<=pi*2/3  % AC phase
        mag1=sqrt(0.95*Vdca^2-3/4*(Um*sin(angle-pi/6))^2)-sqrt(3)/2*Um*cos(angle-pi/6); % A1
        mag2=sqrt(0.95*Vdcc^2-3/4*(Um*sin(angle-pi/2))^2)-sqrt(3)/2*Um*cos(angle-pi/2); % B2
        mag=min(mag1,mag2);
    elseif angle>-pi*2/3&&angle<=0  % AB phase
        mag1=sqrt(0.95*Vdca^2-3/4*(Um*sin(angle+pi/6))^2)-sqrt(3)/2*Um*cos(angle+pi/6); % A2
        mag2=sqrt(0.95*Vdcb^2-3/4*(Um*sin(angle+pi/2))^2)-sqrt(3)/2*Um*cos(angle+pi/2); % C1
        mag=min(mag1,mag2);
    else                        % BC phase
        mag1=sqrt(0.95*Vdcc^2-3/4*(Um*sin(angle-pi*5/6))^2)-sqrt(3)/2*Um*cos(angle-pi*5/6); % B1
        mag2=sqrt(0.95*Vdcb^2-3/4*(Um*sin(angle+pi*5/6))^2)-sqrt(3)/2*Um*cos(angle+pi*5/6); % C2
        mag=min(mag1,mag2);
    end

    if mag<0
        mag=0;
    end
    if SOCm<=0.025
        mag=40*SOCm*mag;
    end
    mag=min(mag,pre_mag+1);
end
pre_mag=mag;
end

```

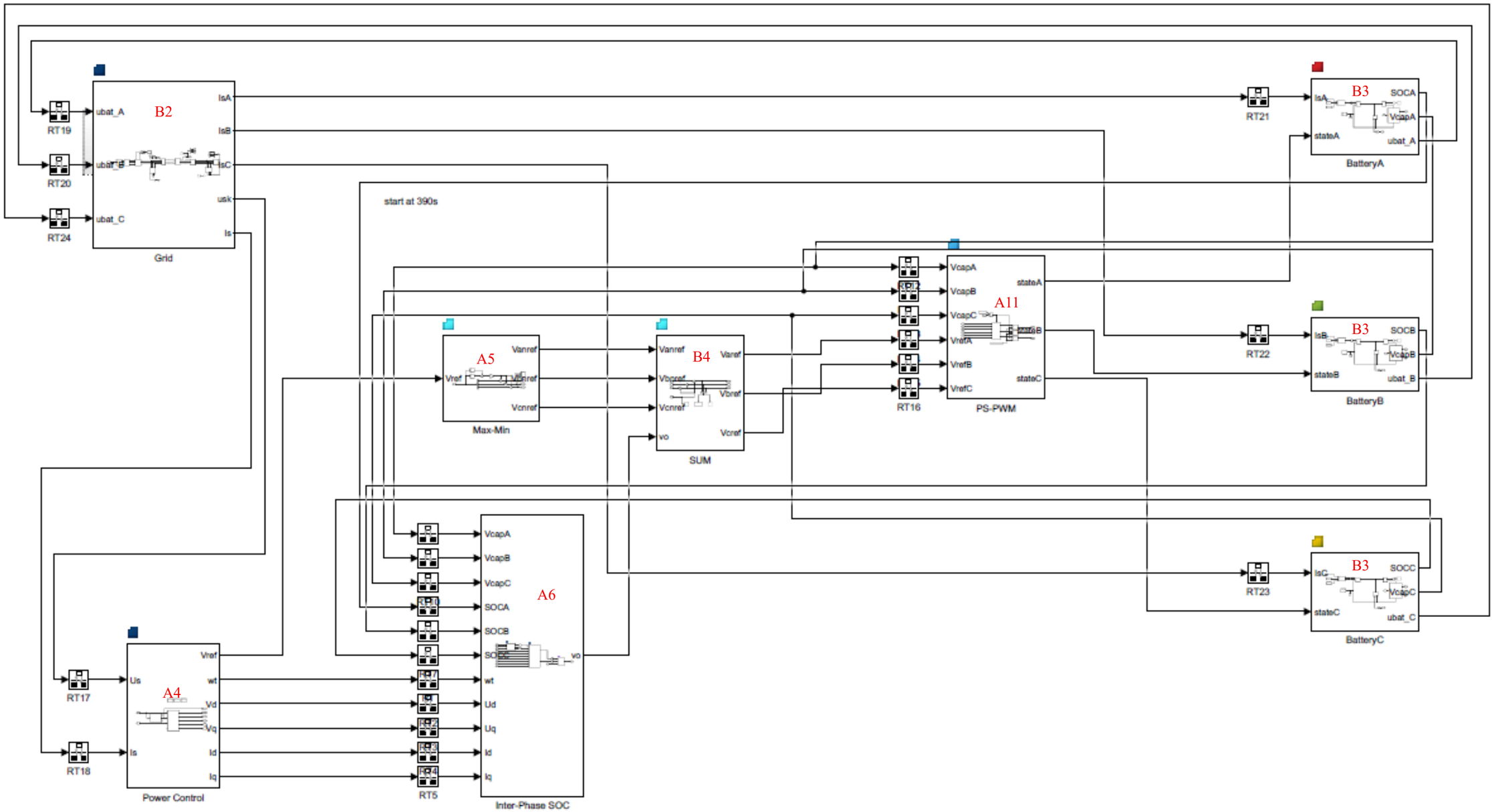
Appendix A11 PS-PWM Sub-model



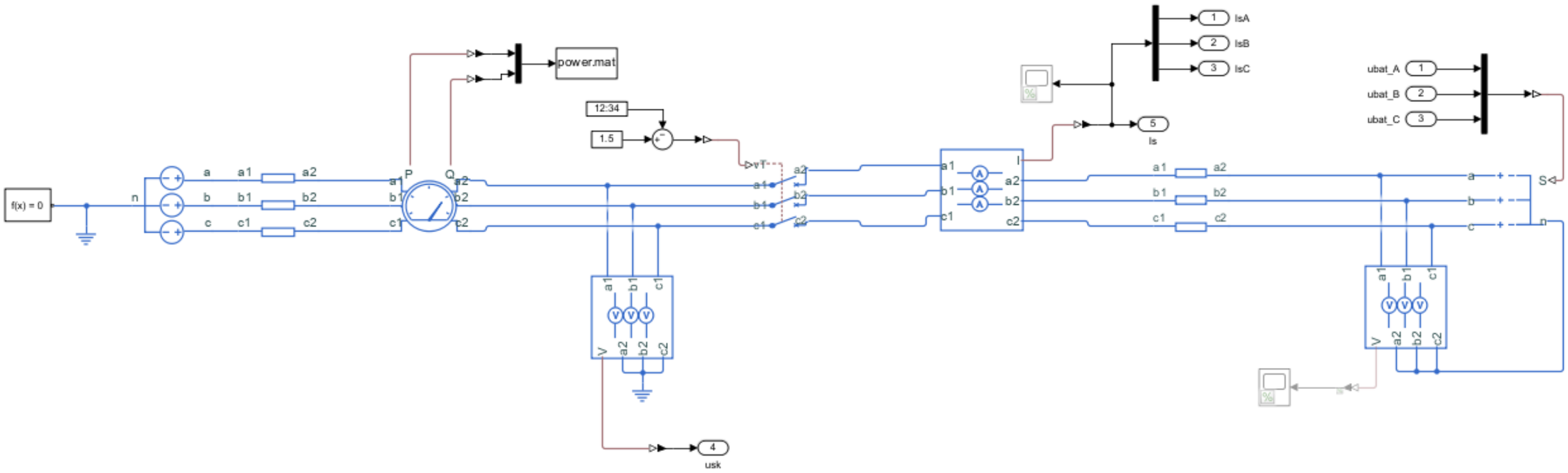
Appendix A12 PS-PWM



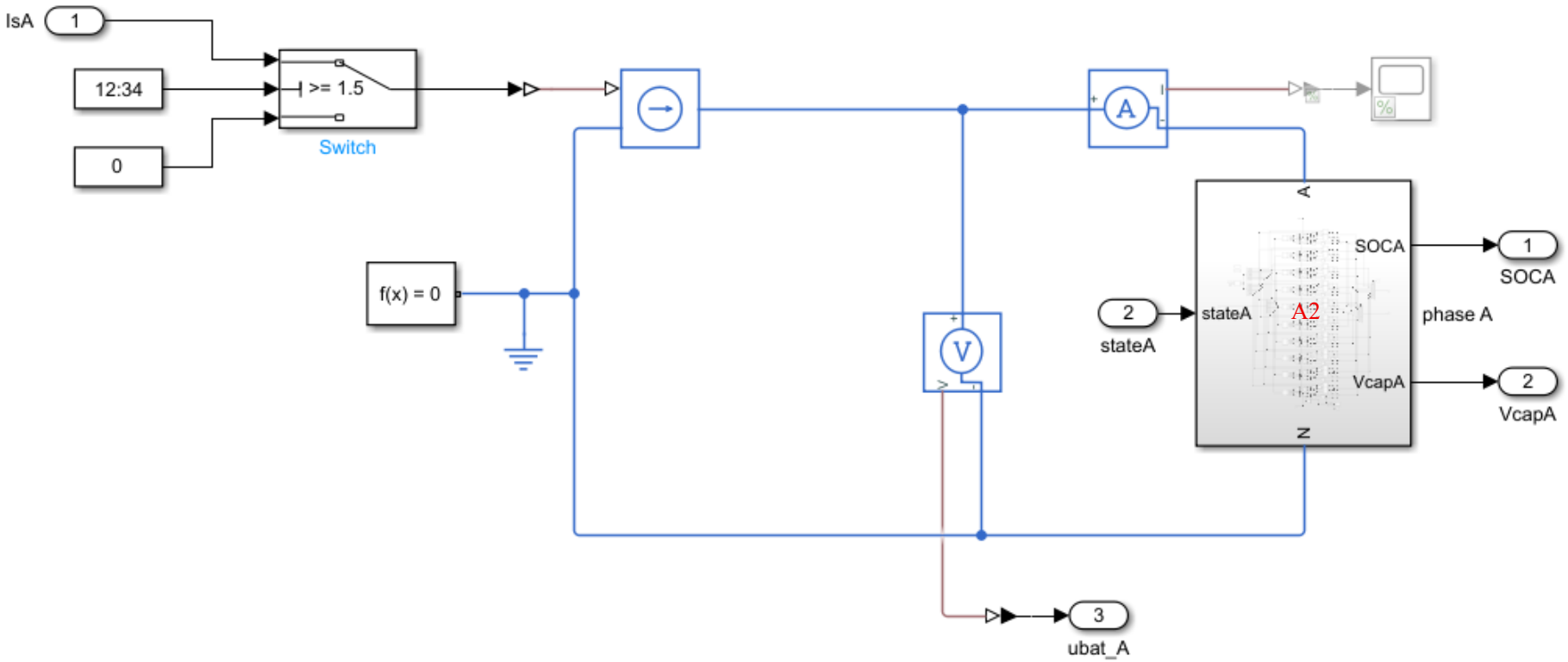
Appendix B1　Simulink Model of Inter-phase SOC balancing Control used for Parallel Calculation



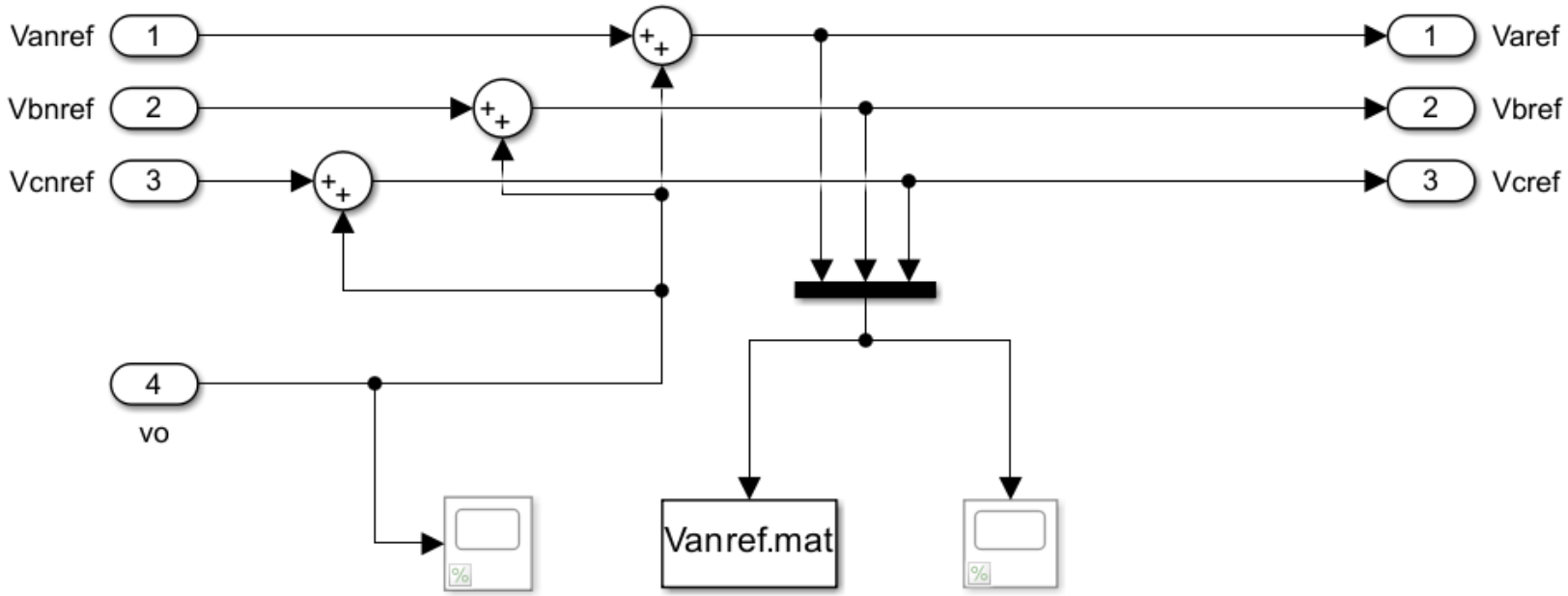
Appendix B2　Power Grid Part of Parallel Model



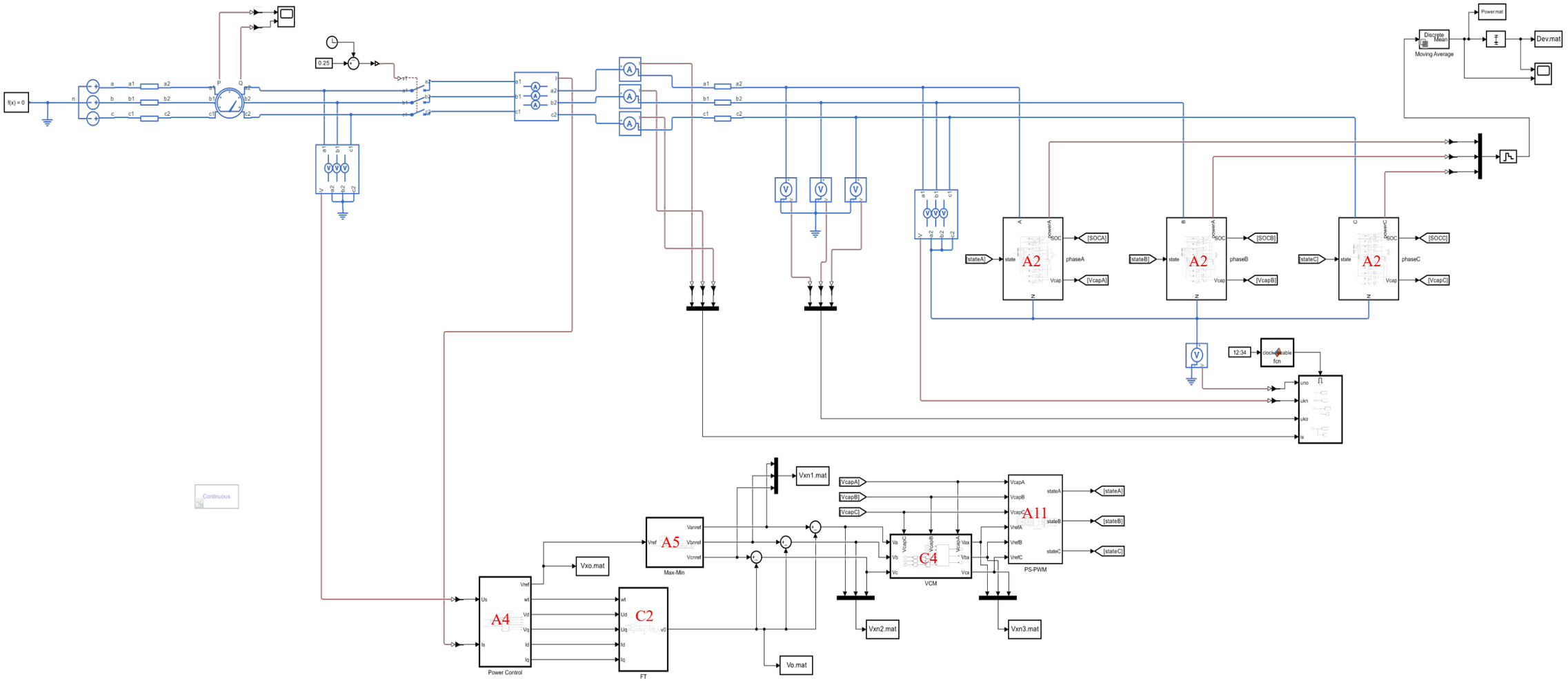
Appendix B3 BESS Part of Parallel Model (Phase A)



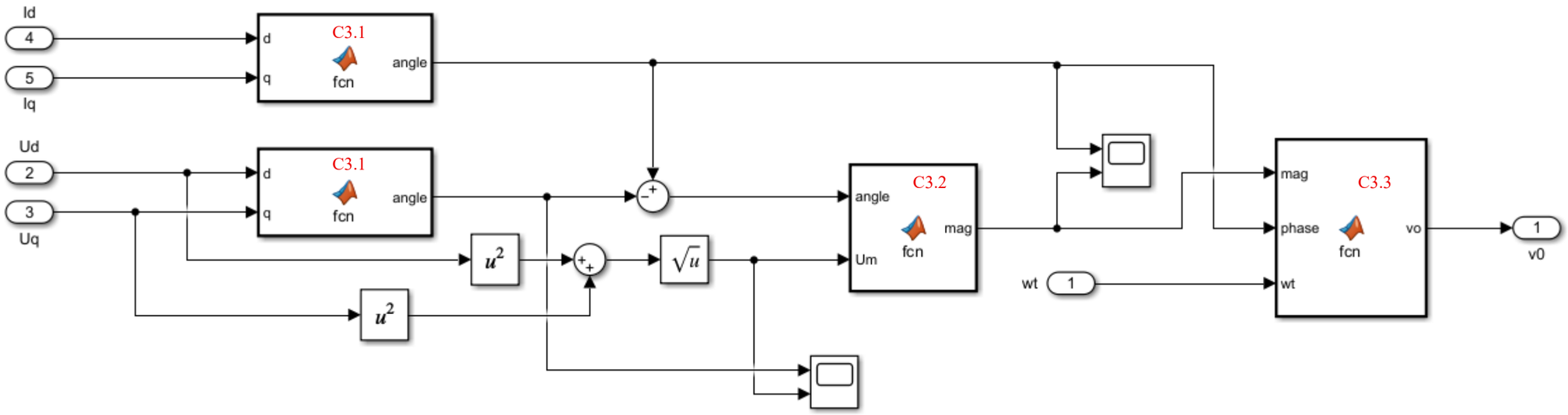
Appendix B4 SUM Module of Parallel Model



Appendix C1 Simulink Model of Fault-tolerance Control



Appendix C2　Fault-tolerance Voltage Calculating Sub-Model



Appendix C3 Matlab Codes Involved in Appendix C2

C3.1 Angle Calculating

```
function angle = fcn(d,q)
if d==0
    if q>0
        angle=pi/2;
    else
        angle=-pi/2;
    end
elseif d>0
    angle=atan(q/d);
else
    angle=atan(q/d)+pi;
end
end
```

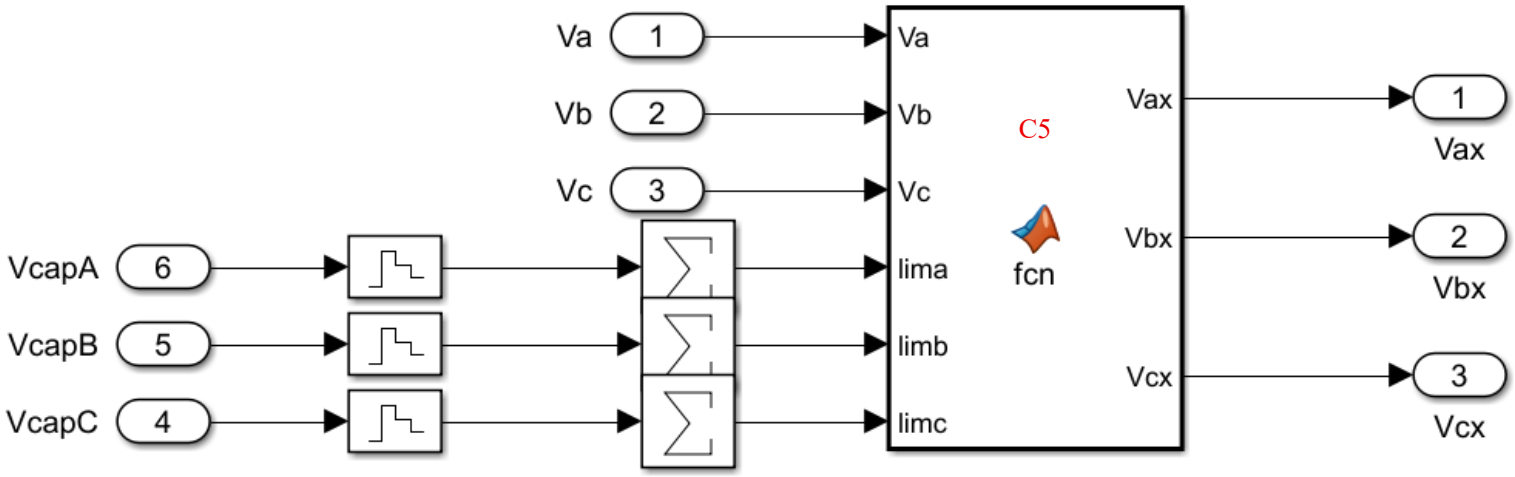
C3.2 Magnitude Calculating

```
function mag = fcn(angle,Um)
N=10;
if angle<=-pi
    angle=2*pi+angle;
elseif angle>pi
    angle=angle-2*pi;
end

mag=2/(3*N-2)*Um*cos(angle);

end
```

C3.3 Voltage Calculating

```
function vo = fcn(mag,phase,wt)
vo=mag*sin(wt+phase-pi/3);
end
```

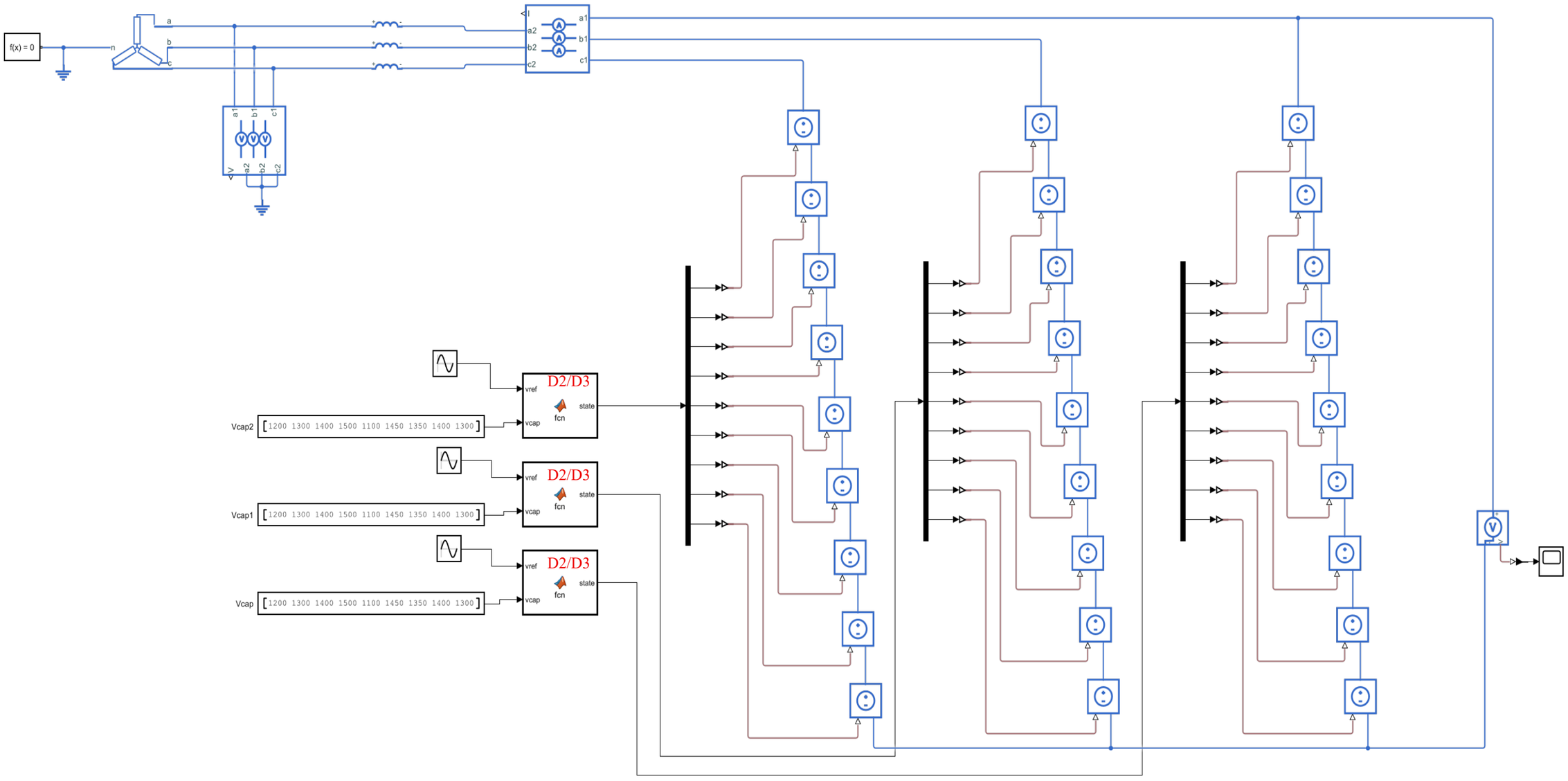
Appendix C4 Modulation Voltage Clapping Sub-model



Appendix C5 Matlab Codes Involved in Appendix C4

```
function [Vax,Vbx,Vcx] = fcn(Va,Vb,Vc,lima,limb,limc)
Vax=Va;
Vbx=Vb;
Vcx=Vc;

if Va>lima
    Vax=lima;
    Vbx=Vb+lima-Va;
    Vcx=Vc+lima-Va;
end
if Va<-lima
    Vax=-lima;
    Vbx=Vb-lima-Va;
    Vcx=Vc-lima-Va;
end

if Vbx>limb
    Vax=Vax+limb-Vbx;
    Vcx=Vcx+limb-Vbx;
    Vbx=limb;
end
if Vbx<-limb
    Vax=Vax-limb-Vbx;
    Vcx=Vcx-limb-Vbx;
    Vbx=-limb;
end

if Vcx>limc
    Vax=Vax+limc-Vcx;
    Vbx=Vbx+limc-Vcx;
    Vcx=limc;
end
if Vcx<-limc
    Vax=Vax-limc-Vcx;
    Vbx=Vbx-limc-Vcx;
    Vcx=-limc;
end
```

Appendix D1 Simulink Model for Modulation Strategies



Appendix D2 Matlab Codes for Nearest Level Modulation

```
function state=fcn(vref,vcap)
sum=0;
state=[0,0,0,0,0,0,0,0,0];

if vref>0
    for i=1:9
        sum=sum+vcap(i);
        if vref>=sum-0.5*vcap(i)
            state(i)=1;
        else
            break;
        end
    end
elseif vref<0
    for i=1:9
        sum=sum-vcap(i);
        if vref<=sum+0.5*vcap(i)
            state(i)=-1;
        else
            break;
        end
    end
end
for i=1:9
    state(i)=state(i)*vcap(i);
end
end
```

Appendix D3 Matlab Codes for Improved Nearest Level Modulation

```
function [state,err,out]=fcn(vref,vcap)
global error;
sum=0;
state=[0,0,0,0,0,0,0,0,0];
out=0;

if vref>0
    for i=1:9
        sum=sum+vcap(i);
        if vref>=sum
            state(i)=1;
        else
            break;
        end
    end
    if error(3)>=0
        state(i)=1;
    else
        sum=sum-vcap(3);
    end
    error(3)=error(3)+vref-sum;
elseif vref<0
    for i=1:9
        sum=sum-vcap(i);
        if vref<=sum
            state(i)=-1;
        else
            break;
        end
    end
    if error(3)<=0
        state(i)=-1;
    else
        sum=sum+vcap(i);
    end
    error(3)=error(3)+vref-sum;
end
for i=1:9
    state(i)=state(i)*vcap(i);
    out=state(i)+out;
end
err=error;
end
```

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