A Modular Multilevel Converter that Integrates Artificial Intelligence for Fault Locating and Protection

Jude Inwumoh

Thesis submitted to Auckland University of Technology in fulfilment of the requirements for the degree of Doctor of Philosophy (Ph.D.)

Supervisors:

Dr. Craig Baguley

Dr. Kosala Gunawardane

School of Engineering

June 2023

DECLARATION

I, at this moment, declare that this thesis has been composed solely by me. To the best of my knowledge, it does not contain materials, in part or whole, submitted or written by any individual for the application of a degree or professional qualification. Except where explicitly stated otherwise by reference or acknowledgement in the text, the submission presented is entirely my own.

Inwumoh Jude

30/10/2022

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincerest gratitude to Dr. Craig Baguley, my primary supervisor, for his advice and support throughout my studies. For me, his amazing intellect and human traits have served as an inspiration. He carefully addressed all my technical questions about the project, offering sound advice and showing me the right direction. This initiative would not have been feasible without him.

It is always a pleasure to extend my sincere gratitude to my co-supervisor, Dr. Kosala Gunawardane, for her support, helpful discussion, and suggestions. Dr. Kosala contributed immensely to the proof-reading of this thesis.

I also would like to thank Prof. Madawala Udaya for his unwavering support, guidance, and progressive meetings. In addition, for giving me access to join his PhD student group, where I received valuable advice that contributed to the success of this thesis. His mentoring has aided in the acceptance of one my journals.

I would also like to thank the Auckland University of Technology for the three years of financial assistance during my research study.

Lastly, I want to use this medium to appreciate the technical staff at AUT for their support.

LIST OF PUBLICATIONS

A.1 PUBLISHED/ACCEPTED PAPERS

- Jude Inwumoh, Craig Baguley, Kosala Gunawardane, “A Dynamic Control Methodology for DC Fault Ride Through of Modular Multilevel Converter based High Voltage Direct Current Systems,” Computers and Electrical Engineering Journal, Volume 100, 2022, 107940, ISSN 0045-7906, https://doi.org/10.1016/j.compeleceng.2022.107940.
- J. Inwumoh, C. Baguley, and K. Gunawardane, “A Fast and Accurate Fault Location Technique for High Voltage Direct Current (HVDC) Systems,” IEEE Canadian Journal of Electrical and Computer Engineering, 2022.
- J. Inwumoh, C. Baguley and K. Gunawardane, "Intelligent Fault Localization for Meshed HVDC Transmission Systems," 2020 Australasian Universities Power Engineering Conference (AUPEC), 2020, pp. 1-6.
- J. Inwumoh, C. Baguley, and K. Gunawardane, “A Novel Single-Clamped Hybrid-Arm MMC with DC-FRT and STATCOM Capability” SPEC 2022 Southern Power Electronic Conference.
- J. Inwumoh, K. Gunawardane and C. Baguley, "Impact of Superconducting Resistive-FCL on MMC-HVDC Fault," 2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia), 2021.

A.2 PAPERS UNDER REVIEW

- J. Inwumoh, C. Baguley, and K. Gunawardane, “A Novel Single-Clamped Hybrid-Arm MMC of HBSM and SCSM with DC Fault ride-through and STATCOM Capability”, Journal of Control, Automation and Electrical systems. (**Final Review Stage**).
- J. Inwumoh, Craig Baguley, Member, IEEE, Udaya Madawala, Fellow, IEEE, Kosala Gunawardane, Senior Member, IEEE, “A Novel Fault Location Strategy based on Bi-LSTM for MMC-HVDC Systems” IET Generation, Transmission & Distribution. (**Under Review**)

ABSTRACT

High Voltage Direct Current (HVDC) transmission has provided a variety of possibilities for renewable energy resources and regional substations to boost power supply reliability and operational flexibility. To accommodate this development and improve power system performance, the Modular Multilevel Converter (MMC) has been comprehensively adopted as a potential converter solution for HVDC applications due to its modularity and scalability. However, challenges such as cost, power losses, faults, regulating AC circulating current and energy balance can hamper their practical applications and deployment, especially in controlling and protecting the MMC-HVDC grid. Furthermore, the most crucial and challenging control issue lies in the inability of the converter to offer DC fault protection, since conventional control schemes always struggle to achieve converter energy balance and DC Fault Ride Through (DC-FRT) capability due to the unbalanced system parameters. Reviewing this research gap, a novel control structure has been proposed in this thesis ensuring a proper dynamic response, balancing the arm and leg internal energies, minimising the oscillations in DC current, offering DC-FRT capability and supporting Static Synchronous Compensator (STATCOM) of AC loads.

Moreover, the proposed control scheme is integrated in a novel MMC topology as a means of providing primary protection against fault. Since a DC fault can cause a severe and sudden rise in the converter's arm current, it will be more detrimental to the Half Bridge (HB) MMCs that lack DC Fault Ride-Through (DC-FRT) capability. Several fault-tolerant converters with DC-FRT capability are surveyed. However, the cost of implementation, power losses, complexity, and controllability of the converters limit their applications. To cut down on the cost and the number of electronic devices, a cascaded hybrid design and an Alternate Arm Converter (AAC) were suggested in literature. However, they require a large number of capacitors and inductors to filter the distortions created by the switching of the MMC's IGBTs. Furthermore, they cannot provide reactive power compensation in the event of a DC short circuit since all their MMC arms will stop conducting as they clear the fault. Therefore, this thesis proposes a novel single-clamped

hybrid-arm MMC topology with STATCOM and DC-FRT capability at reduced losses, cost, and number of electronic devices.

Implementing the proposed control system and the novel converter topology could be limited to non-permanent faults. For a DC overcurrent fault that lasts for an extended period (a permanent fault), the converter cannot sustain the grid with reactive power compensation for that long. Thus, the MMC-HVDC systems would struggle to ensure power supply reliability, thereby shutting down the entire HVDC network. As a result, a reliable backup fault location approach is paramount for grid protection and restoration during such a fault impact. The conventional fault location methods still struggle with setting manual protective thresholds and, they are vulnerable to fault resistance and noise. In most cases, they require a communication channel for the fault data which could potentially lead to signal delay and data loss. In Multi-Terminal (MT) HVDC network, locating a fault is challenging due to the poor selectivity and sensitivity of the traditional location schemes. Therefore, this thesis proposes a robust fault location approach based on Bidirectional Long-Short Term Memory (Bi-LSTM) using deep learning. The proposed method is a simplified decision-making model that uses fault features from only one end of the network to eliminates the need for a communication channel.

The proposed Bi-LSTM fault location scheme is accurate; however, it is critical to locate faults in a sufficiently fast and more accurate manner. This thesis also presented a faster and robust location scheme to minimize the outage time and costs associated with faults on HVDC transmission lines. Therefore, a novel fault location technique is proposed to integrate support vector machine (SVM) algorithms to reduce the time needed to locate faults through fault classification. After classification, Gaussian Process Regression (GPR) is used for location identification.

CONTENTS

List of Figures

LIST OF TABLES

ABBREVIATIONS

HVDC	high voltage direct current
IGBT	insulated gate bipolar transistor
LCC	line commutated converter
VSC	voltage source converter
PLL	phase lock loop
PI	proportional integral
AC	alternate current
DC	direct current
MMC	modular multilevel converter
MT	multi-terminal
HBSM	half bridge submodule
FBSM	full bridge submodule
AAC	alternate arm converter
SCSM	single clamped submodule
AAM	arm equivalent model
PWM	phase width modulation
DC-FRT	direct current fault-ride through
STATCOM	static synchronous compensation
TW	travelling wave
NTW	non-travelling wave

GPS	global positioning system
SSN	state space nodal
AI	artificial intelligence
ML	machine learning
SVM	support vector machine
GPR	gaussian process regression
DL	deep learning
RNN	recurrent neural network
Bi-LSTM	bidirectional long short-term memory
DPL	distributed parameter line
SNR	signal to noise ratio
MSE	mean square error
RMSE	root mean square error
DRTS	digital real-time simulator
GUI	graphical user interface

SYMBOLS

V_{dc}	DC link voltage
I_{dc}	DC current
k_p	proportional gain
k_i	integral gain
x_i	input fault dataset
ξ	coefficient of gaussian noise
v_s	phase voltage
ω	weight parameter
b	bias
L_a	arm inductance
P_{dc}	DC power
d_i	predicted fault distance
P_1	pole 1 to ground fault
P_2	pole 2 to ground fault
R_a	arm resistance
θ	phase angle
A_1	coupling matrix for arm energy balance
A_2	coupling matrix for leg energy balance
i_{cir}	circulating current
μ	location parameter

Chapter 1

1. INTRODUCTION

1.1 BACKGROUND

The reliance on fossil fuels as a major source of energy supply poses serious challenges to the earth's environment and is giving rise to significant climatic changes. The impacts of these changes have motivated initiatives to reduce fossil fuel consumption, and this has led to the renewable energy-based electricity, electrification of industrial heating processes and the transportation sector. To realise gains from these initiatives, green energy sources must be used to generate electricity that do not result in carbon emissions. Renewable energy sources meet this requirement and, accordingly, significant investigations and investment have occurred in the renewable energy power generation sector. However, the deployment of renewable based generation is hindered by a variety of technical factors, one of which is the need to maintain an instantaneous balance between electricity demand and supply. This problem is exacerbated by the inconsistency of renewable based generation on daily and seasonal bases. A potential solution is the use of energy storage to allow energy to be released as required to generate electricity and meet demands. However, this incurs significant expense. Another solution is through diversification and using multiple renewable energy source types with generation characteristics that are complementary in terms of realising a power supply that can meet instantaneous electricity demands. This approach has been adopted in Europe with the integration of southern Europe's solar energy, northern Europe's wind energy, and central Europe's hydroelectric generation facilities. To achieve an integrated electricity sector that is dependent on diverse renewable energy sources over distances as large as that of the European continent, interconnections are required to transport electricity.

High Voltage Direct Current (HVDC) transmission networks are one of the most effective ways of transporting electricity generated from renewable sources to distant locations [1]. HVDC transmission systems in a multi-terminal (MT) network configuration can connect multiple loads and generation sites and can be implemented using subsea cables or overhead transmission lines. Both forms of implementation are commercially viable, and the MT approach provides additional benefits, including power supply flexibility and a high level of reliability. HVDC transmission requires conversion between AC and DC forms of electricity, since most generation and distribution systems are AC. Although AC to DC conversion is achievable through a power converter [2], developments in converter topologies have struggled in terms of efficiency and cost effectiveness. Further, technical issues associated with the control and protection of complex converters and HVDC networks during DC faults pose serious drawbacks to implementation.

1.2 NATURE OF FAULTS ON HVDC SYSTEMS

A fault is a deviation from the normal state of operation. When a fault occurs in an HVDC system, it can cause severe damage to electrical components, leading to a power outage. This interruption in power supply can have serious societal and economic impacts, especially when the blackout lasts for an extended period. The power blackout depends on the extent of the fault impact on the HVDC network, the cost, and the time needed to restart and create an alternative path for power supply continuity.

The impact of DC faults can be so dangerous that they lead to the loss of lives and property. An HVDC fault can result from natural causes, human intervention, or equipment failure. Examples of natural causes are earthquakes, tsunamis, windstorms, wildfires, floods, lightning strikes, and tornados. Human intervention, such as cyber-attacks, war, and sabotage, are likely causes of fault. Equipment failures, such as ageing insulation, mechanical failure of insulators, and overvoltage of power devices, contribute to a higher percentage of incessant blackouts on HVDC networks [3].

The impact of a DC fault was recorded in 2021 when all the major cities in Southern Pakistan were plunged into a massive blackout that affected 210 million people. The cause of the outage

was technical, resulting in the shutting down of HVDC substations. This blackout was Pakistan's second-largest. The worst was in 2015, when rebel attacks on HVDC power lines plunged 80% of Pakistan into total darkness [4].

On the 28th of September 2003, the largest blackout in the continent of Europe was recorded when windstorms destroyed an HVDC transmission line linking Switzerland and Italy. The outage lasted for about 12 hours and affected millions of people in both countries. The damage left people trapped in elevators, and underground metro trains during a snowy night. The event recorded damage worth almost 130 million Euros. Other impacts of faults and their possible causes are shown on Table 1.1 [5].

Table 1. 1: Impact of fault and the causes of the blackout

References	Date	Affected People (millions)	Causes
[3]	30/07/12	620	Transmission line overload
[3]	1/11/14	150	HVDC station outage
[3]	26/01/15	140	Plant technical fault
[6]	23/12/15	230	Cyber-attack
[7]	3/03/16	10	A severe thunderstorm
[3]	28/09/16	1.7	Storm damage to transmission infrastructure
[3]	1/03/17	21	Cascading failure in transmission system
[3]	21/03/18	10	Transmission line failure
[3]	20/12/18	0.6	Winds reached speeds of 100 km/h
[8]	7/03/19	30	Lack of Technical Expertise/Maintenance
[9]	16/06/19	48	500-kilovolt transmission lines disruption
[10]	4/08/19	120	Transmission line failure

From Table 1.1, some of the DC faults are caused by equipment failure. Thus, the maintenance and protection of the switching devices forming converters is of utmost importance and, specifically, the protection against DC faults is one of the most critical challenges. A typical DC

fault affects the normal operation of the HVDC grid leading to the generation of high voltage transients. As such, the converter experiences distortion when balancing the active power from the AC side with the DC network, potentially leading to grid collapse [11].

1.3 MODULAR MULTILEVEL CONVERTER (MMC)

In the 1990s, ABB and Siemens commenced research into VSC-HVDC converters, proposing the use of IGBTs to regulate for sinusoidal voltage and current waveforms on the AC side of a converter [29]. Two-level converters were initially introduced, with filters used to eliminate high frequency harmonics generated through switching [30]. To reduce filter requirements, three-level converters were introduced [31] and [32], which make a connection to a converter neutral point. The advantages of this approach include a reduction in harmonic content and a reduction in voltage stresses on switching elements, which suits high-voltage applications. To further reduce the harmonic content in HVDC applications, Siemens integrated many small cells together as Submodules (SMs), switching particular SMs at a time to produce a staircase waveform. This is the basis of the MMC.

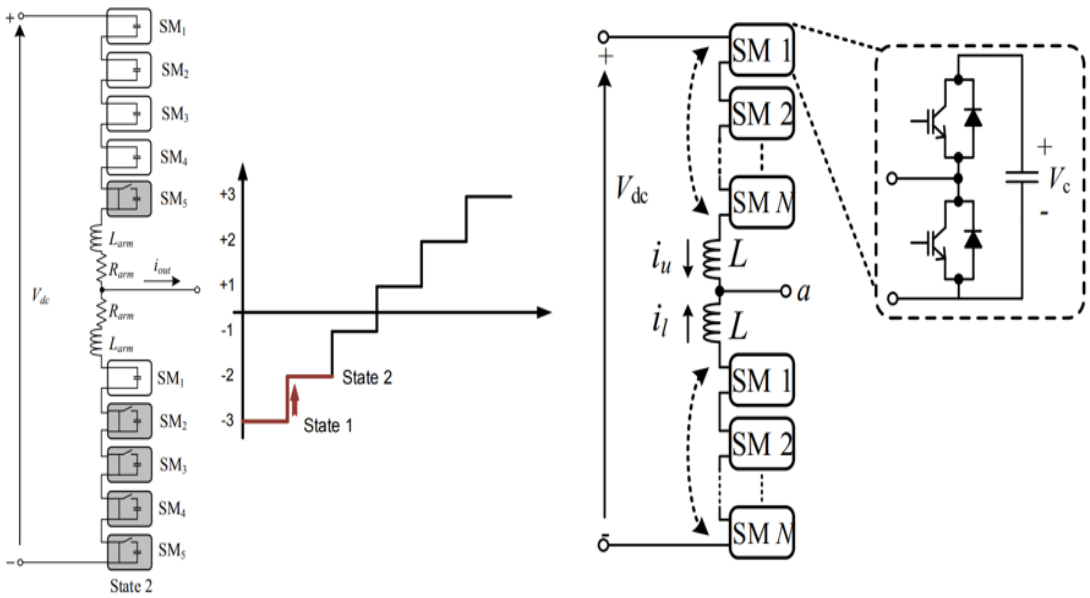


Fig.1. 1: Modular Multilevel Converter (MMC)

Since the inception of the MMC and because of its advantages, it has replaced VSC-HVDC systems that were implemented using two or three-level VSCs. In 2010, the Trans Bay Cable project became the first to make use of MMC-based HVDC technology [33] without using

harmonic filters. [34] performed MMC harmonic studies to verify robustness against harmonic distortion. MMC modules make system capacity upgrade easier and scalable, as well as offering reduced converter losses and excellent steady-state operations [35], [36], [37]. The ease of operating and the low cost of maintenance of an MMC-based HVDC converter are the reasons for its commercial acceptance over other VSC topologies [38].

In summary, MMCs do not require the use of AC side filters and bulky transformers, which are expensive and lossy [39] - [40]. Also, because of its redundant SMs, the MMC converter can continue to operate even if one of the modules fails. This feature makes maintenance feasible and provides enough leeway to isolate the cause of the failure. The modular structure of the MMC can allocate the total power in each module equally, allowing for the use of cheaper components without stress on the grid [41]. Therefore, an HVDC network implemented using an MMC is capable of fast power controllability and capacity upgrade [42]. However, one MMC characteristic that has shortcomings is DC Fault Ride-Through (FRT), which is the ability of an MMC converter to ride through HVDC transmission system faults and disturbances whilst connected to a healthy system circuit [12]. The protection schemes of the MT-HVDC network have encountered numerous challenges regarding the converter topologies used. Some MMC topologies are less robust under DC fault condition and cannot provide HVDC network protection. A typical example is the half-bridge (HB) [13]. This is because HBs cannot generate reverse voltage since they lack a zero-crossing path. On the other hand, some converters can generate reverse voltage to ride through the fault or, in the worst case, reduce the damage caused by the fault. These converters that can offer protection to the network are known as "fault blocking converters", and the protection they offer is known as primary protection [14]. MMC converter topologies are further discussed in Chapter 2.

1.4 PRIMARY PROTECTION

Primary protection is the process of eliminating the DC fault current by the MMC converters. During the occurrence of DC faults, as shown in Fig. 1.2, the HVDC link voltage may collapse as the MMC switches to fault blocking mode. In this scenario, the MMC plays a dual role. The

MMC uses the stored energy in capacitors to temporarily supply energy to loads to ensure a continuous supply of power to the consumers. While that is done, the MMC works to eliminate the fault current by generating fault-blocking voltages. The fault current will start to decay when the total capacitor voltage reaches a sufficient level to stop the conduction by the free-wheeling diodes.

The time required for MMC SMs to clear faults within the fault-tolerant stage and achieve FRT is called the fault clearance time. Some SMs possess fault capability, but it can be time-consuming to resolve a fault due to the magnitude of the fault blocking voltage. If the SMs are unable to clear the fault within a specific time frame, their switching elements will be blocked, and the diodes will become uncontrollable.

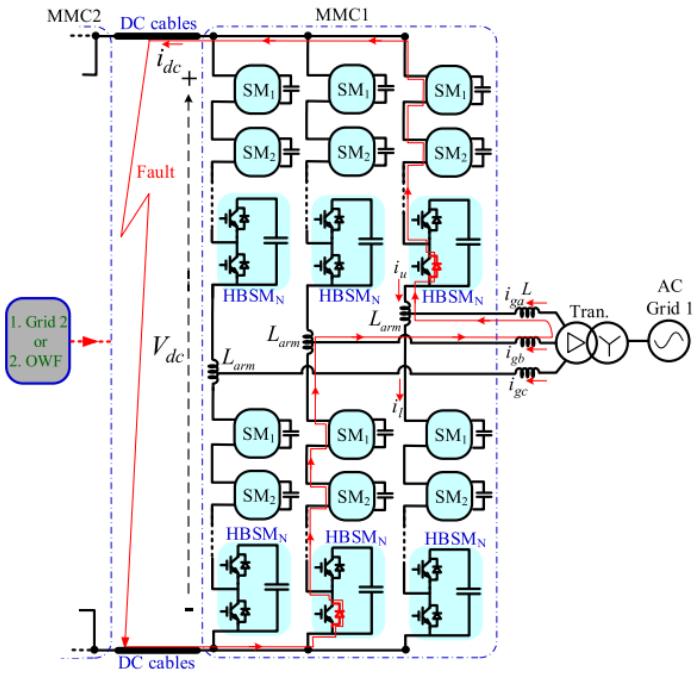


Fig.1. 2: Typical MMC based HVDC system under DC fault

Furthermore, if the severity of the fault persists, sustaining FRT by primary protection will become more challenging [15] - [16]. This drawback is made manifest through increased current stress on the MMC switching elements, which may be short-circuited to protect the MMC. Also, if the faulty circuits are not isolated quickly, the current from the AC source will continue to feed the DC fault through the uncontrollable diodes of the Insulated Gate Bipolar Transistors

(IGBTs). This effect would lead to an increased magnitude of the DC fault current, multiple failures of the MMC modules and the collapse of the entire grid system [11].

Before the collapse of the entire grid, the DC fault extends to the HVDC transmission line. During which, fault location techniques can be employed to protect the system components, as transmission line faults can be detected and located in a timely manner. Further, and in the case of multi-terminal HVDC systems, knowledge of fault locations can allow for power flow to be re-routed through an alternative path to ensure continuity of supply. Therefore, integrating a fast and accurate backup protection strategy with MMC to detect, locate, and isolate DC faults on transmission lines, while realising the continuous operation of a healthy system is a current research issue.

1.5 BACKUP PROTECTION

DC fault protection is a significant issue for MT HVDC transmission systems. The majority of protection studies are focused on primary protection, which involves the use of modified MMC SMs. However, the maloperation and poor sensitivity of primary protection under severe faults affects the reliability of the grid. Thus, backup protection is essential to improve grid stability [17].

Moreover, due to the integration of fast-acting DC systems located within AC power systems, it is essential to detect, classify, and isolate faults as quickly as possible. For the stable operation of a system, a feasible strategy is to monitor the fault signals so that an accurate and fast classification of the fault can be achieved to enable correct protective control decisions. When fault samples are correctly classified, they represent certain regions in the HVDC transmission lines. After classification, obtaining the exact location of a fault can be done quickly.

Research focus has been placed on converter types with fault blocking capability. Thus, an MMC topology and control methodology to offer DC fault ride-through and also support the HVDC network with reactive power compensation during the occurrence of a fault is required. Further to the above protection plan using the converter modules, when the fault severity increases, the primary protection scheme for the HVDC grid tends to fail. As a result, all the MMC SMs would

require a backup protection scheme, especially for faults that last beyond their limit. Thus, protecting the converter devices is an essential requirement for converter stations and to maintain continuous operation of the HVDC grid. Such a protection system must be quick to locate and isolate the DC fault current. Furthermore, the protection system must be sensitive and selective to avoid unnecessary detection and isolation. The primary and backup protection zones in an HVDC network are illustrated in the conceptual diagram in Fig. 1.3.

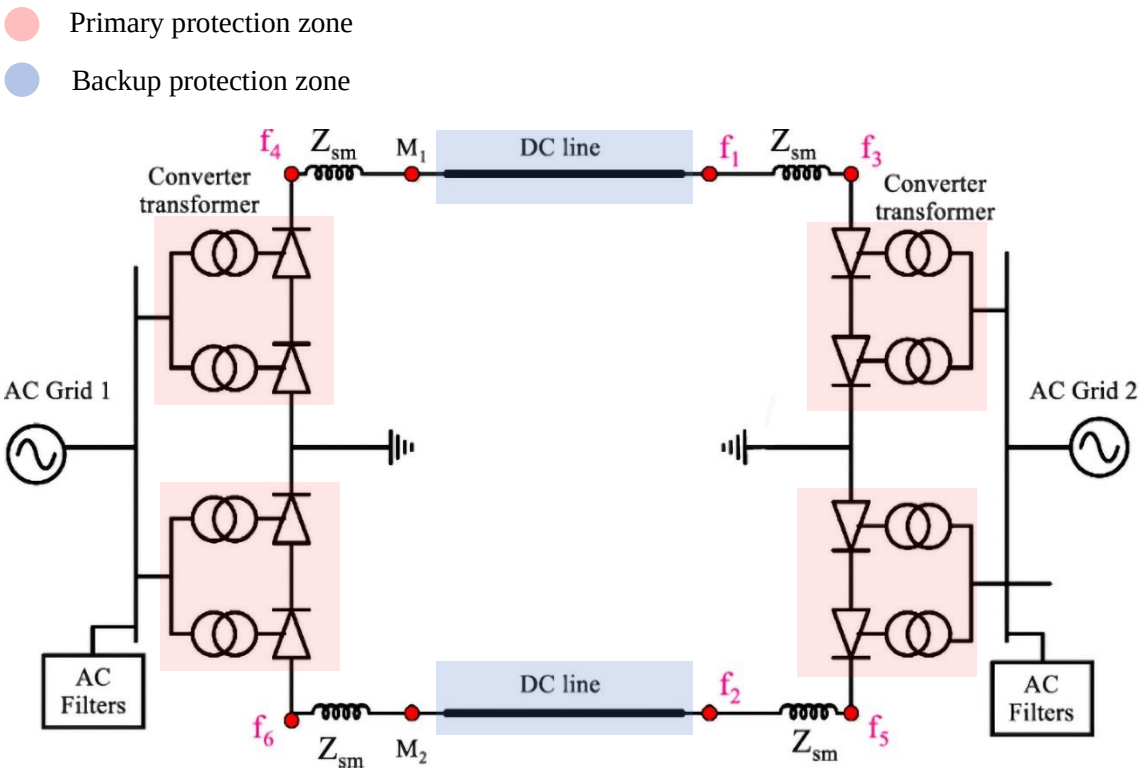


Fig.1. 3: Primary and backup protection zones of an HVDC network

DC faults plague the proper functioning of HVDC networks and can arise from multiple causes for both overhead transmission lines and underground subsea cables. In some cases, DC faults could last for an extended period. These are permanent DC faults, which a converter cannot ride through. Hence, to protect the entire network, a fast and accurate backup protection scheme should be incorporated into a converter to quickly locate the fault and allow it to be isolated. If the fault is isolated rapidly, other power electronic devices forming the MMC experiencing a fault can be protected from the harmful effects. In addition, if the exact fault location is known on a MT network, an alternative route can be used to allow for power supply continuity. At the same time, the affected path can be isolated for quick repairs. In literature, several fault locating techniques

have been proposed. However, these conventional methods are expensive and time-consuming to implement. For example, a fault in the Basslink submarine cable interconnector between Tasmania and mainland Australia took approximately 500 hours to locate and repair [18]. Such lengthy disruptions to power supply are usually unacceptable. Therefore, it is essential to locate the precise position of the fault as soon as possible. Accordingly, a new, rapid, and precise fault location technique is required, suited to locating faults in offshore HVDC lines and cables.

1.6 RESEARCH OBJECTIVES

The purpose of this study is to propose a novel MMC converter topology and control methodology that have a major impact on circuit breaker requirements, protection strategies, and supporting FRT during faults occurring on either the AC or the DC sides. In addition, the control methodology should be able to switch the converter operation between fault mode using a fault blocking converter and normal mode using an HB converter. The effects of this control scheme on MT-HVDC protection systems are thoroughly investigated as a primary protection mechanism.

However, during primary protection when the fault current exceeds the time constraints allowed for MMC switching elements, the converter will not be able to achieve FRT. In this case the fault must be isolated, and an alternative path is determined for power supply reliability. This is feasible with a fault locating backup protection scheme equipped with the following features: accurate fault detection, classification, robustness against varying MMC parameters and transmission line parameters, and sufficiently low computational complexity to enable real-time monitoring and the rapid locating of faults. A desirable feature of the scheme is the elimination of any reliance on a communication channel. Thus, a well-designed backup protection mechanism is investigated via the use of artificial intelligence approaches.

1.7 CONTRIBUTIONS TO KNOWLEDGE

The significant contributions to knowledge outlined in this thesis can be summarized as follows:

- The development of a novel MMC topology and control strategy for switching from normal to fault operation mode for strengthening the FRT capability, reactive power

compensation, and leg/arm energy balance. Moreover, the proposed topology is able to change the switching status of the MMC control's cells from fault tolerant mode back to normal operating mode because of its flexibility. As a result, the MMC blocks the DC fault current and returns to steady state after FRT.

- The development of a novel fault locating strategy implemented on a multi-terminal HVDC system experiencing a permanent DC fault, when the MMC switching elements fail to protect the grid during primary protection. The scheme is developed based on Artificial Intelligence (AI), and can rapidly and accurately predict fault locations, allowing for isolation and the determination of alternative power flow paths for the continuity of power supply.

1.8 THESIS OUTLINE

The remaining chapters of thesis are structured as follows:

Chapter 2 presents a comprehensive literature review on HVDC network converters. The review incorporates the nature of faults on HVDC networks and converter topologies with fault blocking capability. A second review is presented to investigate protection strategies to support the fault blocking converter. This results in an extensive investigation of backup protection schemes to identify the gaps in existing knowledge, from which research questions are developed.

Chapter 3 presents a dynamic control methodology for the DC-FRT capability of MMC-HVDC systems. As a result, the control system for the proposed fault blocking converter is designed to ensure arm and leg energy balance is achieved and static synchronous compensation is done to support AC loads during DC faults. This is the basis for designing a novel single-clamped hybrid-arm MMC topology. This topology is cost-effective and has FRT capability with the capacity to maintain the voltage levels during a DC fault by supplying energy compensation to the transmission line.

Chapter 4 presents a novel backup protection strategy based on bidirectional long-short term memory (Bi-LSTM) to support the converter proposed in Chapter 4. The scheme is powered by

artificial intelligence, and it is used to locate faults on the HVDC transmission lines in cases where the fault blocking converter fails to isolate the fault.

Chapter 5 presents a novel fault locating strategy based on SVM and GPR for bipolar HVDC networks. This scheme improves on the fault location time and accuracy.

Chapter 6 concludes the work done and makes recommendations for future work.

Chapter 2

2. LITERATURE REVIEW

This chapter reviews the operation of HVDC systems, the converters used for these systems, faults on MMC-HVDC systems, and the protection methods related to faults. The chapter is divided into six sections. Section 2.1 presents the concept of HVDC transmission, and the history of voltage source converters used for HVDC networks. Section 2.2 reviews different MMCs and their suitability for primary protection. Section 2.3 reviews different backup protection strategies for locating faults on MMC-HVDC networks. The research questions relating to the gaps in current knowledge on MMC-HVDC systems, converter protection, and fault location are presented in Section 2.4. Section 2.5 states the conclusion.

2.1 CONCEPT OF HVDC TRANSMISSION

Currently, there is a global drive to increase reliance on renewable energy sources. Such energy sources are often located distantly from loads, which gives rise to a need for long distance transmission line systems. HVDC transmission is preferred to its AC transmission alternative, due to key advantages particularly its reliability through redundancy, flexibility of power flow and maximizing the performance of installed assets [19]. Furthermore, it offers the most economically attractive means for long distance transmission through overhead and subsea cables [20]. Fig. 2.1 shows a conceptual comparison of DC and AC transmission in relation to cost and power loss. The cost of installing DC transmission is higher than AC transmission. However, as the transmission distance increases, AC transmission acquires more losses.

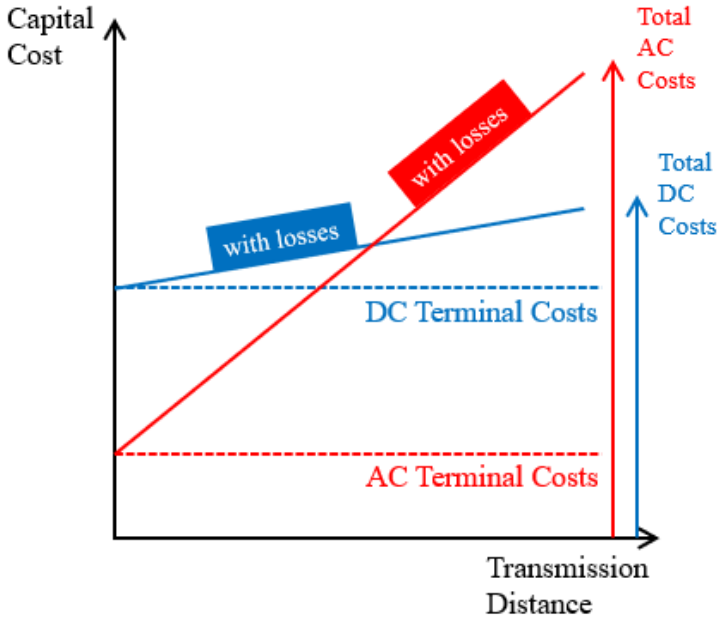


Fig.2. 1: Comparison of HVDC and HVAC capital cost with transmission distance [21]

The average loss in the distribution and transmission of 2.2 GW of electricity via HVAC links in OECD countries was estimated to be 6.6% in 2014 [22]. According to the energy cost analysis, a 1% loss is equivalent to £774.41 M over an expected HVAC link lifetime. This amount is approximately equal to the estimated cost of installing a point-to-point HVDC link of £1.88 Bn [23].

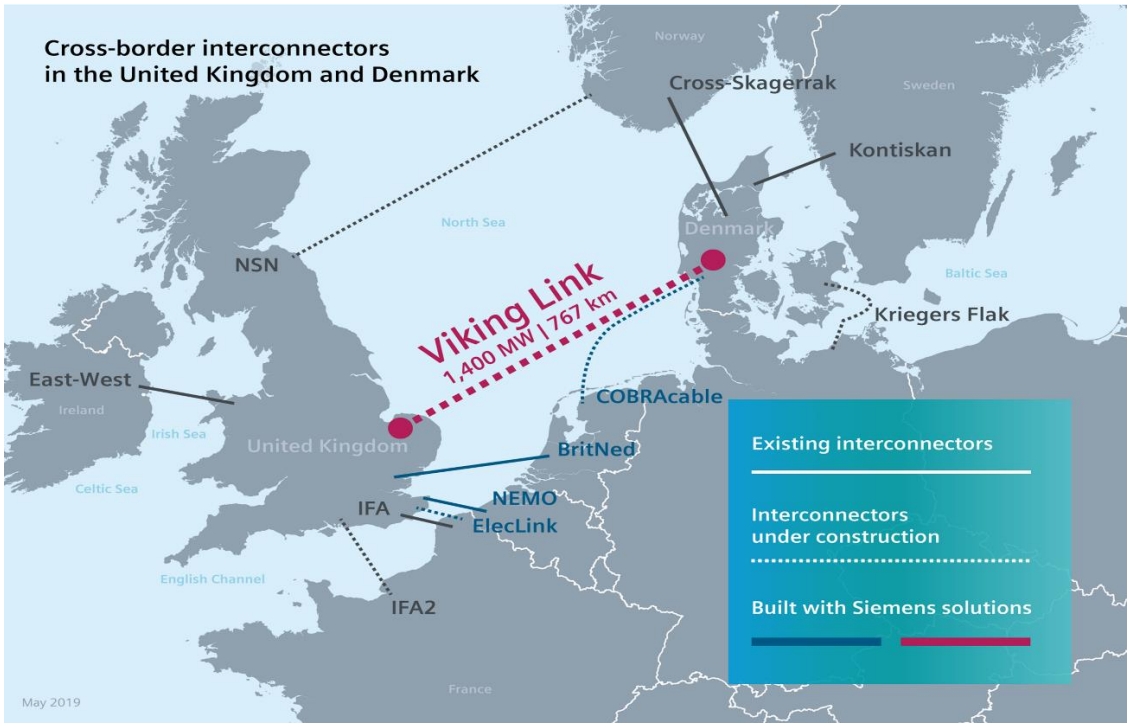


Fig.2. 2: Viking link between Great Britain and Denmark

Countries can be linked via HVDC grids to ensure power supply security and reliability. For example, Siemens was responsible for the supply, design, and installation of a 1400 MW converter system (Viking link), shown in Fig. 2.2. This HVDC technology can transmit at a DC voltage of 500 kV using a 767 km long power cable between Southern Jutland in Denmark and Lincolnshire in Great Britain [21]. HVDC links can also connect the southern and northern parts of a country. For example, in New Zealand, a 610 km HVDC powerline transmits 220 kV DC voltage from Benmore hydroelectric power station in South Island to the Haywards transmission station in North Island.

Considering that the majority of generation and distribution systems are AC, a converter station to interface with HVDC transmission networks is required to facilitate conversion between DC and AC. Currently, there are two types of converters integrated with HVDC transmission: The Line Commutated Converter (LCC) and the VSC [24]. For the VSCs, IGBTs are the most often utilized switching elements, and they are self-commutating. Unlike the VSC, the switching devices in the LCC are thyristors. Thyristors can reach a conducting state when triggered by a gate current. They can be turned off when a reverse voltage is applied to the gate [25]. The difficulty of controlling an LCC is one of two reasons it is less preferred to the VSC. The other is because a VSC allows for independent control over its reactive and active power supply [26]. Moreover, VSC technology has other advantages including flexible control, AC voltage control, network security and a fast dynamic response. Therefore, offshore energy technology will experience improved system efficiency and stability when integrated with HVDC VSCs [27]. The table below gives a comparison between VSC and LCC based HVDC converters.

Table 2. 1: Differences between LCC and VSC based HVDC technology.

System features	**LCC**	**VSC**
Commutation	Dependent	Independent
Reactive power compensation	Compulsory	Not compulsory
Harmonic filters	Compulsory	Filters are not needed

Directional flow of power	Uni-directional	Bi-directional

Currently, there are a small number of VSC based HVDC systems under construction. The Modular Multilevel Converter (MMC) is the most commercially sought-after VSC, having power level capacities up to 4000 MW and DC voltage ratings up to 800 kV [28]. The topologies of the MMC are discussed in the next section.

2.2.1 MMC CONVERTER TOPOLOGIES

The MMC converter has different topologies. The Half-Bridge (HB), Full-Bridge (FB), Clamp-Double (CD), and hybrid types. Fig. 2.4 presents the diagrams of the conventional MMC topologies.

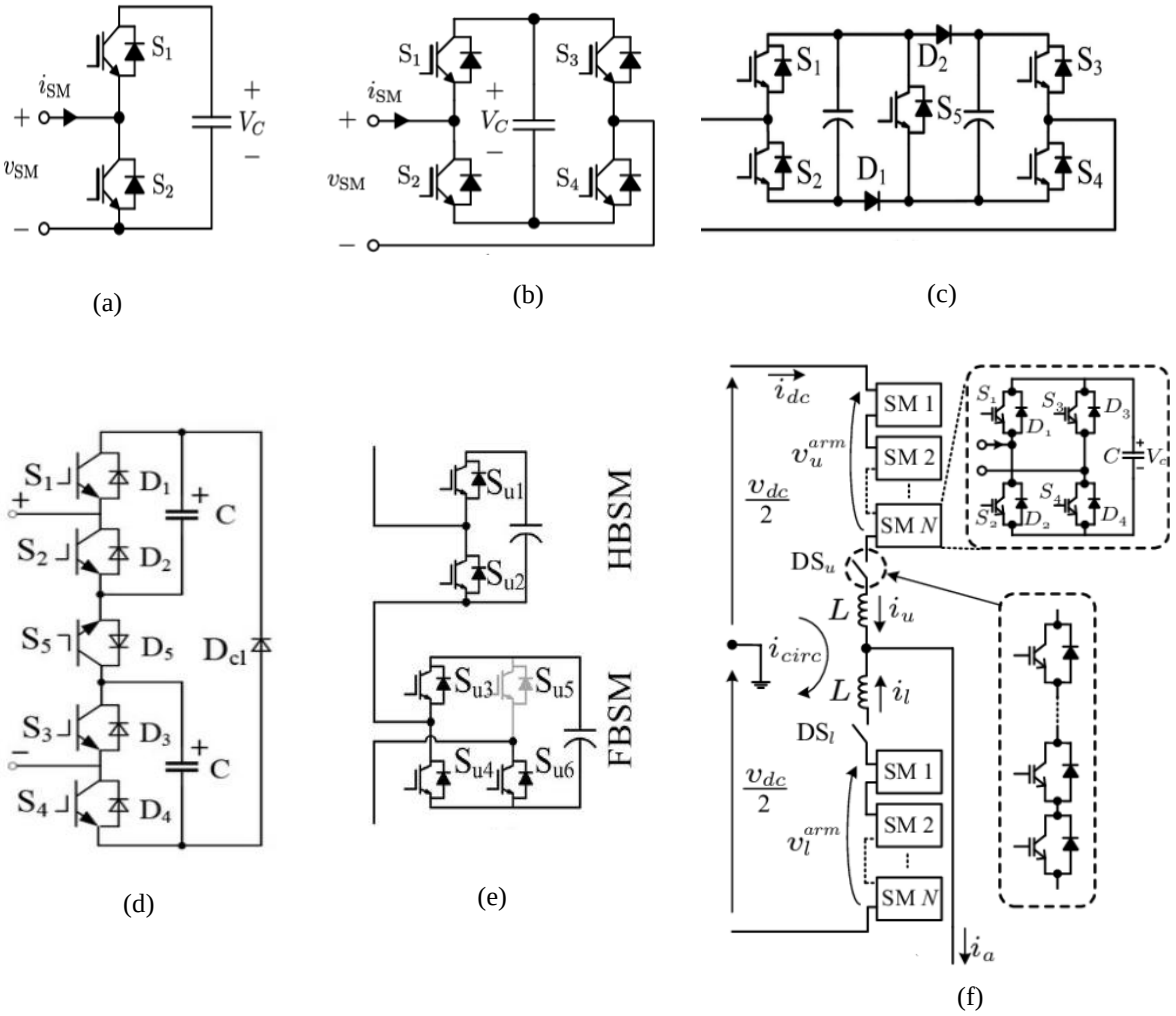
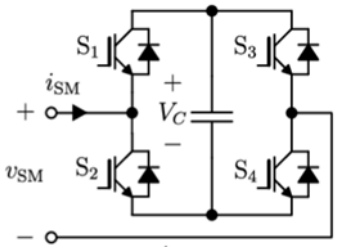


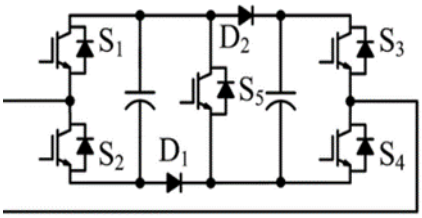
Fig.2. 3: MMC converter topology: (a) HBSM, (b) FBSM, (c) CDSM, (d) SCDSM, (e) Hybrid, (f) AAC.

According to [43], HB Submodules (HBSM) are a promising option for HVDC grid systems due to their low cost of implementation, minimal power loss, reduced footprint, and enhanced waveform. However, they lack fault blocking capability (the ability to self-isolate faults) because HBSMs cannot generate negative DC voltage and do not possess zero-crossing voltage paths [44]. Moreover, during a DC short circuit, the IGBTs of the HBSM are quickly blocked to prevent further damage to its switching elements. As a result, a low impedance short-circuit path is created. Hence, current from the AC grid will continue to feed the fault on the DC side, resulting in a sharp increase in the DC fault current, which could pose a serious threat to the converter or cause the entire HVDC system to shut down [45]−[46]. Due to the challenges associated with the HBSMs, the use of mechanical Circuit Breakers (CBs) on the busbar of the HVDC network with the HBSMs was proposed in [47] – [49] as a traditional solution to isolate the fault currents. In this approach, the currents from the AC side can be prevented from feeding the DC fault by opening all the CBs and isolate the line segments that are affected by the fault to allow the DC fault to be extinguished. In fact, this approach is the most cost-effective, but because the mechanical CBs operate slowly, high-rating semiconductor devices must be used to sustain the overcurrent [13]. Moreover, the entire system will be shut down for an extended period. This is inconvenient and will not be tolerated in a future HVDC system. As a result, [50] and [51] propose the use of solid-state DC CBs for reliable and fast isolation of fault current. However, the lack of a natural zero-crossing current path makes the development of DC CBs extremely challenging, leading to their high capital cost. Moreover, [52], [53] stated that the development of DC CBs for high voltage and high-power applications is not sufficiently mature due to the large magnitude of fault currents involved and the cooling requirement to withstand the on-state heating. Following the limitations associated with the aforementioned CBs, [54] presents the hybrid CBs developed for HVDC transmission systems. These hybrid CBs combine the advantages of mechanical CBs and solid-state CBs. Thus, they have reduced losses and high speed when in operation but may be expensive for large-scale implementation. Conclusively, the application of this CB to the HBSM is based on the trade-off between losses, cost, and speed. As a result of the drawbacks

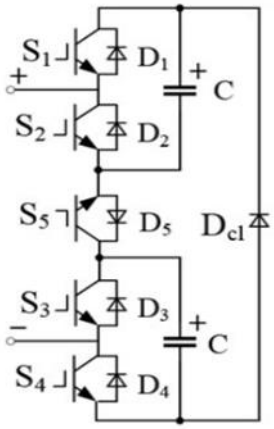
brought about using CBs to aid converter fault capability, researchers decided to modify the HBSMs to topologies with robustness to fault current (fault tolerant converters) [55] – [57]. During normal operation, these topologies can behave as typical HBSMs, but during a short circuit, they can generate bipolar voltages to quickly eliminate the DC fault current. However, when compared to the HBSMs, these SMs require twice as many electronic devices, resulting in substantial cost and power losses.



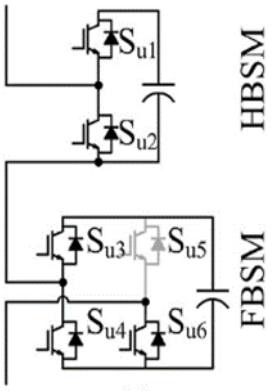
Reference [58] proposed the Full-Bridge SM (FBSM), which is capable of clearing DC fault current, unlike the HBSM. However, [59] acknowledged that the cost of implementation, footprint, and power loss of the semiconductor devices in the conduction path of the FBSM are twice as high as that of the HBSM. This limits the commercial attractiveness of the FBSM.



The use of Clamped Double SM (CDSM) MMC was presented in [60]. It comprises two HBSMs in series with two diodes and two parallel capacitors connected through an anti-parallel diode and an IGBT. When a fault is detected, the two capacitors generate voltages of opposing polarity to block the fault current. The magnitude of these voltages is half the voltage produced by the FBSM; therefore, more time is required to eliminate the fault currents. Thus, CDSM is not a suitable topology for FRT.



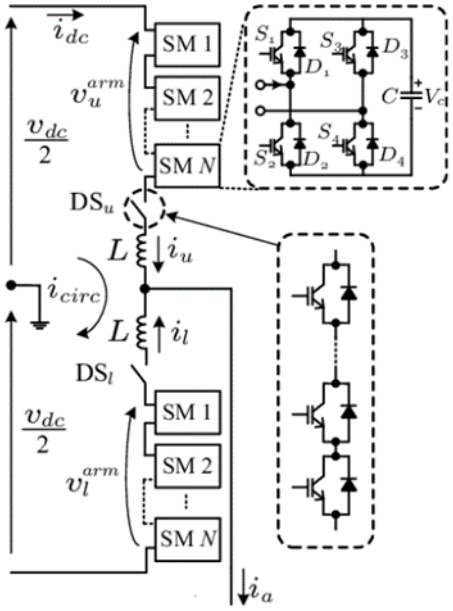
Given this shortcoming, Series-Connected Double Submodules (SCDSM) with only one diode were proposed as an improvement to the CDSM. It can double the reverse bias voltage and improve fault capability, but at the expense of the cost of electronic devices and power loss [61].



Since the modified topologies have improved fault capability at the expense of increased losses, [62] described how a hybrid topology can be formed to have reduced losses and still achieve fault capability. According to [62] two different variants of hybrid topology are:

1 A SM which combines the HBSMs and FBSMs. Such that one arm comprises the HBSM and the other arm comprises the FBSM. Merging the two SMs draws on the strengths of both the HBSM and the FBSM to achieve fault capability and reduce power loss. However, the major challenge with this topology is the high capital cost of implementing the design [63]. Also, it was shown in [64] that this hybrid SM struggles as a static synchronous compensator (STATCOM) since all their converter arms are blocked as they clear the fault current.

2 A SM which combines FBSM with a two-level converter (H-TL). In addition to fault capability, the FBSM acts as an active filter to reduce the switching losses in a conventional two-level converter. The active switches of this hybrid topology require a series connection of IGBTs and a large DC link capacitor. However, during DC faults, the DC capacitor discharge could increase the fault current which would require additional measures to achieve FRT.



To minimise the cost and the number of additional power electronic devices, the Alternate Arm Converter (AAC) was suggested in [65], [66], [67] and [68] as the most efficient modified MMC topology. The AAC draws the advantages of an FBSM and a high voltage IGBT. According to [69], the AAC exhibits fault capability when used in protecting overhead lines DC faults. However, the AAC uses director switches, which utilize an increased number of IGBTs. Moreover, due to the alternative operation of the converter arms, a remarkable sixth-order harmonic component in the DC current exists, which may require a large-sized reactor in the DC side for filtering purposes. Table 2.2 presents a comparison of characteristics of different MMC topologies reported in literature.

Table 2. 2: Comparison of MMC topology [59], [70]

Comparison of the MMC Configurations							
MMC Parameters	HBSMs	FBSMs	CDSM	SCDSM	Hybrid (Mixed-FB+HB)	H-TL	AAC
HVDC-link voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$0.628V_{dc}$
Fault blocking Voltage	✕	Excellent $1.08V_{dc}$	Satisfactory $0.5V_{dc}$	Excellent $1.08V_{dc}$	Excellent $1.08V_{dc}$	Excellent $1.08V_{dc}$	Excellent $1.08V_{dc}$
Blocking Time	✕	12 s	24 s	12 s	5 s	10 s	2-5 s
Fault ride-through	✕	Satisfactory	Very Poor	Satisfactory	Good	Satisfactory	Excellent
Number of SMs/arm	2N	2N	2N	2N	N-HB+N-FB	2N	0.628N
Estimated Power Loss (Switching losses + Conduction losses)	Conduction losses (0.47%) + switching losses (0.16%) Total Losses = 0.63%	Conduction losses (1.88%) + switching losses (0.29%) Total Losses = 2.17%	Conduction losses (1.92%) + switching losses (0.30%) Total Losses = 2.22%	Conduction losses (1.90%) + switching losses (0.30%) Total Losses = 2.20%	Conduction losses (1.75%) + switching losses (0.34%) Total Losses = 2.09%	Conduction losses (1.74%) + switching losses (0.31%) Total Losses = 2.05%	Conduction losses (0.60%) + switching losses (0.20%) Total Losses = 0.80%
Estimated Device Cost	100%	166.70%	126.70%	122%	125%	118%	111%

From Table 2.2, the fault capability of the CDSM is inferior because two of its SM capacitors are in parallel; they would produce a reverse-biased voltage of 0.5 Vdc, which is not sufficient to control the converter phase current. FBSMs and other modified topologies exhibit fault capability for primary protection but at the expense of semiconductor devices, while HBSMs cannot handle fault current. Although, the HBSM offers the lowest number of IGBTs and footprint.

2.2.2 CHARACTERISTIC COMPARISON OF MMC TOPOLOGIES

The following section shows a detailed review of the losses, costs, and fault blocking times of the MMC topologies mentioned above.

A. MMC Loss Evaluation

The total power loss of an MMC is the sum of the switching and conduction losses of all its diodes and IGBTs. In Fig. 2.5, the total power loss is represented by the grey bar, while the conduction and switching losses are represented by the blue and orange bars, respectively. The power loss of the standard HBSM-based MMC is approximately 0.63%, whereas the AAC has losses of approximately 0.80% as seen in Table 2.2.

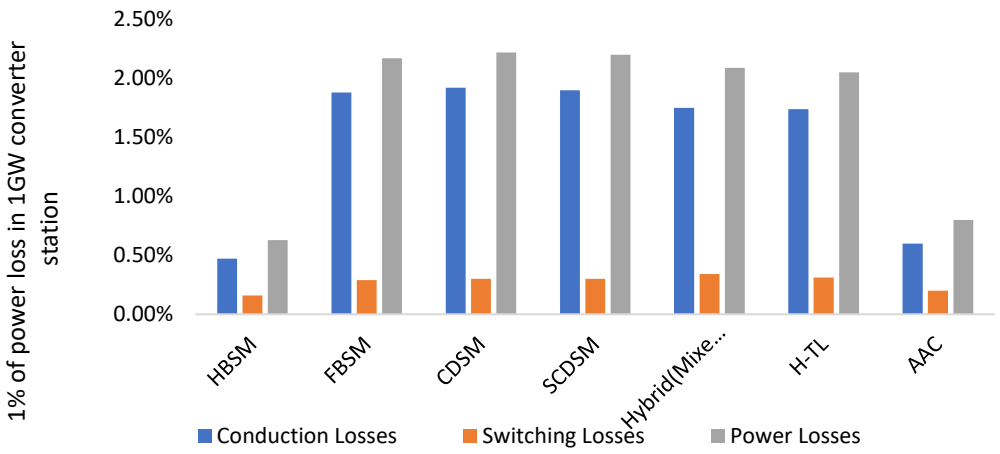


Fig.2. 4: Loss evaluation for MMCs

B. Estimated Cost

The MMC cost consists of the operational and initial components cost. The components cost is dependent on the number of devices per arm of the SMs. The daily cost of operation of the converter can be accounted for by the conduction losses associated with its SMs. These losses are a measure of the power loss cost in a 20-year operating period. Fig. 2.6 gives the estimated cost in percentage drawn from Table 2.2.

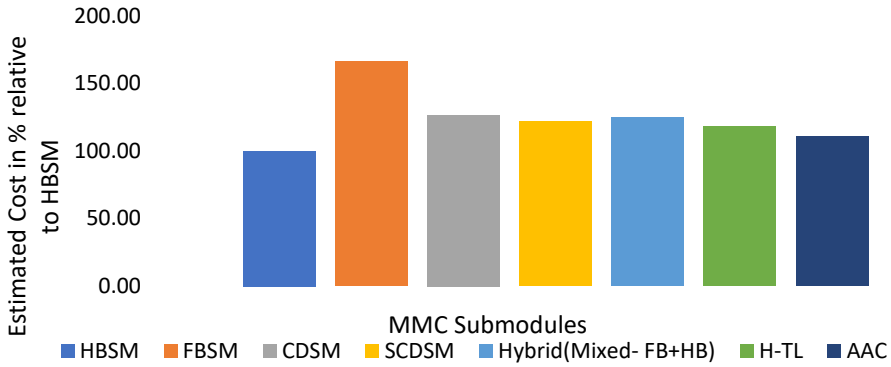


Fig.2. 5: Estimated cost for MMCs

The HBSM-based MMC is considered the standard MMC topology with the least capital cost due to the simplest structure of its SM. All the modified SMs, such as the CDSM, SCDSM, FBSM, and hybrid, require additional devices, which leads to drawbacks such as high cost, large footprint, and the need for a cooling system.

C. Fault Blocking Time

Fault blocking is the ability of the converter to self-isolate a fault by using reverse voltage, while fault blocking time is the amount of time needed for a converter to eliminate faults before the IGBTs are blocked. This is possible during the primary protection stage. Fig. 2.7 shows the fault blocking time in seconds for each converter SM as seen in Table 2.2.

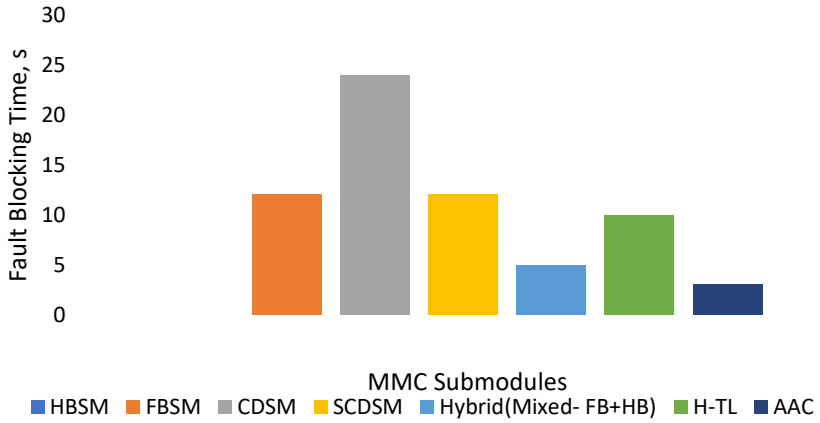


Fig.2. 6: MMCs fault blocking time

When a fault is detected, all the converter IGBTs are quickly switched to the fault-tolerant mode before they are blocked. The shorter the time, the quicker the fault isolation process and the better the FRT.

Further comparison based on the performance of the MMC converter topologies is given in Table 2.3 as shown below.

Table 2. 3: Performance checklist of the various MMC SMs

MMCs Converter Topology	Capacitor Voltage Balancing	Capital Cost	Power Loss	Footprint	FRT	References
HBSMs	✓	✓	✓	✓	×	[71] [72]
FBSMs	✓	×	×	×	✓	[70] [73]
CDSMs	×	×	×	×	×	[74] [75]
SCDSMs	×	×	×	×	✓	[76] [77]
Hybrid (Mixed)	✓	×	×	×	✓	[78] [79]
Hybrid (H-TL)	✓	×	×	×	✓	[80] [81]
AAC	×	✓	✓	✓	✓	[82] [83]

From Table 2.3, the modified topologies utilise additional IGBTs which increase the complexity, cost, and power losses and thereby reduce the attractiveness for large-scale implementation.

The performance of the hybrid MMC is based on a trade-off between the number of HBSMs and FBSMs. The above table suggests that the AAC would be the best option. However, several challenges limit its commercial application, such as the capacitor and energy imbalance [84], and the hard switching effect between the lower and upper arms of the director switches. This could lead to voltage transients and high voltage stress on the IGBTs. The HBSM is the simplest and most cost-effective topology [85] but lacks FRT capability.

Furthermore, Table 2.3 shows that the modified MMC topologies exhibit DC-FRT when deployed on HVDC networks. While these converters can ride through faults, there are still challenges in network management and control methodology that affect the robustness of the fault clearing process and primary protection. For example, during DC faults, a more complex control strategy is required to coordinate the balance of the MMC's circulating current and leg/arm energy [86].

Several control strategies have been proposed for the MMC during normal operation, as implemented in [87] - [90]. For example, a closed-loop control scheme was used to regulate the DC output current and power of the MMC in [91] and [92]. However, during a DC fault incidence, the control strategies for normal operation are not appropriate. To obtain DC fault protection schemes for HVDC systems, an open loop modulation [93] or a direct voltage modulation [94] that relies on using a DC modulation index was proposed. This method of controlling the MMC is known as a non-energy control approach. The control approach is asymptotically stable because its transient depends on the impedance of the converter rather than being imposed by a controller, resulting in undesirable overshoots and slow time constants [95]. Furthermore, the voltage ripples generated during the charging and discharging of the arm capacitors of the MMC are not compensated for in the modulation stage. This leads to insertion index errors. As a result of these errors, the arm capacitor voltages are significantly diverged [96], and the circulating currents are contaminated with large 2nd order harmonics [97], which increase the RMSE value of the converter's internal current with excessive power loss.

Further attempts to eliminate these oscillations have led to the development of resonant controllers [98]. However, these controllers struggle to achieve stable and sensitive control parameters [99]. Moreover, in [100], it was shown that the 2nd order oscillations are caused by an unregulated DC link current and stored energy in the MMC. Therefore, it is necessary to control the internal dynamics (energy and circulating current) of the MMC such that SM charges are distributed equally, thereby preventing the divergence of the arm energies from the desired values.

Several control schemes for ensuring MMC arm energy balance are discussed in [101] - [104]. These schemes focus on the total sum of energy in the MMC's arms. However, they fail to

recognize that the individual converter leg energy could vary with a DC fault, generating differential energy. As a result, the control strategies described in [105] and [106] employ oscillatory components in common mode currents to regulate energy differences. However, this technique can generate undesirable interferences with the DC power, which may lead to fluctuations in the DC grid voltage, therefore posing a challenge to DC-FRT. Thus, there is a need to develop a converter topology that integrates a control system to enhances primary protection with a balance of energy and circulating current.

2.3 REVIEW ON BACKUP PROTECTION STRATEGIES

Backup protection strategies, briefly mentioned in Section 1.4, are discussed in greater detail in this section. The existing backup protection methods can be classified into Travelling Wave (TW) and Non-Travelling Wave (NTW) techniques. The travelling wave (TW) method is the most used among conventional techniques. TW techniques measure the reflection of fault current and voltage from the point of fault impact, as seen in Fig. 2.8. This method's accuracy depends on the arrival time and velocity of the reflected fault wave [107].

Considering a remote fault at a point on a transmission line L, travelling wave techniques can be used to obtain the location of the fault, x using the expression:

$$x = L - \frac{v(t_2 - t_1)}{2}$$

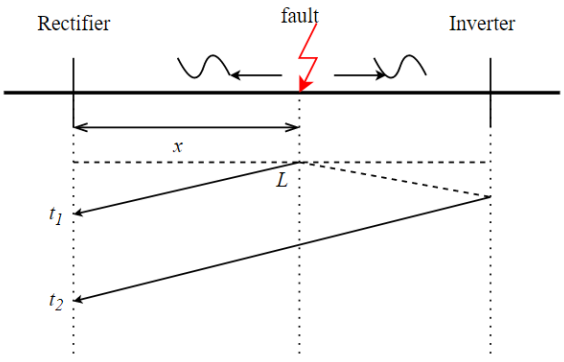


Fig.2. 7: Travelling wave fault location scheme

where, v is taken as the speed of light and t_1 and t_2 are the initial arrival and reflected time of the fault waves.

The TW method struggles to differentiate the waves from a system terminal from those of a fault [108]. In [109], a pilot protection approach that uses the similarities between the cosines of TWs on a single-ended protected HVDC line is proposed. Further, and considering the wave power of reflected and incident TWs, a time-domain fault location scheme was applied to the HVDC grid [110]. However, it was difficult to detect the reflected TW transient. This is due to the small difference in time between successive reflected close-in fault signals, confusion between multiple reflections, and the attenuated magnitude of fault signals [111]. To improve the accuracy of the TW method, a double-ended TW method was proposed to detect only the surge arrival time of the first TW at both terminals [112]. These TW-based fault schemes are prone to communication delays and poor sensitivity; in fact, they must be integrated with a GPS time synchronisation technology and a communication channel [113], which increases the cost of the fault location process [114]. Finally, under high impedance remote faults, the TW signal can be vulnerable to noise and too weak to detect [115], leading to a significant error. This worsens the accuracy of the fault location process.

An alternative scheme to the TW method is the impedance method, which is an NTW technique. The impedance-based technique uses the online voltage and current in pre-fault and during-fault situations to determine the impedance at the fault point [116]. In [117], an impedance-based method was used to locate high-resistance faults and remote faults. The technique measures the characteristic harmonics of the fault current and voltage in the HVDC transmission line to obtain the fault distance. However, since the impedance of the HVDC cable increases with the distance between the fault location and the protective device [118], the location of the fault can be estimated with knowledge of the cable impedance per unit length. Thus, the location accuracy of impedance-based techniques is dependent on fault resistance. As the fault resistance increases, the error between the actual and estimated location increases [119]. Moreover, the technique is susceptible to noise signals and the operating states of the MMC converter. Reference [120] proposes a high-frequency impedance-based method and uses double-ended measurement techniques to locate the fault and overcome difficulties caused by a varying fault resistance. However, at high frequencies, the effect of the distributed capacitance of the HVDC cable creates

new difficulties. In addition, the accuracy of this technique is dependent on fault data from both ends of the transmission line, which adds to the cost of installing communication facilities and microprocessor relays [121].

In [122], the Pearson correlation coefficient on voltage signals was another fault location method for MMC-HVDC systems. Its location process is quite challenging to implement since the voltage signals are easily disturbed by the actions of the fault protection devices. In addition, the Pearson correlation coefficient changes with voltage ripples even when the rate of change of voltage is the same. This could lead to miscalculation of the fault location. In [123], fault location based on Electromagnetic Time Reversal (EMTR) was proposed. This method uses an almost similar approach to the TW fault location techniques by refocusing the peak energy amplitude from time-reversed waves to locate the unknown fault distance. However, it fails to accurately locate high impedance faults, and it requires numerous backpropagation simulations to identify the fault location. In [124], the Prony algorithm was used to locate faults using the principal components of natural frequencies. However, it is prone to location errors since the Prony model is numerically ill-conditioned, non-strict, and sensitive to noise.

Table 2.4 presents a summary of the different TW and NTW backup protection schemes that have been reported in the current literature to reinforce HVDC systems. The table further shows the drawbacks encountered by each technique. It is apparent that the TW and NTW schemes suffer from setting manual protective thresholds, data loss in the communication channel, sensitivity to fault resistance, and vulnerability to noise. Due to these shortcomings, recent work has been reported to improve the performance of TW techniques. According to [125], the surge arrival time difference (SATD) between the line-mode and ground-mode TWs was proposed at 200 kHz. The effects of fault resistance on locating DC faults were greatly improved. However, in actual travelling wave devices, it was difficult to sample at such a high frequency as the wavefront generated was too fast. [107] proposes a morphological gradient TW based on a single-end protection technique. The issues with the communication channels were improved. However, the

method was greatly influenced by resistance, which affects the scheme's accuracy to fault location. In addition, the research did not investigate performance under noise conditions.

Table 2. 4: Reviews on Backup protection strategies

Backup protection	Communication requirement	Sensitivity to resistance	Sampling rate	Calculation Burden	Data Synchronization	Challenges	Sources
Two-end current differential	Yes	Yes	10 kHz	Large	Yes	strict signal synchronization, low operating speed, high sensitivity to white Gaussian noise, poor selectivity during resistance fault	[107] [126]
Travelling Wave (TW)	Yes	Yes	10 kHz	Small	Yes	TW device must be sampled at high frequency to improve accuracy, susceptible to interference and attenuation as it propagates through a long transmission line,	[127]
Ratio of Transient Voltage (ROTV)	Yes	Yes	50 kHz	Large	No	poor sensitivity to fault detection at high sampling rate	[128] [129]
Reactive Energy Comparison	Yes	Yes	10 kHz	Large	No	As fault resistance increases, the reactive energy at both ends weakens leading to sensitivity problem	[130]
Current and Voltage level-based method	Yes	Yes	20 kHz	small	Yes	extensive time domain simulations to determine the protection thresholds for only a specific small-scale test system	[131]
Time reversal electromagnetic based method	Yes	Yes	50 kHz	Large	No	In most practical operations, fault-location results are affected by time asynchronization.	[132]
Pilot Protection based on TW	Yes	Yes	10 kHz	Large	Yes	Due to TW dispersion effect, a stringent requirement on data synchronization is necessary to avoid maloperation	[133] [134]

Given the complexity of today's HVDC grid networks, which include multiple terminal transmission lines and insufficient measuring stations, a wide-area approach to fault estimation holds great promise for the future. In addition, with the limitations of the TW and NTW techniques, a reliable and fast intelligent system that can overcome the challenges listed in Table 2.4 is recommended as backup protection. This can be achieved through secondary protection schemes based on artificial intelligence, as discussed in the next section.

2.3.1 BACKUP PROTECTION BASED ON ARTIFICIAL INTELLIGENCE ALGORITHM

Modern control systems based on AI are robust and reliable. AI is gaining more attention in the field of HVDC transmission for converters, fault diagnosis, and system state estimation. According to [135], the adaptation of AI to MMCs is due to its strong learning capabilities, good performance under noisy signals, and ability to map complex nonlinear behaviour. Hence, AI algorithms can efficiently recognize electrical circuit patterns for fault estimation in DC-AC systems. The application of AI to transmission line fault location is shown in [136], but it is stated that the actual application of fault location requires further research.

AI can either be machine learning (ML) based or deep learning (DL) based. Both ML and DL approaches are very efficient at solving complicated problems. AI algorithms have begun to be applied to various fault location tasks, such as fault location in power systems since they tend to have better adaptability and are less likely to be influenced by fault parameters. Reference [137] proposes the use of an ML Naïve Bayes classifier on a multi-terminal HVDC grid system to expedite backup protection operations for faster fault clearance by relaying algorithms. Reference [138] proposes the use of DL convolutional neural networks for DC fault detection and classification on a two-terminal, 21-level MMC based HVDC system. However, it could not capture time-series features in voltage or current signals. Also, an improved extreme learning machine [175] was designed to locate faults, but it does not consider the time series features. In [176], the Decision Tree Regression (DTR) method was used to extract the characteristics of the voltage and current signals to determine the fault location. However, under some experimental samples, the proposed method produced significant errors. While in [177], fault signals were

processed through Empirical Mode Decomposition (EMD) and used to train a deep learning-based Convolutional Neural Network (CNN). The CNN's classification and linear regression mechanisms were used to achieve fault location on the HVDC network. The model also considers the impact of high impedance ground faults, but it cannot automatically adapt to different fault lines. Moreover, the technique uses a complex feature extraction and working algorithm, and due to the size of the trained dataset and the number of pooling layers in the neural network, it suffers from a large computational burden, which slows the backup operation.

Table 2.5 presents a brief review and comparison of different AI backup protection approaches applied to MMC based multi-terminal HVDC.

Table 2. 5: Comparison of various AI Techniques for backup protection of MMC

AI Fault Location Methods	Overview	Challenges	Sources
Linear Discriminant Analysis (LDA)	LDA algorithm is used to extract the operational time frames and thresholds of both primary and backup protection regions.	LDA suffers from misclassification, practical implementation of LDA algorithm fails since the discriminator is in variance. Besides, its algorithm is synchronised with significant calculation burden.	[139]
K-means data	K-means is applied to post-fault current and voltage data generated in various conditions. The obtained thresholds and centroids are used for detecting, classifying, and locating faults path. There is minimal classification error in the training and testing dataset with reduced sampling rate and no data synchronization.	This approach is slow because the standard deviation of the sampled signals is not discretized and filtered. Also, the K-means algorithm is sensitive to resistance, and the computational burden is enormous.	[140]
Fuzzy Logic	The fuzzy logic controller is highly efficient in controlling nonlinear variables and optimizing HVDC system for fault estimation	The fuzzy logic derivation is relying on human interpretation of system dynamics. They also experience a delay when tuning fuzzy system parameters in complex grid systems.	[141]
Bayesian Networks	The Bayesian network applies the principle of backpropagation algorithm to estimate the fault location of a complex grid. Furthermore, they have precise semantics, powerful error tolerance ability and no convergence problem during the diagnosing procedure.	The algorithm suffers from a significant computational burden which tends to slow their operation	[142]

Neural Networks, NN (Feedforward, Convolutional, Recurrent, Radial basis function, Modular, Multilayer perceptron)	Neural networks have excellent adaptive and self-learning capabilities in pattern recognition problems. The outputs of the ANN are used to trigger the DC line and bus protections and select the faulted poles.	Its performance may sometimes be influenced by weight adaptation algorithms, noisy data, and implicit data representation. The many layers used in its network sometimes leads to many training cycles and computational burden when dealing with complex grid systems.	[143] [144] [145] [146]

2.4 RESEARCH QUESTIONS

According to the above literature review and identified research gaps, the following research questions are developed.

- Can a control methodology and a converter topology be designed at reduced losses, cost, and footprint to allow the MMC-HVDC system to exhibit FRT and support AC loads with energy stored in the capacitor?
- Can a backup protection strategy be developed with improved FRT performance that efficiently locates the faulty terminal and the exact fault point on MMC-HVDC transmission lines for isolation to be performed while reducing economic losses, enhancing quick restoration of services, and promoting power sustainability and reliability in the grid?

2.5 CONCLUSION

In this chapter, an overview of VSC-HVDC technology has been introduced. The features of MMC-based VSC-HVDC systems for multi-terminal operations were also analysed and compared with those of the LCC-based systems. It was shown that MMCs have a developed topology with great flexibility. However, they have a complex control structure, and their topologies with FRT capability are still limited by losses, cost, and increased footprint. There is a need to design a control system and a converter topology that can offer primary protection from faults and meet the above limitations.

Furthermore, it was shown that MMC fault blocking converters struggle with permanent DC faults and would require a backup protection strategy to locate faults while maintaining the operation of the network. Several backup protection strategies were reviewed. The TW method for estimating fault location is the most commonly used for HVDC systems, but it has some drawbacks. Other methods based on cable impedance measurement were used for small-scale or overhead transmission systems. Some of these methods require additional equipment, such as global positioning systems and additional secondary factors. Moreover, the AI backup protection schemes struggle with computational burden and poor sensitivity. Therefore, there is a need to design a low computational method to estimate the location of faults on an HVDC transmission system and realize effective backup protection systems without the need for extra devices or disconnection of the terminals.

Chapter 3

3. A NOVEL SINGLE-CLAMPED HYBRID-ARM MMC WITH A DYNAMIC CONTROL METHODOLOGY FOR DC-FRT AND STATCOM OPERATION

3.1 INTRODUCTION

In this chapter, a single-clamped hybrid-arm MMCs topology is proposed to achieve a 50% and a 29% reduction in the number of IGBTs when compared with the FBSM-based topology and the hybrid-based HBSMs and FBSMs, respectively. The proposed topology is implemented with a novel energy-based control for achieving leg and arm energy balance during DC fault such that the components of the circulating currents responsible for feeding the DC fault with transient DC oscillations are eliminated successfully. Also, the control strategy encourages DC-FRT capability and STATCOM operation through reactive power compensation to support the AC grid voltage. Therefore, the novel hybrid-arm converter topology is proposed to offer one of the most cost-effective methods of providing DC-FRT with a reduced number of power electronic devices while ensuring additional reactive power is supplied to the AC system at reduced losses during the fault clearance.

The rest of the chapter is structured as follows. In Section 3.2, a detailed analysis of the circuit parameters of a typical MMC and its control structure are presented, while Section 3.3 describes the conventional energy-based control of the MMC. The proposed energy-based control needed to achieve DC-FRT is analysed in Section 3.4. In Section 3.5, a detailed analysis of the proposed topology is presented while its operation principle and control structure during normal and faulty scenarios are presented in Section 3.6. Section 3.7 and 3.8 describes the DC-FRT techniques of

the MMC and the STATCOM operation respectively. In Section 3.9, simulation results are conducted to validate the proposed topology and its control methodology. Furthermore, in Section 3.10, comparative analyses are presented with the other converter topologies in terms of the number of power electronic devices used, the associated power losses, cost, and the DC-FRT performance. Section 3.11 is the conclusion.

3.2 MMC SYSTEM DESCRIPTION

The MMC circuit representation in Fig. 3.1, is a typical AC-DC three phase (*a*, *b*, *c*) system, where DC voltage, V_{DC} is split into $\frac{v_{dc}}{2}$ to feed the lower and upper arms. Each arm comprises a series of *N* connected Submodules (SMs), separated by arm impedance (inductor, L_a and resistance, R_a) offering a low of resistance to DC fault current. For this section, an Average Arm equivalent Model (AAM) of the MMC is used, where the stack of SMs is represented by a chopper with a balanced capacitor voltage. The aggregated capacitor is represented by C_{eq}. Where, C_{eq} is given as $\frac{C}{N}$ for the *N* SMs in each arm. The rest of the AAM parameters are discussed in the next section.

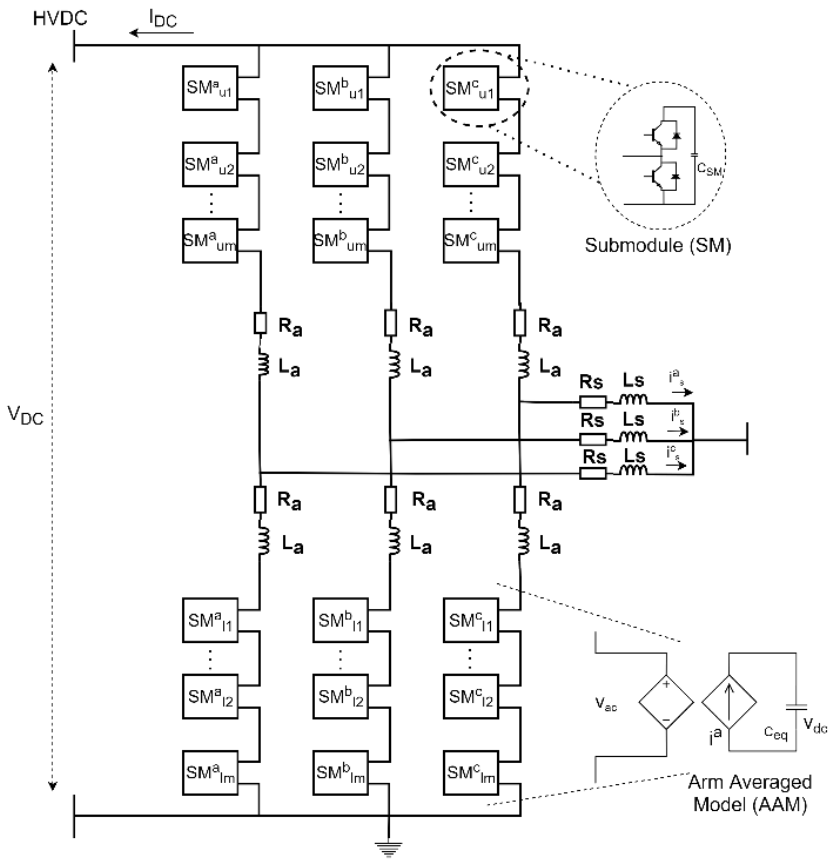


Fig.3. 1: MMC circuit with Average arm model

3.2.1 CIRCUIT PARAMETERS OF AAM

In this model, the MMC independent variables are theoretically explained. The relationship between the current and voltage of the three phases ($j \in \{a, b, c\}$) average arm model is shown in (3.2):

From,

$$i = C\frac{dv}{dt} \tag{3.1}$$

$$i_{Ceq^j} = C_{eq}\frac{dv_{Ceq^j}}{dt} \tag{3.2}$$

To generate the DC and AC control variables of the MMC, Kirchhoff's law is applied to the AAM to obtain (3.3) and (3.4).

$$\frac{v_{dc}}{2} = v_u^j + R_a i_u^j + L_a\frac{di_u^j}{dt} + L_s\frac{di_s^j}{dt} + R_s i_s^j + v_s^j \tag{3.3}$$

$$\frac{v_{dc}}{2} = v_l^j + R_a i_l^j + L_a\frac{di_l^j}{dt} - L_s\frac{di_s^j}{dt} - R_s i_s^j - v_s^j \tag{3.4}$$

where v_s is the phase voltage, v_l^j, v_u^j, i_l^j and i_u^j are the voltages and currents of the lower and upper arms, i_s^j is the grid current through grid resistance, R_s and inductance, L_s. On adding (3.3) and (3.4), the decoupled parameters for the DC side are obtained.

$$\frac{v_{dc}}{2} = v_{sum}^j + R_a i_{cir}^j + L_a\frac{di_{cir}^j}{dt} \tag{3.5}$$

$$i_{cir}^j \cong \frac{i_u^j + i_l^j}{2} \qquad and \qquad v_{sum}^j \cong \frac{v_u^j + v_l^j}{2} \tag{3.6}$$

Likewise, on subtracting, AC side parameters are obtained.

$$v_{diff}^j - v_s^j = L_{eq}\frac{di_s^j}{dt} + R_{eq} i_s^j \tag{3.7}$$

$$L_{eq} = L_s + {}^{L_a}/_2 \;\; and \;\; R_{eq} = R_s + {}^{R_a}/_2 \tag{3.8}$$

$$v_{diff}^j - v_s^j = \left(L + {}^{L_a}/_2\right)\frac{di_s^j}{dt} + \left(R + {}^{R_a}/_2\right) i_s^j \tag{3.9}$$

$$v_{diff}^{j} \cong \frac{v_l^j - v_u^j}{2} \quad and \quad i_s^j = i_u^j - i_l^j \tag{3.10}$$

where, v_{diff}^{j} is the AC internal voltage of the MMC while v_{sum}^{j} is the internal voltage driving the circulating current, i_{cir}^{j}. In normal operation, i_{cir}^{j} is the current that flows between the lower and the upper arm of phase j. The decoupled equations and parameters are prerequisites for understanding the proposed control design.

3.2.2 CONTROL STRUCTURE OF MMC

The control structure of MMC using a proportional integral (PI) controller can be grouped into inner level control and outer level control as shown in Fig. 3.2. The top part of the outer loop comprises the reactive power Q_{ac} control and the AC power P_{ac} control. These control blocks generate the grid side current reference i_s^j which is used as inputs to the inner level control when decoupled to the dq equivalents (i_s^{d*}, i_s^{q*}) via the Phase Lock Loop (PLL) using the inverse park transformation [147]. At the bottom of the outer loop is the energy control that generates the circulating current i_{cir} that flows through the converter.

Considering the inner level control, it comprises the voltage-based control at the top and an extension of the energy-based control at the bottom. From the two loops, the generated voltages can be modulated to produce the gate signals m_u^j and m_l^j for switching the IGBTs of the MMC.

A further study is carried out in the next section to explain the challenges and possible solutions associated with this control system, particularly the energy control system.

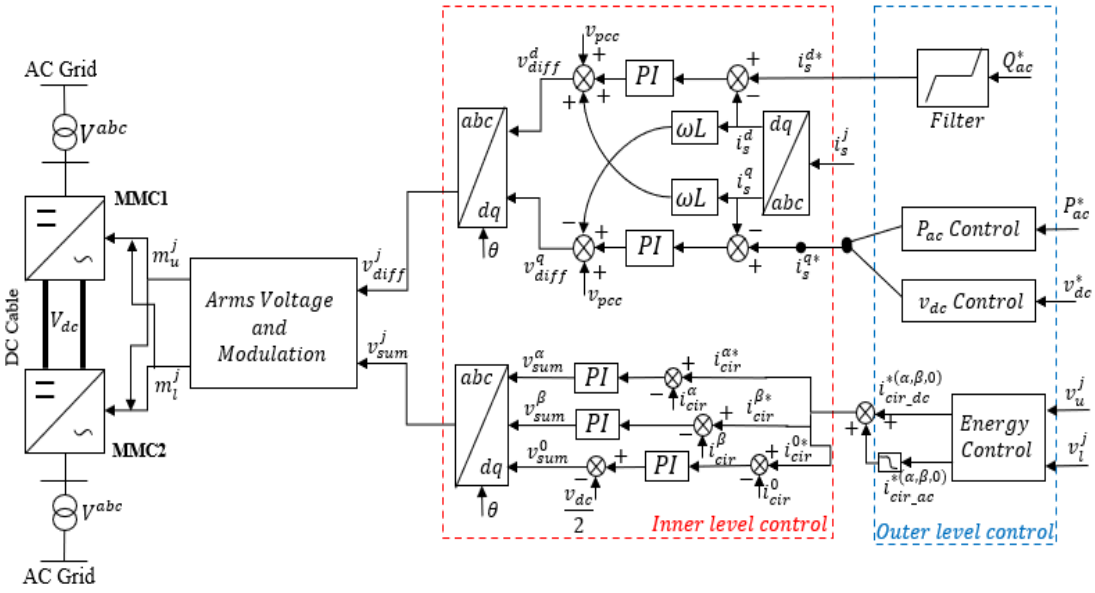


Fig.3. 2: Control structure of MMC

3.3 CONVENTIONAL ENERGY-BASED CONTROL

The energy in the MMC converter is grouped into phase energy, arm energy and total energy based on the decoupled variables in the previous section. The MMC is stable, and its energy is constant during normal operation. However, during short circuit mode, one or more of the converter's SMs in each arm fails, and the remaining SMs are discharged to maintain the pre-fault energy sum, leading to an imbalance in energy. As a result, a control variable can be used to drive the energy difference to zero without disturbing the total arm-energy. This is done using an AC reference increment of the circulating current on a differential arm-energy controller as shown in Fig. 3.3. The challenge with this approach is to ensure the circulating current corresponds to the reference value.

3.3.1 PHASE AND ARM ENERGY

The phase energy is the stored energy in each leg of the MMC, as shown in (3.11). Because the total leg energy fluctuates during short circuit conditions due to capacitor discharge, compensating the energy is required.

$$E_{phase} = E_l + E_u \tag{3.11}$$

The arm energy is measured based on the power needed to charge the capacitors in the upper and lower arms of the MMC SMs. It is dependent on the aggregated capacitor voltage as shown in (3.12).

$$E_{ul}^{j} = \frac{1}{2} C_{eq} v_{C_{eq}}^{2} \tag{3.12}$$

$$E_{sum}^{j} = \frac{1}{2} C_{eq} \left(v_{C_{eq}u}^{2} + v_{C_{eq}l}^{2} \right) \tag{3.13}$$

$$E_{diff}^{j} = \frac{1}{2} C_{eq} \left(v_{C_{eq}u}^{2} - v_{C_{eq}l}^{2} \right) \tag{3.14}$$

where E_{sum}^{j} and E_{diff}^{j} is the sum and difference of the stored energy in each arm. The relationship between these energies in the converter is shown below when losses are negligible.

$$\frac{dE_{sum}^{j}}{dt} \cong p_{dc}^{j} + p_{ac}^{j} \tag{3.15}$$

From (3.6) and (3.10),

$$\frac{dE_{sum}^{j}}{dt} \cong v_{dc} i_{cir}^{j} + \frac{v_{s}^{j} . i_{s}^{j}}{3} \tag{3.16}$$

$$\frac{dE_{sum}^{j}}{dt} \cong v_{dc} i_{cir\_dc}^{j} \tag{3.17}$$

Where the DC and AC power is represented as P_{dc} and P_{ac} respectively. The AC power is the total power divided by 3, while the DC power is the product of DC voltage and DC circulating current as shown in (3.16). During steady states in (3.17), only the DC components of i_{cir}^{j} is used to regulate the average sum of arm energy. Similarly, the average energy difference is regulated by the AC components of the circulating current as shown below.

From (3.14)

$$\frac{dE_{diff}^{j}}{dt} \cong p_{dc}^{j} - p_{ac}^{j} \tag{3.18}$$

$$\frac{dE_{diff}^{j}}{dt} = v_{u}^{j} i_{u}^{j} - 2 v_{diff}^{j} i_{cir}^{j} \tag{3.19}$$

$$\frac{dE_{diff}^{j}}{dt} \cong -2 v_{diff}^{j} i_{cir\_ac}^{j} \tag{3.20}$$

where the circulating current of phase j is regulated through a PI controller to track its nominal value, i_{jcir}^{*}, reduce harmonic distortions, and eliminate the energy imbalance in the converter. The expression for the PI controller is given in (3.21).

$$PI^{E_{diff}} = \frac{-2V_{diff}^{j}\left(i_{cir\_ac}^{j*}\right)}{E_{diff}^{j*} - E_{diff}^{j}} \tag{3.21}$$

From (3.18) - (3.21), the imbalance in energy due to active power transfer in charging and discharging capacitor in the MMC arms can be compensated using the AC components of the circulating currents, $i_{cir\_ac}^{j}$. This AC circulating current must be prevented from flowing to the DC links since it generates transient DC oscillations which is undesirable for achieving DC FRT. The phase and arm energy controller of the conventional MMC lacks the ability to balance this AC circulating current.

Another challenge of implementing the phase and arm energy-based control occurs during a pole-to-pole DC fault, where DC voltage collapses to zero and there is no active power supplied to the DC link. In such a case, the energy controller based on DC current reference will not be a viable option. Hence, a total energy-based controller capable of responding to DC faults by changing completely to AC power should be implemented.

3.3.2 TOTAL ENERGY

As a result of the limitations of the phase and arm energy control where the state variables of the MMC are controlled using only the AC circulating current reference, this section explains the impact of applying a total energy control scheme. This controller uses either the DC circulating current or grid current reference (i_{cir_dc} or i_s) to control the stored energy in all three phases of the MMC as shown in the upper part of Fig. 3.3.

$$\frac{dE_{Total}}{dt} = \frac{1}{2}C_{eq}\frac{d}{dt}\left(\sum v_{C_{eq}u}^{2} + \sum v_{C_{eq}l}^{2}\right) \tag{3.22}$$

$$\frac{dE_{Total}}{dt} = P_{DC} + P_{AC} \tag{3.23}$$

During pole-to-pole short circuit conditions, the total energy control can balance the converter energy using AC power-based control thereby solving the challenges of using only the DC power control. However, during this fault condition, the SMs capacitor is discharged due to the absence of phase and arm energy controller. Therefore, the total energy control scheme should be compensated using $i^{j}_{cir\_ac}$ with a balanced reference as shown in the proposed energy-based scheme in Fig. 3.7.

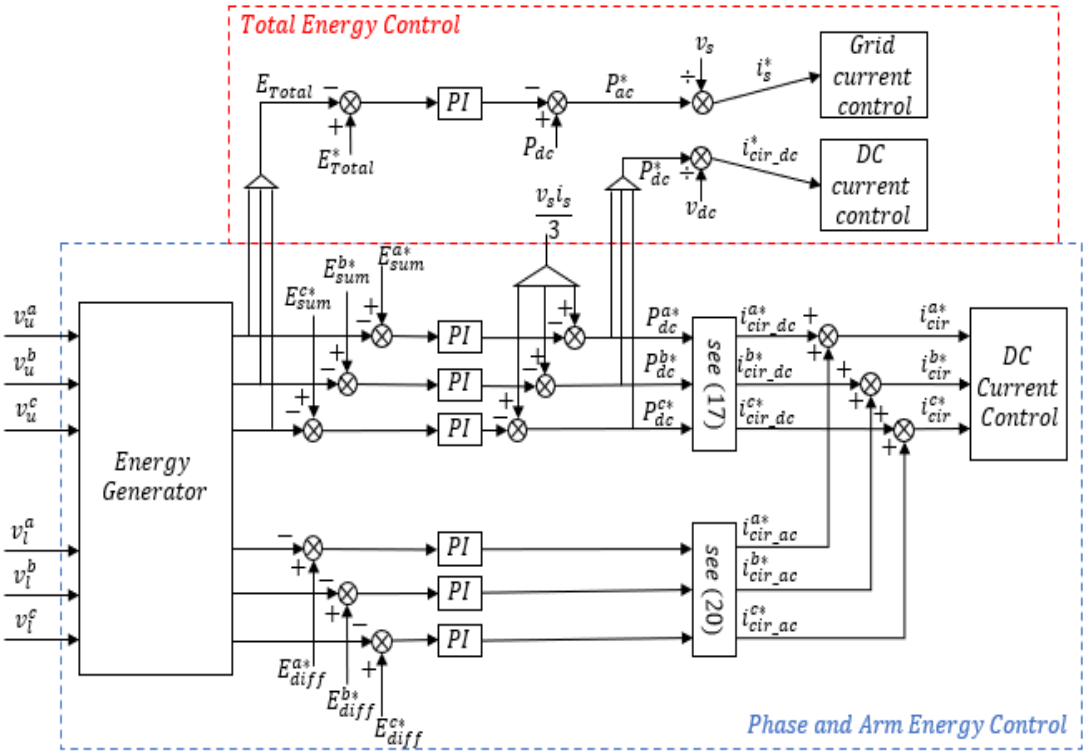


Fig.3. 3: Classical energy-based control

3.4 PROPOSED ENERGY-BASED CONTROL

The proposed energy-based control focuses on regulating the energy balance within the arm and leg of the MMC converter. Section 3.4.1 elaborates on this concept.

3.4.1 LEG AND ARM ENERGY CONTROL

During a pole-to-pole fault, an energy imbalance occurs since some SMs are discharged to provide the affected SMs with energy. Also, no DC current reference is generated since the AC power feeding the network is prevented from flowing to the DC side, hence the DC component of the circulating current reference is zero and only the AC component of the circulating current is used

for balancing the energy difference in the converter as shown in Fig. 3.7. This current provides internal control actions and should not be seen flowing to the DC or AC terminals. This is possible if the AC circulating current reference is zero. Therefore, the imbalance in arm energy during pole-to-pole fault can be regulated using $i^{j}_{cir\_ac}$. However, using $i^{j}_{cir\_ac}$ for the arm energy balance is challenging because it has non-zero sum of magnitude and phase reference which affect its circulating nature within the converter. This non-zero AC currents reference can flow to the DC link and causes large oscillations as they feed the fault and prevent the feasibility of DC-FRT. Hence, the aim is to eliminate the non-zero reference in $i^{j}_{cir\_ac}$ for the arm-energy control.

The circulating current reference generated from the classical energy controller is shown in Fig. 3.4. The sum of the current vectors in each arm of the converter is non-zero. Hence, there is a need to modify the current reference.

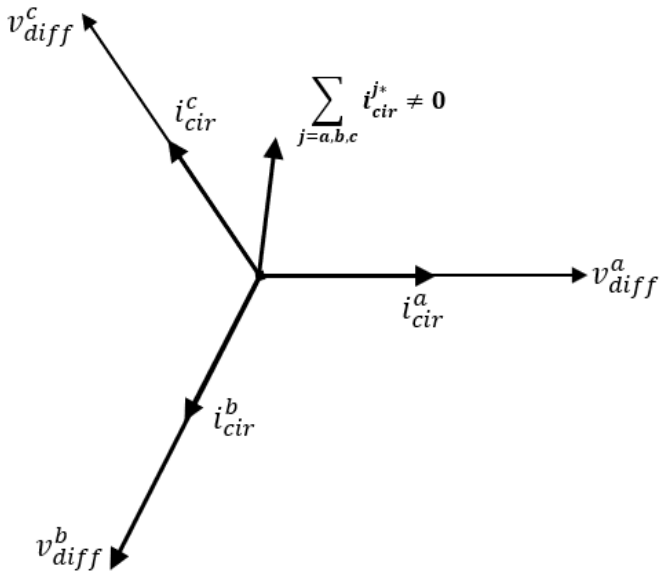


Fig.3. 4: Original AC circulating current vectors.

Fig. 3.5 shows the modified current reference, $i^{j*}_{cir\_ac}$, generated by the *PI* controller in (3.21). The AC phase angle θ is used by the PLL to align the projected current reference with the arm voltage, making sure that the output power is preserved. From this transformation, a zero-reference sum of the circulating current is obtained for the arm energy.

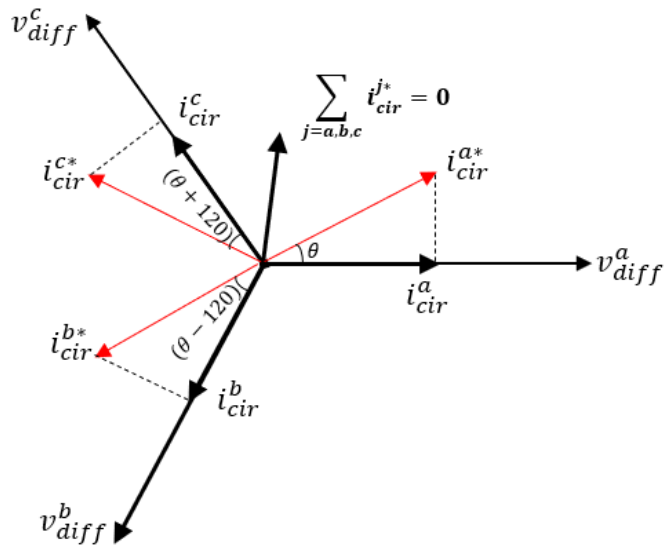


Fig.3. 5: AC circulating current vectors for arm-energy.

Also, from Fig. 3.5, the relationship between the original and the new current reference for the arm energy controller is obtained.

$$\begin{cases} i_{cir}^{a} = i_{cir}^{a*} Cos\theta \\ i_{cir}^{b} = i_{cir}^{b*} Cos(\theta - 120) \\ i_{cir}^{c} = i_{cir}^{c*} Cos(\theta + 120) \end{cases} \tag{3.24}$$

$$\begin{bmatrix} i_{cir}^{a} \\ i_{cir}^{b} \\ i_{cir}^{c} \end{bmatrix} = \begin{bmatrix} i_{cir}^{a*} Cos\theta \\ i_{cir}^{b*} Cos(\theta - 120) \\ i_{cir}^{c*} Cos(\theta + 120) \end{bmatrix} \tag{3.25}$$

Considering phase j for arm-energy balancing

$$\sum i_{cir}^{j} = \sum i_{cir}^{j*} \begin{bmatrix} Cos\theta \\ Cos(\theta - 120) \\ Cos(\theta + 120) \end{bmatrix} \tag{3.26}$$

The *PI* controller is compensated with a coupling matrix, A_1 to improve the gain effect needed to drive $\sum i_{cir}^{j*}$ to zero.

$$A_1 \times \sum i_{cir}^{j*} = 0 \tag{3.27}$$

$$A_1 = \begin{bmatrix} A_{aa} & A_{ab} & A_{ac} \\ A_{ba} & A_{bb} & A_{bc} \\ A_{ca} & A_{cb} & A_{cc} \end{bmatrix} \tag{3.28}$$

The elements of A_1 must have a constant variable along the diagonals, while the corresponding

rows and columns must have variables with similar absolute values.

$$A_1 = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{3.29}$$

Therefore,

$$\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} cos\theta & 0 & 0 \\ 0 & \cos(\theta - 120) & 0 \\ 0 & 0 & \cos(\theta + 120) \end{bmatrix} = 0 \tag{3.30}$$

The above compensation method is efficient for the arm energy controller. However, for leg energy balance, each leg is controlled independently, and the differential current sum ($i_{cir}^{a*} + i_{cir}^{b*} + i_{cir}^{c*}$) may not be zero. This might lead to AC grid current contamination with AC circulating current, resulting in three phase currents with unbalanced reference. Hence, each leg should be controlled individually to achieve energy balance.

Considering *leg a*, to balance its AC circulating current $i_{cir\_ac}^{a}$, the reference should be shifted by 180° from the original current using new current reference from the other two phases, $i_{cir\_ac}^{ba*}$ and $i_{cir\_ac}^{ca*}$ and a coupling matrix. Such that:

$$A_2 i_{cir\_ac}^{a*} + i_{cir\_ac}^{a} = 0 \tag{3.31}$$

where A_2, is a coupling matrix capable of removing the energy fluctuations introduced by the new current reference as analyzed below.

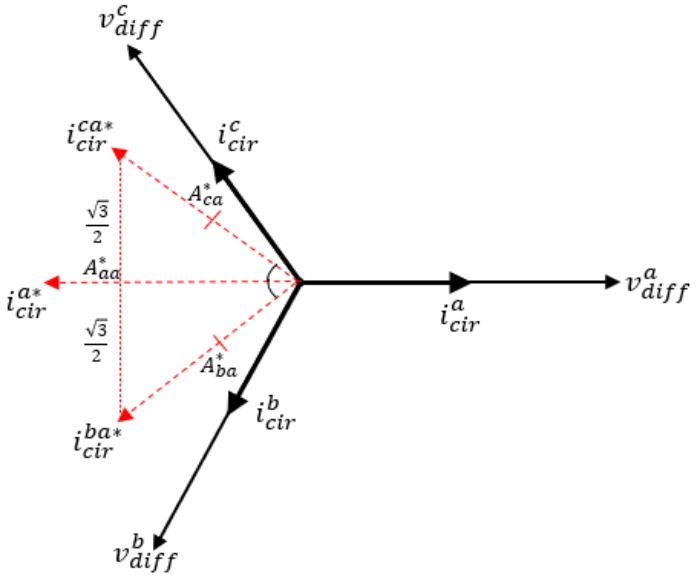


Fig.3. 6: AC circulating current vectors for leg energy balance.

Conditions:

$$A_{aa}^{*} = 1, \ \ |A_{ba}^{*}| = |A_{ca}^{*}| = \frac{1}{\sqrt{3}}$$

$$\begin{cases} i_{cir}^{aa*} = A_{aa}^{*} i_{cir}^{aa} \\ i_{cir}^{ba*} = A_{ba}^{*} i_{cir}^{ba} \\ i_{cir}^{ca*} = A_{ca}^{*} i_{cir}^{ca} \end{cases} \tag{3.32}$$

For $i_{cir}^{aa} = i_{cir}^{a}$, $i_{cir}^{ba} = i_{cir}^{b}$, $i_{cir}^{ca} = i_{cir}^{c}$

Considering *leg a*, and substituting (3.24) into (3.32)

$$\begin{cases} i_{cir}^{aa*} = A_{aa}^{*} i_{cir}^{a*} Cos\theta \\ i_{cir}^{ba*} = A_{ba}^{*} i_{cir}^{a*} Cos(\theta - 120) \\ i_{cir}^{ca*} = A_{ca}^{*} i_{cir}^{a*} Cos(\theta + 120) \end{cases} \tag{3.33}$$

The angle between b and c with reference to a can assume 90° phase shift.

$$i_{cir}^{aa*} = i_{cir}^{a*}[A_{aa}^{*} Cos\theta \quad A_{ba}^{*} Cos(\theta + 90) \quad A_{ca}^{*} Cos(\theta - 90)]$$

$$i_{cir}^{ba*} = i_{cir}^{a*}[A_{ba}^{*} Cos(\theta - 210) \quad A_{aa}^{*} Cos(\theta - 120) \quad A_{ca}^{*} Cos(\theta - 30)] \tag{3.34}$$

$$i_{cir}^{ca*} = i_{cir}^{a*}[A_{ca}^{*} Cos(\theta + 210) \quad A_{ba}^{*} Cos(\theta + 30) \quad A_{aa}^{*} Cos(\theta + 120)]$$

$$\begin{pmatrix} i_{cir}^{aa*} \\ i_{cir}^{ba*} \\ i_{cir}^{ca*} \end{pmatrix} = i_{cir}^{a*} \begin{matrix} Cos\theta & \frac{1}{\sqrt{3}} Cos(\theta + 90) & \frac{1}{\sqrt{3}} Cos(\theta - 90) \\ \frac{1}{\sqrt{3}} Cos(\theta - 210) & Cos\,(\theta - 120) & \frac{1}{\sqrt{3}} Cos(\theta - 30) \\ \frac{1}{\sqrt{3}} Cos(\theta + 210) & \frac{1}{\sqrt{3}} Cos(\theta + 30) & Cos\,(\theta + 120) \end{matrix} \tag{3.35}$$

$$\left(i_{cir}^{aa*} + i_{cir}^{ba*} + i_{cir}^{ca*}\right)$$

$$= i_{cir}^{a*}\left(Cos(0) + \frac{1}{\sqrt{3}} Cos(90) + \frac{1}{\sqrt{3}} Cos(-90) + \frac{1}{\sqrt{3}} Cos(-210)\right.$$

$$\left. + Cos(-120) + \frac{1}{\sqrt{3}} Cos(-30) + \frac{1}{\sqrt{3}} Cos(210) + \frac{1}{\sqrt{3}} Cos(30) + Cos(120)\right)$$

$$\left(i_{cir}^{aa*} + i_{cir}^{ba*} + i_{cir}^{ca*}\right) = 0 \tag{3.36}$$

Hence,

$$A_2 = \begin{bmatrix} Cos\theta & \frac{1}{\sqrt{3}}Cos(\theta+90) & \frac{1}{\sqrt{3}}Cos(\theta-90) \\ \frac{1}{\sqrt{3}}Cos(\theta-210) & Cos(\theta-120) & \frac{1}{\sqrt{3}}Cos(\theta-30) \\ \frac{1}{\sqrt{3}}Cos(\theta+210) & \frac{1}{\sqrt{3}}Cos(\theta+30) & Cos(\theta+120) \end{bmatrix} \quad (3.37)$$

The same approach is used to balance the AC circulating current reference for *leg b* and *leg c*. Therefore, the sum of the opposing currents for each leg is zero, as shown in (3.38).

$$i_{cir\_ac}^{a*} + i_{cir\_ac}^{b*} + i_{cir\_ac}^{c*} = 0 \quad (3.38)$$

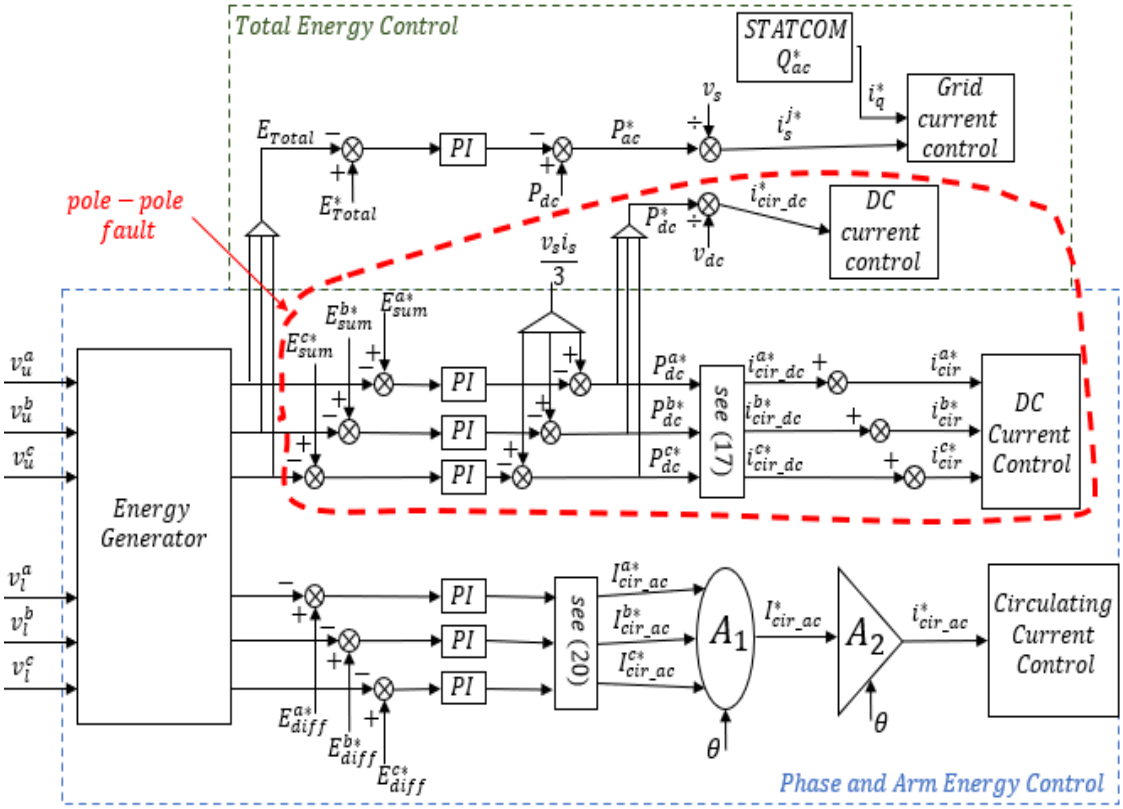


Fig.3. 7: Proposed energy-based control

For this study, to achieve FRT, the energy in the converter should be balanced and the converter must continue to operate during the fault. This is feasible by applying the above energy-based control methodology in (3.38) and in Fig. 3.7 into the proposed fault tolerant converter discussed in the next section.

3.5 PROPOSED CONVERTER TOPOLOGY

The proposed hybrid-arm topology under DC fault is shown in Fig. 3.8. It comprises two independently controlled monopolar MMC that are symmetrically separated into positive terminal,

ground, and negative terminal. Each monopole of the MMC consist of the HBSM arm which is connected to the ground and the SCSM arm attached to both the positive and negative terminals. Both arms of the HBSMs and SCSMs are separated by arm inductor, L_o, which is used to suppress the harmonics content of the circulating current. Although the HBSMs do not possess any DC-FRT capability, they provide the lowest cost, highest efficiency, and least number of components. The SCSMs on the other hand, provide the DC-FRT. In this way, the proposed hybrid-arm design can offer DC-FRT capability at reduced cost and power loss compared to the other SM topologies. In addition, it exhibits low switching losses.

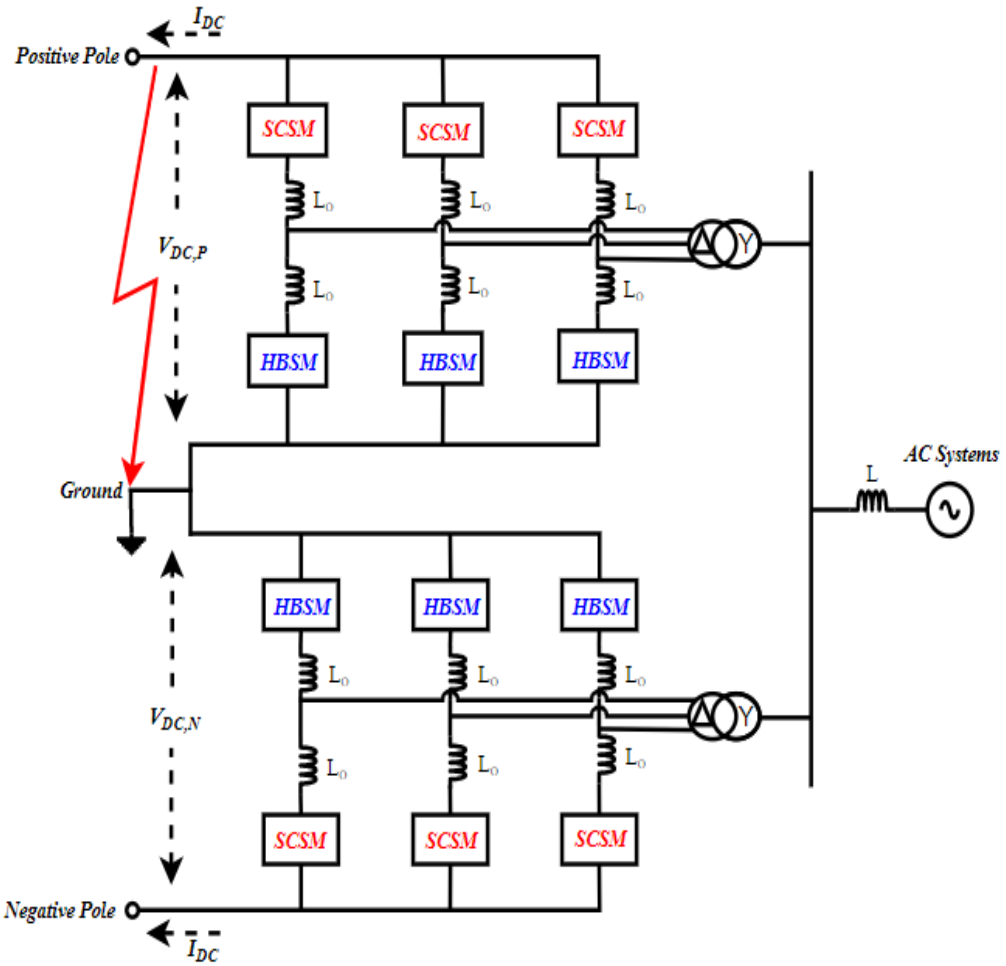


Fig.3. 8: Circuit topology of the proposed Hybrid-Arm.

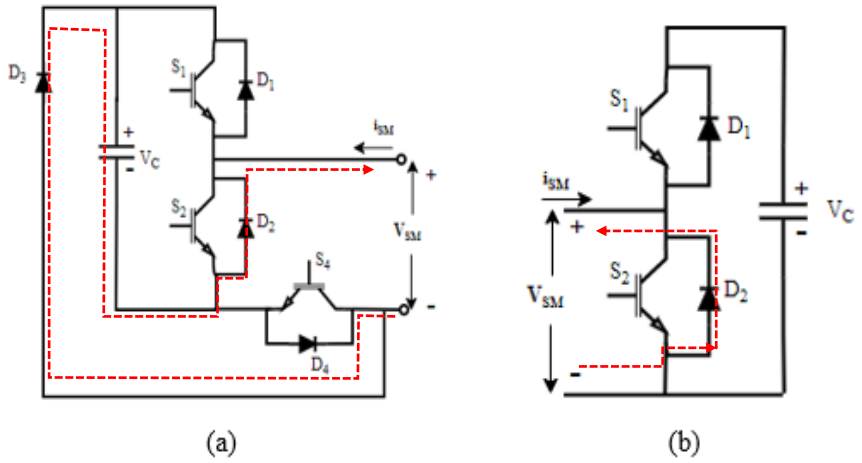


Fig.3. 9: (a) SCSM circuit topology (b) HBSM circuit topology.

The switching state of the hybrid-arm topology is shown in Tables 3.1 and 3.2, where the converter IGBTs can either be inserted, blocked, or bypassed depending on the operation mode of the converter. Before the occurrence of the DC fault, the SCSMs exhibits the features of a typical HBSMs by inserting switch S4, as shown in Fig. 3.9. As such, the overall hybrid-arm generates an output voltage of $0\ or\ V_c$. However, during DC short-circuit when the DC link current exceeds the converter threshold and the switches are blocked, the SCSMs generate $-V_c$ to eliminate the fault. Further explanation of the working methodology of the proposed hybrid-arm converter is provided in the next section.

Table 3. 1: HBSM switching modes

	HBSM				
Switching mode	S_1	S_2	I_{SM}	V_C	V_{SM}
Blocking	0	0	>0	↑	V_C
	0	0	<0	–	0
Bypassing	0	1	>0	–	0
	0	1	<0	–	0
Inserting	1	0	>0	↑	V_C
	1	0	<0	↑	V_C

Table 3. 2: SCSM switching modes

	SCSM					
Switching mode	S_1	S_2	S_4	I_{SM}	V_C	V_{SM}
Blocking	0	0	0	>0	↑	V_C
	0	0	0	<0	↓	$-V_C$
Bypassing	0	1	1	>0	–	0
	0	1	1	<0	–	0

Inserting	1	0	1	> 0	↑	V_C
	1	0	1	< 0	↑	V_C

3.6 OPERATION PRINCIPLE OF THE PROPOSED MMC

This section describes the principles of operation and control methodology of the proposed MMC during normal mode and fault mode. Since the proposed hybrid-arm converter is divided into positive and negative symmetrical MMC, the same principle of operation applies to both sections of the converter. As a result, only the positive part of the MMC is discussed.

3.6.1 NORMAL OPERATION MODE

Considering the positive MMC, during normal operation, the SCSMs exhibit the features of a typical HBSM as explained in the previous section. As a result, they both generate a constant DC voltage, V_{dc}. The system parameters and control variables of the MMC are described using Fig. 3.10.

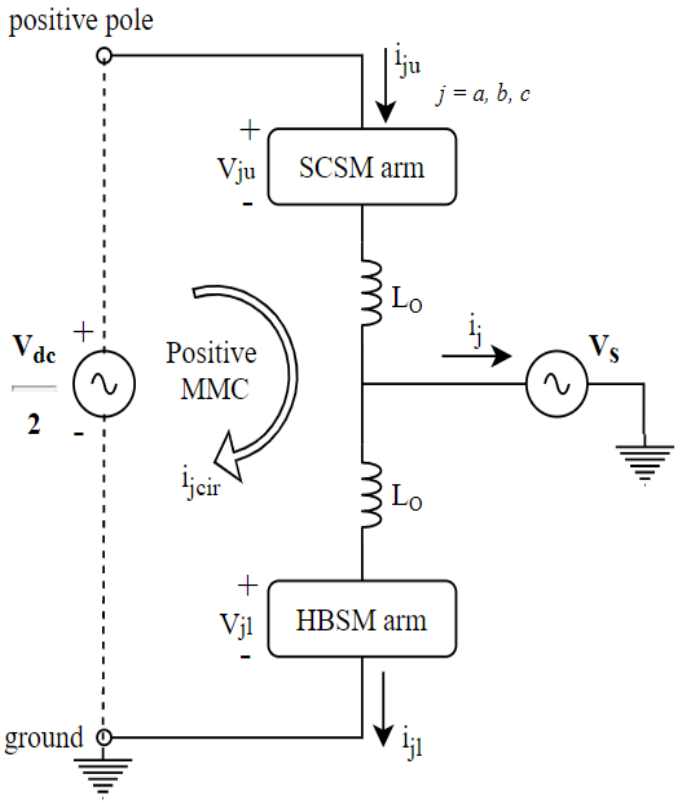


Fig.3. 8: Positive MMC normal mode of operation.

From Fig. 3.10, the expressions for the upper and lower arm currents (i_{ju}) and (i_{jl}) are shown in (3.39) and (3.40) using the Kirchhoff principle.

$$i_{ju}(t) = \frac{i_j(t)}{2} + i_{jcir}(t) \tag{3.39}$$

$$i_{jl}(t) = \frac{-i_j(t)}{2} + i_{jcir}(t) \tag{3.40}$$

where, i_{jcir} is the circulating current and i_j is the AC current of phase j. To obtain the upper arm voltage, V_{ju}, and lower arm voltage, V_{jl}, of the positive MMC in (3.41) and (3.42), the same principle used in Section 3.2.1 is applied.

$$V_{ju}(t) = \frac{V_{dc}}{2} - V_s(t) - \frac{L_o di_{ju}(t)}{dt} \tag{3.41}$$

$$V_{jl}(t) = \frac{V_{dc}}{2} + V_s(t) - \frac{L_o di_{jl}(t)}{dt} \tag{3.42}$$

where, V_s is the instantaneous AC voltage of phase j that supports the AC side current.

To generate the inner dynamics variables of the MMC during normal mode, (3.41) and (3.42) are added to obtain (3.43).

$$\frac{L_o di_{jcir}(t)}{dt} = \frac{1}{2}V_{dc} - V_{jsum}(t) \tag{3.43}$$

$$V_{jsum}(t) = \frac{1}{2}\left(V_{jl}(t) + V_{ju}(t)\right) \tag{3.44}$$

where, the sum of the voltages driving the circulating current in the hybrid-arm is given as V_{sum} and it is regulated by the inner level control in Fig. 3.2.

To regulate the outer dynamics under normal mode, the energies stored in the upper and lower arms of the hybrid-arm converter is controlled by applying the energy control method discussed in Section 3.3. Since the energy balancing techniques using common-mode voltage for FBSM in [148] is very complex with numerous dq-abc transformations. Where the arm energy sum, E_{sum}, is obtained from the power generated in charging the capacitors in the upper and lower arms of the MMC SMs in (3.14) and (3.15). Hence, total energy balance in the hybrid-arm is linked to the

circulating current, i_{jcir}, in (3.17) and for normal operation, only the DC component of i_{jcir} is used to regulate the total arm energy.

Finally, a modulation technique is needed to generate the gating signals m_{ju} and m_{jl} in Fig. 3.2, to control the number of SMs that are inserted or bypassed. Since the SCSMs are working as HBSMs, the same Nearest Level Modulation (NLM) technique used for HBSMs in [149] is applied to the hybrid-arm MMC.

3.6.2 FAULT OPERATION MODE

In this section, the impact of a DC fault on the operation of the hybrid-arm converter is analysed.

Considering the hybrid-arm converter, DC faults can be classified as single pole-ground, double pole-ground, and pole-pole fault. A single pole-ground fault occurs on either the positive or negative pole to ground, as shown in Fig. 3.11. Similarly, a double pole-ground fault occurs on both the positive pole and the negative pole to ground. During this fault, both the positive and negative MMC are short-circuited, and the transfer of active power is truncated until the converter clears the fault. In a pole-pole fault, the positive pole and the negative pole of the MMC are faulty, and the DC voltage in each pole drops to almost zero, with similar effects as the double pole to ground fault.

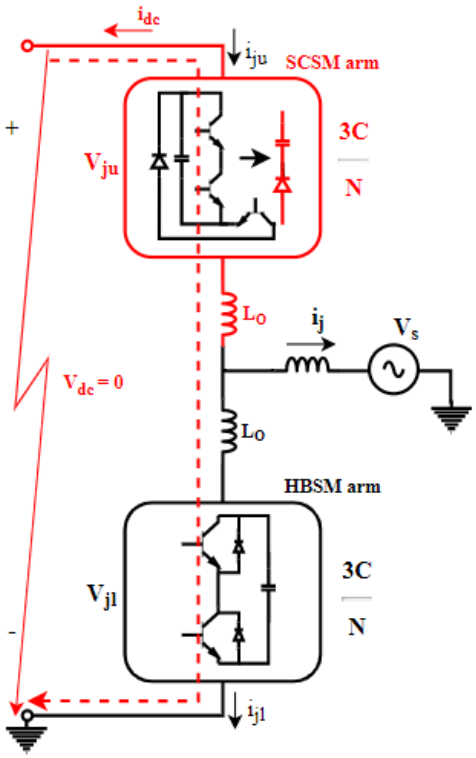


Fig.3. 9: positive hybrid-arm in fault mode.

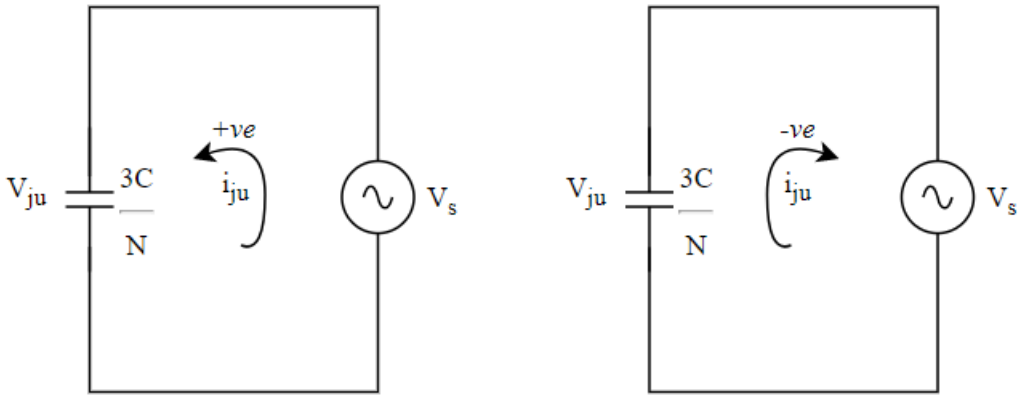
For this Chapter, only positive MMC is considered since the MMC topology exists in a symmetrical monopole configuration. Thus, all the different fault types have a similar principle of operation [150].

From Table. 3.2, when a pole-pole fault is detected, all the IGBTs of the SCSMs in the upper arm are blocked, and the converter generates negative DC voltage from its N-series of inserted capacitors to block the fault current. In addition, the direction of the SCSM diodes is reversed to prevent the flow of i_{ju} as shown in Fig. 3.11. While the SCSMs eliminate the DC fault, the HBSM generates reactive power to support the grid until normal operation resumes. The mechanism of operation of the SCSMs and HBSMs is illustrated mathematically:

Considering the SCSMs arm, (3.41) becomes (3.45). Since V_{dc} = 0

$$V_{ju}(t) = -V_s(t) - \frac{L_o di_{ju}(t)}{dt} \tag{3.45}$$

$$\frac{L_o di_{ju}(t)}{dt} = -\left[V_{ju}(t) + V_s(t)\right] \tag{3.46}$$



In (3.46) and considering the circuit diagram above, when $i_{ju} > 0$, the SCSM diodes are still conducting, and the SCSM's capacitors are charged. However, as i_{ju} turns negative, the upper arm diodes are reversed, and thus the capacitors discharge to produce the current, i_{dc} in (3.47) needed to block and decay the fault current [151].

$$i_{dc} = \frac{3C}{N}\frac{dV_{ju}(t)}{dt} \tag{3.47}$$

As the arms of the SCSMs eliminate the fault current, the arms of the HBSMs exist as a star connected STATCOM to support the grid [152]. To generate the expression for STATCOM mode, (3.42) is changed to (3.48). Also, $V_{dc} = 0$.

$$\frac{L_o di_{jl}(t)}{dt} = V_s(t) - V_{jl}(t) \tag{3.48}$$

Transforming (3.48) from a, b, c coordinates to dq coordinates, the STATCOM expression in (3.49) is generated.

$$\begin{cases} \frac{L_o di_{dl}(t)}{dt} = \omega L_o i_q(t) + V_s^d(t) - V_{dl}(t) \\ \frac{L_o di_{ql}(t)}{dt} = -\omega L_o i_d(t) + V_s^q(t) - V_{ql}(t) \end{cases} \tag{3.49}$$

where i_d is regulated to its reference value i_d^* to keep the average capacitor voltage in the hybrid-arm close to its nominal value during STATCOM operation. This is done through the voltage and power controllers in Fig. 3.2. Also, the value of i_q is regulated to reference value i_q^* by the reactive power controller to regulate the reactive power supplied to the grid.

To balance the energy difference in the converter during fault mode, the differential energy balance in (3.20) is applied with a balanced circulating current reference using (3.38).

Finally, during the fault mode, since the SCSMs can generate negative voltage like the FBSMs, the sorting algorithm modulation technique for FBSMs in [153] is applied to control the blocked SMs and capacitor voltages in the SCSMs. Therefore, the overall control system integrates a combination of NLM modulation techniques for normal operation mode and a sorting algorithm for fault mode as discussed in [154]. Fig. 3.7 presents the entire control system for the hybrid-arm converter.

3.7 DC-FRT MECHANISM

A DC fault is detrimental to power supply reliability and can shut down HVDC network. Therefore, it is necessary to sustain the network to support fault recovery. For this chapter, to achieve FRT, the energy in the converter should be balanced and the converter must continue operation. This is feasible by applying the energy-based control scheme in Fig. 3.7 on the proposed hybrid-arm converter to regulate the bipolar voltages to cause the short circuit current to decay to zero. Thus, the DC-FRT mechanism of the converter is explained based on the internal operation of the control methodology and the visible operation by the converter.

For the control methodology: During fault, the DC voltage is reduced to zero and i_{cir_dc} is zero, as indicated by the red dashed lines in Fig. 3.7. To balance the converter's energy, the circulating current, i_{cir_ac}, reference must be balanced using (3.38) to prevent it from feeding the DC fault with harmonics. While the energy difference within the leg and arm of the converter is balanced, negative voltage with magnitude greater than the grid voltage is used to produce i_s^j in opposite direction to the grid current. This current flows through the antiparallel diode towards the grid side to regulate the AC current feeding the network and the fault. As a result, the fault tarnishes. Also, the AC load is compensated with reactive power using the i_q^* component discussed in Section 3.8.

For the converter operation: The fault ride-through capability in Fig. 3.12 is integrated. During this fault mode, the SCSMs are blocked and generate reverse voltage to clear the fault. If the SCSMs clear the fault when the time to achieve fault ride-through, T_{DC-FRT}, is within 5 s, normal operation resumes, and the hybrid-arm continues to transfer active power. However, if the SCSMs fail to clear the fault within 5 s, the HBSMs switch to STATCOM mode to supply reactive power to support the grid for 120 s, while the SCSMs continue to clear the fault.

Once the converter eliminates the fault within 120 s, the hybrid-arm converter switches to the recovery mode. In this mode, the fault current decays completely to zero and the converter rebuilds the DC current. The STATCOM operation stops as the HBSMs resume normal operation by generating active power while the SCSMs switch to a conducting state and the entire hybrid-arm returns to a steady state.

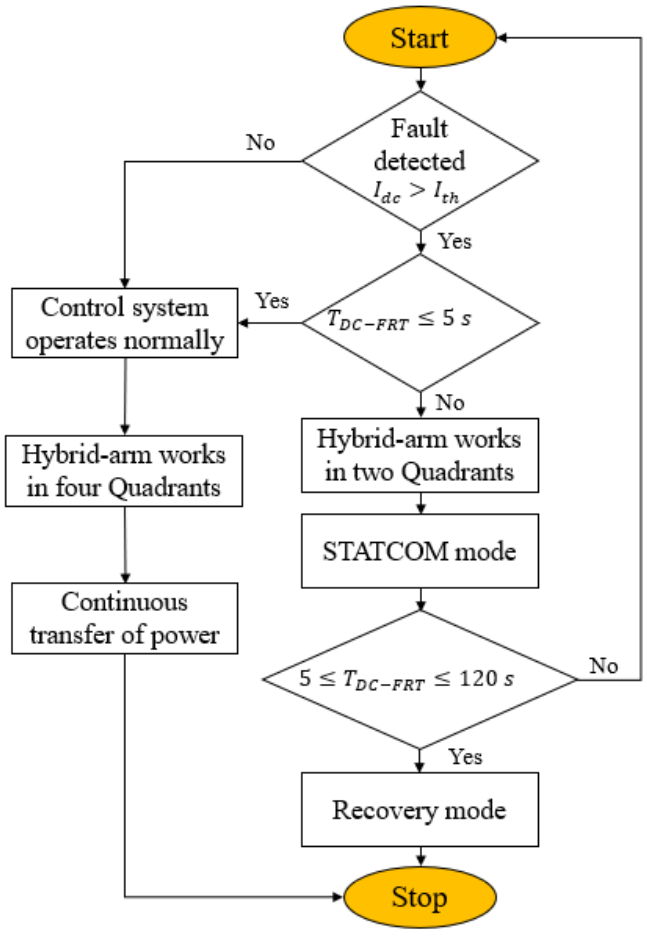


Fig.3. 10: DC-FRT scheme of the proposed hybrid-arm converter.

Hence, for this Chapter, it is assumed that the fault is a non-permanent fault and thus should be cleared within 120 s. However, for a permanent fault, the HBSMs are unable to continuously supply reactive power for a long period of time, and as such, a backup DC-FRT technique is integrated in this thesis to localise and isolate the fault [155].

3.8 STATCOM

During the fault, the converter switches from the normal mode of operation to the STATCOM mode. In this mode, the Q_{ac} controller in Fig 3.7 regulates the amount of reactive power supplied by injecting i_q^* into the AC grid to improve real power transmitted to the load by i_s^* as shown in Fig. 3.13 and to minimize the harmful effect of the fault. The energy of the converter needs to be balanced and the converter station connected to the AC grid to ensure satisfactory STATCOM operation and a quick recovery of the grid to normal operation mode after fault clearance. The expression for the grid current during STATCOM operation is shown in (3.50).

$$I_{grid}^2 = (i_s^*)^2 + \left(i_q^*\right)^2 \tag{3.50}$$

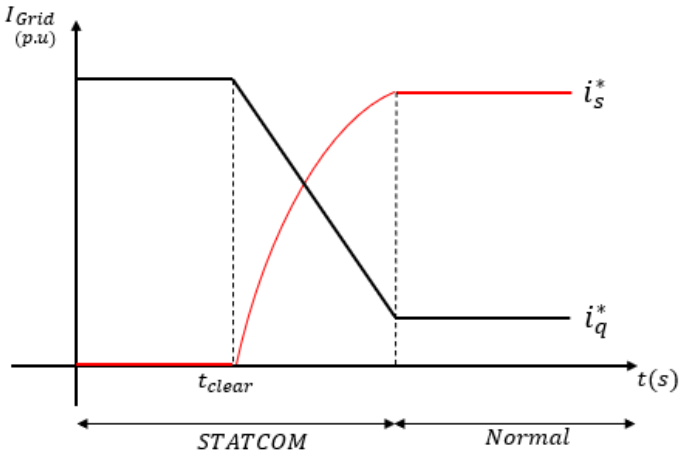


Fig.3. 11: STATCOM and Normal mode of operation

3.9 SIMULATION AND RESULTS

In this section, the simulation results of the proposed MMC are presented to verify DC-FRT mechanism using the system parameters in Table 3.3. A bipolar DC voltage of 100 kV is generated by the 24 SMs hybrid-arm fault tolerant converter in Fig. 3.14. The results of the AC circulating current and its impact on DC current are shown in Section 3.9.1. The impact of the control strategy on the proposed topology during STATCOM operation and DC-FRT while making sure energy is balanced is discussed below. In addition, the performance of the converter is verified for when T_{DC-FRT} is less than 5 s and when T_{DC-FRT} exceeds 5 s. See Table A.1 in Appendix for the control parameters.

Table 3. 3: System parameters for designed simulation

System Parameters	Values
AC nominal voltage	120 kV, 50 Hz
Rated DC link voltage, V_{dc}	$\pm$100 kV
Nominal power of the MMC	20 MW
SM capacitance	15 mF
Number of MMC SMs	24
Arm inductance	4.7 mH
Number of SMs per arm	6 HBSMs + 6 SCSMs
Transformer voltage ratings	120 kV/86 kV
Switching frequency	20 kHz
Carrier frequency	2 kHz
Transformer reactance	0.12 pu
Phase Impedance	0.2 pu

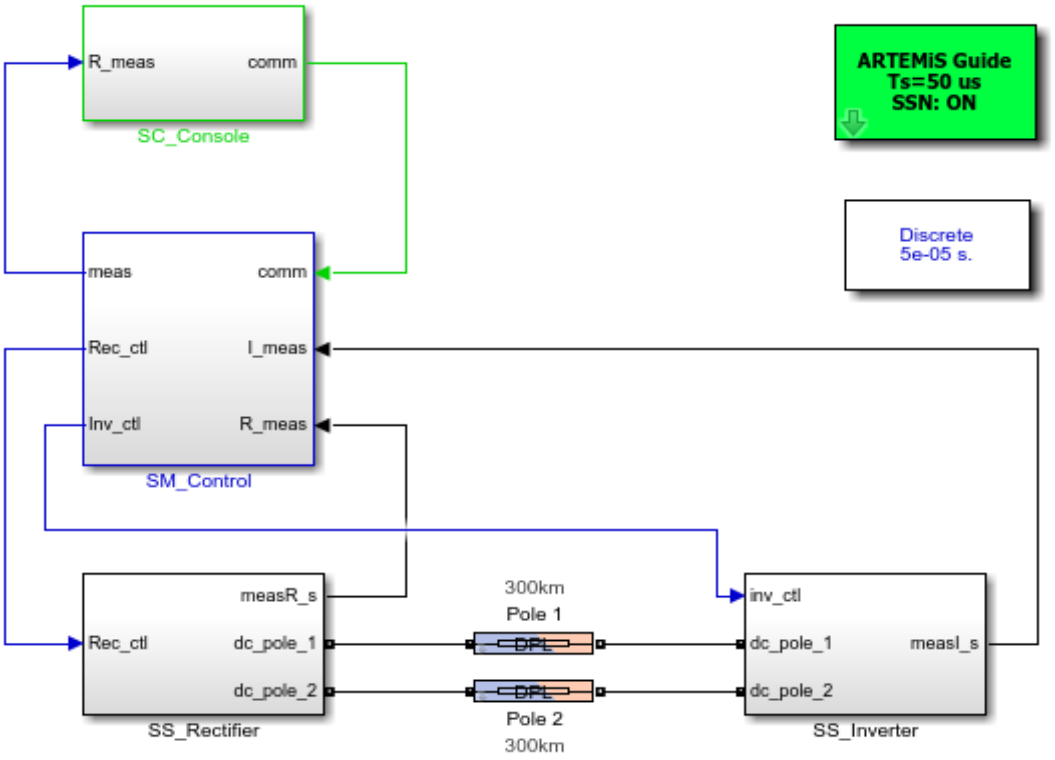


Fig.3. 12: MMC-HVDC system under test

For clarity, the analysis of the results is divided into two sections: The first section describes the impact of applying the control methodology on the proposed converter while the second section explains the two stages of the DC-FRT mechanism.

3.9.1 IMPACT OF THE CONTROL METHODOLOGY ON THE PROPOSED MMC

During fault, the AC circulating current is used to balance the SM energy only if its AC circulating reference is zero, so that it does not flow to feed the DC fault and induce undesirable oscillations on the DC current as explained in Section 3.4. Considering a fault impact at 0.5 sec, the conventional control strategy was implemented with unbalanced AC circulating reference. Fig. 3.15 (a) shows that the current was distorted with irregular magnitude, since there is no balance either among the arms or legs as the different phases possess different current magnitude. This is also evident in Fig. 3.16 (a), where a large oscillation is noticed in the DC current. As a result of this distortion, the coupling matrix A_1 in (3.28) is used to balance the circulating current as shown in Fig. 3.15 (b). It was seen that the top and bottom of the waveform is balanced with the same amplitude; although, there are series of rise and fall in the magnitude of the circulating current as

observed during the fault duration. This is an indication that the approach fails to achieve individual leg balance. The effect of this failure on DC current is shown in Fig. 3.16 (b), where oscillations can still be seen during the fault.

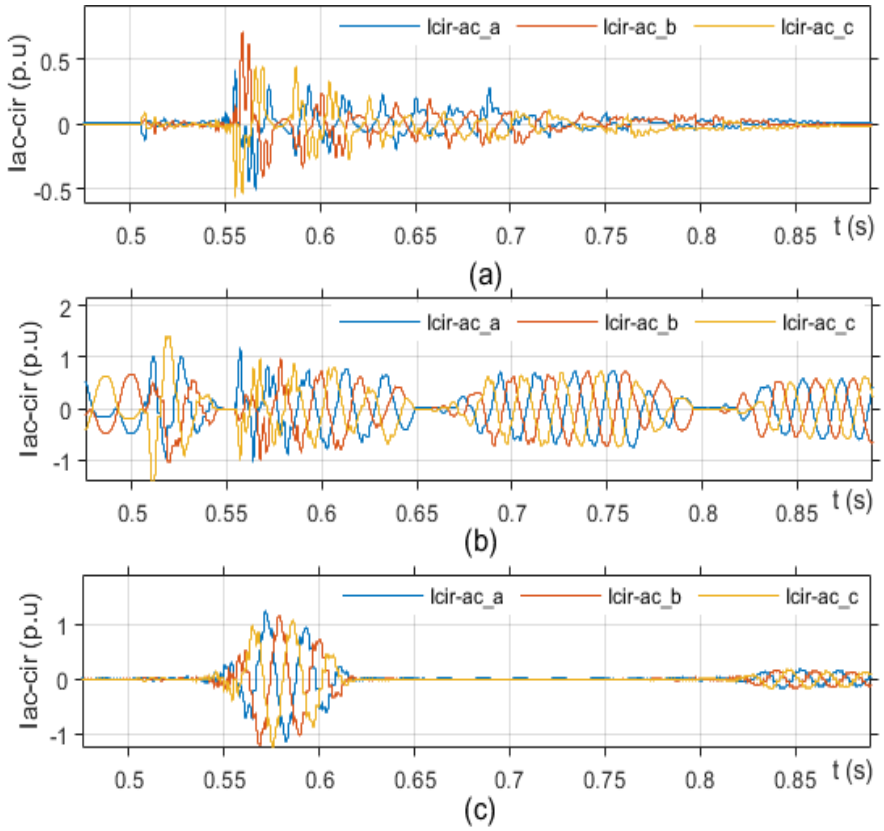


Fig.3. 13: Result of AC circulating current during fault (a) with unbalanced AC circulating reference (b) with coupling matrix A_1 (c) with coupling matrix A_2.

On integrating the coupling matrix A_2, Fig. 3.15 (c) was obtained. It was shown that the AC circulating current in the individual leg is balanced and properly tracked. The effect is also seen in Fig. 3.16 (c), where there is little or no oscillation in the DC current during the fault. This is because the AC circulating current reference has been reduced to zero and the current is balanced and able to regulate the internal energy of the converter.

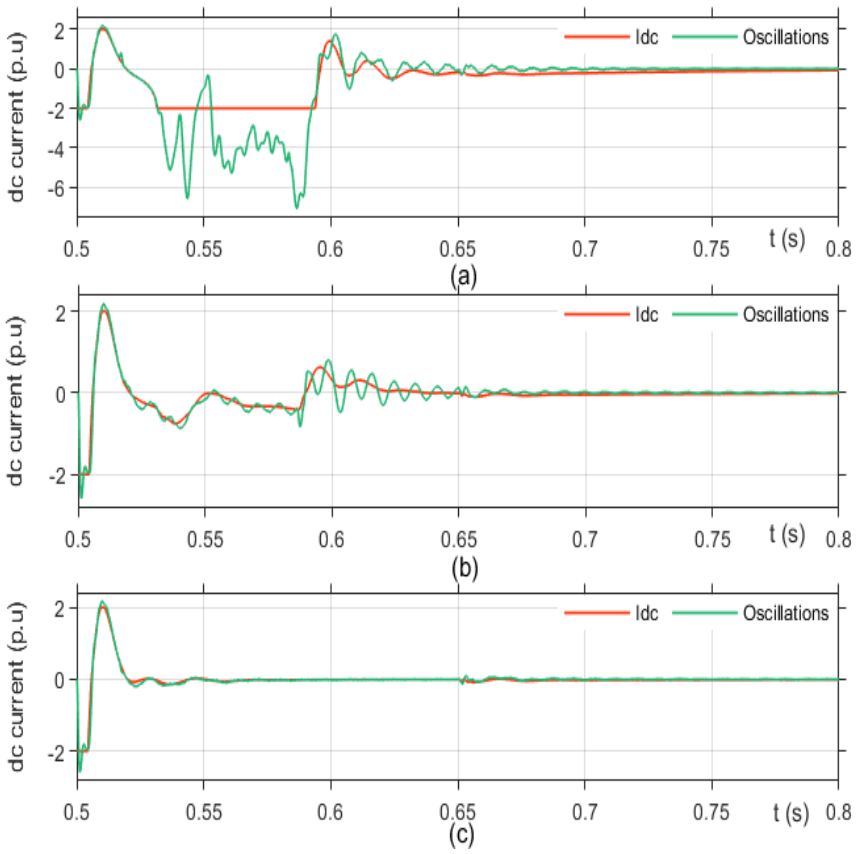


Fig.3. 14: Result of DC current disturbance during fault (a) with unbalanced AC circulating reference (b) with coupling matrix A_1 (c) with coupling matrix A_2.

Further verification of the impact of balancing the AC circulating current is seen in the arm and leg energy balance as shown in Fig. 3.17 and Fig. 3.18. During the fault, the conventional strategy was used as shown in Fig. 3.17 (a), and it was observed that the converter energy diverged in each phase of the converter arm. However, on integrating coupling matrix A_1, the energy controller was able to converge the arm-energy to a common value as shown in Fig. 3.17 (b). This is an indication that the arm-energy is balanced. Despite the contribution of A_1 to balancing the arm-energy, it fails to achieve individual leg energy balance as seen in Fig. 3.18 (a).

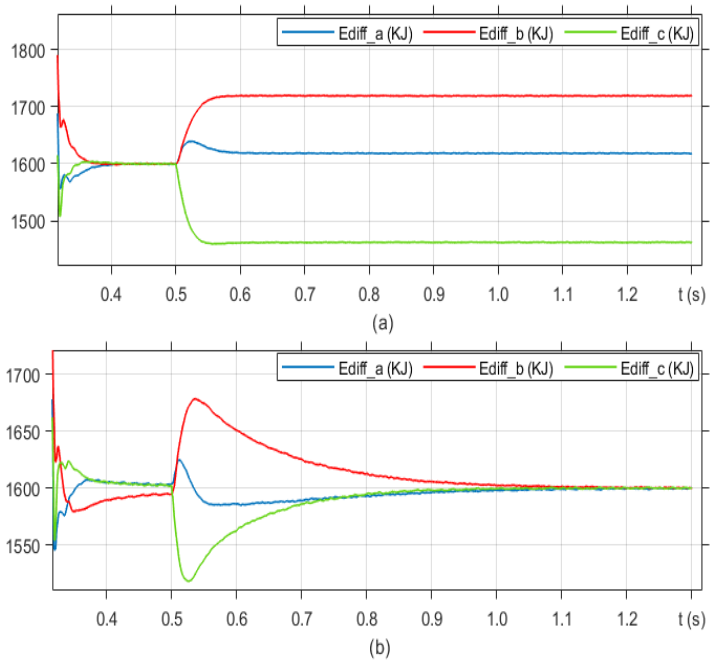


Fig.3. 15: Simulation result for arm-energy balance (a) with conventional strategy (b) with coupling matrix A_1

Fig. 3.18 (b) shows the impact of using coupling matrix A_2 to achieve leg energy balance. It can be seen that the overall energy in each leg is properly matched for phase a, phase b and phase c. Therefore, A_1 can achieve arm-energy balance while A_2 ensures leg-energy balance. Hence, with balanced internal energy, the negative impact of oscillations on DC current is ameliorated and the converter can support DC-FRT as discussed below.

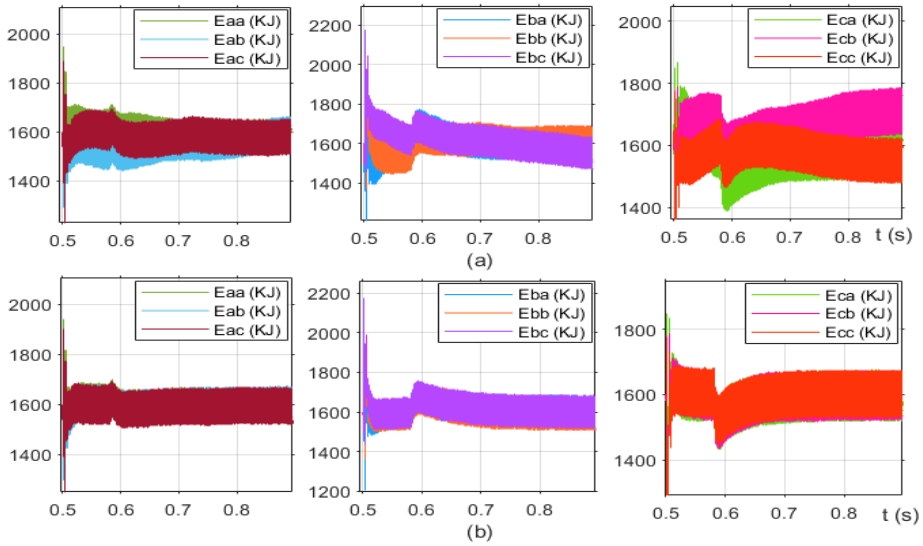


Fig.3. 16: Simulation result for leg energy balance (a) with coupling matrix A_1 (b) with coupling matrix A_2

Another benefit of the proposed algorithm is the injection of reactive power to support the grid as active power drops during fault. From Fig. 3.19, the pole-to-pole fault occurred at 0.5 sec and the converter switched to STATCOM mode soon after the fault, as previously described in Fig. 3.19. The STATCOM mode ends at the point the converter resumes normal operation. Hence, Fig. 3.20 depicts the AC current and voltage of the converter, and it shows that the converter was able to ride through the DC fault as normal operation resumed after 0.5 sec of the fault impact. Therefore, a balanced AC circulating current promotes DC-FRT by reducing the feeding of the DC fault current with harmonics. Also, with balanced internal energy, the STATCOM mode of operation can support fault recovery. See Table A.2 in the Appendix for a comparative analysis of the control schemes.

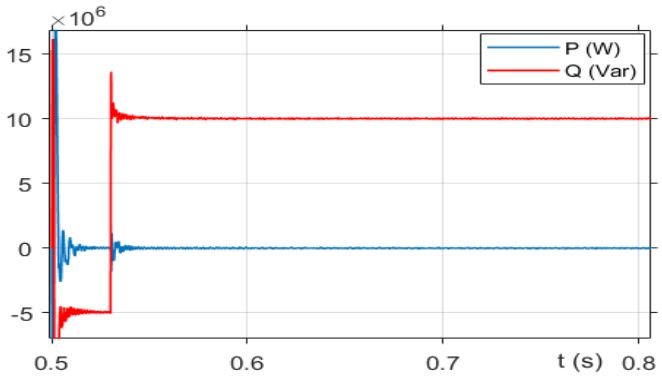


Fig.3. 17: STATCOM mode and DC-FRT

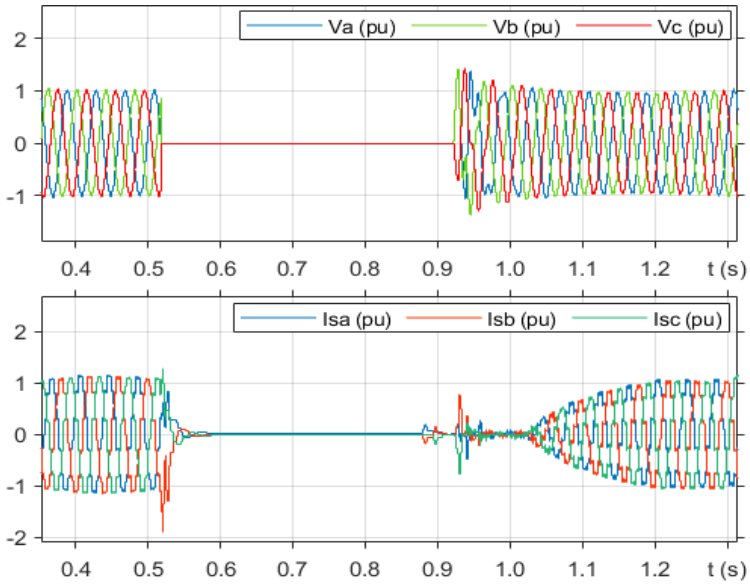
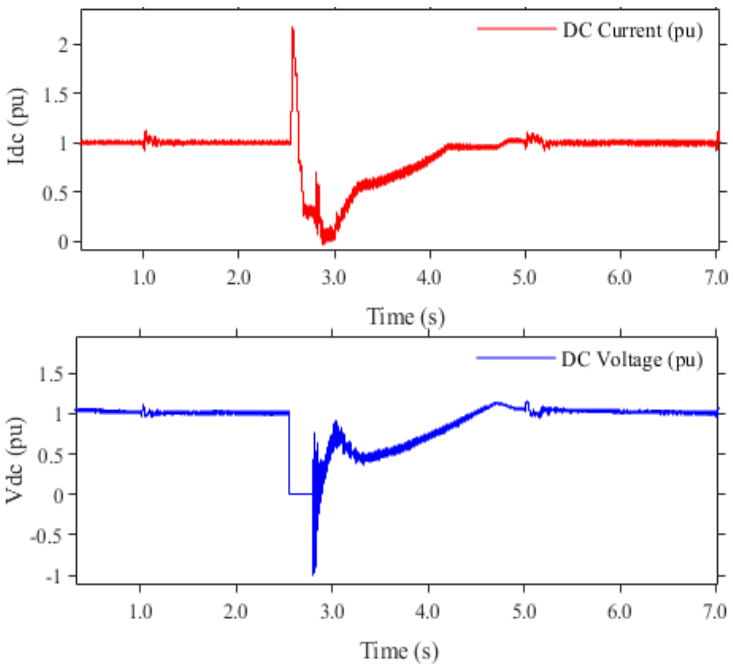


Fig.3. 18: Grid voltage and current during and after fault

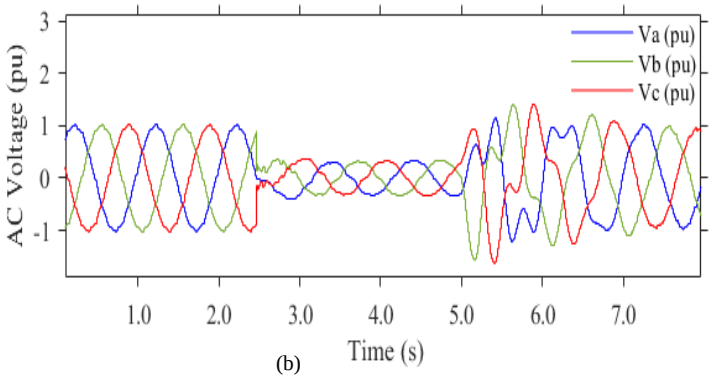
3.9.2 STAGES OF THE DC-FRT CAPABILITY BY THE PROPOSED MMC

Considering the first stage of the DC-FRT, a DC fault with a fault resistance of 10 Ω is detected at 2.5 s. The fault lasted for 2.5 s before it was cleared to resume normal operations. Fig. 3.21 shows the result of the first stage. Where Fig. 3.21(a) depicts the effects of the fault on the DC current and voltage. The voltage drops due to the fault while the current rises above the threshold (twice the current magnitude). Also, the effect of the fault on the AC voltage is shown in Fig. 3.21(b), where the voltage drops to almost half of its rated value.

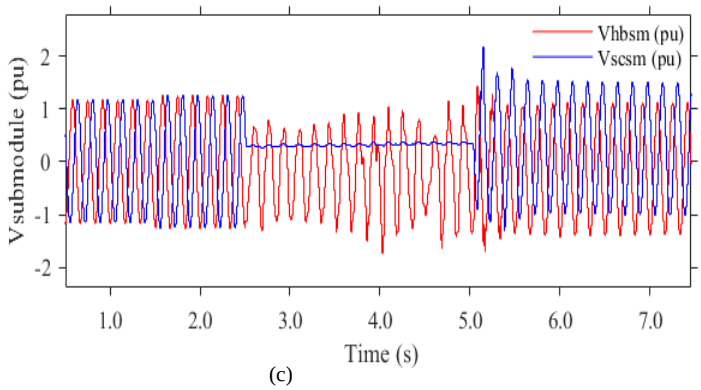
Furthermore, while the HBSMs continue to conduct, as shown by the submodule arm current and voltage in Figs. 3.21(c) and (d), the SCSMs' arm current and voltage remain constant because their IGBTs are blocked to clear the fault. Also, since the fault is cleared within 5 s which agrees with the DC-FRT mechanism described in Section IV, Fig. 3.21(e) demonstrates that the converter can sustain the fault period without the HBSM generating reactive power to keep the grid running. This is evident as the reactive power remains constant despite the presence of the fault. These results verify the effectiveness of the proposed hybrid-arm converter in clearing DC faults and resuming normal operations for fault disturbances with a shorter duration.



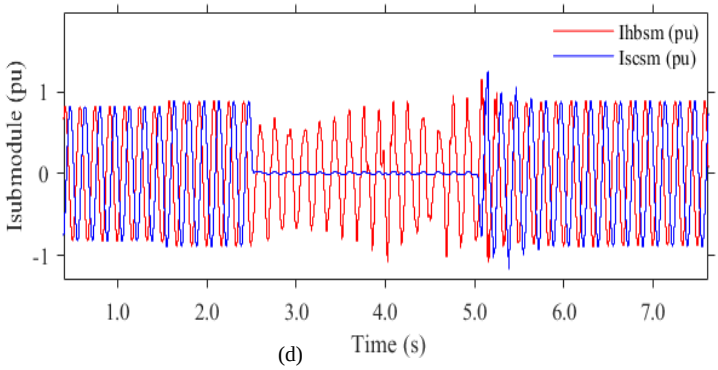
(a)



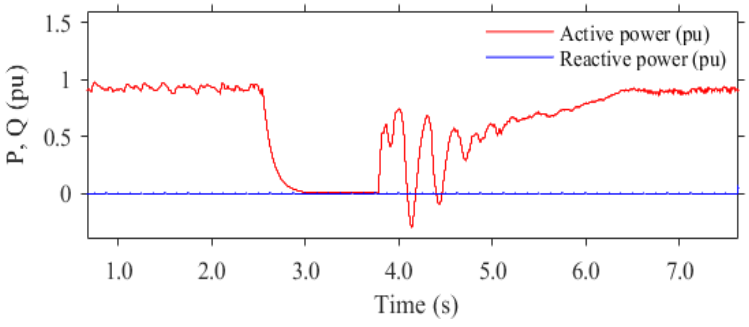
(b)



(c)



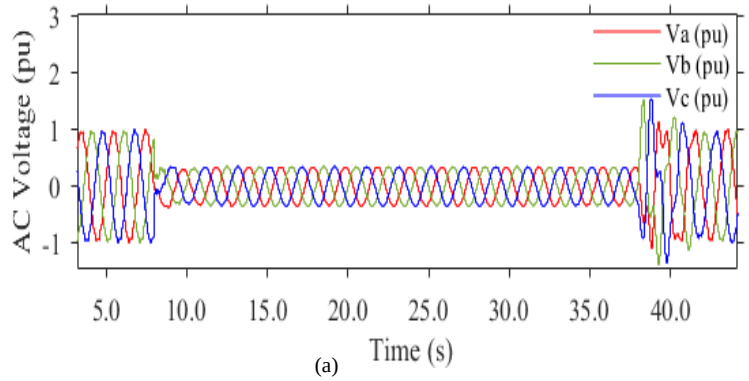
(d)



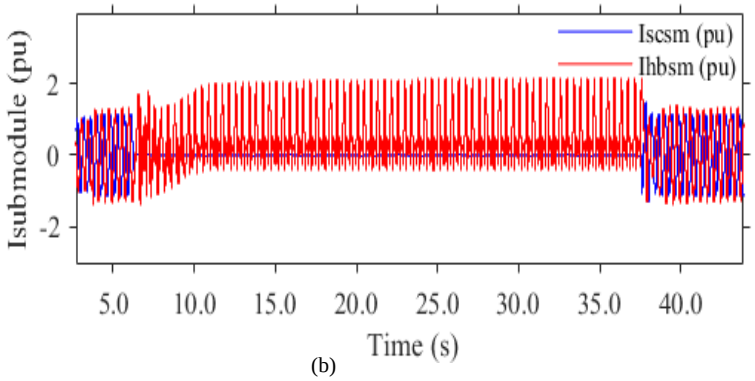
(e)

Fig.3. 19: Display results of first stage: (a) DC current and voltage, (b) AC voltage, (c) Submodule arm voltage, (d) Submodule arm current, (e) Active and reactive power of the hybrid-arm positive MMC.

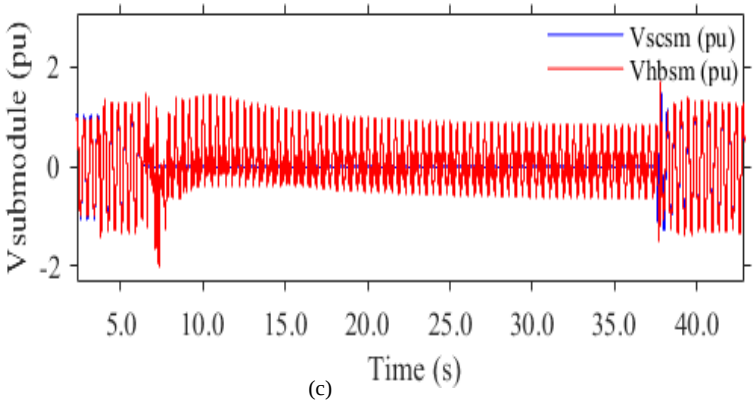
For the second stage, the parameters in Table 4.3 are also implemented. However, the DC fault occurred at 7.5 s and lasted for 30 s before it is cleared. Since the fault period exceeds 5 s in Fig. 3.22, the SCSMs clears the fault while the HBSMs switches to STATCOM mode to support the AC grid with reactive power. Fig. 3.22(a) shows the drop in AC voltage during the fault period, while Figs. 3.22(b) and (c) show that the SCSM current and voltage remain constant as the HBSM current and voltage experience a little fluctuation while they support the load with reactive power, in Fig. 3.22(d). Finally, as normal operation resumes through active power generation, the reactive power drops back to zero to verify the recovery mode.



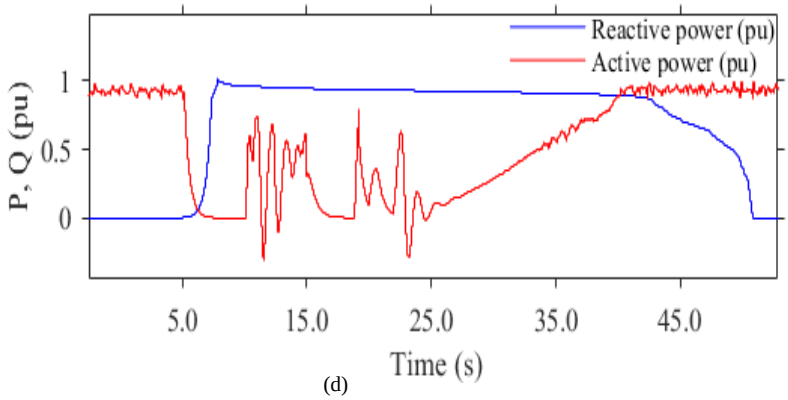
(a)



(b)



(c)



(d)

Fig.3. 20: Display results of second stage: (a) AC voltage, (b) Submodule arm current, (c) Submodule arm voltage, (d) Active and reactive power of the hybrid-arm positive MMC.

3.10 COMPARATIVE ANALYSIS OF MMC CONVERTERS

This section presents a comparison among eight different MMC topologies based on the number of power electronic devices, power losses, DC-FRT capability, and the ability to provide reactive power compensation (STATCOM) when clearing faults, as shown in Table 3.4, using the same parameters highlighted in Table 3.3. The HVDC link voltage, V_{dc}, is applied to all the MMCs and the number of SMs in each arm of the MMCs is given in terms of N, where N is taken as 20. In view of the number of devices per arm of the MMCs, the FBSM has the highest number of IGBTs and diodes per arm, followed by the hybrid combination of HBSM and FBSM. This accounts for the 50% and 29% reduction in size when compared with the proposed hybrid-arm topology. However, the number of IGBTs and diodes of HBSM, CDSM, 3LCCSM, 5LCCSM, and hybrid of HBSM and CDSM is the same as the proposed topology. Considering these topologies, 3LCCSM and CDSM-based topologies have the highest number of extra IGBTs and diodes. Based on this, the HBSM is the least complex, followed by the proposed hybrid-arm topology. Also, since the additional IGBTs are pathways for continuous conduction of arm current, topologies with higher switching devices often encounter more power losses. The estimated power losses for all the topologies are calculated as a percentage of active power transferred using IGBT module FF300R17KE4 in [156], where the HBSM and the proposed topology offers the most reduced power losses. Thus, in terms of complexity and losses, both topologies are cost effective when compared to the rest of the topologies.

Despite the benefits of the HBSMs, they are unable to provide reversed voltage to ride through DC faults, while the CDSMs generates the least reverse voltage due to their number of parallel connected SM capacitors. On the other hand, all the other topologies, including the proposed topology, can offer excellent DC-FRT. Similarly, the proposed hybrid-arm and the rest of the topologies with excellent DC-FRT can provide reactive power compensation (STATCOM) while clearing the fault current. Therefore, the hybrid-arm topology provides DC-FRT and reactive power compensation with the least number of electronic devices, which justifies its cost-effective approach for bulk power HVDC transmission. The comparative analysis is further strengthened with theoretical equations in 3.10.1 and 3.10.2.

3.10.1 POWER LOSS ANALYSIS

The power losses in the MMC can be mainly divided into conduction and switching losses, denoted as P_{con} and P_{sw}. The average power loss over a period is given from (3.51) – (3.53) with full details in [157]:

The expression for the conduction losses of the IGBTs and diodes in the MMC is obtained from the power relation in (3.51).

$$\begin{cases} P_{con\_igbt} = Vi_{con} + i_{con}^2 r \\ P_{con\_diode} = Vi_{con} + i_{con}^2 r \end{cases} \tag{3.51}$$

Also, the switching loss expression is shown in (3.53).

$$P_{sw\_igbt} = \frac{(E_{on}+E_{off})}{T_{sw}} \cdot \frac{V_c i_{sw}}{V_n i_n} \tag{3.52}$$

$$\begin{cases} P_{sw\_igbt} = f_{sw}(E_{on} + E_{off}) \cdot \frac{V_c i_{sw}}{V_n i_n} \\ P_{sw\_diode} = f_{sw} E_{rec} \cdot \frac{V_c i_{sw}}{V_n i_n} \end{cases} \tag{3.53}$$

where i_n and v_n are the rated current and voltage per SM, i_{sw} and i_{con} are the average current in switching and conduction mode. The on-state forward voltage drop is V and r is the on-state resistance. For the IGBTs, the turn on and turn off energy loss is E_{on}/E_{off} while for the diodes, the switching frequency is f_{sw} and E_{rec} is the reverse recovery energy. For N submodules, the capacitor voltage, V_c can be represented in (3.54).

$$V_c = \frac{V_{dc}}{N} \tag{3.54}$$

Considering the HBSM topology and assuming all SMs are balanced, the detailed numerical power loss expression for its IGBTs and diodes has been derived in [158] using (3.51) and (3.53). As a result, the expression for the conduction loss in the HBSM is given in (3.55).

$$\begin{cases} P_{con\_igbt(hbsm)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2}\left(\left(V_{igbt}i_{arm}(\omega t) + i_{arm}^2(\omega t)r_{igbt}\right)sm_{hbsm}(\omega t)\right)d\omega t \\ P_{con\_diode(hbsm)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2}\left((-V_{diode}i_{arm}(\omega t) + i_{arm}^2(\omega t)r_{diode})sm_{hbsm}(\omega t)\right)d\omega t \end{cases} \tag{3.55}$$

where α_1 and α_2 are the conduction intervals of the diodes and the IGBTs. The arm current in the HBSM is i_{arm}. It is positive, when IGBT1 and diode2 conducts and negative when IGBT2 and diode1 conduct. Also, sm_{hbsm} is the duty cycle of the arm SM. It can be obtained using the expression in (3.56).

$$\begin{cases} sm_1(\omega t) = \frac{1-m_a\sin(\omega t)}{2} \\ sm_2(\omega t) = \frac{1+m_a\sin(\omega t)}{2} \end{cases} \tag{3.56}$$

where $m_a\sin(\omega t)$ is the modulating signal of a particular phase in the HBSM.

For switching losses, it is necessary to know the number of power devices in the switching state. The expression for switching losses of the HBSM is shown in (3.57) similar to [158].

$$\begin{cases} P_{sw\_igbt(hbsm)} = \frac{f_{sw}(E_{on}+E_{off})}{2\pi}\cdot\frac{V_c}{V_n i_n}\cdot N\int_{\alpha_1}^{\alpha_2} i_{arm}(\omega t)d\omega t \\ P_{sw\_diode(hbsm)} = \frac{f_{sw}E_{rec}}{2\pi}\cdot\frac{V_c}{V_n i_n}\cdot N\int_{\alpha_1}^{\alpha_2} -i_{arm}(\omega t)d\omega t \end{cases} \tag{3.57}$$

(3.57) can also be represented as (3.58) by substituting (3.54).

$$\begin{cases} P_{sw\_igbt(hbsm)} = \frac{f_{sw}(E_{on}+E_{off})}{2\pi}\cdot\frac{V_{dc}}{V_n i_n}\int_{\alpha_1}^{\alpha_2} i_{arm}(\omega t)d\omega t \\ P_{sw\_diode(hbsm)} = \frac{f_{sw}E_{rec}}{2\pi}\cdot\frac{V_{dc}}{V_n i_n}\int_{\alpha_1}^{\alpha_2} -i_{arm}(\omega t)d\omega t \end{cases} \tag{3.58}$$

From (3.58), the expression for the switching loss of the HBSM is independent on the number of submodules.

Considering the FBSM, three different voltage levels (0, V_c and -V_c) are generated unlike the HBSMs that generates two voltage levels (0 and V_c). Thus, the expression for the FBSMs power losses will incorporate a redundant SMs as illustrated below:

Similar to (3.55) the conduction losses of the FBSM is shown in (3.59).

$$\begin{cases} P_{con\_igbt(fbsm)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2}\left(\left(V_{igbt}i_{arm}(\omega t) + i_{arm}^2(\omega t)r_{igbt}\right)sm_{fbsm}(\omega t)\right)d\omega t \\ P_{con\_diode(fbsm)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2}\left(\left(-V_{diode}i_{arm}(\omega t) + i_{arm}^2(\omega t)r_{diode}\right)sm_{fbsm}(\omega t)\right)d\omega t \end{cases} \quad (3.59)$$

where the duty cycle of the FBSM arm is given in (3.60).

$$\begin{cases} sm_{14}(\omega t) = \frac{3-m_a\sin(\omega t)}{4} \\ sm_{23}(\omega t) = \frac{1+m_a\sin(\omega t)}{4} \end{cases} \quad (3.60)$$

where sm_{14} is for transistors 1 and 4 while sm_{23} is for transistors 2 and 3. From (3.60), it can be deduced that $sm_{fbsm} = 2 \times sm_{hbsm}$. Also, since the conduction losses is proportional to the number of submodules, the conduction losses of the FBSM will be greater than that of HBSM. Thus, it can be deduced that as the number of SMs increases the conduction losses increases.

Also, considering the switching losses of the FBSM in (3.61), It can be seen that a redundant SM is added to (3.57).

$$\begin{cases} P_{sw\_igbt(fbsm)} = \frac{f_{sw}(E_{on}+E_{off})}{2\pi}\cdot\frac{V_c}{V_n i_n}\cdot\left[N\int_{\alpha_1}^{\alpha_2} i_{arm}(\omega t)d\omega t + N_1\int_{\alpha_1}^{\alpha_2} i_{arm}(\omega t)d\omega t\right] \\ P_{sw\_diode(hbsm)} = \frac{f_{sw}E_{rec}}{2\pi}\cdot\frac{V_c}{V_n i_n}\cdot\left[N\int_{\alpha_1}^{\alpha_2} -i_{arm}(\omega t)d\omega t + N_1\int_{\alpha_1}^{\alpha_2} -i_{arm}(\omega t)d\omega t\right] \end{cases} \quad (3.61)$$

$$N_{fbsm} = N + N_1 \quad (3.62)$$

where N_1 is the number of redundant SMs. Thus, the switching losses of the FBSM increases with N_1, so does the total loss of the MMC.

For the hybrid SMs and mixed topologies made of HBSMs, increasing the number of SMs in the HBSMs would not affect switching losses as seen in (3.58) and [159]. However, in (3.61), it does increase losses with the FBSMs and other topologies with higher number of IGBTs as N_1 accounts for IGBTs 3 and 4. Also comparing (3.56) and (3.60), the conduction losses of the FBSM are twice that of the HBSM. Therefore, increasing N will increase the total power loss of the MMC as seen in Table 3.4.

As a result, the proposed hybrid-arm topology with 0.3N of HBSM and 0.3N of SCSM will have reduced power losses compared to all other fault tolerant SMs in Table 3.4.

3.10.2 MMC COST ANALYSIS

The basis of this study is to estimate the cost of additional redundant cells for adequate comparative analysis of the MMC topologies. The cost of the MMCs is done in a standard operation without considering the cost of controlling the voltage ripples associated with the SM capacitor voltage. Thus, a fixed DC voltage of 120 kV as given in Table 3.3 is used.

The total MMC cost of a standard topology is divided into initial cost and power loss cost [160].

$$Cost_{mmc} = Cost_{init} + Cost_{powerloss} \tag{3.63}$$

The initial cost includes the cost of installing the power conversion systems (SM cost) and the cost of installing cooling systems such as HVAC. The initial cost of a QkW MMC system with X redundant SMs is given in (3.64).

$$Cost_{init} = \left[Q \times \left(1 + \frac{X}{N}\right)\right](Cost_{sm}) + Cost_{cooling} \tag{3.64}$$

The cooling system cost is dependent on the volume and weight of the conversion unit, and it is scaled down to 10% of the initial cost according to [161].

$$Cost_{cooling} = 0.1 Cost_{init} \tag{3.65}$$

$$Cost_{init} = 1.11\left[Q \times \left(1 + \frac{X}{N}\right)\right] \times (Cost_{sm}) \tag{3.66}$$

The SM cost is proportional to the ratings of the system. It is grouped into cost of IGBTs and the cost of the capacitors in the submodule since they contribute immensely to the SM weight, footprint, and Capital Expenses (CapEx) [162].

$$Cost_{sm} = Cost_{igbts} + Cost_{capacitor} \tag{3.67}$$

The properties of the IGBTs are taken from the manufacturer datasheets of IGBT module FF300R17KE4. The IGBT cost is calculated based on the nature of the semiconductor chip and the weight (package) since they constitute a larger fraction of the thermal and electrical behaviour of the device [163]. Thus, the cost of the IGBT is given in (3.68).

$$Cost_{igbts} = Cost_{chip} + Cost_{package} \tag{3.68}$$

$$Cost_{chip} = n_{igbt}(1.27V_{cell} - 974[\$]) \tag{3.69}$$

$$V_{cell} = 0.56 \times V_{br} \tag{3.70}$$

$$Cost_{package} = n_{igbt}\left(15.06/_{w_{igbt}}\right) \tag{3.71}$$

$$w_{igbt} = 0.9 \times 10^{-3} V_{cell} - 0.34[kg] \tag{3.72}$$

where V_{br} is the breakdown voltage given as 1700V from the IGBT datasheet and n_{igbt} is the number of IGBTs in the MMC SM. The numerator of (3.71) is taken from the overall package size per unit of a standard IGBT chip as seen in [163]. The 0.34kg is also obtained from the manufacturer's datasheet of the IGBT.

For the cost of capacitors, thin film metallized polypropylene capacitors are the most considered technology for the MMC because of their high reliability, low loss, low cost and high stability over a wide temperature range [164]. As a result, the cost function of the capacitors is modelled below in accordance with the manufacturer's datasheet.

$$Cost_{cap\_film} = n_{cap} \times w_{cap}\ [\$] \tag{3.73}$$

$$w_{cap} = 3.57E_{sm} + 5.92[kg] \tag{3.74}$$

where E_{sm} is the energy storage capacity of the SM in kJ while the number of parallel capacitors is n_{cap}.

Therefore, the total initial cost of X redundant SM in (3.66) can be represented as (3.75):

$$Cost_{init} = 1.11\left[Q \times \left(1 + \frac{X}{N}\right)\right] \times \left(Cost_{chip} + Cost_{package} + Cost_{capacitor}\right) \tag{3.75}$$

From (3.75), the higher the submodule number, the higher the CapEx. Thus, an MMC with an increased number of SMs is expected to incur more initial cost. Considering that the proposed SM has the least number of SM in comparison with other fault tolerant converter, it will incur the least initial cost.

In addition to the initial cost is the power loss cost. The power loss cost is dependent on the conduction losses of the semiconductor devices. Assuming that the SM loss cost is 10 c/kWh and the operating time (OT) of the MMC in a 20-year operating year (OY) is 8760 hr, the power loss cost for a QkW MMC can be obtained using (3.76).

$$Cost_{powerloss} = (1-\eta) \times Q \times 0.1 \times OT \times OY \quad (3.76)$$

$$Cost_{powerloss} = (1-\eta) \times Q \times 0.8760 \times 24 \times 365 \quad (3.77)$$

$$Cost_{powerloss} = (1-\eta) \times Q \times 7673.76 \quad (3.78)$$

where η is the efficiency of the MMCs. Thus, the total MMC cost can be obtained by combining (3.66) and (3.78).

$$Cost_{mmc} = 1.11\left[Q \times \left(1+\frac{X}{N}\right)\right] \times (Cost_{sm}) + (1-\eta) \times Q \times 7673.76 \quad (3.79)$$

From (3.79), the cost of the MMC in Fig. 3.23 is obtained using the information from Table 3.4.

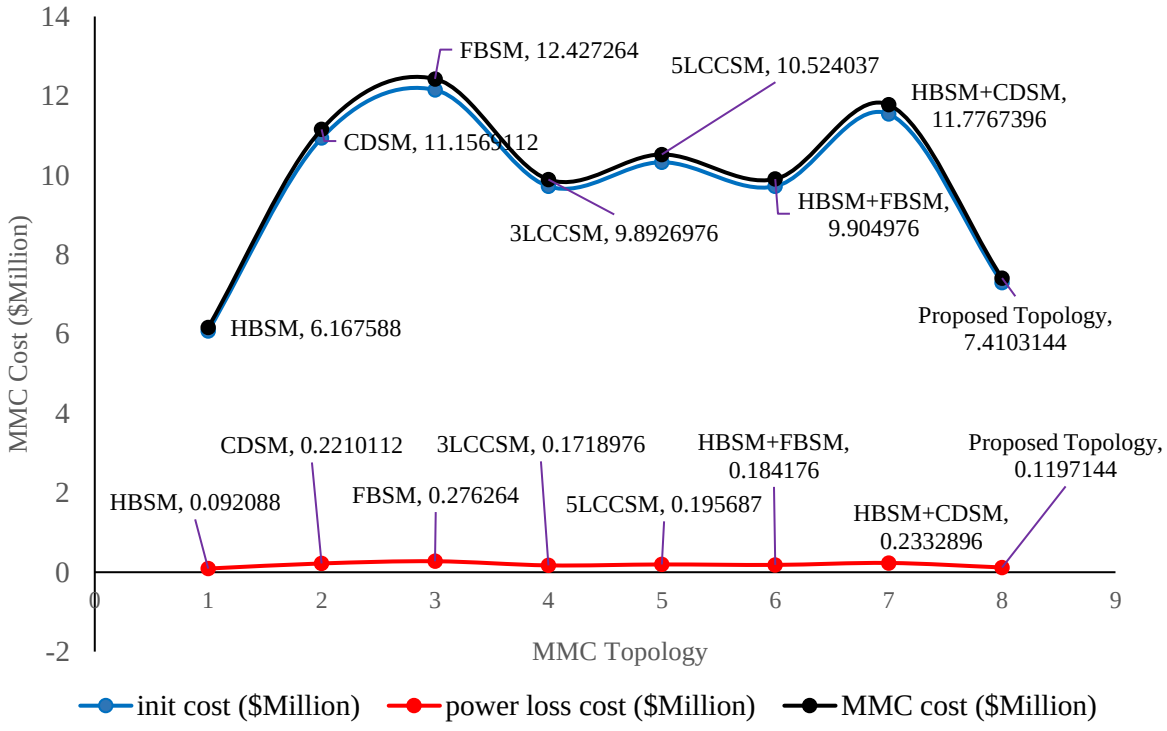


Fig.3. 21 Comparative analysis of MMC topology cost

Table 3. 4: Evaluation of different MMC topologies

MMC Topology / MMC Parameters	Half Bridge (HBSM)	Clamp-double (CDSM)	Full Bridge (FBSM)	3-level cross connected (3LCCSM)	5-level cross connected (5LCCSM)	Hybrid (HBSM+ FBSM)	Hybrid (HBSM+ CDSM)	Proposed Hybrid-arm Topology (HBSM+SCSM)
HVDC link voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
No. of SMs per arm	$0.5N$	N	N	N	N	$0.5NHBSM$ and $0.5NFBSM$	$0.5NHBSM$ and $0.5NCDSM$	$0.3NHBSM$ $+ 0.3NSCSM$
No. of capacitor per arm	N	N	N	N	N	N	N	N
No. of devices per arm (IGBTs and Diodes)	$2N$	$2N$	$4N$	$2N$	$2N$	$2.8N$	$2N$	$2N$
No. of extra IGBTs per arm	0	$0.5N$	0	N	N	0	$0.4N$	$0.4N$
No. of extra diodes per arm	0	N	0	N	0	0	$0.8N$	$0.4N$
Approximated power loss	0.6%	0.8%	0.9%	0.8%	0.8%	0.8%	0.7%	0.65%
DC FRT	No	$Yes\ but\ limited$	Yes	yes	yes	yes	yes	yes
STATCOM	No	No	yes	yes	yes	yes	yes	yes

3.11 CONCLUSION

In this chapter, a novel hybrid-arm topology and a control methodology are proposed for HVDC transmission systems. The topology is made up of positive and negative symmetrical MMCs. Each MMC is a mix of an identical number of SCSMs and HBSMs. It was shown in the result section that when the topology is harnessed with the control methodology, The topology achieved leg and arm energy balance as there were no divergence among the energy values. This is because the DC and AC circulating current references were properly controlled, as the summation of their individual circulating current references is zero ($i_{cir\_ac}^{a*} + i_{cir\_ac}^{b*} + i_{cir\_ac}^{c*} = 0$). Thus, the oscillations that contaminate the DC and AC terminals of the MMC are avoided while enhancing DC-FRT. Furthermore, it was observed that for DC faults with a fault period of less than 5 s, the converter could ride through the fault and resume normal operation without the need to compensate the grid with reactive power. However, for faults with longer durations, the converter generates reactive power from the HBSM arm as the SCSM arm clears the fault. In addition to

the DC-FRT capability of the converter, comparative analysis was done with other converter topologies to verify the commercial viability of the proposed topology. It was seen that the hybrid-arm topology offers a 50% and a 29% reduction in the number of semiconductor devices used when compared with the conventional FBSM and hybrids of FBSM and HBSM, respectively. Moreover, the estimated power loss of the hybrid-arm converter is the lowest for all the topologies except for the HBSM, which lacks DC-FRT capability. Furthermore, considering the energy balancing capability of the proposed converter topology, it can be inferred that the proposed topology exhibits a good balance of the capacitor voltage in each arm at reduced footprint, losses, and operational cost compared to any of the topologies listed in Table 3.4. Therefore, the proposed control methodology and hybrid-arm topology of SCSM and HBSM is a cost-effective option for bulk power transmission.

Chapter 4

4. A NOVEL FAULT LOCATION STRATEGY BASED ON BI-LSTM FOR MMC-HVDC SYSTEMS

4.1 INTRODUCTION

This chapter proposes a new deep learning AI-based fault location method inspired by Bidirectional Long-Short Term Memory (Bi-LSTM). The algorithm can classify fault lines and locate fault distances using a simplified extracting and analysing approach on fault data from only the rectifying end of the MMC-HVDC network, thus eliminating the need for a communication channel. Furthermore, the proposed algorithm learns the time series of the fault current samples from a real-time simulator of bipolar and four-terminal MMC-HVDC systems based on the Artemis and SSN benchmarks. The accuracy of the proposed technique is verified under different fault types, fault impedances, and noise levels. From the above statements, the main contributions of this chapter are summarised as follows: A simple and robust fault classification and location scheme is proposed to handle high-resolution timestep data with the exclusion of complex feature extraction, thus eliminating the issues with the computational burden. In addition, the scheme is resilient against varying fault impedances, noise, transmission line parameters, and operating conditions. The approach can eliminate the issue of vanishing gradients, affecting the deployment of Recurrent Neural Networks (RNN) in practical systems. Finally, the proposed algorithm can adapt to a more complex multi-terminal MMC-HVDC network with less than a 1% location percentage error.

The rest of the chapter is structured as follows: Section 4.2 presents a theoretical analysis of the proposed scheme, while Section 4.3 gives a detailed analysis of the fault location methodology. Section 4.4 discusses the system under test and the data acquisition process. Section 4.5 shows

simulations and results, as well as a set of comparisons with other fault location methods. Conclusions are drawn in Section 4.6.

4.2 DESCRIPTION OF THE PROPOSED SCHEME

The Long Short-Term Memory (LSTM) algorithm is a deep learning algorithm integrated into MMC-HVDC to locate DC faults in the network. The algorithm is a new type of Recurrent Neural Network (RNN). The RNN is an improved version of the Convolutional Neural Network (CNN), one of the most popular deep learning algorithms. The RNN uses previous output data to forecast new data. This ability has led to a significant improvement in time-series forecasting tasks. However, RNN still suffers from gradient disappearance. A condition where the weights of the neurons are unable to learn and update as the time step increases. This condition is severe because the learning rate of the network drops, and the network may fail during the training phase. RNNs also require high computing power during training of data for large scale implementation. These drawbacks to RNN can be linked to the fact that the recurrence of data is done using a single layer. The LSTM solves the issue with the RNN's gradient disappearance using three different gates with separate activation functions to continuously update the data. Moreover, the LSTM has a memory block that can hold information for a long time step thus the name 'Long Memory'.

The gates in the LSTM are the forget gate, the input gate, and the output gate, as shown in Fig. 4.1. These gates control the flow of information in the LSTM. The "forget" gate can be used to remove unwanted data. It uses a sigmoid activation function to refresh the memory of the LSTM. Immediately after the forget gate is the input gate. This gate controls whether the memory should be updated and the elements needed for the update. The output gate determines the features sent out to the hidden state.

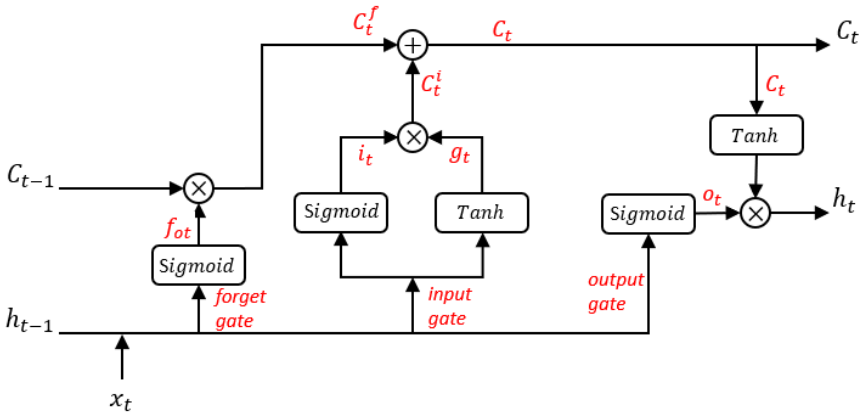


Fig.4. 1: The structure of LSTM

From Fig. 4.1, x_t is the current time-step of the input data while the previous time-step of the cell state and the hidden layer are C_{t-1} and h_{t-1}. The current hidden state, h_t, of the LSTM can be computed by updating the weight and bias parameters of each gate as shown below:

Forget gate,

$$f_{sigmoid} = \left(\omega_{fh} + \omega_{fx} + b_f\right) \tag{4.1}$$

On passing the inputs (h_{t-1} and x_t) through the function, (4.2) is obtained:

$$f_{ot} = \sigma\left[\left(\omega_{fh} + h_{t-1}\right) + \left(\omega_{fx} + x_t\right) + b_f\right] \tag{4.2}$$

$$C_t^f = C_{t-1} * f_{ot} \tag{4.3}$$

Input gate,

$$i_{sigmoid} = (\omega_{ih} + \omega_{ix} + b_i) \tag{4.4}$$

$$i_t = \sigma[(\omega_{ih} + h_{t-1}) + (\omega_{ix} + x_t) + b_i] \tag{4.5}$$

Similarly,

$$g_{tanh} = \left(\omega_{gh} + \omega_{gx} + b_g\right) \tag{4.6}$$

$$g_t = tanh\left[\left(\omega_{gh} + h_{t-1}\right) + \left(\omega_{gx} + x_t\right) + b_g\right] \tag{4.7}$$

$$C_t^i = i_t * g_t \tag{4.8}$$

$$C_t = C_t^f + C_t^i \tag{4.9}$$

Output gate,

$$o_{sigmoid} = (\omega_{oh} + \omega_{ox} + b_o) \tag{4.10}$$

$$o_t = \sigma[(\omega_{oh} + h_{t-1}) + (\omega_{ox} + x_t) + b_o] \tag{4.11}$$

Passing (4.9) through the tanh function and combining it with (4.11) will generate the output of the hidden layer in (4.12):

$$h_t = tanh(C_t) + o_t \tag{4.12}$$

$$tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}} \quad and \quad sigmoid(x) = \frac{1}{1+e^{-x}}$$

where f_{ot}, i_t, g_t, and o_t are the forget gate, input gate, input node and output gate. While ω_f, ω_i, ω_g, and $\omega_o$are the weight parameters. The bias for the gates is b_f, b_i, b_g, and b_o. σ is the sigmoid activation that maintains the gates output between 0 and 1 while the $tanh$ activation controls the outputs between -1 and 1. The current memory cell state, C_t, can be obtained from the current cell state of the input gate, C_t^i, and the forget gate, C_t^f. The latter is generated from the previous cell state, C_{t-1} and f_{ot}. Where f_{ot} is a combination of x_t and h_{t-1}. Setting f_{ot} to zero ignores the old data while setting i_t to zero ignores newly computed data. Similar computation is done to obtain the next hidden layer of the LSTM thus eliminating gradient disappearance.

One of the limitations of using single LSTM is that it uses only historical data during prediction. However, with the use of the Bi-LSTM in Fig. 4.2, this drawback can be eliminated since the algorithm uses both the previous state (h_{t-1}) and the future state (h_{t+1}) by stacking two LSTMs in a forward and backward pattern. With this approach, the proposed algorithm can efficiently extract all the hidden layer features, thus increasing the accuracy of the location process.

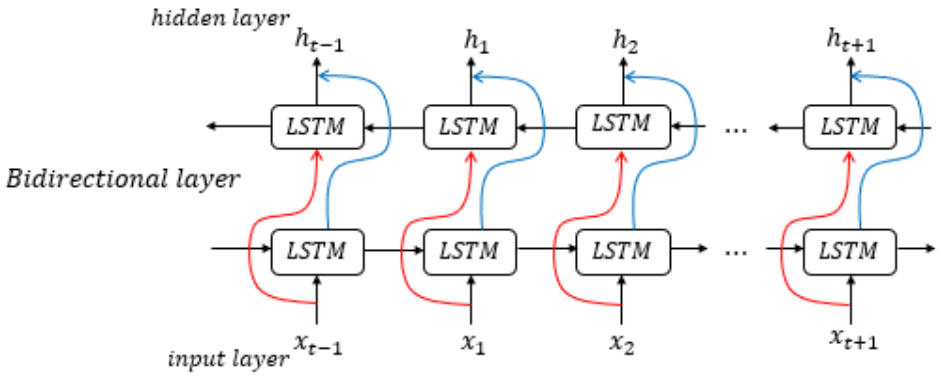


Fig.4. 2: Structure of bidirectional LSTM (Bi-LSTM)

Furthermore, the proposed Bi-LSTM can classify and locate faults on the MMC-HVDC transmission lines using the flow diagram in Fig. 4.3. When a fault is detected in the system, the algorithm collects all the fault samples from the sequence input layer. The output from the Bi-LSTM layer is passed onto the fully connected layer, from which the fault types are classified, and the faulty lines are identified using the SoftMax layer. Once the faulty lines are detected, the output is sent back to the fully connected layer, from which a regression layer is used to locate the fault distance.

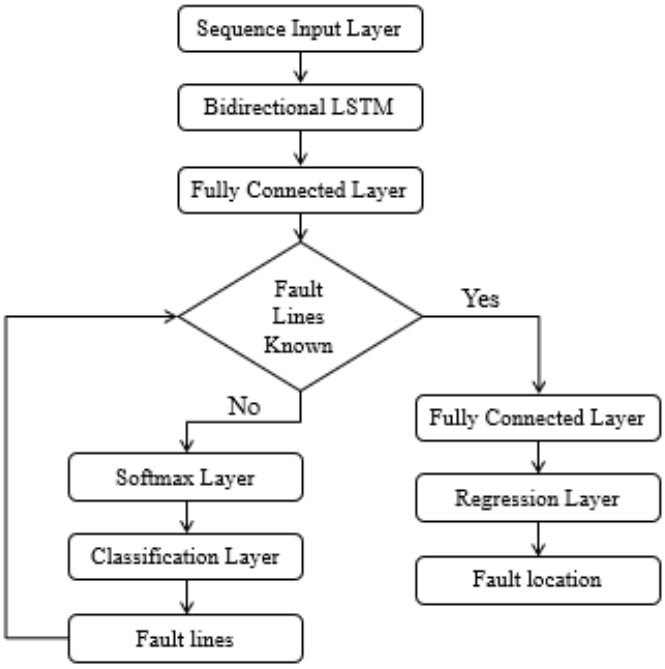


Fig.4. 3: Flow diagram of Bi-LSTM model

4.3 ANALYSIS OF THE FAULT LOCATION APPROACH

The proposed fault location scheme for the MMC-HVDC transmission system is shown in Fig. 4.4. At the top of Fig. 4.4 is a bipolar MMC system with a rectifying and inverting end. Faults such as pole1 to ground (P_1), pole2 to ground (P_2) and pole1 to pole 2 ($P_1 - P_2$) can affect the system. When a fault is detected on the transmission line, the fault current and voltage data are collected from only the rectifying end of the system into the input layer. The fault samples are passed from the input layer to the hidden layer comprising multiple bidirectional LSTM units where unwanted fault samples are removed by the forget gate while the input gate updates the cell state of the Bi-LSTM with the maximum current and minimum voltage fault values. As a result, useful features from the fault data are extracted by the output gate. Thus, the Bi-LSTM improves the accuracy of the fault location scheme by providing the backpropagation needed to minimize the Mean Square Error (MSE) in (4.13) and extract the features containing the information of the faulty lines using the sigmoid and the tanh activation function.

$$MSE = \sum_i^m (D_i - d_R)^2 \tag{4.13}$$

where, D_i is the actual location of the fault, d_R is the predicted location and m is the number of samples.

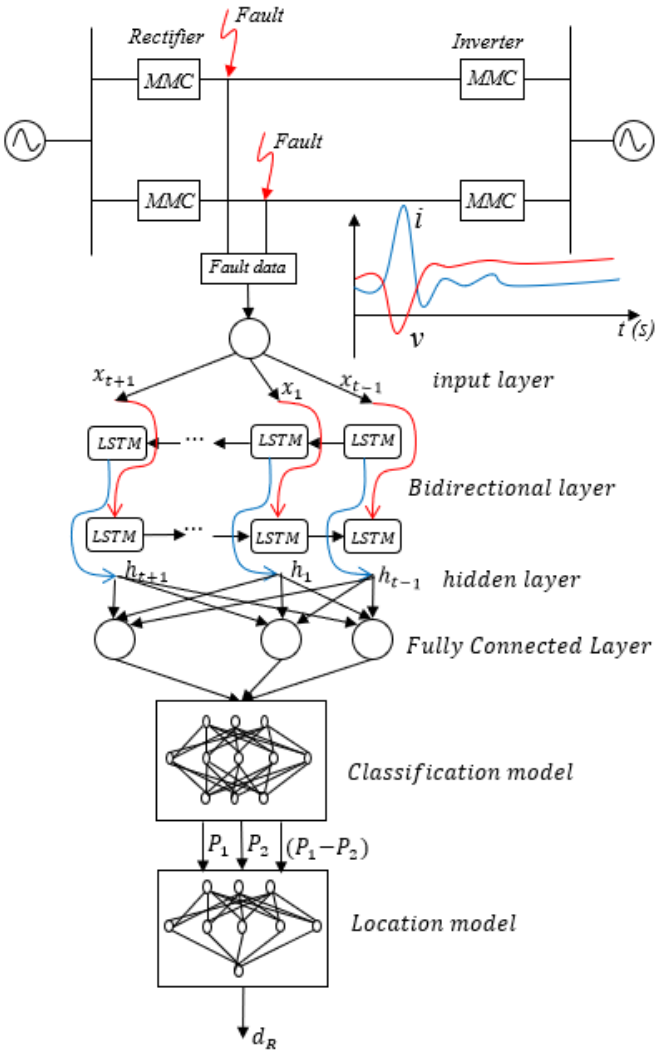


Fig.4. 4: Fault location scheme

Also, from Fig. 4.4, the output from the Bi-LSTM is sent to the fully connected layer. This layer is also known as the dense layer of neurons. A fully connected layer consists of weights (ω) and bias (b) to perform dense multiplication between input features and trainable weights. In Fig. 4.4, the fully connected layer can reduce the structure size of the fault samples to eliminate the computational burden and improve the speed of locating the faulty lines and the fault distance. From the fully connected layer is the classification model. This model can classify the fault samples into the different fault types ($P_1, P_2, P_1 - P_2$). The algorithm in the classification model that is responsible for detecting the faulty lines is the Softmax. The Softmax can perform multi-classifications and represents the results using probability distribution function in (4.14). Thus, output is between 0 and 1 with the faulty region having the highest probability. If the fault occurs on the first transmission line, the Softmax can predict P_1 to have a probability close to 1, while

P_2 and P_1-P_2 have probabilities close to 0. Thus all P_1 fault samples are sent to the location model to speedily obtain the fault distance.

$$Softmax(P_i) = \frac{e^{x_i}}{\sum_{j=1}^{K} e^{x_j}} \tag{4.14}$$

where e^{x_i} is the input vector standard exponential function and e^{x_j} is the output vector standard exponential function. K is the number of fault classes and for this case K is 3.

The fault location model uses regression function to predicts the fault distance (d_R) on the selected transmission line. d_R is measured from the point of fault impact to the rectifier substation.

Considering the fault current and voltage waveform in Fig. 4.4, the fault samples x_t in the input layer consisting of current and voltage can be used to update ω and b in the regression function as shown in (4.15) and (4.16). In addition, the regression function in (4.17) can correlate x_t with the fault distance so that when a new fault impacts the system, d_R can be obtained using (4.18) as shown in Fig. 4.5.

$$\omega = \frac{N\sum t.x_t - \sum t.\sum x_t}{N\sum t^2 - (\sum t)^2} \tag{4.15}$$

$$b = \frac{\sum x_t}{N} - \omega.\frac{\sum t}{N} \tag{4.16}$$

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma(x_t-\lambda)} e^{\left\{-\frac{[\ln(x_t-\lambda)-\mu]^2}{2\sigma^2}\right\}} \tag{4.17}$$

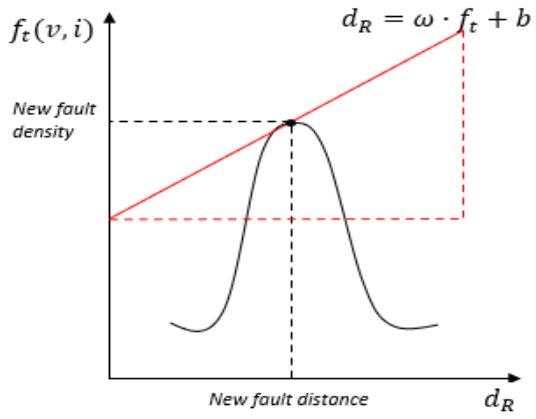


Fig.4. 5: Fault location approach using regression function

$$d_R = \omega.f_t + b \tag{4.18}$$

where t is the duration of the fault, N is the number of fault samples, μ is the location parameter, σ is the standard deviation, λ is the variance and f_t is the fault sample probability function. The point on the probability distribution curve obtained from the classification model with the highest fault sample density is used to predict the fault distance.

4.4 SIMULATION SETUP AND DATA PREPARATION

In this section, the MMC-HVDC system is shown in Section 4.4.1, while simulation of the faults on the systems and the extraction of the fault currents and voltages as training and test datasets are evaluated in Section 4.4.2.

4.4.1 MMC-HVDC SYSTEM

The validation of the fault location scheme is done using fault samples generated from a bipolar HVDC system in Fig. 4.7, designed in MATLAB and simulated in real-time using the OPAL-RT digital simulator in Fig. 4.6. The digital simulator uses the Artemis and State Space Nodal (SSN) solver to simulate the 24-pulse bipolar HVDC on four cores of a 3.2 GHz Xeon V2 (2 cores per station).

The MMC station is a 230 kV, 40 MW, 60 Hz network based on the CIGRE Benchmark. The rectifier and inverter are 12-pulse converters connected using a bipolar link. The link (pole 1 and pole 2) is a 300-km Distributed Parameter Line (DPL) based on Frequency Dependent Model (FDM) [165]. The capacitance, inductance and resistance of the line are 0.014 $\mu F/km$ 0.79 mH/km, 0.02 Ω/km respectively.

Table 4. 1: Simulation parameters for the system under test

Design Parameters	**Values**
AC voltage and frequency	230 kV and, 60 Hz
DC Voltage level	230 kV
Capacity rating	40 MW
SMs capacitor voltage	1.15 kV
Arm inductance	0.026 H
Cell capacitance	0.015 F
Number of MMC SMs	12

Insertion resistance	5 kΩ
Transmission line	DPL model – 300 km, 0.79 mH/km, 0.014 uF/km, 0.02 Ω/km

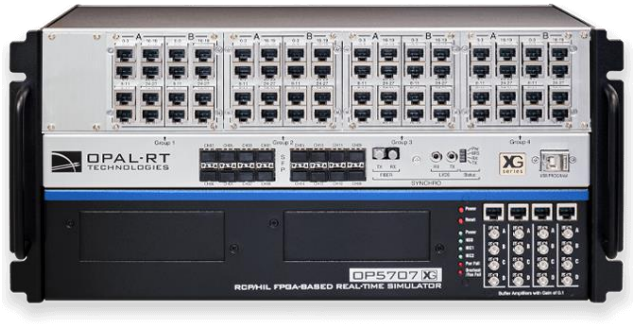


Fig.4. 6: OPAL-RT Digital real-time simulator

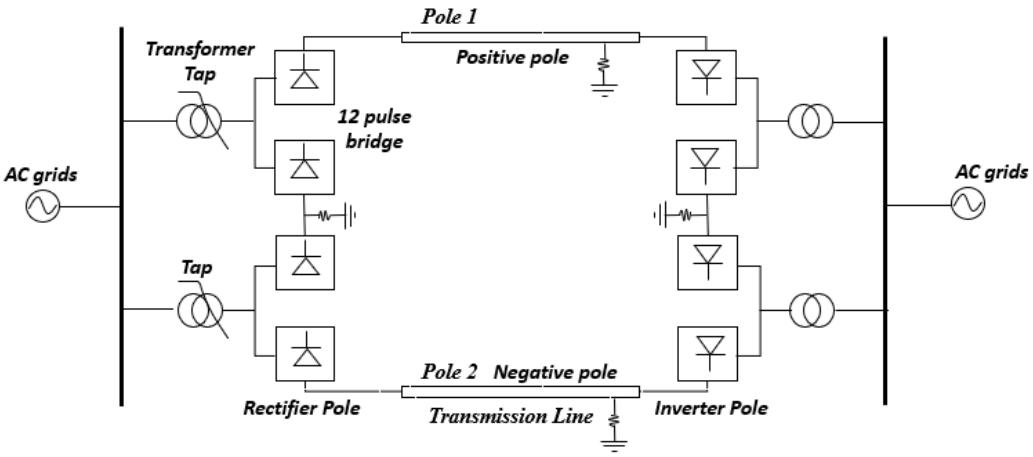


Fig.4. 7: Bipolar MMC HVDC system

4.4.2 FAULT DATASET GENERATION

The first step in the fault location approach is to obtain the fault current and voltage from the network. Fig. 4.8 shows an example of the fault current and voltage display generated from the real-time simulator during the fault and from which the fault data are extracted. From the display, the fault impacted the system at 0.5 s and lasted for 0.7 s. The three different fault types $(P_1, P_2, P_1 - P_2)$ were impacted at four different inception angles (30, 45, 60, and 90) for 30 different positions of the transmission line, with 25 different resistance values selected randomly between 0.01 Ω and 250 Ω. A total of 9000 fault cases (3 fault types, 4 impact angles, 30 fault positions and 25 fault resistances) are obtained using a sampling frequency of 12 kHz. The fault dataset is collected by a measuring relay at the rectifier pole.

The fault current and voltage samples are normalised between 0 and 1 using (4.19) to form the input fault samples (x_i) for the algorithm. This is done to enforce a level of uniformity without distorting the range of the values, thus improving the dataset's quality, and speeding up the fault location process. The result of x_i obtained from the simulation is shown in Fig. 4.9.

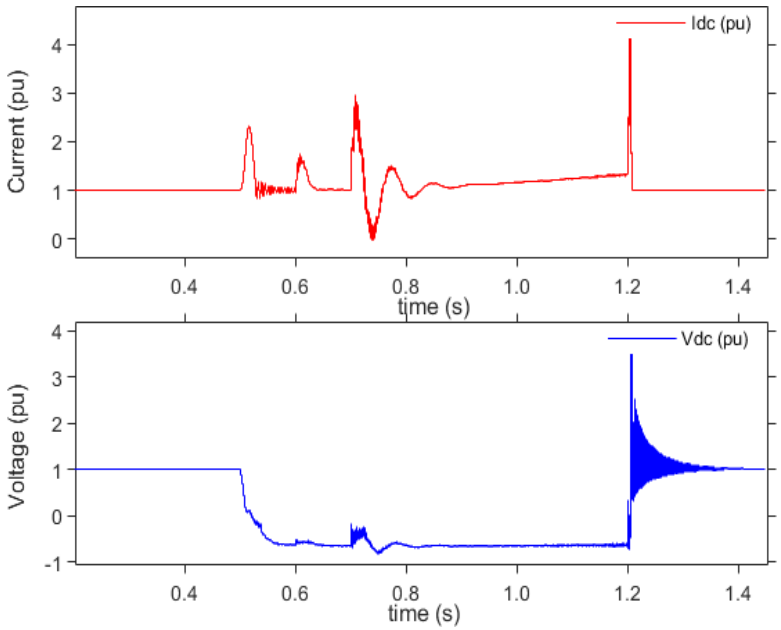


Fig.4. 8: DC fault current and voltage

$$x_i = \begin{cases} \frac{i_i - \min(i)}{\max(i) - \min(i)} & for\ fault\ current \\ \frac{v_i - \min(v)}{\max(v) - \min(v)} & for\ fault\ voltage \end{cases} \quad (4.19)$$

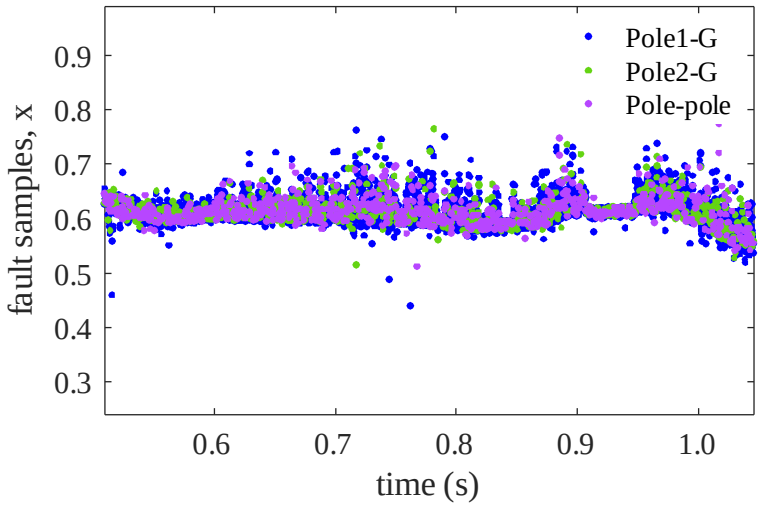


Fig.4. 9: Normalized input fault samples (*x*)

Before x_i is passed to the Bi-LSTM fault location scheme, it is divided into 70% training samples (6300) and 30% test samples (2700). The training fault samples are used to model the algorithm to learn and adapt to the fault features so that they can easily make future predictions when deployed on new fault samples, which in this case are the test samples.

For adequate training and testing, parameters such as the layers, batches, learning rate and epochs of the Bi-LSTM network should be properly selected. Increasing the number of layers, batch size and epochs, improves the performance of the model but adds to the complexity and computational burden thereby increases the locating time. Also, a learning rate not too low or too high should be selected. Because a low learning rate will converge after several iterations thus reduces the speed of location while a learning rate too high will diverge and lead to poor accuracy. As a result, the following parameters: 256 hidden layer, 3 fully connected layer, batch size of 90, 30 number of iterations (epochs) and learning rate of 0.01 are used for training and testing the fault datasets in a timely and accurate manner.

4.5 SIMULATION AND RESULT

This section presents the classification model results for the training and test phase of the fault samples in Section 4.5.1, the location model result is shown in Section 4.5.2. In Section 4.5.3, the effect of noise on the location scheme is analysed. In Section 4.5.4, the Bi-LSTM location scheme is deployed on a four-terminal MMC-HVDC system to verify the scheme's robustness while comparative analysis with other location schemes is presented in Section 4.5.5.

4.5.1 CLASSIFICATION ANALYSIS

The classification model separated the training dataset into the three different fault types ($P_1, P_2, P_1 - P_2$) as shown in Fig. 4.10. Each fault types identifies with the different regions of the transmission lines with corresponding class intervals of 0-1, 1-2, and 2-3. The accuracy of the trained model is shown in Fig. 4.11. The simulation was done for 21 iterations, and it can be seen that a close comparison occurs between the actual fault regions and the classified fault types as the curves approach 100%. This verifies that the trained model has learnt the fault features of the transmission and can further be deployed to predict the fault types of the 2700 test samples. The

identified region of the test sample is shown in Fig. 4.12 while the performance of the prediction model is shown using a confusion matrix in Fig. 4.13. From the confusion matrix, it was seen that only 1 out of the 900 fault samples belonging to pole2-G were wrongly predicted.

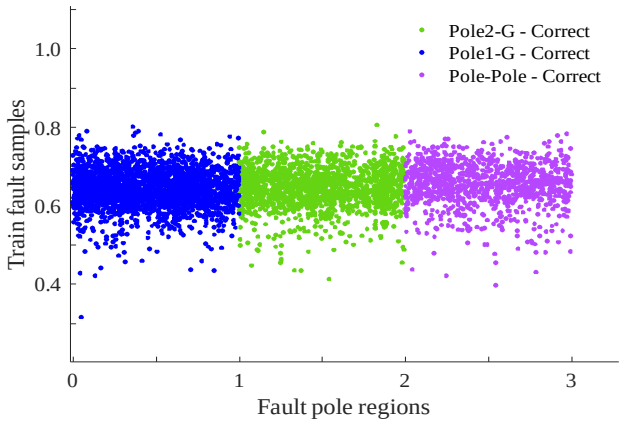


Fig.4. 10: Classified trained fault samples

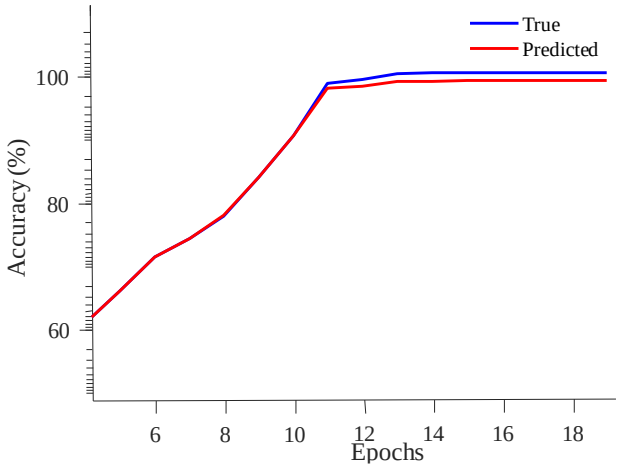


Fig.4. 11: Accuracy of the trained model

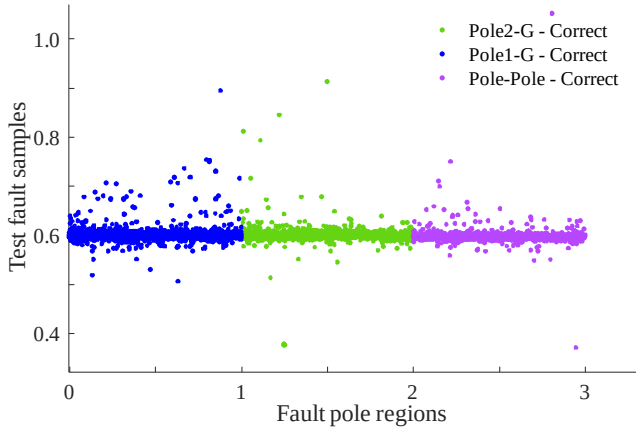


Fig.4. 12: Classified test fault samples

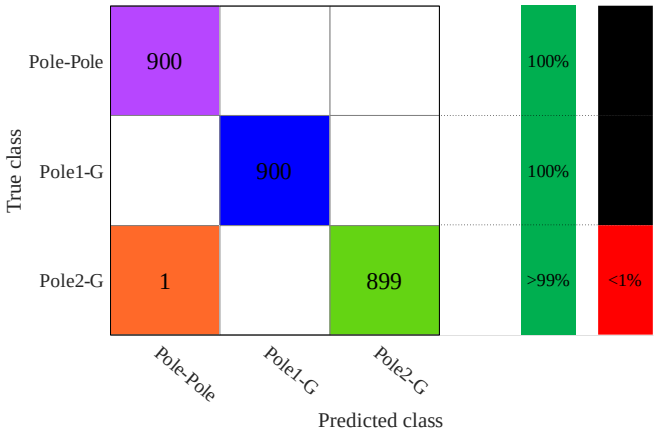


Fig.4. 13: Confusion matrix of classified test model

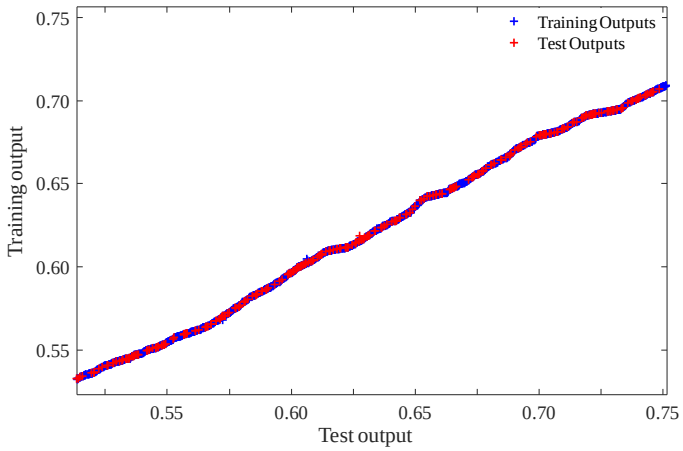


Fig.4. 14: Performance of the classification model

The performance of the classification model is shown by a correlation response plot in Fig. 4.14, such that the trained model was able to predict the test fault samples as both the training and test output converged to the three fault regions of the transmission line. Thus, the proposed classification model is accurate and efficient.

Since the fault region is known, the information from that faulty transmission line is sent to the location model to detect the exact point of fault impact. For example, if the classifier predicts the fault to occur on pole 1 of the bipolar network, only the pole 1 dataset is made available to the location model. This idea reduces the computation complexity in dealing with complex data from all the regions of the transmission line.

4.5.2 LOCATION ANALYSIS

For this section, all the test samples are sent to the location model and considering that they were generated from faults impacted on 30 different positions, the scheme is used to predict the location of each fault impact. Fig. 4.15 shows the distance prediction of one of the fault impacts. From the results, the distance of a pole-pole fault is indicated by a purple sample point located at the top of the probability density curve f(t). The model predicts the fault at 83.25 km since that is the distance with the highest magnitude of f(t). On validating, the actual fault location was at 83 km. Thus, a percentage error of 0.3% was recorded, which shows that the predicted and actual fault distances are in close agreement. Further to the above statement, Fig. 4.16 shows the MSE of the location model. It can be seen that the curve for the predicted distance is close to the true value with a low MSE of 0.006.

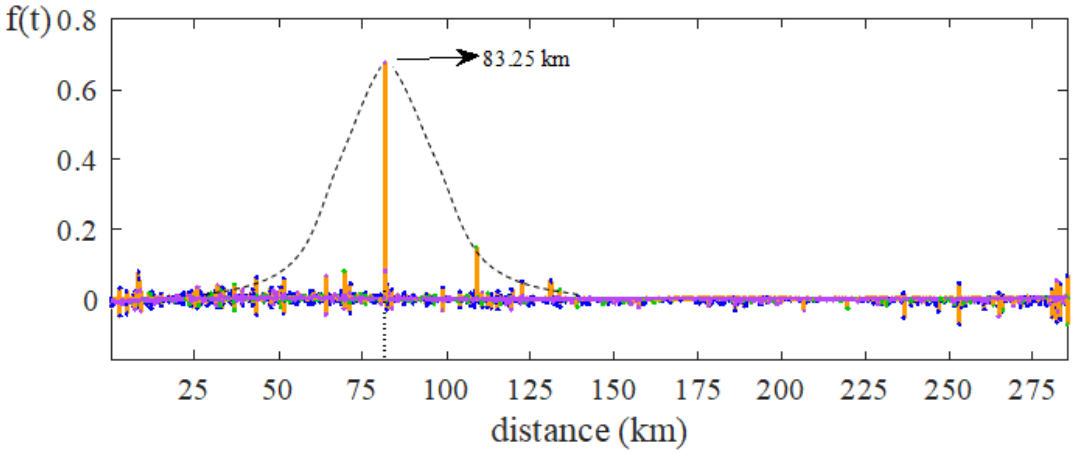


Fig.4. 15: Pole-pole fault distance estimation

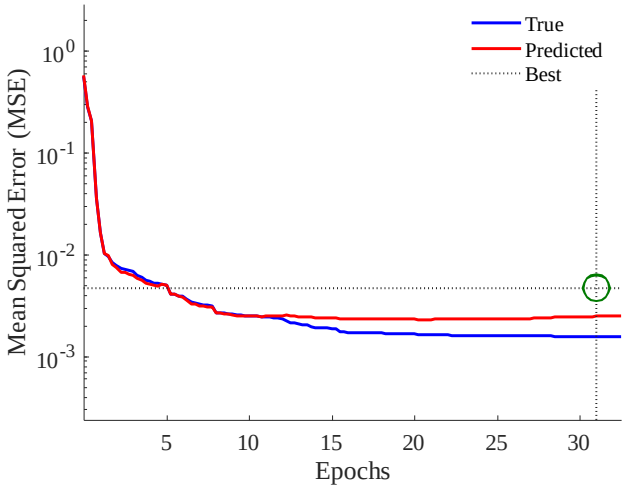


Fig.4. 16: Performance of the location model in MSE

Table. 4.2 presents the percentage error for the fault location of some of the other 29 different positions. From the table, it can be seen that the percentage error for the test samples is less than 1%. This shows that the proposed location scheme has high precision for fault distance estimation.

Table 4. 2: Validation of proposed location scheme

Fault Type	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %
P_1	40	39.75	0.625
	55	55.38	0.686
	108	108.22	0.203
	130	129.25	0.577
	242	242.54	0.223
P_2	50	50.16	0.319
	94	94.69	0.729
	112	111.82	0.161
	256	255.19	0.316
	287	287.86	0.299
$P_1 - P_2$	24	24.11	0.456
	73	72.39	0.836
	100	99.46	0.540
	140	139.54	0.329
	215	215.62	0.286

4.5.3 PERFORMANCE ON NOISY FAULT DATA

In real life scenarios, fault signals are sometimes contaminated with noise from measuring devices and from the environment. Such distortion to fault data can affects the accuracy of the location scheme. To verify the performance of the proposed location scheme in a noise polluted environment, Gaussian noise with Signal to Noise Ratio (SNR) from 40 dB to 10 dB is added to the training and test fault samples. Some of the result of the distance estimation is presented in Table 4.3. From the table, it can be seen that the percentage error was less than 1% for the different noise levels. This verifies that the location scheme is robust against noise.

Table 4. 3: Fault location performance under noisy data

SNR (dB)	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %
40	40	39.644	0.890
30	80	80.73	0.904
20	160	161.49	0.923
10	240	237.72	0.950

4.5.4 PERFORMANCE ON A 4-TERMINAL MMC-HVDC SYSTEM

The proposed location scheme is deployed on a 4-terminal MMC-HVDC system based on the CIGRE benchmark. The system comprises four MMC substations with a 250 kV, 1.5 GW capacity. The MMCs are regulated by a master control (SM_Control) and connected by 4 DPL (150 km, 200 km, 300 km, and 400 km), as shown in Fig. 4.17.

The scheme's performance is verified by simulating pole to ground faults on the four different lines. As discussed in Section 4.4.2, the fault data are generated by varying the resistance, distance, and inception angles. The distance prediction results obtained using the same principle as in Section 4.4 are shown in Table 4.4. The location scheme still maintains the percentage error within 1%. Thus, the performance of the scheme is not affected by system complexities.

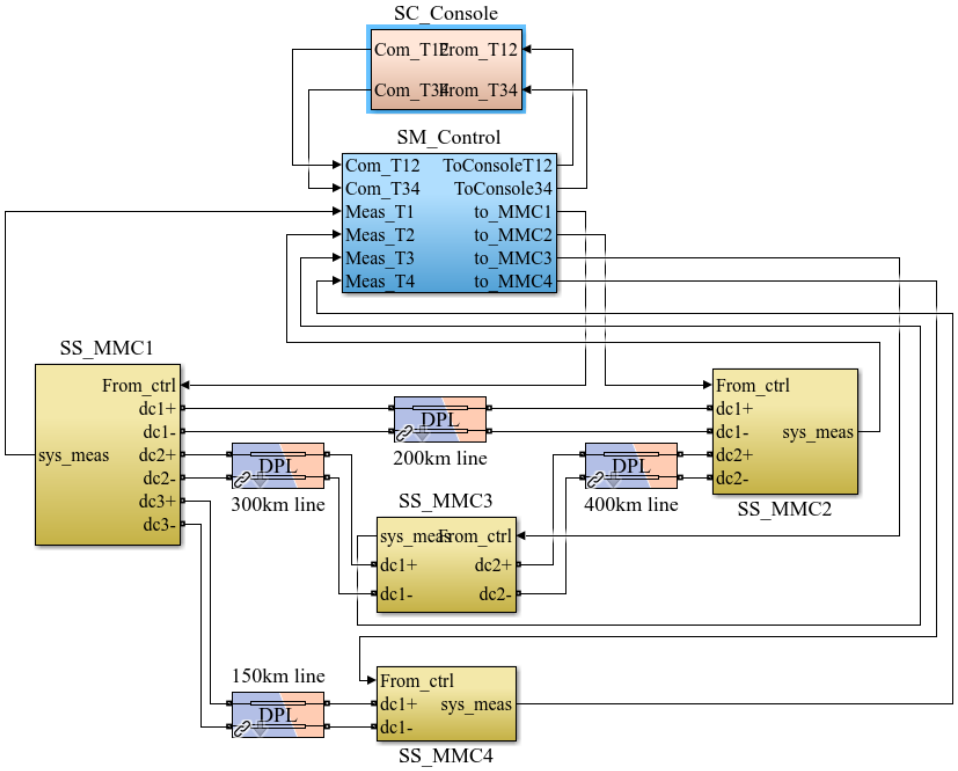


Fig.4. 17: 4-terminal MMC-HVDC system

Table 4. 4: Location scheme on 4-terminal MMC-HVDC

Fault Lines	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %
DPL150km	22	21.92	0.355
	70	70.33	0.469
	130	129.67	0.254
DPL200km	50	50.47	0.931
	110	110.26	0.236
	167	165.9	0.659
	189	189.82	0.432
DPL300km	26	26.19	0.725
	100	99.36	0.640
	265	265.68	0.256
	288	289.70	0.587
DPL400km	80	79.35	0.813
	150	149.54	0.306
	215	216.03	0.477
	376	374.02	0.527

4.5.5 VALIDATION ON A 37-TERMINAL MMC-HVDC SYSTEM

The proposed fault location scheme is validated on an IEEE 37-terminal MMC HVDC system, simulated using the Opal-RT real-time digital simulator under unbalanced load conditions. The HVDC substation is rated at 230 kV with a capacity of 2.5 GW nominal power. Each substation is linked by different lengths of DPL transmission networks in the order of 7xx. The system uses the SSN solver to simulate the model and to section the model to fit into two cores containing the subsystem shown in Fig. 4.18 and the console, which displays the fault dataset in Fig. 4.19.

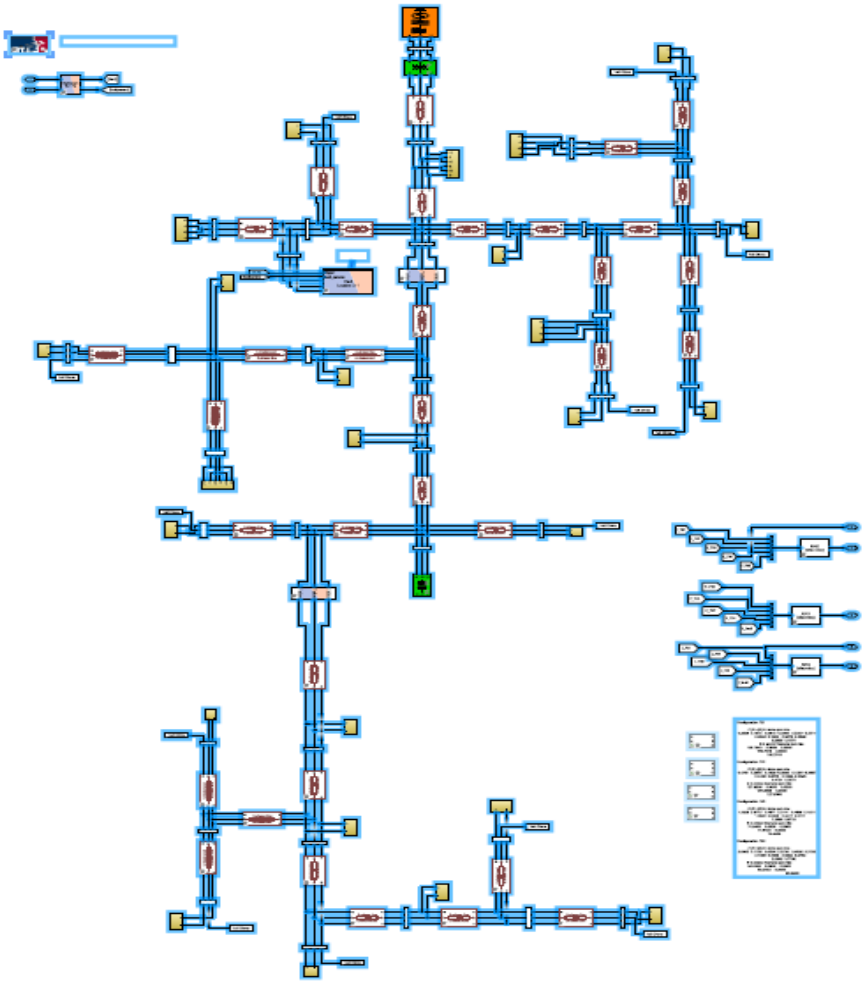


Fig. 4. 18: Subsystem of a 37-terminal MMC HVDC system

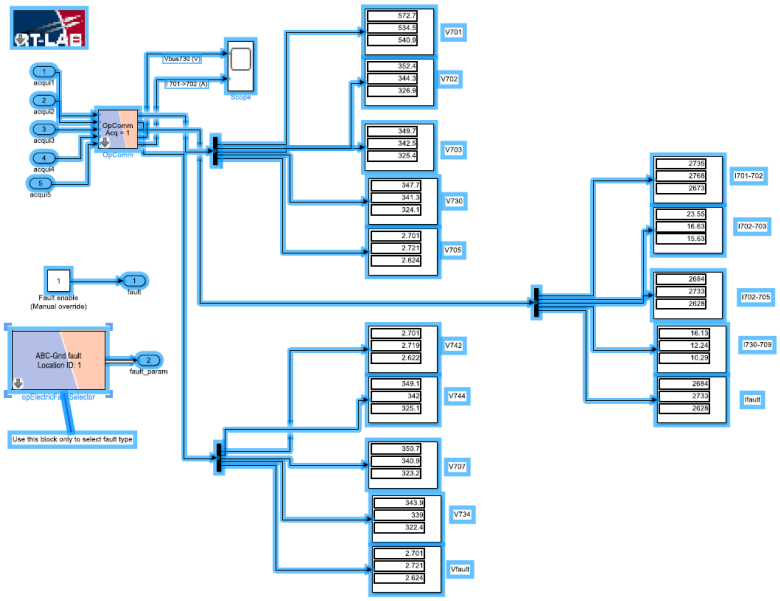


Fig. 4. 19: The console showing fault results.

To further validate the proposed algorithm, DC faults were impacted on less than 1% and more than 99% of the transmission lines. The fault dataset was generated from a combination of different fault scenarios such as different fault locations, different fault resistances (0Ω, 4Ω, 8Ω, 20Ω, 40Ω and 60Ω) and different fault types ($P_1, P_2, P_1 - P_2$).

The display in Fig. 4.20 shows a sample of the fault current and voltage obtained from ten different locations along the transmission line. The algorithm is further deployed to locate the fault points of the new fault samples.

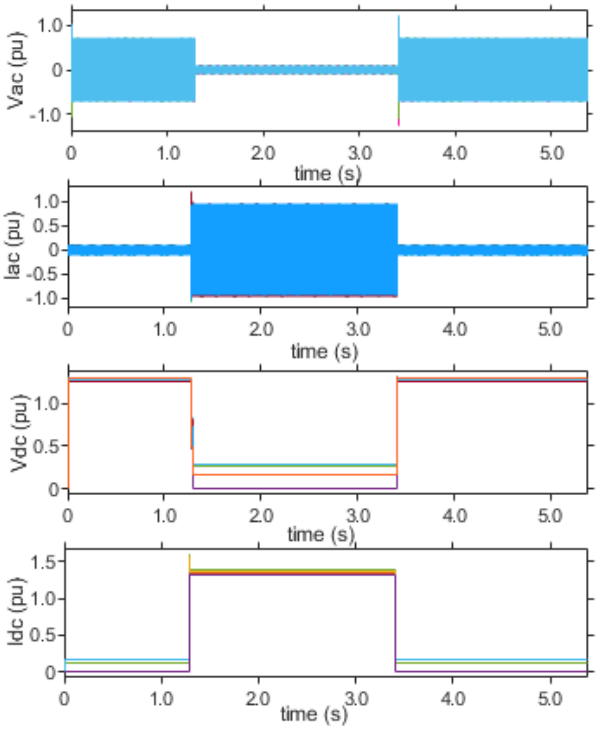


Fig. 4. 20: Current and voltage display of 37-terminal MMC HVDC system.

The performance of the algorithm is shown in Table 4.5 for faults that occur close to the nodes of the bus bar. From this table, it can be seen that the accuracy of the fault location algorithm drops slightly compared with its accuracy in Table 4.4. This is solely due to the closeness of the fault impact to the transmission line terminals, which might add some errors to the data as a result of reflections. However, the overall performance of the algorithm is still very high, with a 1% deviation in accuracy. Thus, it can be concluded that the algorithm is robust to faults occurring close to the nodes of the transmission lines and that no communication channel is required. Furthermore, it can be seen that the complexity of the network has no effect on the performance of the algorithm, as the percentage error falls within the proposed 1% tolerance.

Table 4.5: Location results for 37-terminal MMC HVDC system

Fault lines	**<1% of Transmission line**			**>99% of Transmission line**		
	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %
DPL 701 – 702	0.198	0.20	1.120	19.820	20.042	1.119
DPL 702 – 703	0.590	0.586	0.752	59.460	59.009	0.758
DPL 703 – 727	0.178	0.176	1.034	17.840	17.656	1.031

DPL 703 – 730	0.346	0.349	0.971	34.690	35.028	0.974
DPL 704 – 720	0.396	0.392	0.950	39.640	39.260	0.958
DPL 706 – 725	0.693	0.698	0.726	69.370	68.872	0.718
DPL 707 – 720	0.545	0.549	0.808	54.510	54.952	0.810
DPL 709 – 731	0.297	0.294	0.996	29.730	29.434	0.995
DPL 714 – 718	0.099	0.100	1.420	9.910	9.769	1.421
DPL 733 – 734	0.495	0.490	0.911	49.550	50.003	0.914

4.5.6 COMPARISONS WITH OTHER LOCATION SCHEMES

This section presents a brief comparison in Table 4.6 and Table 4.7 between the existing fault location methods and the proposed scheme under the same fault scenarios. One of the points of comparison is the requirement for a communication channel. Location methods that require a communication channel often encounter time delays since they need time synchronisation between installed relays on each end of the network. The AI location scheme does not have to go overcome this challenge. Also, the proposed location scheme has the least MSE (0.006).

Table 4.6: comparative analyses among AI-location schemes

Fault location methods	Communication channel requirement	Computational burden	Robustness to Noise	Sampling rate	Performance (MSE)
Decision Tree	No	Medium	High	Medium	0.048
K-nearest neighbor	No	Medium	High	High	0.670
ANN + Fast Fourier Transform	No	High	Low	High	0.889
ANN + Discrete Wavelet Transform	No	High	High	High	0.906
SVM based particle swarm optimization	No	Medium	NA	High	0.590
CNN	No	High	Medium	High	0.012
Proposed bi-LSTM	No	low	High	Medium	0.006

Table 4.7: comparative analyses among Non AI-location schemes

Fault location methods	Communication channel requirement	Computational burden	Robustness to Noise	Sampling rate	Performance (MSE)
TW	Yes	Medium	Low	High	1.990
Impedance-based	Yes	Medium	Low	High	1.206
Current differential	Yes	Medium	Low	Medium	1.405
Pearson Correlation Coefficient	Yes	Medium	Low	High	0.951
EMTR	Yes	High	Medium	High	1.153
Prony algorithm	Yes	High	Low	High	2.016
Voltage rate change	Yes	low	NA	Medium	2.301

Moreover, it can be seen from both Tables 4.6 and 4.7 that the proposed bi-LSTM has a low computational burden, and since it is independent of the communication channel, that makes it the optimal scheme for locating HVDC faults.

4.6 CONCLUSION

This chapter has proposed a fault location scheme based on the Bi-LSTM algorithm. The scheme can classify and locate faults on the transmission lines of an MMC-HVDC system with a lower sampling rate than the conventional TW based methods. The scheme can eliminate the challenges of complex data extraction and preprocessing, a condition that could lead to a high computational burden and performance limitation in real engineering applications. In addition, the scheme is accurate, without requiring a communications channel. From the simulation results obtained, it was shown that the scheme could classify fault regions with very high accuracy, and the location model could predict fault distance with a low MSE of 0.006. In addition, the location scheme is not affected by system complexities, noise, different fault types, and resistance since the percentage error obtained from each case is within 1%.

Chapter 5

5. A FAST AND ACCURATE FAULT LOCATION TECHNIQUE USING SVM AND GPR FOR HIGH VOLTAGE DIRECT CURRENT (HVDC) SYSTEMS

5.1 INTRODUCTION

In this chapter, a novel ML fault location scheme is proposed to guarantee fast fault location and improved accuracy when compared to the DL fault location scheme discussed in Chapter 4. This method utilizes data from a single source and significantly reduce computational burdens. A single-source data approach does not require a communication channel. Using a communication channel may cause unnecessary delays and poor accuracy in determining the fault location due to attenuation, interference, and multiple reflections of fault signals. Furthermore, it adds to the network's complexity and necessitates the use of a Global Positioning System (GPS) which is costly to install and maintain. Therefore, the benefits arising from the proposed technique include: improved accuracy in fault classification and location, robustness against varying fault parameters such as fault impedance, noise, and fault inception angle, the elimination of the need for a communication channel, and a computationally straightforward system that allows for real-time monitoring and fault location in a very short time frame. The proposed technique is verified using an MMC-HVDC system model that is implemented on a digital real time simulator.

The rest of the chapter is structured as follows. In Section 5.2, a detailed description of the fault location technique is presented, Section 5.3 describes the MMC-HVDC model and the real-time simulation test procedure. A comprehensive set of scenarios are then investigated, and the results

are presented in Section 5.4. To validate the proposed technique, the results are compared with other AI approaches. Section 5.5 is the conclusion.

5.2 THE FAULT LOCATION TECHNIQUE

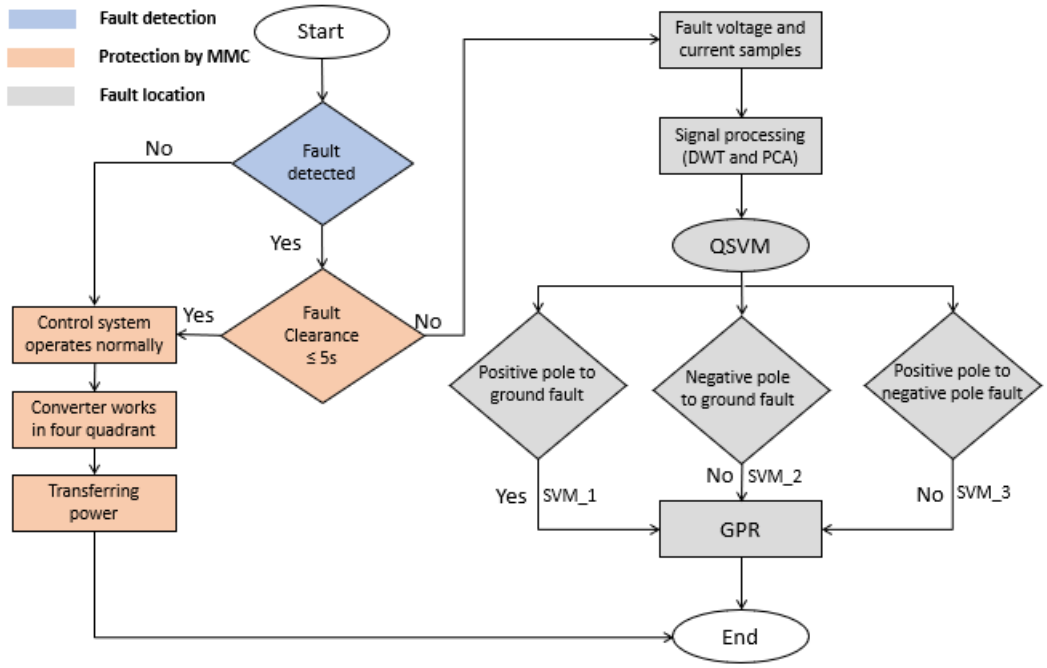


Fig.5. 1: Flow chart of the proposed technique

In Fig. 5.1, the proposed fault location technique is represented using a flowchart. The processing of the fault samples is not covered in detail; however, Discrete Wavelet Transform (DWT) is used to process the fault current and voltage samples. DWT is a feature selection method used to process fault samples because it offers better resolution, eliminates redundant fault samples, reduces the dimension of huge data sets, thereby eliminating computational burden and finally enhances speed and accuracy of the classifier [166].

The overall scheme in the flowchart comprises three stages, starting from detecting fault current and voltage signals, classifying the processed fault samples using Quadratic Support Vector Machine (QSVM) and finally, locating the fault point on the transmission line using Gaussian Process Regression (GPR). These three stages are necessary to ensure accurate fault estimation is achieved. The contribution of each stage to fault location is described below.

5.2.1 FAULT DETECTION

Fault detection is done by intelligent protective relays placed on the rectifying end of the transmission lines. Voltage and current are fed to the built-in algorithm in the relay. When a disturbance occurs in the system, a fault threshold method is used to determine the existence of fault in the system. The fault is detected when the current rises above or the voltage drops below a certain threshold. The fault detection method can be mathematically explained by obtaining the expression of the fault current.

$$i_{fault} = i_{dc} + i_{transient} \tag{5.1}$$

Since a fault causes a rapid change in the DC current, the fault information is contained in $i_{transient}$. Thus, the rate of change of current can be used to determine the presence of a fault on the system.

Considering the arm current and voltage in the MMC in Chapter 3.2.1, (5.2) and (5.3) is shown:

$$V_l = \frac{1}{2}V_{dc} + V_{ref} \qquad i_{ju} = \frac{1}{2}i_j + i_{jcir}$$

$$V_u = \frac{1}{2}V_{dc} - V_{ref} \qquad i_{jl} = \frac{-1}{2}i_j + i_{jcir} \tag{5.2}$$

And

$$V_{ju} = \frac{V_{dc}}{2} - V_s - L_o\frac{di_{ju}}{dt}$$

$$V_{jl} = \frac{V_{dc}}{2} + V_s - L_o\frac{di_{ju}}{dt} \tag{5.3}$$

Also, from the inner dynamic equations in (3.41) and (3.42), the expression for the circulating current is shown:

$$L_o\frac{di_{jcir}}{dt} = \frac{V_{dc}}{2} - \frac{1}{2}\left(V_{jl} + V_{ju}\right) \tag{5.4}$$

From (5.4), the circulating current, i_{cir} can be directly controlled by $\left(V_{jl} + V_{ju}\right)$. During a DC fault, the voltage drops below V_{dc}, consequently a high DC fault current is produced at the

converter arms. Also, from (5.4). It can be seen that the discharge of the DC fault current is governed by the DC components. Thus, the capacitor voltage dynamic of the SMs of the affected MMC units is defined as:

$$i_{Cj} = C\frac{dV_{Cj}}{dt} \tag{5.5}$$

Similarly, the net DC-side voltage dynamic is given by:

$$C_{eq}\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_p} - (i_{dcu} + i_{dcl}) \tag{5.6}$$

$$C_{eq} = \frac{3C_{sm}}{N_{arm}} \tag{5.7}$$

where C_{sm} is the submodule capacitance and N_{arm} is the number of SMs. Based on the power balance equation of the MMC, (5.8) is deduced:

$$i_{dc} = \frac{1}{V_{dc}}(v_a i_a + v_b i_b + v_c i_c) \tag{5.8}$$

The above equation represents the mathematical model of the net DC bus of the HVDC system in the abc frame. Thus, converting the abc model to dq0 frame using [167], (5.9) is obtained.

$$i_{dc} = \frac{1}{V_{dc}}\left(v_d i_d + v_q i_q\right) \tag{5.9}$$

Substitute i_{dc} from (5.9) into (5.6) gives:

$$C_{eq}\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_p} - \frac{1}{V_{dc}}\left(v_d i_d + v_q i_q\right)_l - \frac{1}{V_{dc}}\left(v_d i_d + v_q i_q\right)_u \tag{5.10}$$

According to [168], (5.10) can be written as (5.11) after multiplying both side by V_{dc}

$$\frac{d\left(\frac{1}{2}C_{eq}V_{dc}^2\right)}{dt} = -\frac{V_{dc}^2}{R_p} - \left(v_d i_d + v_q i_q\right)_l - \left(v_d i_d + v_q i_q\right)_u \tag{5.11}$$

Simplifying (5.11) by eliminating the dq0 components, (5.12) is obtained:

$$\frac{\frac{1}{2}C_{eq}d\left(V_{dc}^2\right)}{dt} = -\frac{V_{dc}^2}{R_p} \tag{5.12}$$

From (5.4), while $V_{dc} = i_{cir}R_p$

$$L_o \frac{di_{jcir}}{dt} = \frac{V_{dc}^2}{2i_{cir}R_p} - \frac{1}{2}\left(V_{jl} + V_{ju}\right) \tag{5.13}$$

Differentiating both sides gives:

$$L_o \frac{d^2 i_{jcir}}{dt^2} = \frac{1}{2i_{cir}R_p}\frac{dV_{dc}^2}{dt} - \frac{1}{2}\frac{d}{dt}\left(V_{jl} + V_{ju}\right) \tag{5.14}$$

Inserting (5.12) into (5.14) to generate (5.15)

$$L_o \frac{d^2 i_{jcir}}{dt^2} = \frac{-i_{cir}}{C_{eq}} - \frac{1}{2}\frac{d}{dt}\left(V_{jl} + V_{ju}\right) \tag{5.15}$$

where $\frac{(V_{jl}+V_{ju})}{2} = V_{dc}$

$$\frac{d^2 i_{jcir}}{dt^2} + \frac{R_p}{L_o}\frac{di_{cir}}{dt} + \frac{i_{cir}}{L_o C_{eq}} = 0 \tag{5.16}$$

Thus, the fault current can be deduced as:

$$\frac{d^2 i_{fault}}{dt^2} + \frac{R_{eq}}{L_{eq}}\frac{di_{fault}}{dt} + \frac{i_{fault}}{L_{eq}C_{eq}} = 0 \tag{5.17}$$

Where $R_{eq} = R_o + R_{line}$ and $L_{eq} = L_o + L_{line}$. The second order differential equation can be solved under the initial condition $i_{fault}(0) = I_{dc}$ to give (5.18).

$$i_{fault}(t) = e^{-\alpha t}\left[V_{dc}\sqrt{\frac{C_{eq}}{L_{eq}}}sin(\omega t) + I_{dc}\cos(\omega t)\right] \tag{5.18}$$

where $\alpha = \frac{R_{eq}}{2L_{eq}}$ and $\omega = \sqrt{\frac{1}{L_{eq}C_{eq} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}}$

The expression in (5.18) is used to configure the zone relay to a pre-set value of fault current such that when the rated current rises to the pre-set threshold, a fault signal is sent, and the fault is detected.

5.2.2 QUADRATIC SVM (QSVM)

The Support Vector Machine (SVM) identifies the faulty transmission line in a multi-terminal network. It generates an optimal plane that separates the different fault samples into distinct

regions to aid classification using the weight, ω and bias, b support vectors. In this work, the algorithm uses a quadratic kernel parameter to improve the gap between the hyperplanes of each class. QSVM can map the fault current and voltage samples into a unique global solution without overfitting (a condition where the algorithm cannot accurately classify new test samples).

Considering a bipolar network, three different regions are characterized as shown in Fig. 5.2. SVM_1 represents the region for positive pole to ground faults, SVM_2 is for the negative pole to ground faults, while SVM_3 is for the positive pole to negative pole faults.

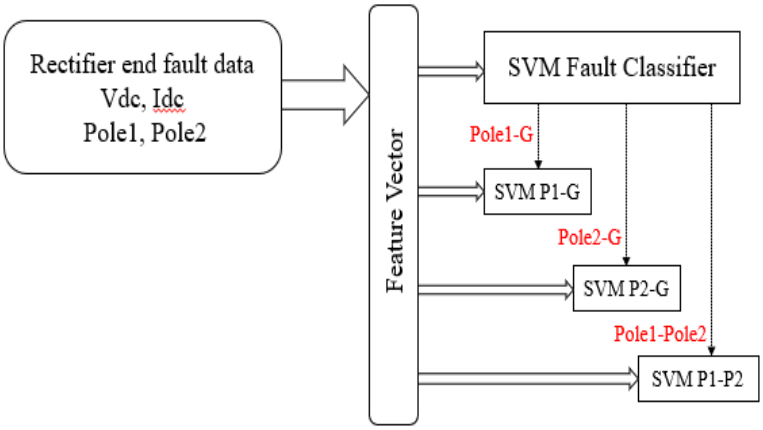


Fig.5. 2: Proposed SVM classifier

Given a training dataset of fault current and voltage samples,

$$X = \{x_1, x_2, \dots, x_n\}, x \in R^{m_0} \tag{5.19}$$

Where each training sample set x_n has m_0 input features describing a class. Three class labels are possible, one for each of three types of faults that can occur. The goal is to obtain an optimal decision boundary (hyperplane) to separate each fault sample into one of the three classes. The hyperplane is described by the equation,

$$g(x) = \omega . x + b \tag{5.20}$$

Where the weight vector, ω and constant, b are developed in a way that fault data is accurately classified. This can be done by increasing the margin of separation, d between each class. The distance, d, as a function of ω, b and x_i is given by:

$$d\big((\omega, b), x_i\big) = \frac{y_i(x_i.\omega+b)}{\|\omega\|} \tag{5.21}$$

Where, y_i is the class label. From the fault dataset X, the values of $d\big((\omega, b), x_i\big)$ for each training sample are computed. Let M be the smallest value of d obtained. M is given by:

$$M = \min_{i=1\ldots m} y_i \frac{(x_i.\omega+b)}{\|\omega\|} \tag{5.22}$$

To find an optimal hyperplane, the values of ω and b must be extrapolated. The problem of solving for the values of ω and b is the optimization problem. Therefore, to solve the optimization problem a constraint is needed where d of each fault sample will be equal to, or greater than M:

$$max_{\omega,b} M$$

$$subject\ to\ d_i \geq M, i = 1 \ldots m \tag{5.23}$$

Supposing $\not{f} = y(g(x))$ and F is the least $\not{f}$ obtained. Then:

$$F = \min_{i=1\ldots m} y_i(\omega \cdot x + b) \tag{5.24}$$

Hence, combining (5.22) and (5.24), $M = \frac{F}{\|\omega\|}$. The above optimization problem can be rewritten as:

$$max_{\omega,b} M$$

$$subject\ to\ \not{f}_i \geq F, i = 1 \ldots m \tag{5.25}$$

If the values of ω and b are rescaled, M could still be maximized, leaving the optimization result unaltered. Through rescaling ω and b as well as making $F = 1$, (5.25) can be written as:

$$max_{\omega,b} \frac{1}{\|\omega\|}$$

$$subject\ to\ \not{f}_i \geq 1, i = 1 \ldots m \tag{5.26}$$

The maximization problem in (5.26) is equivalent to the following minimization problem:

$$min_{\omega,b} \|\omega\|$$

$$subject\ to\ \not{f}_i \geq 1, i = 1 \ldots m \tag{5.27}$$

Hence, (5.26) can be written as:

$$min_{\omega,b}\frac{1}{2}\|\omega\|^2$$

$$subject\ to\ y_i(\omega \cdot x + b) - 1 \geq 0, i = 1 \ldots m \tag{5.28}$$

The above statement is the SVM optimization problem. However, it can also be restated as (5.29) using the Lagrange multiplier method to obtain the minimum of $\not{f}$ and based on (5.20).

$$\nabla\not{f}(x) - \alpha\nabla g(x) = 0 \tag{5.29}$$

Where α is called the Lagrange multiplier.

Using (5.28), the Lagrangian function is then written as:

$$\mathcal{L}(\omega, b, \alpha) = \frac{1}{2}\|\omega\|^2 - \sum_{i=1}^{m}\alpha_i[y_i(\omega \cdot x + b) - 1]. \tag{5.30}$$

To solve $\nabla\mathcal{L}(\omega, b, \alpha) = 0$ analytically, the problem is represented using the duality principle [169]. After solving the dual problem, the Lagrangian multiplier value for every fault sample is obtained. The values of ω and b, which determines the hyperplane can then be extracted. From (5.30),

$$\omega - \sum_{i=1}^{m}\alpha_i y_i x_i = 0 \tag{5.31}$$

$$\omega = \sum_{i=1}^{m}\alpha_i y_i x_i \tag{5.32}$$

Using,

$$y_i(\omega \cdot x_i^* + b) - 1 = 0 \tag{5.33}$$

and multiplying both sides by y_i and based on $y_i^2 = 1$, then

$$b = y_i - \omega \cdot x_i^* \tag{5.34}$$

Thus, b is computed as:

$$b = \frac{1}{X}\sum_{i=1}^{X}[y_i - \omega \cdot x_i^*] \quad (5.35)$$

For a bipolar MMC, X is given as either SVM_1, SVM_2 or SVM_3.

When the hyperplane is extrapolated and each region classified, the occurrence of a positive pole to ground fault, for example, is depicted by SVM_1 displaying +1, while SVM_2 for negative pole to ground and SVM_3 for pole-pole faults will both display -1. At this stage, each fault sample can be classified.

The benefit of classification is that it allows for higher computational speeds, as a large amount of data processing based on fault classifications that are irrelevant can be avoided. This is a key advantage of the proposed technique.

After classification, the Gaussian Process Regressor (GPR) approach is used to locate the fault point on the transmission line. The classification process realizes a significant advantage of the proposed approach, because only one type of fault needs to be checked for, on the transmission line.

5.2.3 GPR WITH SQUARED EXPONENTIAL KERNEL

A Gaussian Process Regression (GPR) approach is used to obtain the fault point on the grid using the mean and covariance function defined by:

$$\mathcal{y}'(d) \sim \mathcal{GP}(m(l), k(l, l')) \quad (5.36)$$

Where, $m(l)$ is the mean function and $k(l, l')$ is the covariance function. From (5.36),

$$m(l) = \mathbb{E}[\mathcal{y}'(l)] \quad (5.37)$$

$$k(l, l') = \mathbb{E}[(\mathcal{y}'(l) - m(l))(\mathcal{y}'(l') - m(l')] \quad (5.38)$$

Where $\mathbb{E}$ is the expectation. In the training phase, a set of data, S, of size *N*, from the selected transmission line, given by:

$$\mathrm{S} = \{(l_1, f_1), (l_2, f_2), \ldots, (l_N, f_N)\} \quad (5.39)$$

is collected, where l_N is the distance from the protective device to the fault point on the 300 km

transmission line and f_N is the fault generated. Assuming a fault occurred on the pole1 to ground (Pole1-G) terminal as indicated by the SVM, the distribution of faults generated at different distances is given by:

$$p(f(l)|S)\sim\mathcal{N}\big(m(l),K(l,l)\big) \tag{5.40}$$

The notations from (5.40) can be obtained using the expressions below:

$$l \triangleq [l_1, l_2, \dots, l_N]^T \tag{5.41}$$

$$f(l) \triangleq [f_1, f_2, \dots, f_N]^T \tag{5.42}$$

$$m(l) \triangleq [m(l_1), m(l_2), \dots, m(l_N)]^T \tag{5.43}$$

$$K(l,l) \triangleq \begin{bmatrix} k(l_1,l_1) & k(l_1,l_2) & \dots & k(l_1,l_N) \\ k(l_2,l_1) & k(l_2,l_2) & \cdots & k(l_2,l_N) \\ \vdots & \vdots & \ddots & \vdots \\ k(l_N,l_1) & k(l_1,l_2) & \cdots & k(l_N,l_N) \end{bmatrix} \tag{5.44}$$

When a new fault,f_* is introduced into the above equations, the distribution of the fault outputs, f and the predicted value of distance, l_* can be obtained using:

$$\begin{bmatrix} l \\ l_* \end{bmatrix} \sim \mathcal{N}\left(0, \begin{bmatrix} K(f,f) & K(f,f_*) \\ K(f_*,f) & K(f_*,f_*) \end{bmatrix}\right) \tag{5.45}$$

If there are N training points and N_* test points, then $K(f,f_*)$ denotes an $N \times N_*$ matrix of the covariance evaluated at all pairs of training and test points. The probability of an observed DC fault at a new location, l_* can be obtained using (5.46):

$$p(l_*(f_*)|S)\sim\mathcal{N}(\hat{\mu}(f_*),\hat{\sigma}^2(f_*)) \tag{5.46}$$

where,

$$\hat{\mu}(f_*) = K(f_*,f)K(f,f)^{-1}l_*, \tag{5.47}$$

$$\hat{\sigma}^2(f_*) = K(f_*,f_*) - K(f_*,f)K(f,f)^{-1}K(f,f_*) \tag{5.48}$$

The location value l_* (corresponding to the DC fault f_*) can be obtained by evaluating the mean and covariance matrix from (5.47) and (5.48).

In most realistic situations, the fault dataset could have noisy function values defined by:

$$g(x) = f(x) + \xi \tag{5.49}$$

Where, ξ is the Gaussian noise with variance σ_n^2. Therefore, the joint distribution for the predicted location becomes:

$$\begin{bmatrix} l \\ l_* \end{bmatrix} \sim \mathcal{N}\left(0, \begin{bmatrix} K(f,f) + \sigma_n^2 I & K(f,f_*) \\ K(f_*,f) & K(f_*,f_*) \end{bmatrix}\right) \tag{5.50}$$

The key predictive equations for the GPR given in (5.46) - (5.47), become.

$$p(l_*(f_*)|S) \sim \mathcal{N}(\hat{\mu}(f_*), \hat{\sigma}^2(f_*)) \tag{5.51}$$

$$\hat{\mu}(f_*) = K(f_*,f)[K(f,f) + \sigma_n^2 I]^{-1} l_*, \tag{5.52}$$

$$\hat{\sigma}^2(f_*) = K(f_*,f_*) - K(f_*,f)[K(f,f) + \sigma_n^2 I]^{-1} K(f,f_*) \tag{5.53}$$

Equations (5.51) - (5.53) are the mathematical equations used for modelling signals that include noise. It allows for the prediction of a fault location under noisy conditions to show the robustness of the proposed technique.

5.3 MMC-HVDC SYSTEM SET-UP FOR REAL-TIME SIMULATION

To verify the theory presented in Section 5.2, tests are undertaken using the model of an MMC-HVDC system implemented on a real time simulation system. A diagram illustrating the MMC-HVDC system is given in Fig. 5.3 and comprises MMC substations and HVDC transmission lines as key components. In Section 5.3.1 the MMC converter topology and the HVDC transmission line model are described. In Section 5.3.2 the real time simulation system is analyzed, along with the procedure used to verify the proposed theory.

5.3.1 THE MMC TOPOLOGY AND THE HVDC TRANSMISSION LINE

The MMC is implemented using a three-phase hybrid-arm MMC topology described in Chapter 3. Each phase of the MMC comprises an N-number of Submodules (SMs) in the lower and upper

arms of the converter. From Table 5.1, the parameters needed to model the 12 MMC SMs are presented. A fixed DC voltage of 230 kV and a grid side AC voltage of 230 kV are selected with a 26 mH inductance and a 15 mF capacitance, in accordance with the ARTEMis and SSN benchmarks available in OPAL-RT [170].

The MMC circuitry at both ends of the HVDC system model are linked by a 300 km transmission line. Previous work has shown a nominal-π lumped model is ineffective in producing accurate results for transmission line lengths exceeding $250\,km$ during fault conditions [171]. Accordingly, Bergeron's model for Distributed Parameter transmission Lines (DPL) [172], is used. For Bergeron's model, the distributed LC line is related to the impedance of the line, Z_c and the speed of wave propagation, v which are obtained using the values of inductance and capacitance in per-unit length. From Table 5.1, L and C are given as 0.792 mH/km and 0.0144 $\mu F/km$ while the resistance of the line, R is given as 0.015 Ω/km.

5.3.2 REAL-TIME SIMULATOR

The MMC-HVDC system is simulated in real-time using an OPAL-RT digital real-time simulator (DRTS) eFPGAsim OP5700, as shown in Fig. 5.4. The MMC-HVDC system is tested and validated under normal operation and fault operation conditions, with faults simulated at different distances. The fault samples for training the algorithms are generated for different fault scenarios including pole1-G, pole2-G and pole-pole fault types. These fault types are sampled at 50 μs from the rectifying end of the HVDC network, for 29 different positions along $300\,km$ transmission line with varying resistance values ranging from 0 to 1000 Ω. A total of 8700 (3 fault types, 29 fault distances and 100 fault resistances) processed fault samples were obtained from both lines and randomly split into 77% for training and 23% for testing the scheme.

An example of the fault cases obtained from the real-time simulator using the MMC-HVDC system under test are shown in Fig. 5.5. These results show the DC current and voltage from which fault samples are obtained. From the graphs it is apparent the fault occurs at 0.5 s and lasts for 0.6 s before being cleared. Also, from Fig. 5.5, a large oscillation is observed within the fault period soon after the IGBTs of the converter are blocked to prevent further damage to its switching

devices. This is caused by some non-zero AC current appearing on the DC link as discussed in Chapter 3, thus causing an energy imbalance and introducing harmonics while feeding the fault [173].

Using the approach described in this section, results can be obtained and used to verify the accuracy of the proposed fault location technique, as given in Section 5.4.

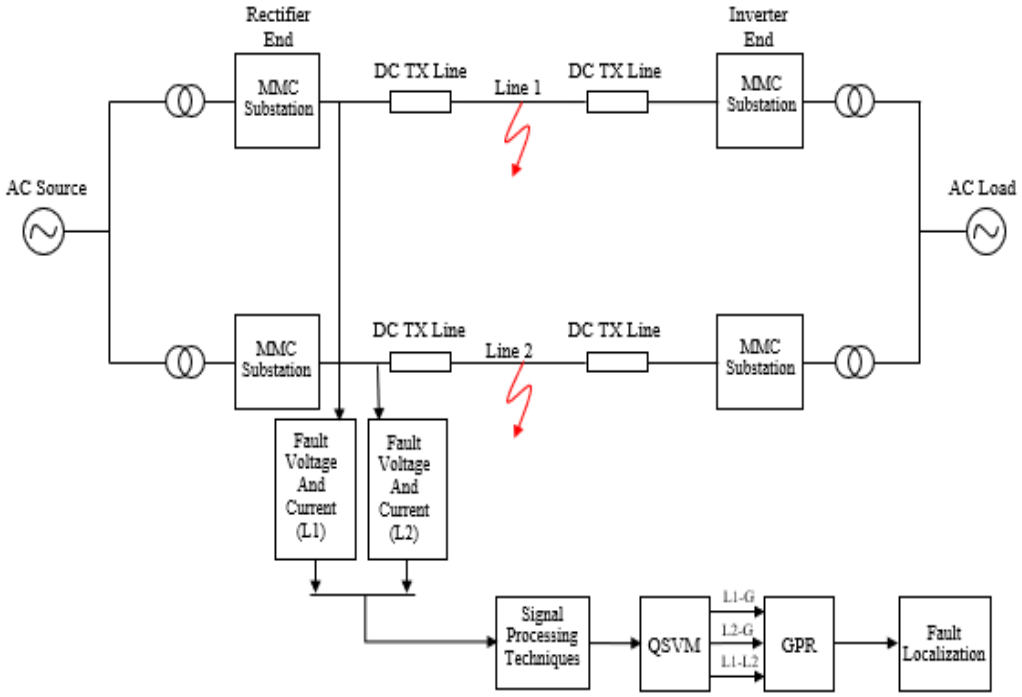


Fig.5. 3: Connection of MMC-HVDC system for testing

Table 5. 1: System parameters for designed simulation

Design Parameters	**Values**
Grid voltage	230 kV and, 60 Hz
DC Voltage	230 kV
Nominal power rating	40 MW
Capacitor voltage of SMs	1.15 kV
MMC DC current	86.96 A
Arm inductance	26 mH
Cell capacitance	15 mF
Number of MMC SMs	12
Insertion resistance	5 kΩ
Transmission line model	DPL (Bergeron) – 300 km, 0.792 mH/km, 0.0144 uF/km, 0.015 Ω/km

Fig.5. 4: OPAL-RT eFPGAsim with GUI

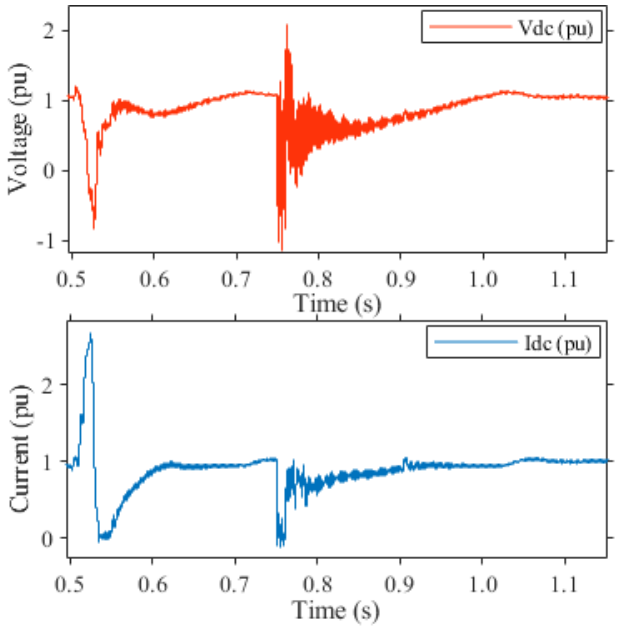


Fig.5. 5: DC current and voltage during fault

5.4 RESULTS AND ANALYSIS

The results presented in this section verify the accuracy of each of the key parts of the proposed location technique. This includes the accuracy of the SVM in classifying fault types in Section 5.4.1, and the accuracy of the fault locating in Section 5.4.2. Section 5.4.3 and Section 5.4.4 show the accuracy of the proposed technique under varying fault resistance and noise conditions, while Section 5.4.5 compares different AI fault location schemes with the proposed scheme.

5.4.1 SVM CLASSIFICATION RESULT AND ANALYSIS

To verify the SVM approach described in Section 5.2, the scheme is trained and then used to classify fault samples. The training is achieved with 6699 fault samples using a quadratic kernel function to accommodate all parameters. The outcome of the trained SVM is shown in Fig. 5.6, where the fault samples are accurately classified into three different fault types. The separating class intervals 0-1, 1-2, and 2-3 correspond to pole2-G, pole1-G, and pole-pole fault, respectively. Once the fault samples are separated, the algorithm learns and extracts the features of the faulty path of the transmission line so that when a new fault occurs on the transmission line, it can identify the exact path of the transmission line where it occurs. Fig. 5.7 shows the accuracy of the fault classification during the training phase.

The trained SVM is deployed to classify 2002 fault samples into the three different types of faults for the bipolar networks. Fig. 5.8 shows a scatter plot for the sets of fault samples of each fault type separated into different classes (Pole1-G, Pole2-G and Pole1-Pole2) using hyperplanes with a margin of 1. The high magnitude fault samples are those with low fault resistance, while the low magnitude samples have the highest resistance. Outliers are fault samples that are wrongly classified. During this test phase, five outliers were obtained from the fault samples that were classified. The misclassified fault samples belong to either the Pole1-G class or the Pole2-G class as seen in Fig. 5.8.

The performance of a typical classifier can be represented using a confusion matrix, where the accurately classified fault samples are placed on the diagonal of the matrix. Fig. 5.9 shows the confusion matrix for the test phase of the SVM. The classification accuracy is 99.7 %, which indicates that the proposed classifier is robust.

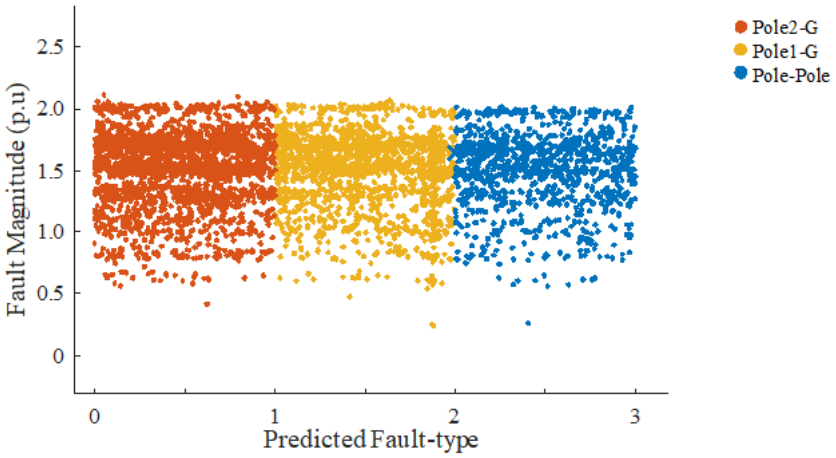


Fig.5. 6: SVM class of fault types during training phase

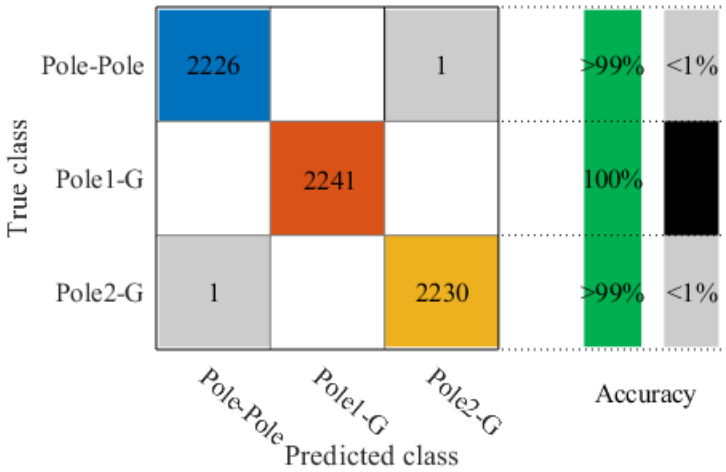


Fig.5. 7: Confusion matrix for SVM training phase

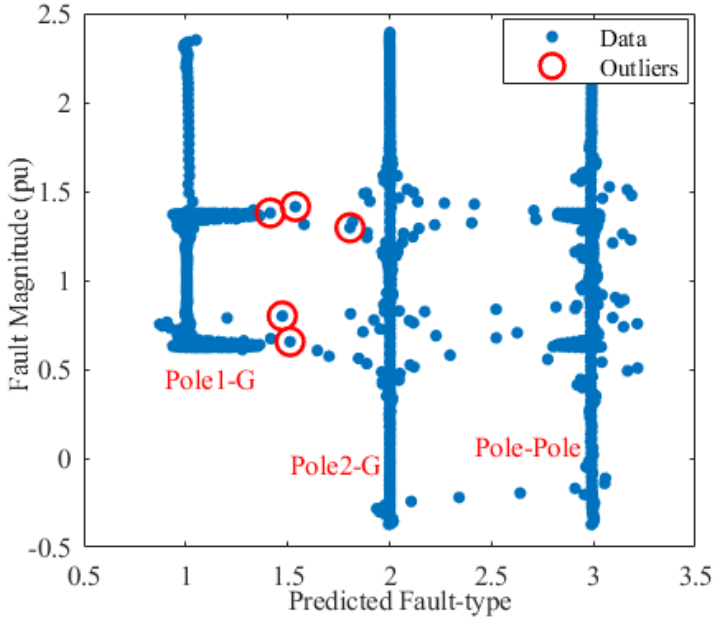


Fig.5. 8: SVM prediction of each fault types during test phase

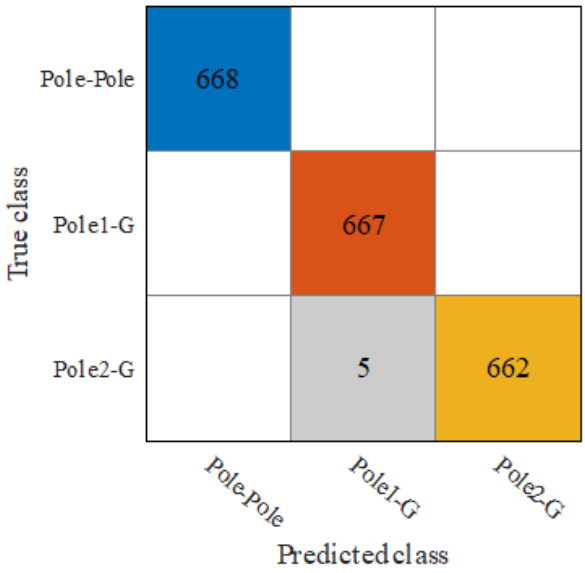


Fig.5. 9: Confusion matrix for SVM test phase

After classification, GPR can be applied to locate faults in a faster manner because the fault type is known. Locating faults using the GPR is explained in the following Section 5.4.2.

5.4.2 FAULT LOCATION RESULT AND ANALYSIS BY GPR

The GPR is trained with the fault samples generated from the different regions of the transmission lines (Pole1-G, Pole2-G and Pole1-Pole2). To verify the performance of the GPR, it is deployed to predict the location of an unknown fault. A new pole1-G fault is applied on the HVDC transmission line for 1.2 s before being cleared. The algorithm maps the fault to its trained pattern and extrapolates the distance by pattern recognition. From Fig. 5.10, the GPR measures the covariance between the true (blue fault samples) and predicted fault samples (red samples) to map out its target function, which in this case is the distance. The algorithm predicted the location to be 149.89 km by tracking the point where the magnitude of the fault is highest. The actual fault location is at 150 km on the transmission line. This shows a close agreement between the true and predicted distance.

The results of using the GPR to locate other pole1-G faults, as well as pole2-G faults and pole-pole faults, are shown in Table 5.2. The maximum time spent locating a fault of any type is 0.5197

seconds, with a Root Mean Square Error (RMSE) of 6.52e-5 percent. These results show that the proposed technique is fast and accurate.

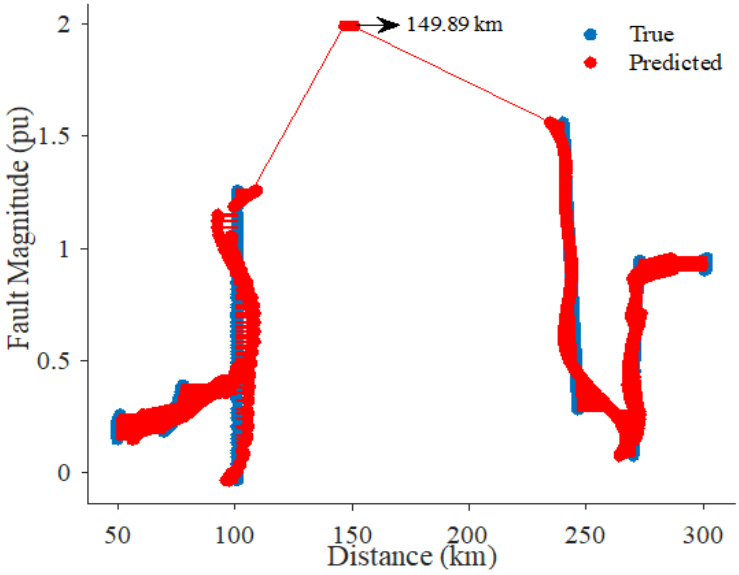


Fig.5. 10: Prediction of distance (d_*) for the new fault (f_*)

Table 5. 2: Validation of GPR result

Fault Type	Actual Fault Location, km	Predicted Fault Location, km	Percentage error, %
Pole1-G	50	49.95	0.100%
	70	70.07	0.100%
	100	99.89	0.110%
	140	140.25	0.179%
	270	270.04	0.015%
Pole2-G	50	50.01	0.020%
	70	70.22	0.314%
	100	100.28	0.280%
	240	240.11	0.046%
	270	269.99	0.004%
Pole1-Pole2	50	50.22	0.440%
	70	69.88	0.171%
	100	99.96	0.040%
	240	239.64	0.150%
	270	270.22	0.081%

5.4.3 IMPACT OF FAULT RESISTANCE ON LOCATION

During high resistance faults, locating faults is more challenging because the magnitude of the fault current is reduced, as apparent from Fig. 5.11. This tends to affect the accuracy of most locating techniques. However, for the proposed technique, it is still possible to accurately locate a fault. Table 5.3 shows the effect of resistance on fault location by testing with various fault resistances. The distance prediction error is low, and the varying fault resistance does not affect the locating time significantly. This is an indication that the proposed technique is robust to variations in resistance during a fault.

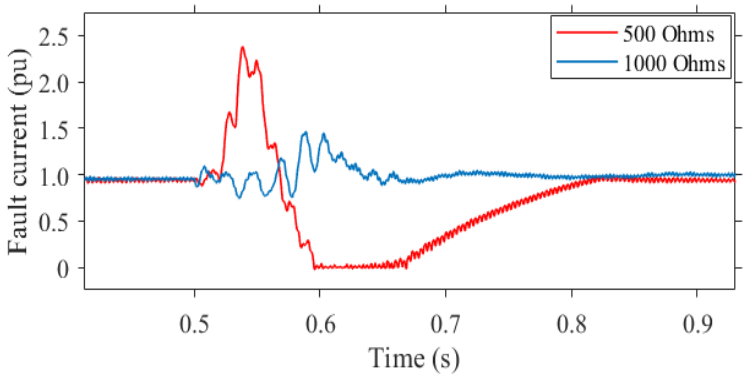


Fig.5. 11: Fault samples at different resistance

Table 5. 3: Effect of varying resistance on fault distance

Fault Resistance	0.001Ω	250 Ω	500 Ω	1000 Ω
Predicted Location at 50 km	49.95	49.01	48.76	48.02
Predicted Location at 240 km	240.11	239.78	241.55	238.89
Fault Location Time (s)	0.5193	0.5194	0.5194	0.5199

5.4.4 IMPACT OF NOISE ON LOCATION

To investigate the impact of noise on the proposed location technique, white Gaussian noise of 30 dB magnitude is added to the measured current and voltage data during the testing phase. The contaminated DC voltage is shown in Fig. 5.12. In Table 5.4, the location error from 10 dB to 90

dB is considered. As the SNR increases, the location error reduces slightly, but overall, there is no significant effect on accuracy. Hence, the proposed location scheme is robust against noise.

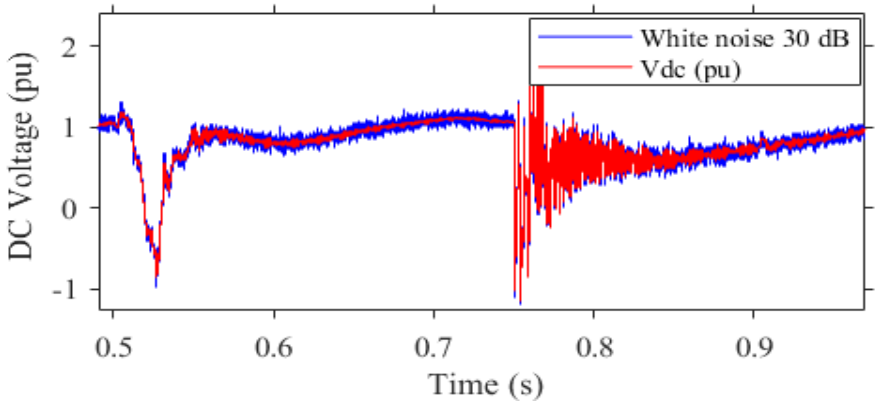


Fig.5. 12: DC voltage contaminated with 30 dB white noise

Table 5. 4: Impact of white noise on GPR location scheme

SNR (dB)	10	30	90
Fault Location error (km)	0.1052	0.0782	0.0760

5.4.5 COMPARISON AMONG DIFFERENT FAULT LOCATION SCHEMES IN IDEAL CONDITIONS

In this paper, the proposed technique is compared with existing fault location techniques under the same case study conditions as illustrated in Section 5.3. Table 5.5 shows the proposed technique has improved fault classification and location accuracy compared to alternatives. Table 5.6 shows that the computational speed of the proposed techniques is high and superior to alternatives. This performance demonstrates the effectiveness of the proposed technique over alternatives. Moreover, considering that the proposed Bi-LSTM scheme from Chapter 4 is a deep learning-based approach with numerous connected layers, it tends to be slower than the proposed approach in this chapter. Adequate tuning of the hyperparameters of the Bi-LSTM can help improve its performance.

Table 5. 5: RMSE Comparison among AI based schemes.

Location Schemes	**Root Mean Square Error (RMSE)**
Ensemble (Boosted Trees)	0.3601
Traditional Convolutional NN (CNN)	0.2371

Signal-to-Image CNN	0.1725
Bi-LSTM	0.006
Proposed scheme	6.52E-07

Table 5. 6: Speed comparison among AI based schemes.

Location Schemes	Average Location Time (s)	Number of Samples	Reference
CNN	4.08	630	[174]
Auto encoder based Deep Neural Network	2.10	630	[174]
Softmax	1.53	630	[174]
Bi-LSTM	1.053	2002	This chapter
Proposed scheme	0.5197	2002	This chapter

5.5 CONCLUSION

In this chapter, an MMC-HVDC system was modelled and simulated under normal and fault conditions through real-time simulation. The protection scheme was applied to fault data generated from only one end of the network (the rectifying end), to highlights the lack of need for a communications channel. Classification of the fault data was done after signal processing. This reduces the computational burden and the delays currently associated with AI-based techniques. Moreover, from the results obtained, it was observed that faults on the bipolar network were efficiently classified using the SVM algorithm with an accuracy of 99.7%, which is far better than current classification techniques. In addition, fault location was achieved within 0.5197 seconds, which is fast enough to prevent blocking of the MMC switching element when a fault occurs. The accuracy of the locating technique was high, with a 6.52e-5% RMSE value. Also, for further validation, the scheme was tested on a single pole to ground fault at different resistance values and noise at different SNR. It was observed that, even at high resistance, the scheme could offer high accuracy in locating faults. Thus, the application of the proposed scheme to a four-or five-terminal MMC HVDC system will be suggested as future work in this regard.

Chapter 6

6. CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

This thesis presented a novel control methodology and topology in Chapters 3 to aid DC-FRT as a means of providing primary protection against DC fault. It was shown that using the proposed solutions, DC faults can be tolerated for a period of 120 s, which is a desirable time for clearing the non-permanent faults. However, the grid is more prone to total blackouts if the fault extends beyond the specified time. A condition that would jeopardise the reliability of the power supply and result in blackouts. As such, Chapter 4 presents a backup protection strategy based on deep learning that can locate faults on a multi-terminal network so that an alternative path can be suggested for power flow. The location technique is very accurate. However, due to the number of neurons in the deep learning network, they tend to be reasonably slow. As a result, a fast and more accurate backup location scheme was presented in Chapter 5. It was shown that the scheme could locate the fault faster, meeting the speed requirement of a flexible MMC-HVDC transmission system.

6.2 SUGGESTIONS FOR FUTURE WORK

The proposed primary and backup protection scheme was simulated in real-time using the OPAL-RT digital real-time simulator. OPAL-RT offers fast control prototyping technologies to assist engineers in developing and testing novel MMC control schemes, as well as MMC lab-scale test benches to enhance technological solutions. OPAL-RT simulators imitate industry-standard communication protocols, allowing users to run the most realistic real-time simulations. The simulator infrastructure is proposed to use standard Commercial-Off-The-Shelf (COTS) components to lower system costs and maximise flexibility.

Future work is to implement the proposed schemes in an actual practical system to validate the performance of the primary and backup protection schemes. However, I do not expect much difference in the DC-FRT capability of the proposed control methodology and converter topology. Also, because the OPAL-RT simulator is a close substitute for real engineering systems, I expect the fault location accuracy and speed for MMC-HVDC systems to fall within acceptable tolerances.

REFERENCES

[1] Z. Geng and M. Han, "Fault Localization Strategy for Modular Multilevel Converters in Rectifier Mode Under Submodule Switch Open-Circuit Failure," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 12, pp. 3222-3226, Dec. 2020.

[2] J. Wang, M. Huang, C. Fu, H. Li, S. Xu and X. Li, "A New Recovery Strategy of HVDC System During AC Faults," in *IEEE Transactions on Power Delivery*, vol. 34, pp. 486-495, April 2019.

[3] Haes Alhelou, H., et al., A survey on power system blackout and cascading events: Research motivations and challenges. Energies, 2019. 12(4): p. 682.

[4] Olga P. Veloza, Francisco Santamaria, Analysis of major blackouts from 2003 to 2015: Classification of incidents and review of main causes, The Electricity Journal, Volume 29, Issue 7, 2016.

[5] Hooper, John (September 30, 2003). "Italy's blackout raises questions". The Guardian. Retrieved August 11, 2016.

[6] Kang, J.-W., I.-Y. Joo, and D.-H. Choi, *False data injection attacks on contingency analysis: Attack strategies and impact assessment.* IEEE Access, 2018. **6**: p. 8841-8851.

[7] Bambaravanage, T., S. Kumarawadu, and A. Rodrigo, Comparison of three Under-Frequency Load Shedding Schemes referring to the Power System of Sri Lanka. Engineer: Journal of the Institution of Engineers, Sri Lanka, 2016. 49(1).

[8] Criss, Doug. "Puerto Rico's power outage is now the second-largest blackout in history". CNN. Charts by Paul Martucci. Retrieved June 18, 2019.

[9] South America blackout leaves tens of millions without power". apnews.com. June 16, 2019. Retrieved June 16, 2019.

[10] Power outage hits Jakarta and Indonesia's Java and Bali islands". UPI. August 4, 2019. Retrieved August 5, 2019.

[11] M. H. Rahman, L. Xu, and L. Yao, "DC fault protection strategy considering DC network partition," in *2016 IEEE Power and Energy Society General Meeting (PESGM)*, 2016, pp. 1-5: IEEE.

[12] O. Cwikowski, H. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, "Modular multilevel converter DC fault protection," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 291-300, 2017.

[13] Y. Xue, X. Yang, T. Q. Zheng, B. Chen, and Y. Li, "A novel sub-module topology for MMC against DC side short-circuit faults," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4185-4189: IEEE.

[14] S. Yan, Z. He, J. Yang, M. Kong and M. Hu, "Optimized Protection Strategies for HVDC Grid with Fault-blocking Modular Multilevel Converters for Overhead Line Applications," in *Journal of Modern Power Systems and Clean Energy*, vol. 8, no. 6, pp. 1168-1177, November 2020.

[15] F. Sass, T. Sennewald, F. Linke, and D. Westermann, "System security of hybrid AC-HVDC-systems challenges and new approaches for combined security assessment, preventive optimization and curative actions," *Global Energy Interconnection*, vol. 1, no. 5, pp. 585-594, 2018.

[16] M. S. Alam, M. A. Y. Abido, and I. El-Amin, "Fault current limiters in power systems: A Comprehensive Review," *Energies*, vol. 11, no. 5, p. 1025, 2018.

[17] Q. Huai *et al.*, "Backup-protection scheme for multi-terminal HVDC system based on wavelet-packet-energy entropy," *IEEE Access*, vol. 7, pp. 49790-49803, 2019.

[18] Trip of transmission lines in tasmania followed by the loss of basslink on 10 and 16 dec 2014, and 23 feb 2015.

[19] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *ieee transactions on power electronics*, vol. 30, no. 1, pp. 124-137, 2014.

[20] R. Marquardt, "Modular Multilevel Converters: State of the Art and Future Progress," in IEEE Power Electronics Magazine, vol. 5, no. 4, pp. 24-31, Dec. 2018.

[21] K. Das and N. A. Cutululis, "Offshore Wind Power Plant Technology Catalogue-Components of wind power plants, AC collection systems and HVDC systems," 2017.

[22] K. Vaillancourt, G. Simbolotti, and G. Tosato, "Electricity transmission and distribution," *IEA ETSAP-Technology Brief E,* vol. 12, 2014.

[23] K. Nieradzinska, C. MacIver, S. Gill, G.A. Agnew, O. Anaya-Lara, K.R.W. Bell, Optioneering analysis for connecting Dogger Bank offshore wind farms to the GB electricity network, Renewable Energy, Volume 91, 2016, Pages 120-129.

[24] X. Ni, A. M. Gole, C. Zhao and C. Guo, "An Improved Measure of AC System Strength for Performance Analysis of Multi-Infeed HVdc Systems Including VSC and LCC Converters," in *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 169-178, Feb. 2018.

[25] Y. Xue, X. Zhang and C. Yang, "Commutation Failure Elimination of LCC HVDC Systems Using Thyristor-Based Controllable Capacitors," in *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1448-1458, June 2018.

[26] Á. Mayor, M. Rizo, A. Rodríguez Monter and E. J. Bueno, "Commutation Behavior Analysis of a Dual 3L-ANPC-VSC Phase-Leg PEBB Using 4.5-kV and 1.5-kA HV-IGBT Modules," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1125-1141, Feb. 2019.

[27] M. F. M. Arani and Y. A. I. Mohamed, "Analysis and Performance Enhancement of Vector-Controlled VSC in HVDC Links Connected to Very Weak Grids," in *IEEE Transactions on Power Systems*, vol. 32, no. 1, pp. 684-693, Jan. 2017.

[28] D. Dinkel, C. Hillermeier and R. Marquardt, "Direct Multivariable Control for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 7819-7833, July 2022.

[29] Martinez-Rodrigo, F., Ramirez, D., Rey-Boue, A.B., De Pablo, S. and Herrero-de Lucas, L.C., 2017. Modular multilevel converters: Control and applications. *Energies*, *10*(11), p.1709.

[30] S. Yang, Z. Shao, W. Zheng and F. Chen, "Mitigation of Background Harmonics Effect on MMC Controller Based on a Novel Coordinate Transformation Technique," in *IEEE Access*, vol. 7, pp. 167113-167126, 2019.

[31] Rui Li, Jing Wu, Liangzhong Yao, Yan Li and B. Williams, "Hybrid modular multilevel converter with reduced three-level cells in HVDC transmission system," *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 708-712.

[32] L. M. Bieber, L. Wang and W. Li, "A Low-Loss Thyristor-Based Hybrid Three-Level and Modular Multilevel Converter with DC Fault Blocking Capability for HVDC Transmission," in *IEEE Open Access Journal of Power and Energy*, vol. 7, pp. 111-121, 2020.

[33] L. Zhang, T. Nengling, W. Huang, L. Jian, and W. Yanhong, "A review on protection of DC microgrids," *Journal of Modern Power Systems and Clean Energy*, vol. 6, no. 6, pp. 1113-1127, 2018.

[34] G. Zou, Q. Huang, S. Song, B. Tong, and H. Gao, "Novel transient-energy-based directional pilot protection method for HVDC line," *Protection and Control of Modern Power Systems,* vol. 2, no. 1, p. 15, 2017.

[35] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit topologies modeling control schemes and applications of modular multilevel converters", *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[36] S. Debnath, J. C. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: a review,” IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[37] Y. Chen, Z. Li, S. Zhao, X. Wei and Y. Kang, "Design and implementation of a modular multilevel converter with hierarchical redundancy ability for electric ship MVDC system", *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 189-292, Mar. 2017.

[38] F. Martinez-Rodrigo, D. Ramirez, A. B. Rey-Boue, S. De Pablo, and L. C. Herrero-de Lucas, "Modular multilevel converters: Control and applications," *Energies,* vol. 10, no. 11, p. 1709, 2017.

[39] A. Sahoo, "Modular Multilevel Converter based Power Electronic Transformers for Grid Integration of Renewables and Motor Drives," 2016.

[40] R. Alaei, "Modular multilevel converters for power transmission systems," 2017.

[41] A. B. Acharya, M. Ricco, D. Sera, R. Teodorescu, and L. E. Norum, "Arm power control of the modular multilevel converter in photovoltaic applications," *Energies,* vol. 12, no. 9, p. 1620, 2019.

[42] G. Stamatiou, "Converter interactions in VSC-based HVDC systems," 2015.

[43] Z. Zheng, T. Tai, J. S. Thorp, and Y. Yang, "A transient harmonic current protection scheme for HVDC transmission line," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 2278-2285, 2012.

[44] E. Kontos, G. Tsolaridis, R. Teodorescu and P. Bauer, "On DC fault dynamics of MMC-based HVDC connections", *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 497-507, Feb. 2018.

[45] Li, R., Xu, L., Holliday, D., et al.: 'Continuous operation of radial multiterminal HVDC systems under DC fault', IEEE Trans. Power Deliv., 2016, 31, pp. 351–361.

[46] H. Liu, K. Ma, Z. Qin, P. C. Loh and F. Blaabjerg, "Lifetime estimation of MMC for offshore wind farm HVDC application", *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 504-511, Jun. 2016.

[47] Li, X., Yuan, Z., Fu, J., et al.: 'Nanao multi-terminal VSC-HVDC project for integrating large-scale wind generation'. Proc. IEEE PES General Meeting, National Harbor, MD, 2014, pp. 1–5.

[48] S. Sarkar and A. Das, "Fault Limiting Circuit based protection for DC and AC Faults in HB-MMC HVDC Systems," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021.

[49] J. Inwumoh, K. Gunawardane and C. Baguley, "Impact of Superconducting Resistive-FCL on MMC-HVDC Fault," *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, 2021, pp. 1088-1092.

[50] G. Zhang, H. Chen, L. Qu, S. Chen, and Y. Zhang, "A Family of Y-Impedance-Network Half-Bridge Converters with Additional Voltage Adjustment Function," *Energies*, vol. 12, no. 18, p. 3430, 2019.

[51] N. Ahmed et al., "Efficient modeling of an MMC-based multiterminal dc system employing hybrid HVDC breakers", *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 1792-1801, Aug. 2015.

[52] I. A. Gowaid, "A low-loss hybrid bypass for DC fault protection of modular multilevel converters", *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 599-608, Mar. 2017.

[53] S. Wang, C. E. Ugalde-Loo, C. Li, J. Liang and O. D. Adeuyi, "Bridge-Type Integrated Hybrid DC Circuit Breakers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1134-1151, June 2020.

[54] H. R. Wickramasinghe, G. Konstantinou, J. Pou, and V. G. Agelidis, "Asymmetric overlap and hysteresis current control of zero-current switched alternate arm converter," in *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 2526-2531: IEEE.

[55] Z. Shen and V. Dinavahi, "Real-Time MPSoC-Based Electrothermal Transient Simulation of Fault Tolerant MMC Topology," in *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 260-270, Feb. 2019.

[56] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah and T. Leibfried, "On Full-Bridge Bipolar MMC-HVDC Control and Protection for Transient Fault and Interaction Studies," in *IEEE Transactions on Power Delivery*, vol. 33, no. 6, pp. 2864-2873, Dec. 2018.

[57] Y. Meng, Y. Zou, H. Wang, Y. Kong, Z. Du and X. Wang, "Novel Submodule Topology with Large Current Operation and DC-Fault Blocking Capability for MMC-HVDC," in *IEEE Transactions on Power Delivery*, vol. 36, no. 3, pp. 1542-1551, June 2021.

[58] T. Zhang, Y. Xu, and L. Shi, "A Submodule Topology for Modular Multilevel Converter with Self-cleaning Ability of Direct Current Fault A Submodule Topology for Modular Multilevel Converter with Self-cleaning Ability of Direct Current Fault."

[59] X. Meng, K.-J. Li, Z. Wang, W. Yan, and J. Zhao, "A hybrid MMC topology with dc fault ride-through capability for MTDC transmission system," *Mathematical Problems in Engineering*, vol. 2015, 2015.

[60] M. Priya, P. Ponnambalam, and K. Muralikumar, "Modular-multilevel converter topologies and applications–a review," *IET Power Electronics*, vol. 12, no. 2, pp. 170-183, 2018.

[61] K. Sun, "Modular Multilevel Converter and Fault Current Management in Medium Voltage DC System of an Electric Ship," 2016.

[62] R. Li and L. Xu, "Review of DC fault protection for HVDC grids," *Wiley Interdisciplinary Reviews: Energy and Environment*, vol. 7, no. 2, p. e278, 2018.

[63] R. Zeng, L. Xu, L. Yao and D. J. Morrow, "Precharging and DC Fault Ride-Through of Hybrid MMC-Based HVDC Systems," in *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1298-1306, June 2015.

[64] S. Cui, S. Kim, J. Jung and S. Sul, "principle control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability", *Proc. IEEE 29th Appl. Power Electron. Conf. Expo.*, pp. 610-616, 2014-Mar.

[65] H. R. Wickramasinghe, G. Konstantinou, and J. Pou, "Zero-Current Switching for the Alternate Arm Converter through On-Load Tap Changers," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1342-1347: IEEE.

[66] H. R. Wickramasinghe, G. Konstantinou, Z. Li, and J. Pou, "Alternate arm converters-based HVDC model compatible with the CIGRE B4 DC grid test system," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 149-159, 2018.

[67] M. M. C. Merlin et al., "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability", *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310-317, Feb 2014.

[68] H. R. Wickramasinghe, G. Konstantinou, Z. Li and J. Pou, "Alternate Arm Converters-Based HVDC Model Compatible with the CIGRE B4 DC Grid Test System," in *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 149-159, Feb. 2019.

[69] M. Shafiul Alam and M. A. Y. Abido, "Fault ride-through capability enhancement of voltage source converter-high voltage direct current systems with bridge type fault current limiters," *Energies*, vol. 10, no. 11, p. 1898, 2017.

[70] J. Zhu, T. Wei, Q. Huo, and J. Yin, "A Full-bridge Director Switches based Multilevel Converter with DC Fault Blocking Capability and Its Predictive Control Strategy," *Energies*, vol. 12, no. 1, p. 91, 2019.

[71] J. Xu, M. Feng, H. Liu, S. Li, X. Xiong, and C. Zhao, "The diode-clamped half-bridge MMC structure with internal spontaneous capacitor voltage parallel-balancing behaviors," *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 139-151, 2018.

[72] J. Yin, J. I. Leon, L. G. Franquelo, S. Vazquez, and A. Marquez, "Cost-effective Design of Modular Multilevel Converter Employing Full-bridge Submodules," in *2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2019, pp. 1-6: IEEE.

[73] S. Wenig, "Potential of Bipolar Full-Bridge MMC-HVdc Transmission for Link and Overlay Grid Applications," 2019.

[74] A. Saha, "Control of Multilevel Converters for Voltage Balancing and Fault-tolerant Operations," University of Akron, 2017.

[75] H. You, X. Cai, L. Yao, Y. Cao, and Z. Wang, "DC fault analysis of modular DC/DC converter employing a new submodule with damping-resistor," *IEEE Access*, vol. 6, pp. 67625-67636, 2018.

[76] K. Al Hosani, T. H. Nguyen, and N. Al Sayari, "Fault-tolerant control of MMCs based on SCDSMs in HVDC systems during DC-cable short circuits," *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 379-390, 2018.

[77] X. Xia, Y. Zhou, C. Fu, Z. Zhou, and Y. He, "Research on high voltage DC transmission system optimal control based on MMC," *International Journal of Electrical Power & Energy Systems*, vol. 82, pp. 207-212, 2016.

[78] R. Li, L. Xu, L. Yu, and L. Yao, "A hybrid modular multilevel converter with reduced full-bridge submodules," *IEEE Transactions on Power Delivery*, 2019.

[79] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on power electronics*, vol. 30, no. 3, pp. 1137-1146, 2014.

[80] O. E. Oni, I. E. Davidson, and K. N. Mbangula, "A review of LCC-HVDC and VSC-HVDC technologies and applications," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1-7: IEEE.

[81] M. Ye, Q. Wei, W. Ren, and G. Song, "Modified Modulation Strategy of 1: 1: 2 Asymmetric Nine-Level Inverter and its Power Balance Method," *Electronics*, vol. 9, no. 1, p. 75, 2020.

[82] D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, "Drivers for the development of HVDC grids," *HVDC Grids Offshore Supergrid Future, Wiley*, 2016.

[83] G. Konstantinou, H. R. Wickramasinghe, S. Ceballos, and J. Pou, "Submodule voltage balancing and loss equalisation in alternate arm converters based on virtual voltages," in *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, 2018, pp. 3117-3122: IEEE.

[84] L. Zeni, *Power system integration of VSC-HVDC connected offshore wind power plants*. DTU Wind Energy, 2015.

[85] R. Li, L. Xu, and L. Yao, "DC fault detection and location in meshed multiterminal HVDC systems based on DC reactor voltage change rate," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1516-1526, 2016.

[86] Y. Liu, Y. Jin, Z. Li, Y. Liu, B. Li and Z. Duan, "Mechanical DC Breakers and Hybrid MMC Based Coordinated Strategy for MMC-HVDC DC Fault Riding Through," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[87] Y. Li, F. Gruson, P. Delarue and P. Le Moigne, "Design and control of modular multilevel DC converter (M2DC)," 2017 19th European Conference on Power Electronics and Applications.

[88] B. Li, S. Shi, Y. Zhang, R. Yang, G. Wang and D. Xu, "Analysis of the operating principle and parameter design for the modular multilevel DC/DC converter," *2015 9th*

International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015.

[89] Y. Li, X. Lyu and D. Cao, "A Zero-Current-Switching High Conversion Ratio Modular Multilevel DC–DC Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 151-161, March 2017.

[90] S. Du, B. Wu, K. Tian, D. Xu and N. R. Zargari, "A Novel Medium-Voltage Modular Multilevel DC–DC Converter," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7939-7949, Dec. 2016.

[91] S. Du, J. Liu and T. Liu, "Modulation and Closed-Loop-Based DC Capacitor Voltage Control for MMC With Fundamental Switching Frequency," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 327-338, Jan. 2015.

[92] C. Zeng, X. Du, J. Zhang and C. Du, "AC Side Impedance Modeling of Grid-Tied Modular Multilevel Converter Using Double Closed Loop Control Strategy," *2019 IEEE Innovative Smart Grid Technologies - Asia (ISGT Asia)*, 2019.

[93] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis and H. Nee, "Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy," in *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2516-2524, Nov.-Dec. 2011.

[94] J. Lyu, J. Dai, C. Zhang, J. Zhang, and X. Cai, "Impedance Characteristics Analysis of Modular Multilevel Converter with Direct Modulation and Compensated Modulation," *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019.

[95] E. Prieto-Araujo, A. Junyent-Ferre, C. Collados-Rodrıguez, G. Clariana-Colet, and O. Gomis-Bellmunt, “Control design of Modular Multilevel Converters in normal and AC fault conditions for HVDC grids,” Electr. Power Syst. Res., vol. 152, pp. 424–437, 2017.

[96] S. Wang, G. P. Adam, A. M. Massoud, D. Holliday and B. W. Williams, "Analysis and Assessment of Modular Multilevel Converter Internal Control Schemes," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 697-719, March 2020.

[97] W. Xiao-xue, A. Ting, Y. Jie and Z. Cheng-yong, "Conditions on Optimum Percentage of Second-order Harmonic Circulating Current Injection Based on MMC," *2019 IEEE 3rd Information Technology, Networking, Electronic and Automation Control Conference (ITNEC)*, 2019.

[98] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo and Y. Li, "An Inner Current Suppressing Method for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4873-4879, Nov. 2013.

[99] Marta Haro-Larrode, Maider Santos-Mugica, Pablo Eguia, Raul Rodriguez-Sanchez, Asier Gil-de-Muro, Impact of proportional resonant controller parameters of VSC connected to AC grids with variable X/R characteristic on the small signal stability, International Journal of Electrical Power & Energy Systems, Volume 118, 2020.

[100] G. Bergna, J. A. Suul, E. Berne, P. Egrot, J. Vannier and M. Molinas, "Analysis of Modular Multilevel Converters under unbalanced grid conditions with different load current control strategies and Lagrange-based differential current control," *2013 1st International Future Energy Electronics Conference (IFEEC)*, 2013.

[101] J. Kolb, F. Kammerer, M. Gommeringer and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 349-357, Jan. 2015.

[102] M. Espinoza, R. Cárdenas, M. Díaz and J. C. Clare, "An Enhanced dq-Based Vector Control System for Modular Multilevel Converters Feeding Variable-Speed Drives," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2620-2630, April 2017.

[103] A. E. Leon and S. J. Amodeo, "Energy Balancing Improvement of Modular Multilevel Converters Under Unbalanced Grid Conditions," in *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6628-6637, Aug. 2017.

[104] M. Schroeder, F. Mahr, J. Jaeger and S. Haensel, "Energy balancing in the modular multilevel converter under unbalanced grid conditions," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017.

[105] Dierks, Rebecca, Jakub Kucka, and Axel Mertens. "Using Both the Circulating Currents and the Common-Mode Voltage for the Branch Energy Control of Modular Multilevel Converters." *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*. IEEE, 2020.

[106] P. Delarue, F. Gruson and X. Guillaud, "Energetic macroscopic representation and inversion-based control of a modular multilevel converter," *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013.

[107] R. Muzzammel *et al.*, "MT–HVdc Systems Fault Classification and Location Methods Based on Traveling and Non-Traveling Waves—A Comprehensive Review," *Applied Sciences*, vol. 9, no. 22, p. 4760, 2019.

[108] Huibin Jia, "An Improved Traveling-Wave-Based Fault Location Method with Compensating the Dispersion Effect of Traveling Wave in Wavelet Domain", *Mathematical Problems in Engineering*, vol. 2017.

[109] Y. Wang, Z. Hao, B. Zhang, and F. Kong, "A pilot protection scheme for transmission lines in VSC-HVDC grid based on similarity measure of traveling waves," IEEE Access, vol. 7, pp. 7147–7158, 2019.

[110] M. Ikhide, S. Tennakoon, A. Griffiths, H. Ha, S. Subramanian, and A. Adamczyk, "Transient-based protection technique for future dc grids utilising travelling wave power," J. Eng., vol. 2018, no. 15, pp. 1267–1273, 2018.

[111] W. Li, A.Monti, and F. Ponci, "Fault detection and classification in medium voltage dc shipboard power systems with wavelets and artificial neural networks," IEEE Trans. Instrum. Meas., vol. 63, no. 11, pp. 2651–2665, Nov. 2014.

[112] SEL-411L: Line Current Differential Protection Automation and Control System. Pullman, WA, USA: Schweitzer Engineering Laboratories, Inc., 2018.

[113] A. Ahmadimanesh and S. M. Shahrtash, "Transient-based fault-location method for multiterminal lines employing S-transform", *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1373-1380, Jul. 2013.

[114] A. T. Johns, M. A. Martin, A. Barker, E. P. Walker, and P. A. Crossley, "A new approach to E.H.V. direction comparison protection using digital signal processing techniqles," IEEE Trans. Power Del., vol. PWRD-1, no. 2, pp. 24–34, Apr. 1986.

[115] S. Lin, L. Liu, P. Sun, Y. Lei, Y. Teng and X. Li, "Fault Location Algorithm Based on Characteristic- Harmonic Measured Impedance for HVdc Grounding Electrode Lines," in IEEE Transactions on Instrumentation and Measurement, vol. 69, no. 12, pp. 9578-9585, Dec. 2020.

[116] Jia, Ke. Impedance based fault location in power distribution systems. Diss. University of Nottingham, 2012.

[117] S. Lin, L. Liu, P. Sun, Y. Lei, Y. Teng and X. Li, "Fault Location Algorithm Based on Characteristic- Harmonic Measured Impedance for HVDC Grounding Electrode Lines," in IEEE Transactions on Instrumentation and Measurement, vol. 69, no. 12, pp. 9578-9585, Dec. 2020.

[118] W. A. Lewis and L. S. Tippett, "Fundamental Basis for Distance Relaying on 3-Phase Systems," in Transactions of the American Institute of Electrical Engineers, vol. 66, no. 1, pp. 694-709, Jan. 1947.

[119] K. Jia, D. W. P. Thomas and M. Sumner, "A New Double-Ended Fault-Location Scheme for Utilization in Integrated Power Systems," in *IEEE Transactions on Power Delivery*, vol. 28, no. 2, pp. 594-603, April 2013.

[120] C. Xing, S. Li and X. Xi, "Research on a Fault Location Method for a Pole-to-Pole Short-Circuit Fault in an LCC-MMC Hybrid DC Transmission System," in IEEE Access, vol. 8, pp. 165683-165692, 2020.

[121] Dutta, P., Esmaeilian, A., & Kezunovic, M. (2014). Transmission-line fault analysis using synchronized sampling. *Power Delivery IEEE Transactions on, 29*, 942–950.

[122] M. Farshad and J. Sadeh, ‘‘A novel fault-location method for HVDC transmission lines based on similarity measure of voltage signals,’’ IEEE Trans. Power Del., vol. 28, no. 4, pp. 2483–2490, Jul. 2013.

[123] Z. Wang, R. Razzaghi, M. Paolone and F. Rachidi, "Electromagnetic Time Reversal Similarity Characteristics and Its Application to Locating Faults in Power Networks," in *IEEE Transactions on Power Delivery*, vol. 35, no. 4, pp. 1735-1748, Aug. 2020.

[124] L. Wang, L. Huang, P. H. Huang et al., “Fault location method for DC hybrid line based on VMD-backward prediction Prony,” *Power Grid and Clean Energy*, vol. 36, no. 10, pp. 61–67+72, 2020.

[125] X. Pei, H. Pang, Y. Li, L. Chen, X. Ding, and G. Tang, "A Novel Ultra-High-Speed Traveling-Wave Protection Principle for VSC-based DC Grids," *IEEE Access*, vol. 7, pp. 119765-119773, 2019.

[126] J. G. Rao and A. K. Pradhan, "Improved Transverse Current Differential Protection Resistant to Power Swing," *INAE Letters*, vol. 1, no. 2, pp. 53-58, 2016.

[127] A. Maheshwari, V. Agarwal, and S. K. Sharma, "Comparative Analysis of ANN-Based FL and Travelling Wave-Based FL for Location of Fault on Transmission Lines," *Journal of The Institution of Engineers (India): Series B*, pp. 1-10, 2019.

[128] B. Li, J. He, Y. Li, and B. Li, "A review of the protection for the multi-terminal VSC-HVDC grid," *Protection and Control of Modern Power Systems*, vol. 4, no. 1, p. 21, 2019.

[129] Q. Yang, S. Le Blond, B. Cornelusse, P. Vanderbemden, and J. Li, "A Novel Fault Detection and Fault Location Method for VSC-HVDC Links Based on Gap Frequency Spectrum Analysis," *Energy Procedia*, vol. 142, pp. 2243-2249, 2017.

[130] M. Mahzarnia, A. Sheikholeslami, and J. Adabi, "A voltage stabilizer for a microgrid system with two types of distributed generation resources," *IIUM Engineering Journal*, vol. 14, no. 2, 2013.

[131] J. Descloux, "Protection contre les courts-circuits des réseaux à courant continu de forte puissance," Grenoble, 2013.

[132] G. Lugrin, R. Razzaghi, F. Rachidi, and M. Paolone, "Electromagnetic time reversal applied to fault detection: The issue of losses," in *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. 209-212: IEEE.

[133] S. Xue *et al.*, "The applicability of traditional protection methods to lines emanating from VSC-HVDC interconnectors and a novel protection principle," *Energies*, vol. 9, no. 6, p. 400, 2016.

[134] S. Xue, J. Lu, C. Liu, Y. Sun, B. Liu, and C. Gu, "A Novel Single-Terminal Fault Location Method for AC Transmission Lines in a MMC-HVDC-Based AC/DC Hybrid System," *Energies*, vol. 11, no. 8, p. 2066, 2018.

[135] J. Shabbir and T. Anwer, "Artificial intelligence and its role in near future," *arXiv preprint arXiv:1804.01396*, 2018.

[136] W.-l. LIANG and L.-q. SHANG, "The review of high voltage DC transmission lines fault location," *methods*, vol. 13, p. 15, 2014.

[137] A. Raza *et al.*, "A protection scheme for multi-terminal VSC-HVDC transmission systems," *IEEE Access*, vol. 6, pp. 3159-3166, 2017.

[138] J. Wang, X. Zheng, and N. Tai, "DC Fault Detection and Classification Approach of MMC-HVDC Based on Convolutional Neural Network," in *2018 2nd IEEE Conference on Energy Internet and Energy System Integration (EI2)*, 2018, pp. 1-6: IEEE.

[139] M. Abedrabbo and D. Van Hertem, "A primary and backup protection algorithm based on voltage and current measurements for HVDC grids," in *2016 International High Voltage Direct Current Conference (HVDC 2016)*, 2016, pp. 854-859.

[140] M. Farshad, "Detection and classification of internal faults in bipolar HVDC transmission lines based on K-means data description method," *International Journal of Electrical Power & Energy Systems*, vol. 104, pp. 615-625, 2019.

[141] S. Mehto, R. Agarwal, and M. Shah, "A Comparative Study Based on PI and Fuzzy Control of Inverter fed Induction Motor Drive," *International Journal of Research (IJR) Vol-2, Issue-2 February*, pp. 75-79, 2015.

[142] S. Dambone Sessa, A. Chiarelli, and R. Benato, "Availability Analysis of HVDC-VSC Systems: A Review," *Energies*, vol. 12, no. 14, p. 2703, 2019.

[143] K. Nagar and M. Shah, "A Review on Different ANN Based Fault Detection Techniques for HVDC Systems," *International Journal of Innovative Research in Engineering & Management (IJIREM) ISSN*, pp. 2350-0557, 2016.

[144] R. C. Santos, S. Le Blond, D. V. Coury, and R. K. Aggarwal, "A novel and comprehensive single terminal ANN based decision support for relaying of VSC based HVDC links," *Electric Power Systems Research*, vol. 141, pp. 333-343, 2016.

[145] A. Abu-Jasser and M. Ashour, "A backpropagation feedforward NN for fault detection and classifying of overhead bipolar HVDC TL using DC measurements," *Journal of Engineering Research and Technology*, vol. 2, no. 3, 2016.

[146] C.-W. Chang, H.-W. Lee, and C.-H. Liu, "A review of artificial intelligence algorithms used for smart machine tools," *Inventions*, vol. 3, no. 3, p. 41, 2018.

[147] Ö. C. Sakinci and J. Beerten, "Equivalent Multiple dq-Frame Model of the MMC Using Dynamic Phasor Theory in the alpha beta -Frame," in *IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2916-2927, Dec. 2020.

[148] S. Cui, S. Kim, J. Jung, and S. Sul, “Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability,” in Proc. IEEE 29th Appl. Power Electron. Conf. Expo., Mar. 2014, pp. 610–616.

[149] Y. Wang, C. Hu, R. Ding, L. Xu, C. Fu and E. Yang, "A Nearest Level PWM Method for the MMC in DC Distribution Grids," in *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9209-9218, Nov. 2018.

[150] X. Li, Q. Song, W. Liu, H. Rao, S. Xu and L. Li, "Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems," in *IEEE Transactions on Power Delivery*, vol. 28, no. 1, pp. 483-490, Jan. 2013.

[151] X. Li *et al*., "HVdc Reactor Reduction Method Based on Virtual Reactor Fault Current Limiting Control of MMC," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 9991-10000, Dec. 2020.

[152] Y. Shi, B. Liu, Y. Shi and S. Duan, "Individual Phase Current Control Based on Optimal Zero-Sequence Current Separation for a Star-Connected Cascade STATCOM Under Unbalanced Conditions," in *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2099-2110, March 2016.

[153] T. Bandaru, T. Bhattacharya and D. Chatterjee, "Modified predictive sorting algorithm for full-bridge MMC in HVDC application," *2017 National Power Electronics Conference (NPEC)*, 2017.

[154] J. Niu and F. Wang, "The Impact of Execution Frequency in Sorting Algorithm on Nearest Level Modulated Modular Multilevel Converter," *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019.

[155] B. Wang, Y. Liu, D. Lu, K. Yue and R. Fan, "Transmission Line Fault Location in MMC-HVDC Grids Based on Dynamic State Estimation and Gradient Descent," in *IEEE Transactions on Power Delivery*, vol. 36, no. 3, pp. 1714-1725, June 2021.

[156] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," *2011 IEEE Power and Energy Society General Meeting*, 2011.

[157] Hui Li, Xiangjie Xie, Alasdair McDonald, Zhaosen Chai, Tian Yang, You Wu, Wei Yang, Cost and reliability optimization of modular multilevel converter with hybrid submodule for offshore DC wind turbine, International Journal of Electrical Power & Energy Systems, Volume 120, 2020.

[158] M. Zygmanowski, B. Grzesik, M. Fulczyk and R. Nalepa, "Analytical and numerical power loss analysis in Modular Multilevel Converter," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 465-470.

[159] X. Xie, H. Li, Y. Hu, T. Yang, Y. Wu and Z. Chai, "Analysis of Power Loss and Reliability on Hybrid Modular Multilevel Converter with Redundancy Configuration for Offshore Wind Turbines," *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019, pp. 1-6.

[160] R. M. Burkart and J. W. Kolar, "Comparative Life Cycle Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η- ρ-σ Multiobjective Optimization Techniques," in *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4344-4358, June 2017.

[161] P. Tu, S. Yang and P. Wang, "Reliability- and Cost-Based Redundancy Design for Modular Multilevel Converter," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2333-2342, March 2019.

[162] G. Tsolaridis, H. A. Pereira, A. F. Cupertino, R. Teodorescu and M. Bongiorno, "Losses and cost comparison of DS-HB and SD-FB MMC based large utility grade STATCOM," *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1-6.

[163] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 2139-2146.

[164] Y. Tang, L. Ran, O. Alatise and P. Mawby, "Capacitor Selection for Modular Multilevel Converter," in *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3279-3293, July-Aug. 2016.

[165] J. R. Martí and A. Tavighi, "Frequency-Dependent Multiconductor Transmission Line Model with Collocated Voltage and Current Propagation," in *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 71-81, Feb. 2018.

[166] Pasi Luukka, Feature selection using fuzzy entropy measures with similarity classifier, Expert Systems with Applications, volume 38, Issue 4, 2011, Pages 4600-4607.

[167] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAR compensators," in Proc. Inst. Elect. Eng. C, Jul. 1993, vol. 140, no. 4, pp. 299–306.

[168] J. Qin and M. Saeedifard, "Predictive Control of a Modular Multilevel Converter for a Back-to-Back HVDC System," in *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1538-1547, July 2012.

[169] Scholkopf, Bernhard, and Alexander J. Smola. *Learning with kernels: support vector machines, regularization, optimization, and beyond*. Adaptive Computation and Machine Learning series, 2018.

[170] J. Wang, et al., "Performance Evaluation of Distributed Energy Resource Management via Advanced Hardware-in-the-Loop Simulation," IEEE Innovative Smart Grid Technologies Conference (ISGT), 17-20 Feb. 2020, Washington DC, USA.

[171] S. Mazumdar and K. Basu, "Hardware Emulation of Energization of a Long Transmission Line by High-Frequency Power Electronic Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9267-9280, Sept. 2020.

[172] G. Song, J. Suonan, Q. Xu, P. Chen and Y. Ge, "Parallel Transmission Lines Fault Location Algorithm Based on Differential Component Net", IEEE Trans. Power Del., vol. 20, no. 4, Oct. 2005.

[173] S. Samimi, F. Gruson, P. Delarue, F. Colas, M. M. Belhaouane and X. Guillaud, "MMC Stored Energy Participation to the DC Bus Voltage Control in an HVDC Link," in *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1710-1718, Aug. 2016.

[174] Wang, Q.; Yu, Y.; Ahmed, H.O.A.; Darwish, M.; Nandi, A.K. Fault Detection and Classification in MMC-HVDC Systems Using Learning Methods. *Sensors* 2020.

[175] Arsalan Hadaeghi, Haidar Samet, Teymoor Ghanbari, Multi extreme learning machine approach for fault location in multi-terminal high-voltage direct current systems, Computers & Electrical Engineering, Volume 78, 2019.

[176] A. Swetapadma and A. Yadav, "A Novel Decision Tree Regression-Based Fault Distance Estimation Scheme for Transmission Lines," in *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 234-245, Feb. 2017.

[177] S. Lan, M. -J. Chen and D. -Y. Chen, "A Novel HVDC Double-Terminal Non-Synchronous Fault Location Method Based on Convolutional Neural Network," in *IEEE Transactions on Power Delivery*, vol. 34, no. 3, pp. 848-857, June 2019.

APPENDIX

The control parameters for tuning the MMC-HVDC system to achieve DC-FRT are shown in Table A.1 where a damping coefficient of ζ = 0.707 is assumed. The transfer function, G(s) of the *PI* controller is given below.

Table A. 1: Parameters for the control system

	Voltage Regulator		Current Regulator		PLL (regulator gain)	
	Kp	Ki	Kp	Ki	Kp	Ki
Rectifier	0.030	3.50	0.045	4.50	0.06	1.40
Inverter	0.055	1.25	0.035	2.25	0.06	1.40

$$G_{PI}(s) = \frac{V_d(s)}{e_{i,d}(s)} = \frac{sk_p + k_i}{s}$$

$$G_{MMC}(s) = \frac{1}{sL + R}$$

$$G_{CO}(s) = G_{PI}(s) \times G_{MMC}(s) = \frac{sk_p + k_i}{s^2L + sR}$$

$$1 + G_{CO}(s)H(s) = 0$$

$$1 + \frac{sk_p + k_i}{s^2L + sR} = 0$$

$$s^2 + \left(\frac{k_p + R}{L}\right)s + \frac{k_i}{L} = 0$$

$$G_{CC}(s) = \frac{G_{CO}(s)}{1 + G_{CO}(s)H(s)} = \frac{sk_p + k_i}{s^2L + s\left(R + 2k_p\right) + k_i}$$

$$G_{CC}(s) = \frac{\frac{sk_p + k_i}{L}}{s^2 + \frac{s\left(R + 2k_p\right)}{L} + \frac{k_i}{L}}$$

$$G(s) = \frac{K\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

The expression for Kp and Ki is given below:

$$k_i = L\omega_n^2$$

$$k_p = 2L\zeta\omega_n - R$$

where ω_n is the natural frequency and for optimum design, it is assumed to be 628 *rad/s.*

Table A. 2: Comparative analysis on control schemes

Control technique	Energy balance	i_{cir} Suppression	DC-FRT
[42], [43], [50]	Only E_{sum}	X	X
[33]	X	X	√
[54]	E_{sum}, E_{diff}	X	√
Proposed scheme	$E_{sum}, E_{diff}\ and\ E_{total}$	√	√