Characterization of low-temperature bulk micromachining of silicon using an SF_6/O_2 inductively coupled plasma

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Abstract

The principal aim of this work was to characterize deep silicon etching at sample temperatures well-below room temperature, using SF_6/O_2 inductively coupled plasma (ICP) for micro-electro-mechanical systems (MEMS) applications. In this paper, a study of the etch rates and etch profiles of deep silicon trenches has been undertaken for a series of etching parameters, including RF power, sample stage temperature, and O_2 gas flow rate. Based on the experimental observations, the formation of an SiO_xF_y passivation layer, the rate of ion collision through the sheath field, and the silicon crystallographic orientation, are found to be the three main parameters that affect the etching process. In addition, the formation mechanism of "black silicon" (nanopillar-based Si structures) has also been proposed based on the experimental data and a simple physical model. For the purpose of silicon bulk micromachining, an optimized recipe has been developed that is suitable for the fabrication of high aspect ratio Si cantilevers on silicon-on-insulator (SOI) based waveguide wafers.

Introduction

The continued development of plasma etching technology is extremely important to the semiconductor device manufacturing industry, as well as being an essential process for the

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fabrication of micro-electro-mechanical systems (MEMS)[1-5], which often involves deep etching of bulk silicon. During MEMS fabrication, etching processes generally need to satisfy several requirements simultaneously, such as a high aspect ratio of physical features, high etch selectivity, near vertical etched profiles, high lateral resolution, anisotropic etch directionality and high etch rates[6]. Inductively Coupled Plasma (ICP) etching systems have been shown to be an appropriate tool for meeting these requirements due to their ability to independently control reactive species, pressure and plasma density[7].

Over the past two decades, many studies have been undertaken to achieve high silicon etch rates, anisotropic etching profiles and high aspect ratios, primarily based on either cryogenically-cooled ICP or Bosch etching processes[6,8]. Both of these deep reactive ion etching processes rely on an inductively coupled fluorine based plasma combined with the formation of a passivation layer on the exposed sidewalls to enhance the etch directionality. The primary difference between the two processes is that the Bosch process separates the etch step and the passivation step, whereas in the cryogenically-cooled process both the etch and passivation processes occur simultaneously. Compared to the Bosch process for etching silicon, cryogenically-cooled etching results in higher etch rates, lower sidewall roughness and higher etch selectivity to physical masking layers[9,10].

From a manufacturing point-of-view, it is always preferable to have processes that yield high etch rates in order to increase the throughput. In deep silicon etching, high aspect ratio physical features are generally required with nearly vertical etch profiles. In contrast, for applications requiring "through-silicon" interconnects, although high etch rates are preferred, the etch profiles are deliberately tapered to accommodate the subsequent back-side metallization process[11].

In SF_6/O_2 cryogenically-cooled ICP etching of silicon, deposition of a passivation layer on the trench sidewalls has been considered the principle mechanism whereby an anisotropic profile is achieved. During this process, O_2 supplies the O radicals that form the passivation layer, and cryogenic cooling aids formation of the passivation layer due to a reduction in both the chemical reactivity and volatility of the reaction product (SiF_4)[6]. The physical masking layer, ion energy and

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chamber pressure also have an influence on the Si etching profiles and etch rates. Although low sample stage temperature aids in formation of the passivation layer on the sidewalls that tends to prevent etching into the sidewall, a negative profile, where the trench width increases with etch depth, has been observed when the sample stage temperature is below $-130°C$[12,13]. The crystallographic orientation has been recognized as the main cause of negative trench etch profiles due to two main reasons. McFeely *et al.*[14] observed a lower etch rate on the {111}silicon surface compared to the {100} surface due to the higher energy required to break Si-Si bonds on the {111} oriented surface. In addition, Dussart *et al.* [12,13] have suggested that oxygen adsorption on {111} Si surfaces is less efficient than on {100} surfaces. Both of these mechanisms tend to result in a passivation layer on {111} oriented silicon surfaces being thinner than the passivation layer on {100} surfaces for temperatures < -130 ^{o}C. Another important issue is the regular observation of Si nanopillar structure formation during cryogenically-cooled ICP plasma etching, although no clear mechanism has been identified to explain the formation of these structures[13,15]. Initially, the physical masking layer, residual SiO_2 and dust were recognized as contributing to the formation of pillar structures (grass-like formations at the bottom of the trench)[16]. However, nanopillar structures have also been observed on bare Si wafers under a high vacuum cryogenically-cooled ICP process[13]. Dussart *et al.* observed that SiF_x is redeposited on the Si surface during such a process, possibly acting as a source to create a thicker passivation layer on the {100} oriented surface.

In this paper, sample stage temperature, O_2 gas flow, and RF power are independly varied during the etching process in order to investigate their influence on Si etching profiles and etch rates. Based on the resulting etch profiles, an optimized procedure for cryogenically-cooled silicon etching is determined. In addition, experimental evidence for the influence of crystallographic orientation on the Si trench profile was investigated, guided by the previous results of McFeely *et al.* and Dussart *et al.* Based on the rate of passivation layer formation, crystallographic orientation effects, and existing published data, a mechanism is proposed for Si nanopillar structure formation.

Experimental procedures

All etching experiments were carried out in an Oxford Instruments PlasmaLab100 RF ICP reactor. The SF_6/O_2 gas mixture was injected into the chamber via mass flow controllers (up to 200 sccm for SF_6 and up to 100 sccm for O_2). In the ICP etching system, the Si samples were attached to a handle wafer (a full-size 4 inch diameter Si wafer) using wax to ensure good thermal contact, and the handle wafer was placed on the liquid nitrogen-cooled substrate electrode. Helium backside cooling was incorporated to provide efficient temperature control of the sample, at temperatures ranging from −140 °C to −10 °C. A thermocouple is located underneath the sample stage, which is also connected with a thermal-resistance sensor. Based on the temperature of the sample stage, the thermal-resistance sensor can be used to automatically switch on/off the liquid nitrogen gas to adjust the stage temperature, resulting in a temperature error of less than 1 °C. The lower electrode was powered by an RF source at 13.56 MHz, and the chamber was pumped by a corrosion-resistant turbo-molecular pump. The chamber pressure was controlled by a 0−100 mTorr high resolution capacitance manometer. The etching conditions investigated in this study are listed in Table 1.

Silicon samples (15×15 mm^2 in area, {100} orientation, n type, 1-20 ohm·cm) were used for all cryogenically-cooled ICP etching studies. Prior to processing, the samples were first ultrasonically cleaned in successive baths of acetone, methanol and isopropyl alcohol and subsequently baked on a hot plate at 120 °C. A 1.5 µm thick patterned layer of AZ 2035 negative photoresist (MicroChem) served as a physical masking layer on the Si surface for all etching processes. Prior to cryogenically-cooled ICP etching, all photoresist-coated samples were baked on a hot plate at 120 °C for 30 min. MEMS devices typically require deep Si etching of the order of 100 µm deep,

Table 1. The etching conditions used in this study for SF_6/O_2 ICP cryogenically-cooled etching of silicon

Etching conditions	sample stage temperature (°C)	RF Power (W)	ICP Power (W)	Chamber pressure (mtorr)	O_2 gas flow (sccm)	SF_6 gas flow (sccm)	Cooling (helium) flow (sccm)	Etching time (min)
α	−105	4–14	600	10	11.5	80	10	10
β	−5 to −140	4	600	10	12	80	10	10
γ	−105	4	600	10	10–15	80	10	10

which is the target value used in this paper. In addition, since photoresist has a simple preparation process and a relatively high etch selectivity to Si during cryogenic etching, AZ 2035 negative photoresist has been chosen as a physical masking layer to form the test patterns for deep Si etching experiments. The etching time for all samples in this study was fixed at 10 min, which is approximately equal to the time required for the final device fabrication process.1-1

The etch rate of Si for each processing condition was determined from etch depth measurements using a stylus surface profilometer (Dektak 150), with an accuracy of ±10 nm. Etch depth measurements were taken on several samples that had been etched under identical conditions, and the measurements were subsequently averaged to determine the etch rate value. The silicon etching trench profiles, and any observed black silicon nanopillar features, were studied by scanning electron microscopy (SEM), with the cross-sectional profiles of the Si trenches being acquired by cleaving the samples across the etched trenches.

Experimental Results and Discussion

Figure 1 shows SEM images of trenches etched in silicon after 10 min of cryogenically-cooled ICP etching at a constant sample temperature of -105°C under condition set α (see Table 1), for RF power of 4 W (Fig. 1a), 10 W (Fig. 1b) and 14 W (Fig. 1c). It is evident that the sidewall profiles of the Si trenches become more and more negative (width at the bottom of the trench wider as the etch proceeds downwards from the top surface) with increasing RF power. The corresponding etch rates for these samples are plotted in Fig. 2, indicating a slow decrease in etch rate with increasing RF power for two RF power intervals: from 4 to 8 W and from 10 to 14 W.   However, the etch

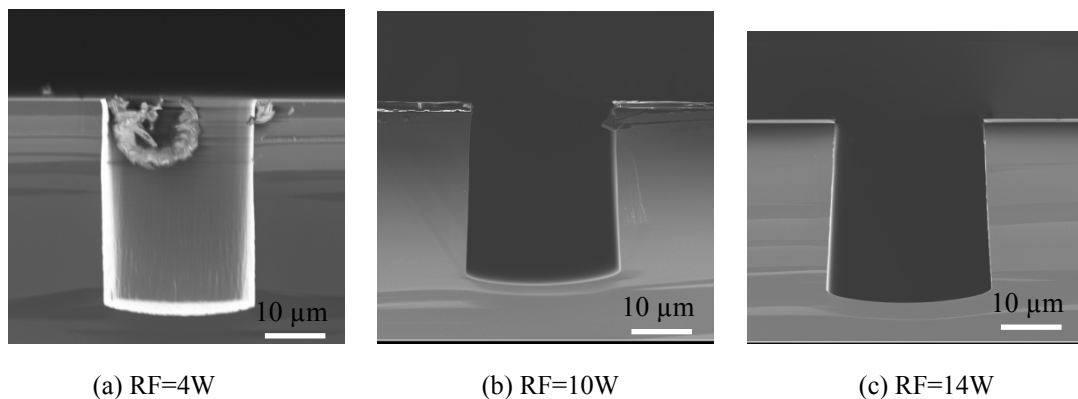| (a) RF=4W | (b) RF=10W | (c) RF=14W |

Fig. 1. SEM images of trenches etched in silicon using cryogenically-cooled ICP etching at a constant sample temperature of -105°C (condition set α in Table 1)
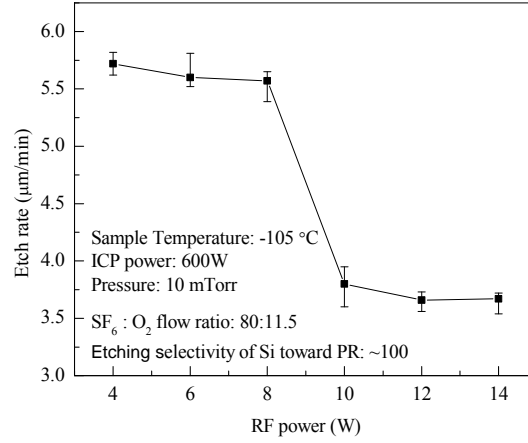
Fig. 2. Effect of RF power on silicon etch rate for etch condition set α (see Table 1)

rate shows a rapid decrease from 5.5 µm/min to 3.5µm/min as the RF power is increased from 8 W to 10 W. Essentially, ideal near-vertical etch profiles combined with high etch rates were observed for RF power in the range of 4 – 8 W. The etch selectivity of Si to photoresist (PR) for all etching recipes is around 100.

Figure 3 shows the SEM images of trenches etched in silicon using a constant RF power of 4 W

(a) Stage temperature=-5°C (b) Stage temperature=-80°C (c) Stage temperature=-90°C

(d) Stage temperature=-105°C (e) Stage temperature=-115°C (f) Stage temperature=-130°C
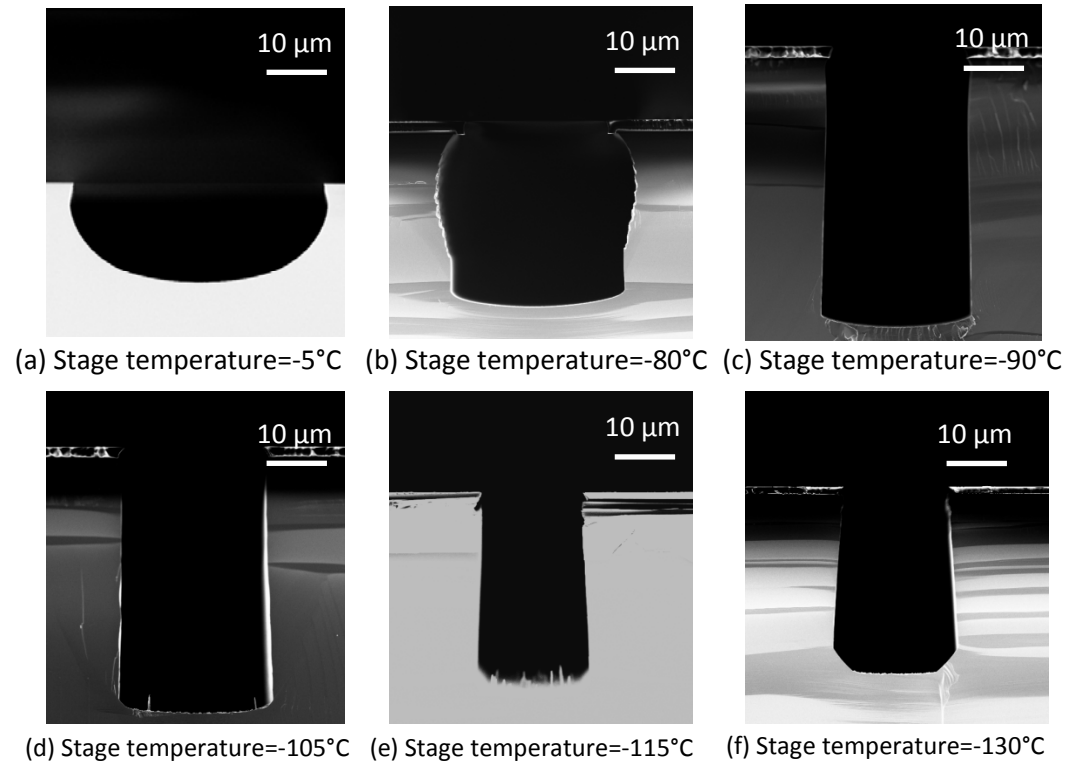
Fig. 3. SEM images of trenches etched in silicon at a constant RF power of 4 W (condition set β in Table 1).
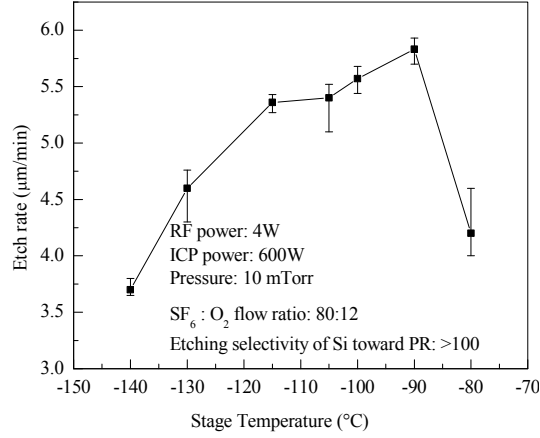
Fig. 4. Effect of sample stage temperature on Si etch rate under etch condition set β (see Table 1) and for various sample stage temperatures ranging from −5 to −130 °C. Four district trench shapes can be identified. Firstly, when the sample stage temperature is at −5 °C, the trench shows an etch profile that is indicative of isotropic etching. Also, there is no photoresist remaining after 10 min of ICP plasma etching. In the second case, the trench profile indicates partial etching anisotropy when the stage temperature is set to -80 °C. The third type of trench etch profile had nearly vertical sidewalls, and occurred for sample stage temperature in the range from -90 to -105 °C. Sample stage temperatures at -115°C and lower resulted in the fourth district trench profile shape, characterized by negative sidewall profiles and the presence of artifacts at the bottom corner of the trench associated with crystallographic orientation.

Figure 4 shows the relationship between the sample stage temperature and the resulting Si etch rate at a constant RF power of 4W (condition set β in Table 1). In general, the etch rate was found to decrease slowly with decreasing stage temperature over the range from -90 to -140 °C. However, the Si etch rate shows a much more rapid decrease, from 5.3 µm/min to 3.8 µm/min, when the sample stage temperature is reduced from -115 °C to -130 °C. A similar rapid decrease in Si etch rate was observed when the stage temperature is increased from -90 °C to -80 °C. During these etching processes, the etch selectivity of Si to PR is greater than 100.

Figure 5 shows SEM images of Si trenches etched at -105 °C with O_2 gas flows ranging from 10 sccm to 15 sccm (condition set γ in Table 1). With increasing O_2 gas flow, it is evident that the trenches etched in silicon exhibit a sidewall profile that changes gradually from a negative to a
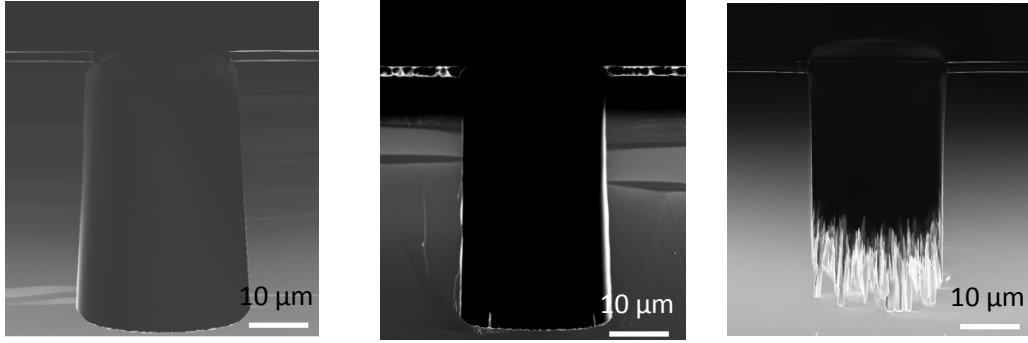
| (a) O$_2$ gas flow=10sccm | (b) O$_2$ gas flow=12sccm | (c) O$_2$ gas flow=15sccm |

Fig. 5. SEM images of trenches etched in silicon at -105 °C (condition set γ in Table 1)

positive profile. The negative, vertical and positive sidewall profiles shown in Fig. 5 (a), (b) and (c), correspond to the three O$_2$ flow rates of 10 sccm, 12 sccm and 15 sccm, respectively. In addition, when the O$_2$ gas flow rate reaches 15 sccm, a large number of miniature pillars in a "grass-like" pattern are formed at the bottom of the trench.

The influence of O$_2$ flow rate on the Si etch rate at -105 °C is plotted in Fig. 6. It is evident that higher O$_2$ gas flow rates correspond to reduced Si etch rates. The etch rate shows a rapid decrease for O$_2$ gas flow in the range from 11 sccm to 13 sccm and tends to level off outside this range. The etch selectivity of Si to PR is also greater than 100 for various O$_2$ gas flows.

Effect of RF power

The applied RF power produces an electric field between the plasma and the sample stage
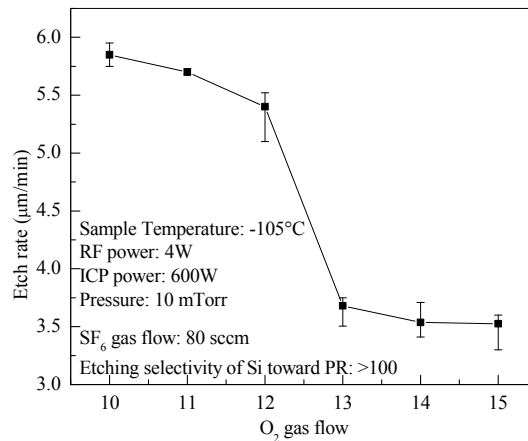

Figure 6. Etch rate of Si at -105 °C as a function of O$_2$ gas flow for etch condition set γ (see Table 1)

electrode. This electric field accelerates the ions of reactive species towards the sample, and has been recognized as the most important parameter for controlling the ion bombardment process, which directly affects the Si cryogenic etching process[9]. Increasing the RF power usually increases the energy of impinging ions which enhances the physical bombardment of the sample to be etched and, hence, results in higher physical etch rates. However, RF power also influences the intensity and size of the sheath field thickness, thus affecting the ion collision and ion bombardment direction, and the resulting sidewall profile of the trench. The condition necessary for anisotropic etching in the ICP RIE is for the ions generated via the ICP power source to pass through the dark sheath field without any collision, and thus be essentially aligned with the electric field. Based on previous studies[17], the distribution of ion bombardment angle is influenced by three main parameters, including ion-to-neutral mass ratio, the mechanism of ion-neutral scattering, and the dc value of the electric field to pressure ratio (ratio of dark sheath thickness to mean-free-path). When the ratio of sheath thickness to mean-free-path is low (less than 1), ions pass through the sheath incurring few collisions. However, when the ratio of sheath thickness to mean-free-path is larger than 1, the ion distribution angle relies on the three parameters mentioned above. In this study, SF_6 is part of the discharge gas and the ion interaction through the sheath field is a hard sphere interaction resulting in an angular distribution of bombardment ions[17]. In addition, larger ratios of sheath thickness to mean-free-path result in a greater ion angular distribution and lower ion bombardment energy.[17] The results shows in Figs. 1 and 2 are in general agreement with these previous studies.

Figure 7 shows schematically the etching mechanism for different RF powers during cryogenically-cooled ICP etching of Si. For a constant ICP power and chamber pressure, the densities of F and SF_n radicals and their mean-free-path will be constant. Two distinct etching regimes can be identified for the range of RF powers used in this study (see Fig. 7). In Regime 1, when the RF power is less than 8 W, a low sheath thickness exists in this regime, which also means a low sheath thickness to free-mean-path ratio. Because of this low ratio, few ion collisions occur through the sheath field, which contribute to ions having a narrow angular distribution. Consequently, this leads to a large ion energy obtained from the sheath, which is more efficient in
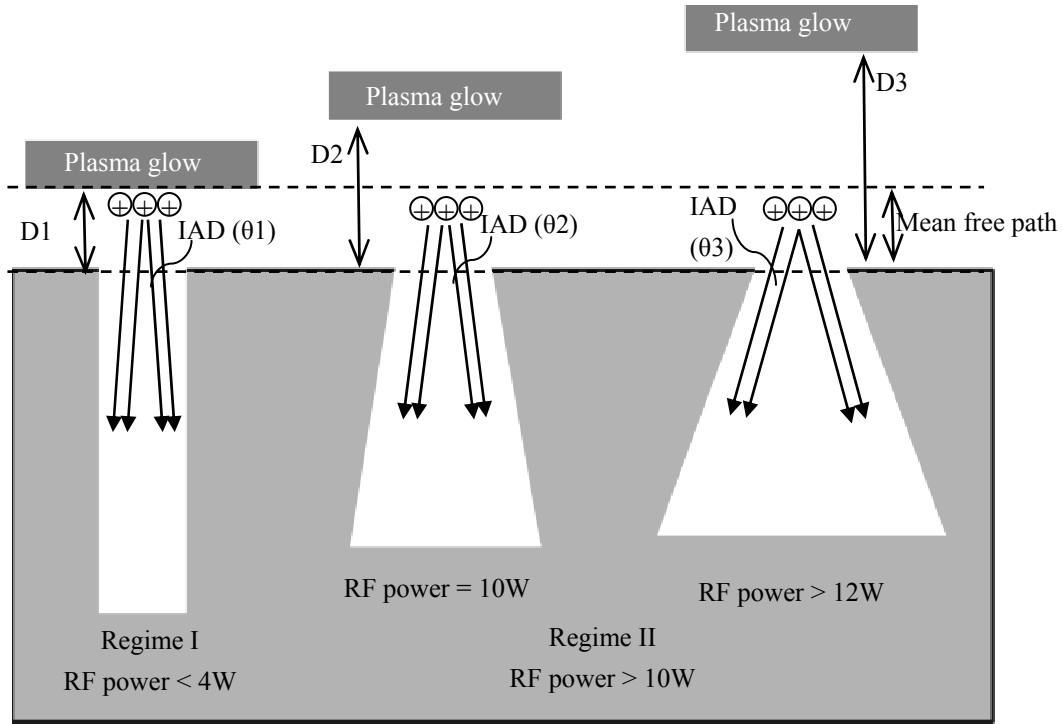
Fig. 7. Schematic demonstrating the influence of changes in RF power on the dark sheath field thickness, D, and the resulting etching mechanism (IAD: ion angular distribution)

removing the passivation layer, thus resulting in a higher Si etch rate. At the same time, passivation layer formation on the sidewall of the trench is sufficient to prevent ion bombardment because of the relatively few collisions with the trench sidewall. Therefore, a high each rate and vertical trench sidewalls can be obtained in this regime. In Regime 2 (RF > 8 W), with increasing RF power, the thickness of the sheath field increases such that it is larger than the fixed mean–free-path. In this situation, a broader ion angular distribution is present due to the larger ratio of sheath thickness to mean-free-path. Therefore, high RF powers result in increased physical ion bombardment on the trench sidewalls, removal of the sidewall passivation layer and, hence, an increase in etching of the silicon sidewall leading to negative trench profiles. In addition, the average ion energy at the bottom of the trench is reduced with increasing ratio of sheath thickness to mean-free-path, which lowers the Si etch rate. However, when the ratio is greater than about 7,[15] the average ion energy at the bottom of the trench remains a constant, which results in a constant Si etch rate, which is consistent with the etch profiles and etch rates shown in Figs. 1 and 2.

To our knowledge, no published data exist that report the effects of ICP RF power on the etch

profiles and etch rates for Si. However, studies have been undertaken on the effects of tuning the DC-bias voltage of the RF power electrode at a fixed chamber pressure to study the effect of ion energy distribution on plasma etching. Liu *et al.*[18] reported on the pressure effects on ion bombardment in RF plasmas, which indicated that larger ion incident angle corresponds to higher chamber pressure. At the same time, ions with large incident angles were shown to have much lower energies than those that were incident normal to the surface. Becker *et al.*[19] tuned the DC-bias voltage to change the sheath field thickness, which in turn modifies the distribution of ion incident angles. In general, both higher pressure and higher DC-bias correspond to higher ion incident angles, which lead to negative sidewall profiles and lower ion bombardment energy at the bottom surface of the trench. All of these results are consistent with this work: increasing RF power increases the ion incident angle distribution leading to negative etch profiles and lower etch rates.

Effect of sample stage temperature

In a cryogenically-cooled ICP etching system, the stage temperature has been recognized as the main parameter that affects the rate of formation of the passivation layer[6,20]. In particular, when the stage temperature is lower than -80 °C, lower O_2 flow is required to form a sufficiently thick SiF_xO_y passivation layer on the sidewall, which results in anisotropic etching. However, when the temperature is reduced below -130 °C, crystallographic structure effects will begin to influence the etching process, leading to differential etch rates between {111} and {100} surfaces, which results in the formation of different thicknesses of passivation layer on the respective facets of the Si surface. Figure 8 schematically summarizes the mechanism of Si cryogenically-cooled ICP etching for three ranges of stage temperature. Since insufficient SiO_xF_y is formed in the Si trench for T > -80 °C to impede the effect of physical bombardment, isotropic chemical etching results in this regime. In comparison to lower temperatures, a larger Si area is exposed to F radicals, and the lower etch rate could be the consequence of a lower local F concentration being available for Si etching. When the stage temperature is between -90 °C and -115°C, more SiF_xO_y passivation layer forms around the trench to impede physical bombardment, leading to an anisotropic profile. For

Regime I: T > –80°C   Regime II: –90 > T > –115 °C   Regime III: T < –130°C
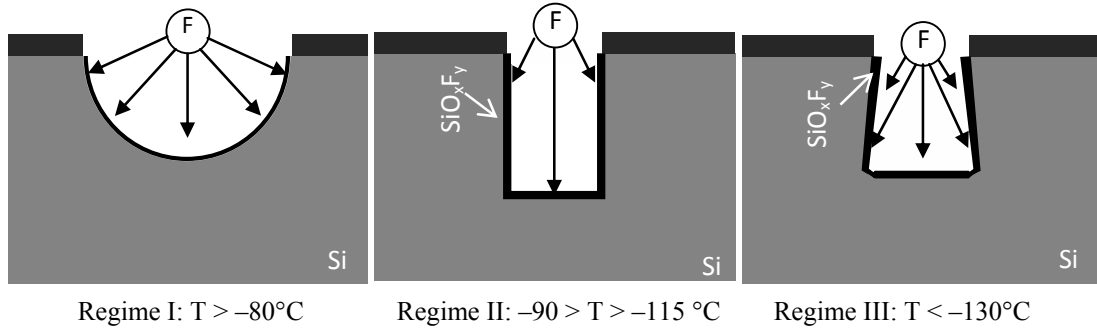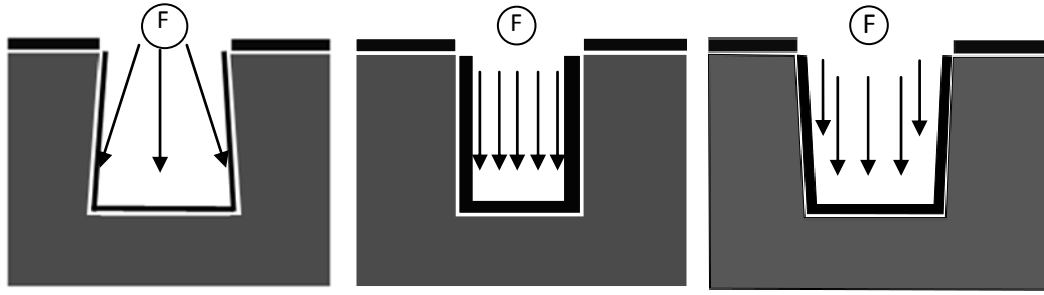
Fig. 8. Proposed etching mechanism as a function of sample stage temperature. The black area is passivation layer

sample stage temperatures lower than -130°C (third temperature regime), a thinner passivation layer will be formed on the {111} facet compared to the {100} facet, resulting in {111} facets being preferentially etched. However, considering the high energy required to break the Si-Si bonds on the {111} surface, the etch rate in the <111> direction is significantly lower in comparsion to the <100> direction. Therefore, the preferential etching and slower etch rate in the <111> direction leads to a crystallographic structure being formed at the bottom of the trench. Similarly, since more passivation inhibitor is deposited on the {100} surface for temperatures <-130°C, this leads to lower Si etch rates in this regime (see Fig. 4). This phenomenon of preferential etch rates for two different orientations in two different temperature regimes leads to the crystallographic etching results observed in this study. The proposed mechanisms affecting etch rate and etch profile are consistent with the observations shown in Figs. 3 and 4, as well as a previous study[21].

Effect of O$_2$ flow rate

The presence of oxygen is recognized as the main element responsible for forming the passivation inhibiting layer during SF$_6$/O$_2$ ICP cryogenically-cooled Si etching[9,22]. Three etching regimes are evident in our study with increasing O$_2$ gas flow, as shown in Fig. 9. In Regime I, the lower O$_2$ gas flow rate limits the formation of the SiO$_x$F$_y$ passivation inhibitor. Therefore, any passivation layer formed on the sidewall is easily removed by physical bombardment and, subsequently, the Si is etched primarily via F chemical action. With increasing O$_2$ gas flow rate, additional passivation inhibitor is deposited on the trench sidewalls (Regime II), such that the removal rate of the

Regime I.O_2 flow < 11 sccm   Regime II.O_2 flow=11-14 sccm   Regime III.O_2 flow >14 sccm

Fig. 9. Etching mechanism as a function of O_2 gas flow rate for a fixed SF_6 gas flow rate.

passivation layer by physical bombardment is balanced by the formation of passivation inhibitor, thus leading to a vertical sidewall. In Regime III, the passivation inhibitor is deposited on the sidewalls and is not readily removed by physical bombardment, resulting in a positive slope to the trench sidewalls. At the same time, the thicker passivation layer formed at the bottom of the Si trench leads to a lower etch rate, which is consistent with the results shown in Fig. 6.
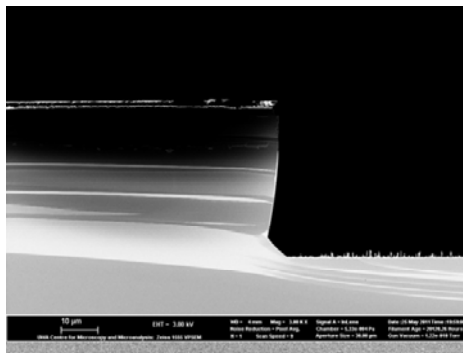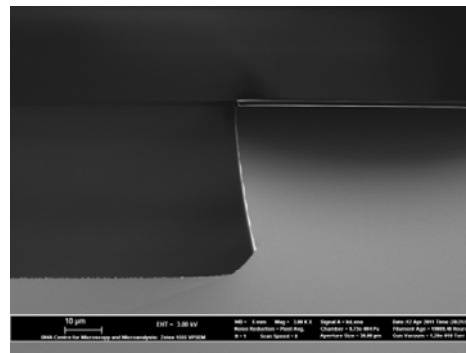
Mechanism of nanopillar structure formation
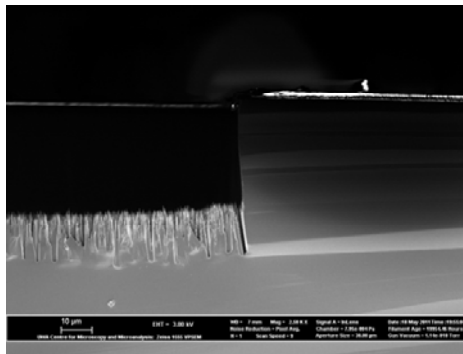
(b) Sample stage temperature= -120 °C
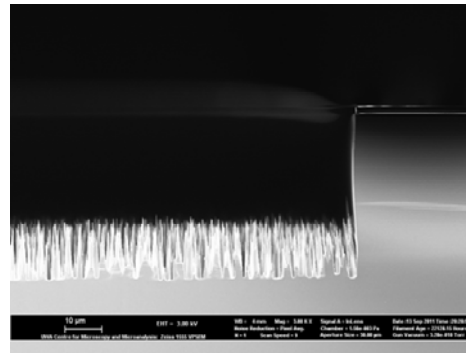
(a) Sample stage temperature= -105 °C

(c) Sample stage temperature= -130 °C

(d) Sample stage temperature= -140 °C

Fig. 10 SEM images of Si trenches after SF_6/O_2 cryogenically-cooled ICP plasma etching for various sample stage temperatures. Gas flow SF_6:O_2=80:14.5, Pressure=10mtorr, RF power=4 W, ICP power=600 W, He flow=10 sccm, Etching time=10 mins.

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In this study, nanopillar structures have been observed for the case of cryogenically-cooled ICP Si etching with high O_2 gas flow, as shown in Fig. 10 (a, b). However, when the sample stage temperature is lower than -130°C, no nanopillar structures were evident, as shown in Fig. 10 (c, d).

Dussart et al.[12,13] were able to systematically produce Si nanopillar structures for various etching recipes, including changes to SF_6/O_2 gas flow ratios, sample stage temperature, chamber pressure, and plasma bias voltages. In addition, SiF_4 re-deposition on the Si surface was found to play an important role in creating pillar structures. However, a consistent mechanism for nanopillar formation has yet to be been reported. Based on the results of Dussart et al., and the results presented in Figs. 10 to 12, the mechanism for Si nanopillar formation can be clearly explained. Figure 11 provides a simple description of nanopillar formation and its subsequent disappearance as a function of sample stage temperature. When the sample stage temperature is between -105°C and -120 °C, SiF_4 re-deposits onto the Si surface, and absorbs O to produce a random distribution of particles that form a strong passivation layer in the form of protective islands on the surface (Fig. 11a). Based on the results of Dussart et al.[13], this strong passivation layer is penetrated at many different sites due to ion bombardment. During the etching process, sufficient SiF_xO_y passivation layer is deposited on the sidewall of the islands because of the high O_2 gas flow, thus the Si nanopillar structures are gradually formed. With increasing etching time, the nanopillar structures "grow" as the etch progresses, as shown in Fig 11 (b, c). In contrast, when the stage temperature is lower than -130°C, preferential crystallographic etching result in a negative

(a) SiF$_4$ redeposited islands

(b) Positive nanopillar formation

(c) Nanopillar growth

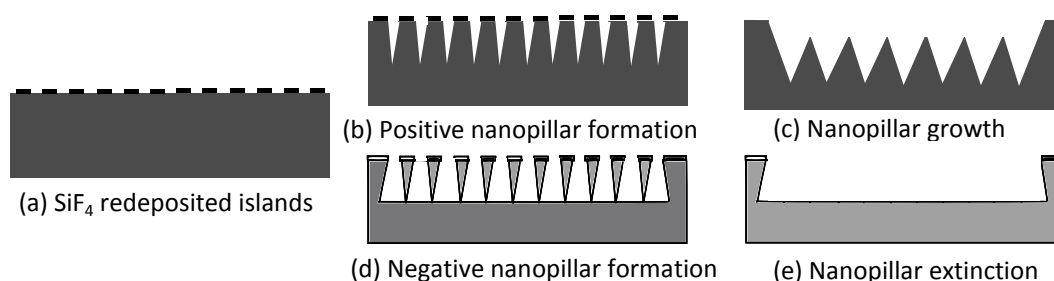(d) Negative nanopillar formation

(e) Nanopillar extinction

Fig. 11. Schematic of nanopillar formation and extinction for two different sample stage temperature ranges. (b) and (c) correspond to between -105 and -120 °C, whereas (d) and (e) correspond to T < -130 °C.

etch profile, which consumes the nanopillar structure by under-cutting with increasing etching time, as shown in Fig. 11(d, e).

Figure 12 shows the experimental results from our study, which matches well with the proposed model, shown in Fig. 11. After 1 min of etching, a high density of tiny islands of passivation are formed on the Si surface, as shown in the top left-hand image of Fig 12(a). Subsequently, the islands grow with increasing etching time.

Applications to Si cantilever fabrication

Cryogenically-cooled ICP etching, with process parameters carefully chosen from the results of this study to produce high etch rates and near vertical sidewall profiles, was used to fabricate Si cantilevers using SOI (Silicon on Insulator) wafers. ICP etching was used to etch through the underlying (100 μm thick) silicon substrate before releasing the cantilevers by removing the SiO_2 sacrificed layer. Figure 13 shows SEM images of Si cantilevers
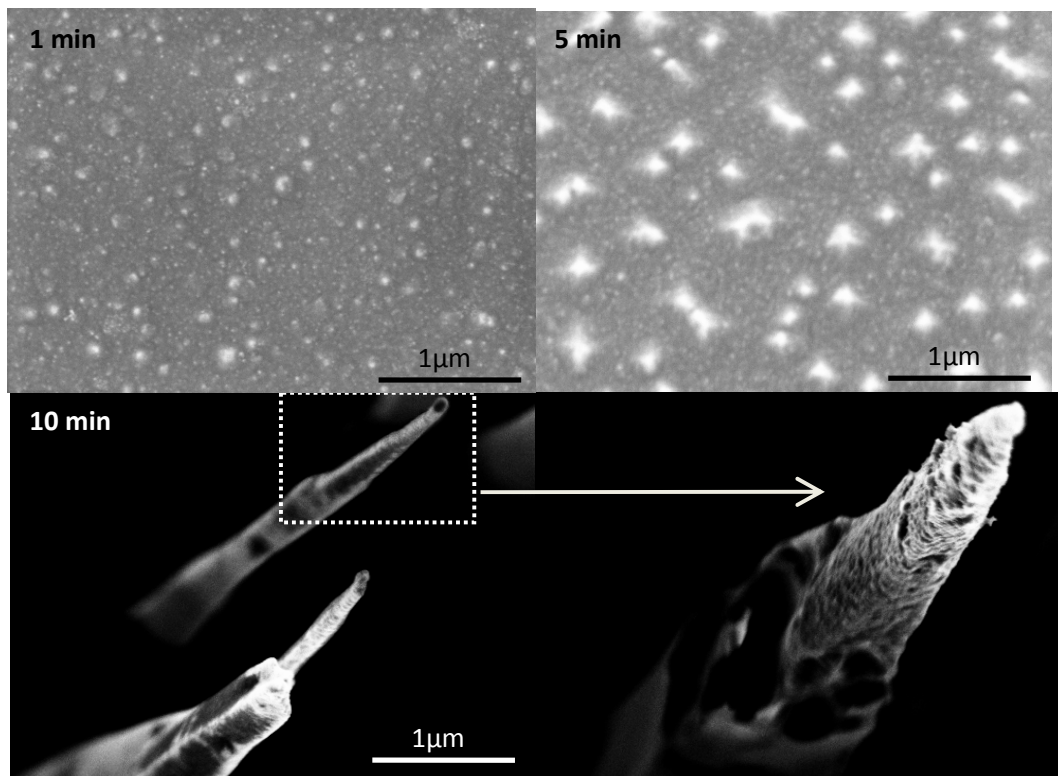

Fig. 12 Si nanopillar structure growth with increasing etching time

fabricated using the cryogenically-cooled ICP plasma etching method. Figures 13 (a, b) show side-view images of the top and bottom Si (~250 nm thick and ~100 μm thick, respectively) vertical profiles obtained after plasma etching, while Fig. 13 (c) shows a top-view of the SEM image of the Si cantilever structures. The characterization of Si cantilever structures fabricated using the cryogenically-cooled ICP etching process will be the topic of a separate study.
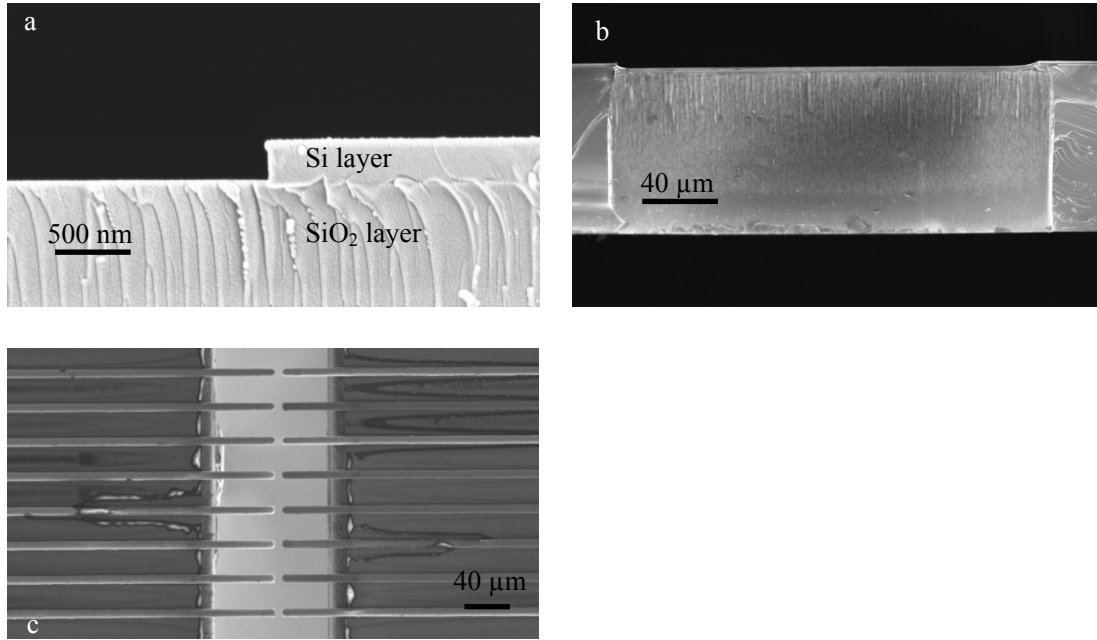

Figure 13. (a) top Si layer profile, (b) bottom Si layer trench profile; (C) Si cantilevers structure

Conclusions

A systematic study has been undertaken of cryogenically-cooled ICP etching in order to understand the effects of RF power, sample stage temperature, and O_2 gas flow rate. This work has been demonstrated that control of the resulting etch profiles require a delicate balance between deposition of SiO_xF_y passivation layer and physical ion bombardment, which needs to be carefully controlled by appropriate adjustment and control of the etching process parameters. In addition, the ratio of sheath thickness to mean-free-path, and the influence of crystallographic structure have been considered as additional parameters that can affect the etch profile. Based on this study, it is evident that changing RF power influences the ion directionality and physical bombardment energy by changing the ratio of sheath thickness to

mean-free-path. Both the sample stage temperature and O_2 gas flow have been shown to affect the Si etch rates and profiles by modifying the thickness of resulting SiO_xF_y passivation layer. A Si nanopillar formation mechanism has been proposed, which is dependent on SiF_4 redeposition, passivation layer formation, and preferential etching of different crystallographic orientations. The proposed mechanism is consistent with previous observations as well as the results of this study. The optimized etching recipe has been used to fabricate and release vertical-walled Si waveguide cantilevers on SOI wafers that have excellent mechanical and optical properties.

Acknowledgements

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