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Enhanced LV solid-state DC circuit breaker design with divided surge absorption technique☆

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ABSTRACT

This article presents an innovative design for low-voltage (LV) solid-state DC circuit breaker (SS-DCCB), incorporating the divided surge absorption technique (DSAT). This novel approach divides the circuit-breaking process into two distinct sections: a line-side surge absorber and a load-side surge damper. Upon detecting a fault through embedded current transformer (CT) measurements and microprocessor-defined thresholds, the SS-DCCB rapidly protects the system by disconnecting the load, ensuring reliable performance. The line-side surge is absorbed via a bypassed path utilizing silicon-controlled rectifier (SCRs) and a series electrolytic capacitor based subcircuit, while the load-side surge is mitigated through a circulation diode pathway. The adaptability of the proposed DSAT technique is assessed at two voltage levels: V1=300 V and V2=48 V, demonstrating its effectiveness and potential to extend in a wide range of LV and medium voltage (MV) levels. These findings validate the theoretical concept through MATLAB simulations and in-lab practical analysis demonstrated by the proposed model.

1. Introduction

The design of DC Circuit Breakers (DCCBs) for evolving network architectures presents a range of challenges, particularly with the rising integration of DC microgrids, where surge absorption is a crucial concern [1,2]. As DC systems grow more prevalent, addressing the limitations of conventional surge management techniques becomes essential [3–5]. Existing solutions, such as Mechanical DCCBs (M-DCCBs) and Hybrid DCCBs (H-DCCBs), offer potential methods for dealing with these challenges [6,7] However, they are constrained by their relatively slow response times, as M-DCCBs require milliseconds to disconnect, making them unsuitable for high-speed DC load interruptions where microsecond-scale responses are required [8]. Surge absorption technologies, particularly Metal Oxide Varistors (MOVs), have been widely used in DC systems [9]. However, these components come with significant drawbacks, including gradual degradation, increased clamping voltage, current leakage, and added capacitance, which can create safety risks in DCCB applications [10]. Despite advancements in DCCB design, a gap remains in achieving an MOV-free solution that enhances surge absorption while optimizing performance [11].

In terms of lifespan in DC applications, an MOV typically has a defined lifetime of 5.6 years [12], while an electrolytic capacitor is rated for 60,000 h at 60 °C. It is also confirmed that the DC electrolytic capacitor's impedance is minimized within a frequency range of 40 kHz [13]. In this research, based on the selected parameter values, discharge time ($t = 5 \times \tau = 5 \times RC$), and considering that the capacitor is not continuously connected to the circuit, its lifespan is expected to reach around 120 million switching cycles and surge absorption events. However, factors such as temperature and humidity can affect the performance of the surge absorber [13]. This study introduces a novel topology for DCCBs, designed to overcome the speed limitations and complexity of existing models. The proposed model has been validated at 48 V and 300 V for current thresholds of 12 A, 20 A, and 30 A, demonstrating improvements in overvoltage management across the main switch. In comparison to the BiTriCap technique, which relies on capacitors for surge absorption, the proposed design significantly increases switching speed, reduces the number of active components, simplifies control circuits, and lowers manufacturing costs [11]. Several existing DCCB designs, such as the SCR-BCB [14] and TCB [15] models, incorporate transformers, MOVs, and other active components. While these designs are effective, they introduce increased system complexity, cost, weight, and potential additional surge sources. Likewise, RB-IGCT model employing MOV-C snubbers and parallel energy absorption components face similar challenges [16]. Furthermore, previous designs that utilized capacitors for surge absorption have yet to adequately

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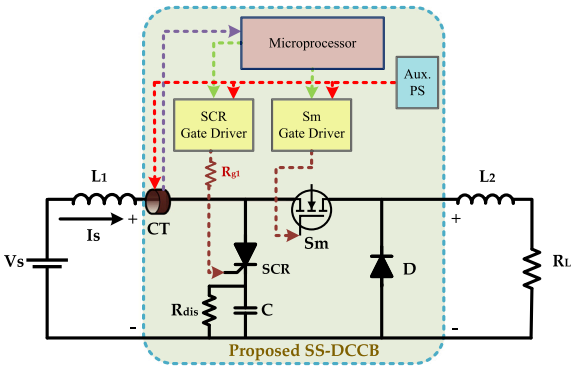


Fig. 1. Proposed SS-DCCB model scheme.

address cost concerns or account for the impact of load or line inductance on DCCB performance in practical applications [17,18]. The key innovation in this study is the development of SS-DCCB design that partitions DC surges caused by circuit interruptions into two distinct segments, one on the load side and the other on the line side. This approach ensures high-speed, reliable performance while addressing the shortcomings of existing designs. The proposed DSAT topology offers several highlighted advantages and contributions, as outlined below.

- Improved switch protection and reduced overvoltage across the main switch eliminate the need for parallel surge suppressors, thereby extending the switch's lifespan.
- The design principle has been validated for voltages up to 300 V and offers potential for further studies to adapt the design for higher voltage levels in SS-DCCBs.
- The proposed SS-DCCB incorporating the DSAT technique exhibits reliable performance, effectively absorbing surges through the capacitor's charge and discharge operation.
- Consideration of both line and load inductances ensures effective suppression of released energy, making the SS-DCCB design applicable in real-world scenarios.
- Swift switch performance, with disconnection occurring within 10 μs, ensures rapid protection of the system, SS switch, and load, thereby minimizing voltage surge.
- Efficient absorption and redirection of circuit inductive energy ensure optimal management of released energy through separate bypass routes.
- Minimization of active and passive components enhances efficiency and simplifies the design.

This study introduces an innovative model founded on the principle of dividing the effects of faults. The proposed model undergoes simulation for two distinct voltage and DC system configurations, encompassing both V_1 = 300 V and V_2 = 48 V scenarios. Additionally, practical experimentation is carried out specifically at 48 V, providing comprehensive validation of the model's flexibility across various voltage levels. The voltage levels of DC Microgrids are specified within the standards IEC60077-3, IEC61660-1, and IEC60947-2 [19].

In the proposed SS-DCCB model as shown in Fig. 1, the surges generated during switching and fault detection are carefully divided into two distinct sections: the line side and the load side. Within this design framework, the primary switch (S_m) receives protection through shock redirection employing the DSAT technique. The circuit achieves a switching frequency (rise time) of approximately 100 kHz, corresponding to a switching time of 10 μs. Upon detecting a fault threshold, the STM controller issues commands to both switches—an ON command to the SCR and an OFF command to the MOSFET. A 1 μs delay in deactivating the MOSFET is applied to account for the

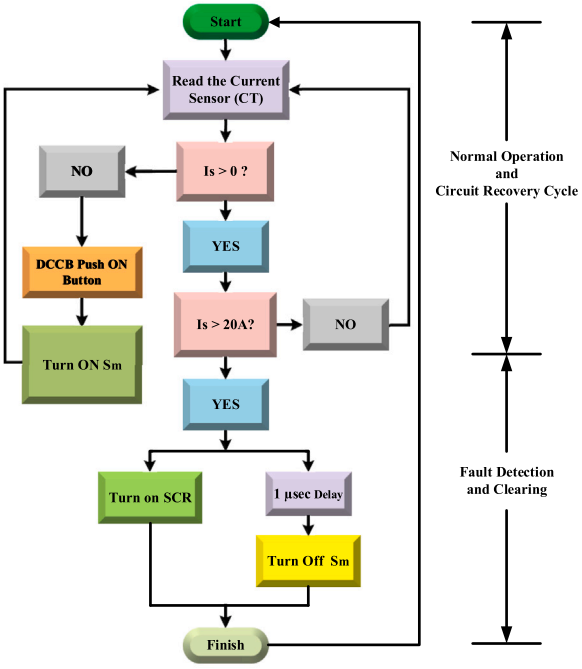
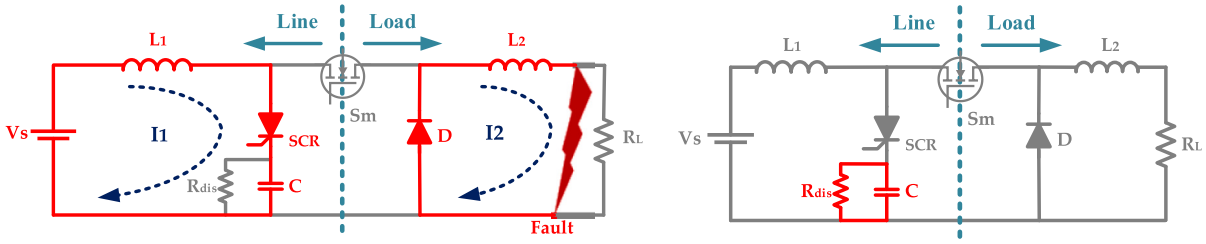


Fig. 2. Circuit operational control flowchart.

differences in switching characteristics and operational speeds between the SCR and MOSFET. This delay is accounted for in the ARM controller programming as a corresponding delay in turning on the MOSFET. According to the SKKT27B12E SCR datasheet, the SCR has a switching speed of 1 μs (equivalent to a 1 MHz switching frequency). Meanwhile, the IXFP110N15T2 MOSFET has a rise time of 44 ns, enabling it to handle circuit interruption. The overall switching operation of the proposed SS-DCCB occurs within the microsecond range. Upon receiving the SCR activation command, the released inductive energy on the line side is directed towards the electrolytic capacitor via a bypassed path, while on the load side, the discharged energy is channelled into the circulating loop created by the diode. In this design, the capacitor functions as a zero-current source (ZCS) or current-blocking element. The circuit mechanism is visually represented in the flowchart depicted in Fig. 2. During normal operation of the SS-DCCB, the circuit's current (I_s) level is checked by collecting its value by a line current transformer (CT) at intervals of 147 ns. Concurrently, the microprocessor continuously observes the circuit's performance at time intervals of 0.75 μs. Upon detection of a fault current exceeding the predefined threshold (greater than 20 A), protection command is swiftly sent to SCR, followed by a command to the Sm after 1 μs to bypass the surge into the capacitor. In proposed model, as depicted in the flowchart presented in Fig. 2, a push button is considered to activate the gate signal of S_m.

In such scenarios, the line side loop functions to block the current on the line side after absorbing the switching effects induced by L_1, effectively mitigating its impact. Simultaneously, the load side loop automatically and efficiently discharges the energy stemming from the inductance of the load side, L_2, facilitated by the inclusion of a carefully selected diode. This comprehensive approach ensures the seamless operation of the SS-DCCB, guaranteeing robust protection. In the proposed model, R_{g1} represents the gate resistance of the SCR and serves two key functions: first, it limits the output current from the gate driver, and second, it protects the microprocessor from potential damage. This strategic placement ensures the controlled and safe activation of the SCR, reducing risks and enhancing overall circuit performance. Unlike MOSFETs, which have a voltage-driven gate, the SCR gate is current-driven. To prevent current flow from the microprocessor to the thyristor, R_{g1} is incorporated into the gate circuit. To maintain



(a) Fault Detection (b) Capacitor Discharge Process

Fig. 3. Circuit fault detection operation.

uniformity in the control side of the proposed model, identical A341H gate drivers are employed.

2. Design methodology

In the process of circuit design and component selection, careful consideration must be given to two distinct categories of components: active and passive. When selecting active components, parameters such as voltage and current ratings, operational temperature limits, and the ability to handle circuit fault current based on manufacturer specifications are taken into account. For the calculation and design of passive components, such as the line side ZCS capacitor, it is imperative that they have the capability to absorb and contain the surge originating from the line side while effectively blocking the passage of current. Consequently, it is essential for the capacitor's capacity to exceed the energy released by the inductance, ensuring optimal performance as presented in Eq. (1)

$$\frac{1}{2}CV_s^2 > \frac{1}{2}L_1 I_s^2 \tag{1}$$

where, C represents the bypass ZCS capacitor, V_s denotes the voltage of the DC system, L_1 represents the inductance on the line side, and I_s signifies the maximum current flowing through the capacitor. Taking into account Eq. (1), the calculation of C can be performed for both V_1 (as described in Eq. (2)) and V_2 (as outlined in Eq. (3)) SS-DCCB designs.

$$\frac{1}{2}C_{V1}(300^2) > \frac{1}{2}(15\times10^{-3})(30^2) \tag{2}$$

$$\frac{1}{2}C_{V2}(48^2) > \frac{1}{2}(0.67\times10^{-3})(20^2) \tag{3}$$

As the simulation of the proposed model covers both V_1 and V_2 voltage levels using the same formulation, the capacitor can be determined to be C_{V1} = 150 μF for V_1 design and C_{V2} = 116 μF for V2 design.

As a critical component of the SS-DCCB design, careful consideration must be given to the discharge of the capacitor to ensure it has sufficient capacity to absorb the system surge. To assess the line and load inductances, whether for underground or overhead lines, the inductors can be calculated using the following formulas:

- For overhead transmission lines:

$$L = 2\times10^{-4}/\ln(\frac{D}{r})$$

- For underground lines:

$$L = \frac{\mu_0}{2\pi} ln(\frac{2h}{r})\times1000$$

In these equations, L represents inductance per kilometre, r and D denote the radius and diameter of the conductor, h is the depth of the conductor, and μ_0 is the permeability of free space, approximately $4\pi\times10^{-7}$ [11].

To discharge the capacitor after switching and fault detection surge absorption, the circuit utilizes a simple passive RC sub-circuit with a time constant for capacitor discharging, as implemented in this paper. Fig. 3 depicts the circuit performance during fault detection, highlighting that all current in the line side loop must flow through the capacitor, while the current through the thyristor must remain below its holding current. The holding current of the thyristor, specifically the SKKT27B12E, is 100 mA, so the current in the discharge resistor (R_{dis}) must not exceed this threshold according to the manufacturer's specifications. Therefore, once the capacitor is fully charged, the current flowing through the thyristor must remain below 100 mA, indicated as $I_1 = I_H < 100$ mA. If this condition is not met, the current could flow through the path comprising V_s-L_1-SCR–R_{dis}, potentially leading to damage to the system.

$$V_C = V_{R_{dis}} = R_{dis} I_H \tag{4}$$

where, VC represents the voltage across the capacitor, Rdis denotes the discharge resistance, and IH stands for the holding current of the SCR. For the V2 design with VS = 48 V, the maximum voltage across the capacitor would be VC = 76.8 V. Accordingly, Rdis is calculated as 768 Ω. Using a similar calculation, in the scenario of V1 application with VS = 300 V, the capacitor voltage increases to VC = 363 V during fault detection. Consequently, the discharge resistor can be determined as R_{dis} = 3630 Ω.

When designing the diode for the load side, it is imperative to ensure its capability to withstand the current released in the load side inductance. This consideration serves to minimize the complexity of the circuit design.

When a fault occurs across the load, such as a short circuit, the line current measured by the sensor (CT) is compared with a predefined setpoint within the controller. The controller conducts measurements of the current sensor value seven times per microsecond. Upon detecting a short circuit, indicated by the measured current exceeding the defined threshold, the controller commands the SCR connection and then main switch (MOSFET) disconnection. In this scenario, the circuit is divided into two sections, as depicted in Fig. 3(a). As a result, two distinct loops emerge. The fault current and the released energy from the load side loop are discharged via the D-L_2-$Fault$ path. Meanwhile, on the line side, the released energy is redirected to the capacitor through the V_s-L_1-SCR-C path. Subsequently, once the ZCS capacitor is fully charged, the current is obstructed from the path, effectively creating an open circuit.

Once the capacitor has fully absorbed the surge, the SCR automatically turns off, as the current is blocked in loop 1. The capacitor then discharges through the R_{dis}-C loop, as illustrated in Fig. 3(b).

The primary achievements of this technique include: (1) load protection, (2) shielding the solid-state main switch from surges and shocks during switching operations, (3) simplifying the DCCB and circuit design, (4) fortifying the circuit's resilience against faults, whether they occur on the line or load side, (5) reliable operation, and (6) quick performance.

By considering the circuit performance depicted in Fig. 3, it becomes feasible to compute the currents circulating within each loop. In order

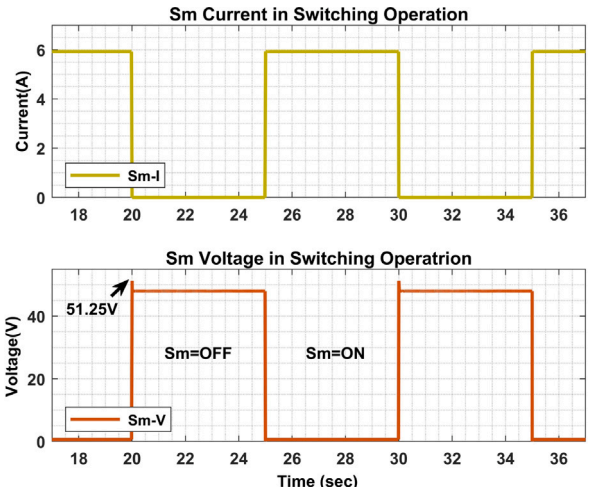


Fig. 4. Simulation results: S_m current and voltage in switching operation.

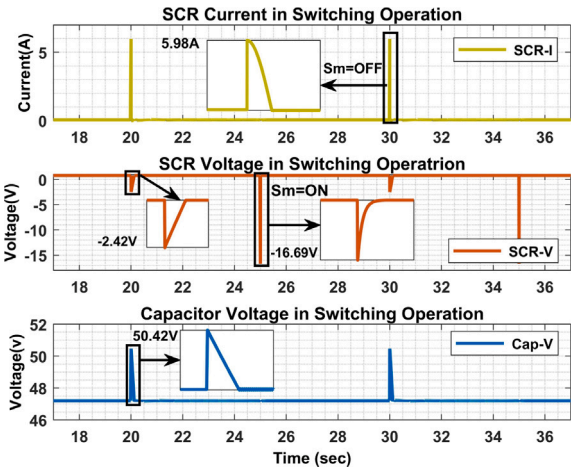


Fig. 5. Simulation results: SCR current and voltage, Capacitor voltage in switching operation.

to characterize the transient behaviour of I_1, Eq. (5) is employed based on KVL in V_S-L_1-SCR-C.

$$I_1(t) = \frac{1}{L_1}\int \left(V_s - V_{SCR} - V_C\right) dt + i_1(t_f) \tag{5}$$

where, I1 represents the current flowing through loop 1 during fault time, with L_1 denoting the inductance on the line side. Additionally, Vs signifies the voltage of the DC system, V_{SCR} represents the voltage across the SCR, V_C stands for the capacitor voltage, and $i_1(tf)$ indicates the initial current in the inductance during fault time. Moreover, the calculation of the current in loop 2 can be conducted using Eq. (6).

$$I_2(t) = \frac{1}{L_2}\int V_D dt + i_2(t_f) \tag{6}$$

where, I_2 represents the current circulating through loop 2 during fault time, while V_D denotes the voltage across the diode. Furthermore, L_2 signifies the inductance on the load side, and $i_2(tf)$ indicates the initial current of L_2 during fault time. In the proposed DSAT, the maximum fault current can be determined using Eq. (7).

$$i_{f-max} \approx (V_P + V_D)/((L_1 + L_2).\omega f).e^{-\gamma t} sin(\omega f.t) \tag{7}$$

where, V_{sm} represents the switch voltage, and V_P, ω f, ω 0, and γ can be computed using Eq. (8).

$$\begin{aligned} VC &= (V_{SCR} + VC), \omega_f = \sqrt{\omega_0^2 - \gamma^2}, \omega_0 \\ &= 1/\sqrt{L1 + L2.C}, \gamma = R_{dis}.C, R_{eq} \approx R_{on}, S_m + R_{dis} \end{aligned} \tag{8}$$

It has been established that the behaviour of the loop currents in both loops follows an exponential trend. Subsequent simulations and practical tests have been conducted to validate the formulations presented. The outcomes from these endeavours corroborate the theoretical predictions, lending further credence to the accuracy and reliability of the proposed models.

2.1. Switching operation of the proposed model

to demonstrate the circuit switching performance by repeatedly operation of S_m, a test is carried out. The test utilized a command signal with a 20-s symmetrical ON-OFF cycle for switching of S_m. During the interruption, the main switch voltage peaked at 51.25 V, resulting in a 3.25 V (6.7%) overvoltage. No current surge was detected in the main circuit path, validating the effectiveness of the proposed DSAT (see Fig. 4).

In this scenario, the energy released from the inductances is redirected into the corresponding sub-circuits. Fig. 5 illustrates the behaviour of the SCR voltage and current during the switching operation of the Sm. When the OFF command is given, the energy released from the line inductance flows through the SCR (5.98 A) and is absorbed by the capacitor. The ON and OFF operations are as follows: S_m = ON: V_{SCR} = −16.69 V, I_{SCR} and I_{Cap} = 0, SCR = OFF. S_m = OFF (Surge Absorption): $V_{SCR} = V_s - V_{Cap}$ = −2.42 V, V_{Cap} = 50.42 V, I_{SCR} and I_{Cap} = 5.98 A.

The current flowing through the SCR and capacitor in the OFF state demonstrates the capacitor's effectiveness in absorbing the switching surge.

The circuit operation shows that the circuit is robust against multiple switching operation.

3. Simulation results and analysis

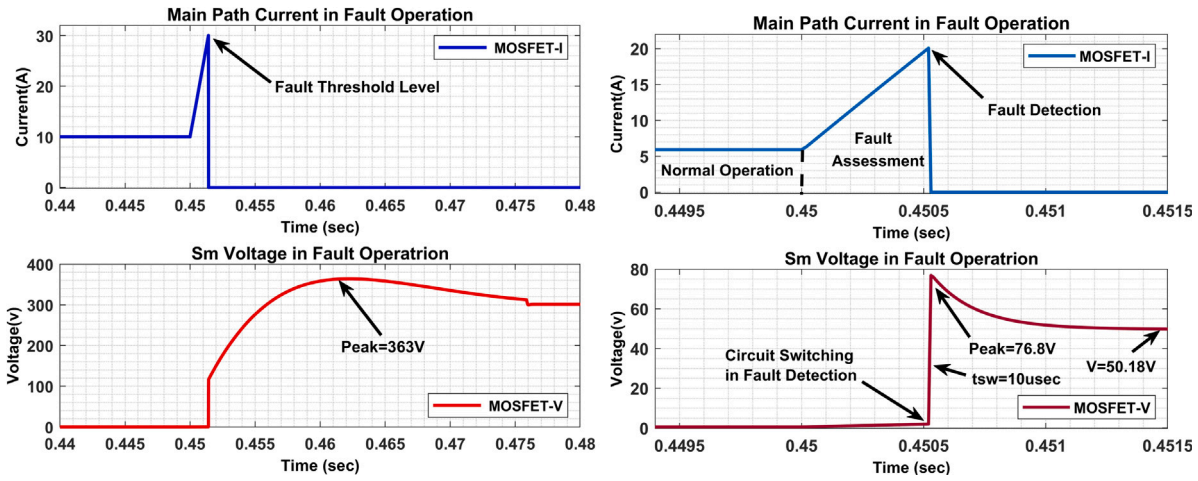
In this phase of the research, simulations were conducted to assess parameter variations for two input DC voltage levels ($V_1 = V_s$ = 300 V and $V_2 = V_s$ = 48 V) and two set of parameters within the system. The inductance values were deliberately adjusted to observe the impact of the proposed model on the variation of energy release in the system.

For the V_1 voltage level, the threshold current is defined as 30 A, while for the V_2 voltage design, it is set at 20 A. The performance of the main switch (S_m) is depicted in both simulated models, as shown in Fig. 6.

In both Figs. 6(a) and 6(b), upon occurrence of a fault within the system, the current undergoes an increase, prompting the microprocessor to evaluate its magnitude and compare with the predefined setpoint. When the line current reaches the threshold level, the microprocessor issues distinct commands to both active switches. A deactivation command is sent to S_m while an activation command is dispatched to the SCR.

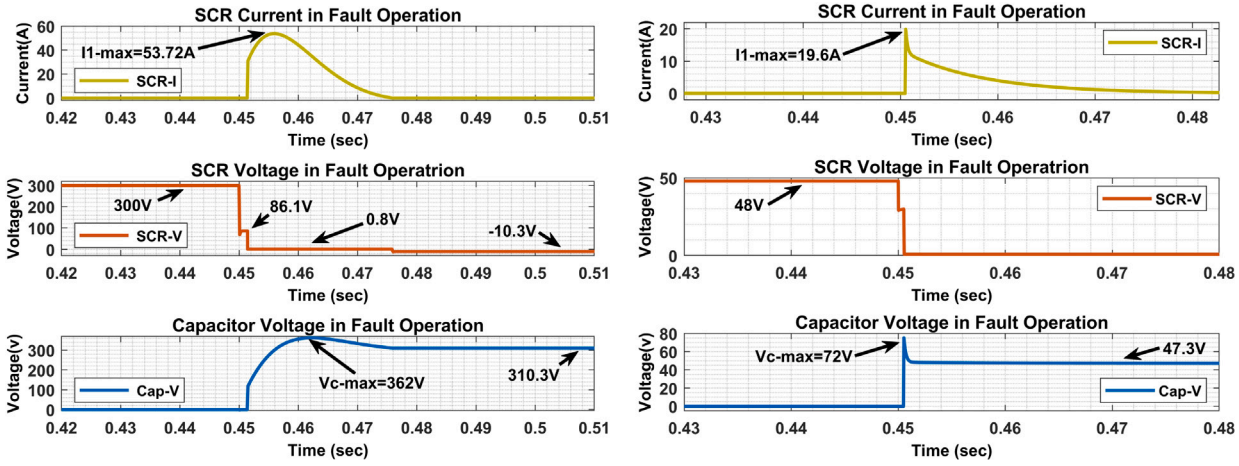
In Fig. 6(a), the test is performed with parameters set as follows: V_1 = 300 VDC, L_1 = 15 mH, L_2 = 6 mH, R_L = 30 Ω, and C = 470 μF. Under these conditions, the overvoltage across the main switch (S_m) of the safeguarded circuit registers at 63 V, approximately 21% of the circuit's nominal voltage. This level falls within the acceptable range for circuit-breaking applications, and the voltage tolerance of the IXFP110N15T2 MOSFET remains within this range of shock. The threshold current (I_{th}) for fault detection in this test is configured at three times the nominal current (I_n) of the system, denoted as $I_{th} = 3 \times I_n$.

In Fig. 6(b), the test is carried out with the parameters configured as follows: V_2 = 48 VDC, L_1 = 0.67 mH, L_2 = 1.03 mH, R_L = 8 Ω, and C = 470 μF. Under these conditions, the voltage overshoot of the protected circuit amounts to 28.8 V, which is approximately 60% of the circuit's nominal voltage. In this scenario, the threshold current (I_{th}) for fault



(a) S_m (MOSFET) voltage and current in V_s=300V, L_1=15 mH, L_2=6 mH (b) S_m (MOSFET) voltage and current in V_s=48V, L_1=0.67 mH, L_2=1.03 mH

Fig. 6. Simulation results: S_m voltage and current in (a) V_1 design, and (b) V_2 design.



(a) SCR and capacitor voltage and current (V_1 design) (b) SCR and capacitor voltage and current (V_2 design)

Fig. 7. Simulation results: comparison of voltage and current of SCR and capacitor and impact of released energy of SS-DCCB in V_1 and V_2 designs.

Table 1
Overvoltage value vs. Threshold current level.

Voltage level	Threshold current	Overvoltage value	Percentage
300 V	$I_{th} = 3 \times I_n$	63 V	21%
48 V	$I_{th} = 3.3 \times I_n$	28.8 V	60%
48 V	$I_{th} = 2 \times I_n$	3.7 V	7%

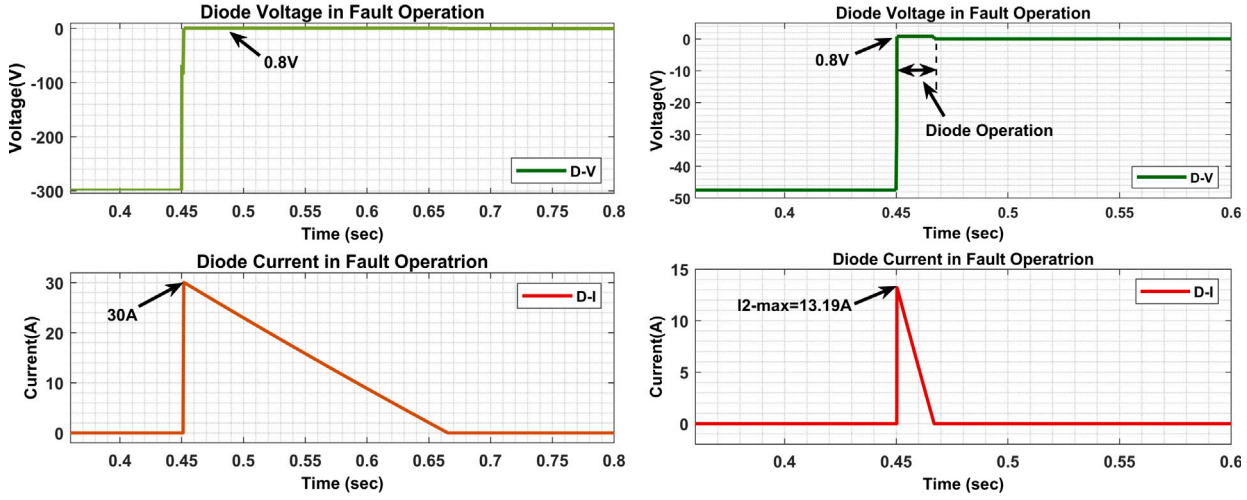
detection is set at 3.33 times the nominal current (I_n) of the system, expressed as $I_{th} = 3.33 \times I_n$.

Based on the IEC60898-3 and IEC60947-2 standards for Circuit Breakers it is evident that the selected fault current level of the DCCB should be chosen with caution to protect the system and prevent overvoltage of the switch [20,21]. A higher threshold current level results in the release of more square energy as mentioned in and Eq. (1). Considering the threshold fault current as twice the line nominal current ($I_{th} = 2 \times I_n$) would lead to negligible voltage overshoot (in the range of 3.7 V or 7% of the DC system voltage).

To emphasize the influence of the threshold fault current level on the overvoltage across the main switch, comparative results are presented in Table 1. It is evident that the overvoltage across the main switch is directly influenced by the chosen threshold for fault current, which in turn is tied to the energy released within the system. When the threshold current is set at Ith = 3.3 × In, the maximum overvoltage reaches 60% of the DC system voltage across the main switch. Conversely, the minimum overvoltage occurs at $I_{th} = 2 \times I_n$, which is 7%.

The design concept presented herein demonstrates a high degree of flexibility, rendering it suitable for deployment in both LVDC Microgrids and MVDC Microgrids. Notably, the circuit response time within V_2 systems is measured at t_{sw} = 10 μs, an interval deemed sufficiently expedient to effectuate the disconnection of the load side and ensure the protection of the DC system from potential hazards. In a comprehensive analysis depicted in Fig. 7, the comparison of voltage and current characteristics between SCR and capacitor is provided, alongside an examination of the consequential impact stemming from the release of energy on the bypassed line side of the SS-DCCB within both V_2 and V_1 configurations. These results meticulously scrutinize the implications of varying voltage levels and system inductance on the overall switching performance, thereby elucidating crucial insights essential for informed decision-making in the realm of DCCB design and operation.

In Fig. 7(a), an observation reveals that the transient bypassed current traversing through the thyristor surges to 53.7 A, surpassing the nominal line current by 23.7 A. This surge is attributed to the elevated level of inductance incorporated within the system, specifically denoted



(a) Diode voltage and current in fault operation in V_1=300V

(b) Diode voltage and current in fault operation in V_2=48V

Fig. 8. Simulation results: Diode voltage and current in both designs.

Table 2
System parameters and components.

Parameter	Acronym	Value	Unit
Input DC voltage	V_S	48	VDC
Snubber capacitor	C	470	μF
Microprocessor	ARM Microcontroller	STM32F407VG	–
Main switch	S_m (MOSFET)	IXFP110N15T2	–
Bypass thyristor	SCR	SKKT27B12E	–
Diode	D	HER303	–
Gate driver	GD	A341H	–
Line side inductance	L_1	670	μH
Load side inductance	L_2	1.03	mH
Load resistance	R_{load}	9.6	Ω
Gate resistance	R_{g1}	20	Ω
Current transformer	CT	LEM 100P	–

as L_1 = 15 mH. During the period of SCR conduction in fault operation, the voltage across the capacitor escalates to 362 V, effectively absorbing the shock generated during switching.

Comparatively, in Fig. 7(b), the transient shock is analysed in contrast to the findings in Fig. 7(a). Herein, a transient shock measuring I_{1-max} = 19.6 A is discerned within the bypassed branch, while concurrently, the capacitor voltage ascends to V_{C-max} = 72 V. Subsequently, the capacitor undergoes a full charge, stabilizing the capacitor voltage at 47.3 V. This comparative analysis between Figs. 7(a) and 7(b) elucidates the nuanced dynamics of transient shock responses and capacitor behaviour, furnishing insights for system optimization and performance enhancement. In Fig. 8, the voltage behaviour of the load side diode and its conduction characteristics are depicted, alongside the transient performance of the current within L_2-$Fault$-D loop. Both Figs. 8(a) and 8(b) illustrate the dissipation of released energy from the inductance, facilitated through the formation of the loop. Notably, in the V_2 DCCB design, the maximum current within loop 2 is denoted as I_{2-max} = 30 A, whereas in the V_1 DCCB design, this maximum current is observed to be I_{2-max} = 13.19 A. These findings underscore the differential transient performance between V_1 and V_2 configurations.

4. Experimental validation

The experimental test was carried out to assess the performance of the proposed V_2 SS-DCCB design operating at 48 VDC. The primary objective of this test was to validate both the proposed topology and the DSAT technique against simulation results. The technical specifications and part numbers of the components are detailed in Table 2.

For validation of the proposed model, the experimental setup utilized a Chroma DC Power Supply (62100H-100P) as the system's power source, while a Programmable DC Load (Chroma 63204-5.2 kW) functioned as the load. Additionally, a 30 V/2 A auxiliary power supply was integrated to provide power to the gate drivers and the STM ARM Controller. The practical implementation of the proposed SS-DCCB integrated with the DSAT technique is visually depicted in Fig. 9, providing a tangible representation of the experimental setup, and facilitating further analysis and evaluation of its performance characteristics.

Another advantage of the proposed DSAT topology is its robustness when connected to a DC power supply or DC Microgrid with an integrated buck converter. During switching and fault detection operations, the surge generated by the L_B inductance is absorbed by the CB shunt capacitor in Fig. 9, while the surge from L_1 is expected to be dampened in capacitor (C) after the SCR is triggered.

The threshold fault detection current level, denoted as I_f = 20 A, has been established, representing 3.33 times the nominal current of the DC system, which is 6 A, as depicted in Fig. 9. Upon the occurrence of a fault within the system, the STM32 controller initiates an evaluation process. Once the current threshold is detected, a response command is transmitted to the switch, prompting it to disconnect the load. The response time of the primary switch is recorded at t_{sw} = 10 μs. While detecting faults, an overshoot in voltage of 68.8 V is noted, comprising 43% of the system voltage (V_S) amplitude, which is 13% less than the simulation outcome. Notably, adjustments to the current threshold level can yield variations in the observed overshoot voltage, as evidenced by conducted tests. Lowering the threshold current level results in a commensurate reduction in the overshoot voltage, offering insights into real-world potential optimization strategies for system performance and reliability. As shown in Fig. 10, the current slope is approximately 7 A/ms. According to the LEM-100P CT datasheet, the sampling interval for measuring circuit current is 147 ns, while the Arm Microprocessor's prescaler for this process is set to 0.75 μs. Consequently, even during rapid current changes, the CT will consistently transmit measurement signals to the microprocessor, enabling the interruption command to accurately disconnect the circuit without affecting its operation. Furthermore, the di/dt of the SCR, based on the IXFP110N15T2 datasheet, is 150 A/μs, which satisfies the circuit's interruption requirements.

In Fig. 11, analysis reveals a peak current flow through the bypass branch, marked as I_{1max} = 18.35 A. Concurrently, a transient voltage shock of 76 V amplitude is observed across the SCR. This voltage surge is likely attributed to system switching dynamics and the subsequent

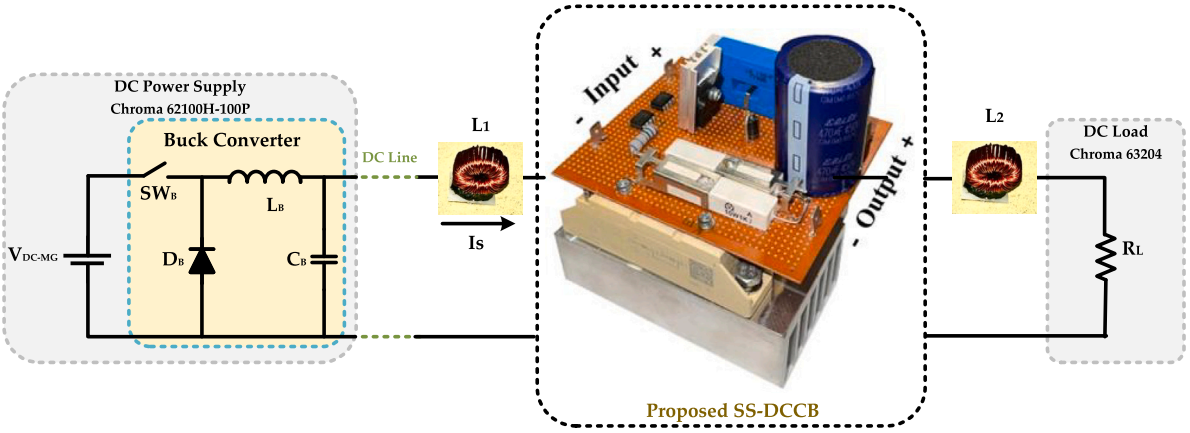


Fig. 9. Practical setup of proposed SS-DCCB with DSAT technique.

Table 3
Comparison of different DC circuit breaker topologies.

Reference	Proposed model	[11]	[14]	[15]	[16]
Category	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB
Technique	DSAT	BiTriCap	SCR-BCB1	TCB	RB-IGCT
Normal reclosing capability	Yes	Yes	Yes	Yes	Yes
Switch type	MOSFET	IGBT	SCR	SCR	IGCT
Total active components	1 × MOSFET	1 × SCR 1 × IGBT	2 × SCR	4 × SCR	4 × IGCT
Diode	1	0	2	3	0
Capacitors	1	1	2	1	1
Inductors	0	0	2	2	0
Resistors	1	1	1	2	1
Circuit control complexity	Low	Medium	High	Medium	High
Surge absorber type	Capacitor	Capacitor	MOV-RC	MOV-RC	MOV-RC
Mechanical switches	0	0	0	2	0
Surge arresters	0	0	1	1	1

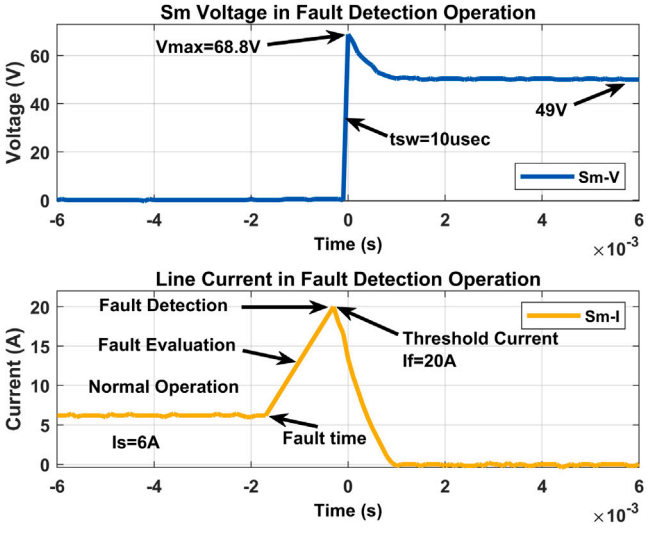


Fig. 10. Experimental results: S_m (MOSFET) voltage and line current performance in fault detection operation.

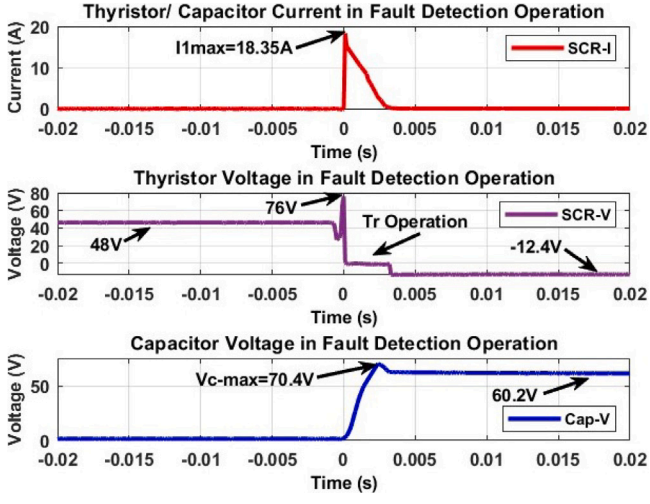


Fig. 11. Experimental results: SCR current, voltage, capacitor voltage.

release of energy within the bypass route. Notably, a differential voltage of V_S-V_C = –12.4 V is noted across the thyristor, stemming from the variance between the capacitor voltage of V_C = 60.2 V and the V_S = 48 V power supply voltage.

In Fig. 12, the damping time (t_d) of the discharge for released energy on the load side is determined to be t_d = 1.6 ms. However, it becomes evident that upon the occurrence of a short circuit in the load, the formation of a loop on the load side ensues following the operation of the main switch. Consequently, the energy stored in the inductance dissipates rapidly along the path of *L2-Fault-D*.

During the design phase, it is crucial to verify that the components can withstand the circuit conditions. In this research, as shown in Fig. 12, the surge current circulating on the load side is 10.5 A. The selected HER303 diode has a peak surge current rating of 50 A, indicating that it can tolerate the instantaneous surge current generated by the load side inductance (L_2).

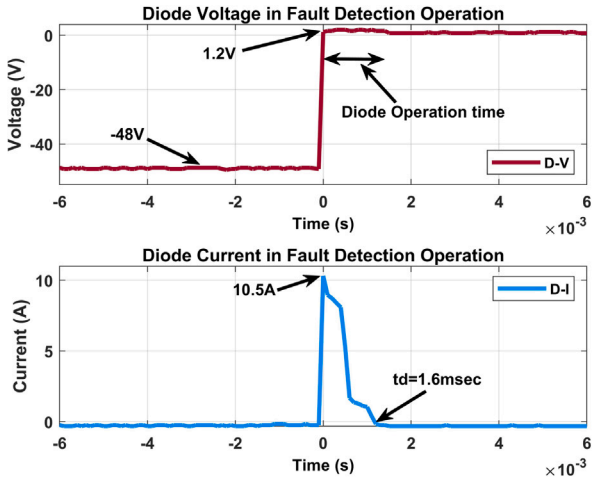


Fig. 12. Experimental results: Diode voltage and loop 2 current in fault operation.

5. Discussion

This section presents a comparative analysis to validate the proposed design by comparing it with existing techniques. The analysis, showed in Table 3, highlights the simplicity and efficiency of the design, which uses minimal active components to mitigate switching effects in SS-DCCB during fault detection in DC microgrids. A real-world DC system model is employed to simulate realistic conditions, confirming the design's effective performance. Overall, the proposed model demonstrates robust and practical fault management, performing as well as or better than more complex designs.

6. Conclusion

The study introduces a novel approach utilizing a SS-DCCB coupled with DSAT methodology for fault current interruption. Simulations were conducted for two distinct system setups: one with an input voltage of 300VDC, a nominal circuit current of 10 A, and a threshold current of 30 A; the other with a system voltage of 48 VDC, a line current of 6 A, and a fault threshold current of 20 A. Meanwhile, experimental testing was carried out for the 48 VDC system to validate both the proposed model and the simulation outcomes. Results demonstrated successful circuit disconnection within a remarkable 10 μs. The proposed model partitions the circuit into two distinct line and load segments, ensuring swift switch operation and mitigating shock hazards. Response time of 10 μs was consistently achieved across simulation and experimentation. In the line side loop, fault current is absorbed and blocked by a ZCS capacitor through the V_S-L_1-SCR-C loop to prevent its flow, while in the load side loop, a diode discharges the released energy through the L_2-$Fault$-D loop. Control of the proposed DSAT is facilitated by an ARM STM32 controller. The proposed model of SS-DCCB adopts a design approach that eliminates the necessity for a suppressor across the main switch. This is achieved through the implementation of the DSAT technique, which facilitates the separation of the circuit. The utilization of DSAT ensures efficient and reliable circuit interruption without the need for supplementary suppression components. This design innovation not only enhances the operational efficiency of the SS-DCCB but also contributes to its robustness and durability. The results of this paper are compared with recent studies to assess the performance of the proposed model against other techniques.

CRediT authorship contribution statement

Mehdi Moradian: Writing – review & editing, Writing – original draft, Validation, Software, Methodology, Formal analysis, Data curation, Conceptualization. **Tek Tjing Lie:** Supervision, Conceptualization. **Kosala Gunawardane:** Supervision.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Mehdi Moradian reports financial support was provided by Auckland University of Technology. Mehdi Moradian reports a relationship with Auckland University of Technology that includes: funding grants and travel reimbursement. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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