Wireless Sensor Technology for Collecting Surface Electromyography Signals

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Abstract

This main purpose of the research was to develop and manufacture a prototype for a new Wireless Surface Electrode for acquiring surface Electromyography (sEMG) signals from the vastus lateralis muscle from the quadriceps of the knee in real-time.

Initially an extensive literature review was carried out which looked at literature either presented at recognised international conferences or published in journals. The literature review focused on papers from the year 2000 using two keywords, which were 'Wireless' and 'Electromyography'. This showed that the majority of papers had been presented at conferences and published in their proceedings. The literature review showed that there were three main techniques used for wireless transmission with a large variation in the settings for the gain used, filtering and data acquisition of the sEMG signals.

For this research the overall design of the new Wireless Surface Electromyography (WsEMG) Electrodes consisted of two newly designed and developed components: (a) an Electrode Interface Node and (b) a Computer Interface Node.

The wireless link between the two nodes used a ZigBee protocol. The data acquisition was carried out using LabVIEW software to develop a new virtual instrument.

The electrode interface node used an integrated circuit chip from a family programme system on the chip (PSoC®). The PSOC® chip enable module configuration of the instrumentation amplifier, the low-pass filter, the analogue to digital convertor and it also required a universal asynchronous receiver/transmitter to interface to an XBee® transceiver module.

The computer interface node was developed to be a USB dongle to connect to a laptop computer. The USB dongle consisted of another XBee® transceiver module and a USB universal asynchronous receiver/transmitter.

The VI was designed and developed using LabVIEW software which allowed for the initial settings for the overall gain and low-pass cut off frequency to be made to the PSoC® chip by wireless communication before data acquisition started. The sEMG signal of the muscle was displayed in real time on the laptop and stored as a data file for analysis at a later date.

The subjects used for this research to test the performance of the new WsEMG electrodes and data acquisition were volunteers and for which Ethics Approval was given by the Auckland University of Technology Ethics Committee.

The initial results showed that favourable results were achieved that were comparable to currently used standard wired sEMG electrode systems.

Table of Contents

Table of Figures

List of Tables

Statement of Originality

'I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for qualification of any other degree or diploma of a university or other institution of higher learning, except where due acknowledgement is made in the acknowledgements.'

Yuting Zhu

29th November 2013

Chapter 1
Introduction

1.1 Background

Contractions of skeletal muscles fibres perform movement or force from bioelectrical pulses. Electromyography (EMG) is the term used to describe the study of muscle activity, and is used for measuring the bioelectric pulses. This allows medical professions and researchers to see how a patient's muscles are performing and to make decisions about what can be done to improve the performance of particular muscles.

Formal definitions of EMG include:

> *"EMG means the recording, registration and evaluation of muscle action potentials"[1]*

Or

> *"An electromyographic (EMG) examination is a functional evaluation of the motor unit. It can assess the location, severity, chronology, and prognosis of injuries, diseases, or other compromises of the motor unit. The motor unit is made up of the anterior horn cell, its axon, and all of the muscle fibers innervated. Some wish to characterize electro diagnosis as synonymous with EMG, and that is historically and conventionally correct, if not correct technically."[2]*

The invasive method of EMG measurement was done by the insertion of needles/wire into the muscles of a patient. This is both painful and unwelcome in many cases. The other practice uses a non-invasive method where electrodes are placed on the surface of the muscle of interest. One of the earliest examples of the study of EMG with the placement of surface electrodes was carried out by Piper [3].

Using these surface electrodes were an improvement to invasive insertion devices but still need to be linked to the data recorder/analyser by a set of wires. This required the patient to be ‘wired-up’ during testing. The early devices required the wires to be close to the data recorder/analyser, which restricted the usefulness of this technique. As surface electromyography became the customary practice the devices improved, but were still hampered by the endless wires and the back pack that the patient was required to carry for the data to be recorded and analysed.

The changes from wired to wireless surface devices only began to occur when wireless technology developed in other fields such as communication and the military and when this technology became readily available. Wireless devices used for surface Electromyography (sEMG) now included a variety of computerised functions which can report directly to the examiner via computer software to exact features in order to examine the nature of muscular function or dysfunction under investigation.

EMG data received was given in the form of *‘wave’* patterns or digitised signals, which could be used to diagnose a problem, which needed to be addressed and whether this was within a normal pattern. Early recording required a skilled clinician and frequently the patient did not take part in the conversation as to the problems identified by the procedure. Today with the advancement of technology the clinician can read the muscular activity on the screen of a hand device. This now allows the patient to be able to participate and see the results of muscular activity at the time of the testing. So the patient can be given immediate feed-back in real time and also be encouraged to correctly replicate muscular movements to improve muscular activity if this is the required outcome. Using wireless technology has greatly benefited the clinician and researcher to obtain useful information of how muscles function without the need of a wired system connected to the patient’s body.

The following section will cover the various electrodes used today for the collection of electromyography signals.

1.2 Electromyography (EMG) Electrodes

The electrodes are the sensors that measure the bio electrical pulses made by the nerves and muscles. They are either inserted (needle and wire) electrodes or surface electrodes. When electrodes are used individually they are mono-polar and when used in pairs are known as bipolar. Respectively the EMGs readings are acquired as mono-polar or bio-polar configurations [3].

The first principle of designing electrodes is that they must be brought close enough to the muscle under study to pick up the current generated by the muscle movement.

1.2.1 Needle and Wire Electrodes (Invasive)

The most commonly used electrodes for invasive data collection of EMG signals are shown in Figure 1.1 [4].

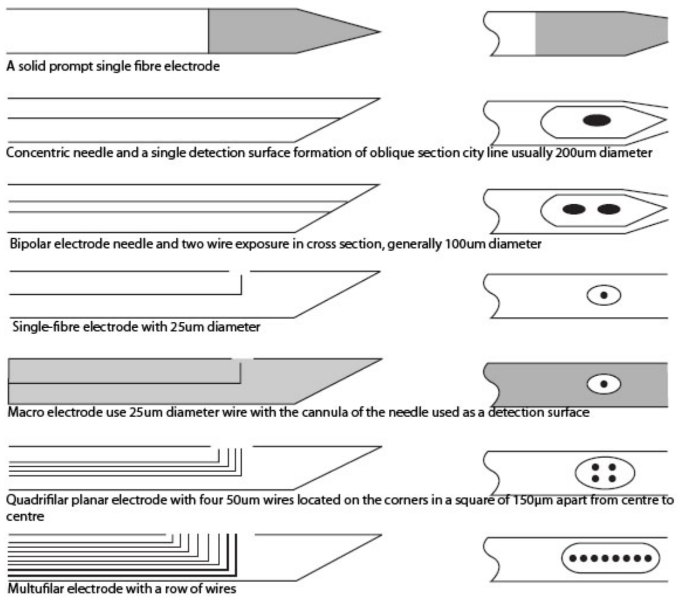


Figure 1.1 – Examples of different needle electrodes

Needle electrodes have changed as a result of improved technologies for testing and recording methodologies. Despite the development and use of surface electrodes, needle electrodes still have a place in the collection of EMG signals.

De Luca et al. [3] described the commonly uses of needle electrodes over surface electrodes, they are:

Motor Unit Action Potential [MUAP] characteristics

Control properties of motor units (firing rate, recruitment, etc.)

Exploratory clinical electromyography

With the development of the wire electrode, De Luca et al. [3]:

Kinesiological studies of deep muscles

Neurophysiological studies of deep muscles

Limited studies on motor unit properties

Comfortable recording procedure from deep muscles

Wired electrodes have led to improvement in muscle measurement knowledge and improved technology has led to an improved understanding of muscle activity. The ability to do further study however, still relies on the agreement of the patient to have a variety of needles inserted into the body; this is uncomfortable and likely to cause some distress to the patient. Whilst the skin surface can be anaesthetised for the needle(s) to be inserted this can cause the 'deadening' of the muscles and so no electrical pattern can then be detected. These factors have given pressure for an alternative method to be found to make these readings possible and with less discomfort to the client, which has led to the development and use of surface electrodes.

1.2.2 Surface Electrodes (Non-invasive)

There are two types of surface electrode: ***Passive*** and ***Active***. In each case the electrode head maybe the same but the reading and the recording of the EMG signal is different.

A ***Passive Electrode*** is shown in Figure 1.2, which has a wider range of reading of muscle activity than the actual focus of the examination. This method gives a less accurate reading as it has greater input impedance. When using passive electrodes the subject will possibly get a small tingling feeling on the skin due to the current produced between the electrode and the surface of the skin.

Figure 1.2 – Passive Electrodes

The simplest form of a passive electrode is a silver/silver chloride plate, which adheres to the skin by the application of conductive gel. Impedance between the electrode and the skin can be further reduced by removing any hair and exfoliating the skin before the electrode is attached. Later versions of the passive electrode the conductive gel was part of the electrode. Once a passive electrode has been used for testing purposes it is usually discarded and not used again for future testing. Passive electrodes used today are now all disposable and discarded after use.

The ***Active Electrode*** shown in Figure 1.3 usually has the ability to reduce the impedance of between the electrode and the skin above the muscle being examined. This is achieved by the inclusion of a high input impedance amplifier in the same housing of the surface electrodes. This arrangement gives the ability to exclude localised impedance and therefore improves the quality of the readings obtained.

Figure 1.3 – Photo of Active Electrode

The impedance again can be further reduced by removing any hair and exfoliating the skin before the electrode is attached. Active surface electrodes have been further developed to eliminate the need for skin preparation and for the conductive gel. These are called ‘dry’ or ‘paste-less’ electrodes.

The active electrode also has its own filtering system using resistances and capacitances within the head of the electrode, which allows the filtering to be coupled close to the skin.

The active electrode has the benefit of being reusable. This requires after use care in terms of storage and hygiene. The multiple uses of the active electrode are also part of its long term unreliability for the following reasons:

1. The constant hygiene cleaning requirements after each and every use means the surface area of the electrode can be vulnerable to minute surface changes which will skew future readings after repeated use.
2. Existing sweat and the erosion of its surface can lead to changes in its electrical properties and also skew later readings.
3. At this time there appears to be no alternative solution to these two problems with active electrodes.

The surface electrode has further described by De Luca et al. [3] and is now mostly used for:

Time-force relationship of EMG signals
Kinesiology studies of surface muscles
Neurophysiological studies of surface muscles
Psychophysiological studies
Interfacing an individual with external electromechanical devices

The greatest advantage of surface electrodes is that they are non-invasive and do not give the patient any discomfort. Moreover, surface electrodes are able to sample a larger volume of muscle but one significant disadvantage is that they can only be used effectively with superficial muscles and they cannot be used to detect signals selectively from small muscles.

Surface electrodes can cause difficulties for the patient when recording movement. The individual is hampered with a multitude of electrodes and wires and so movement maybe difficult or unnatural when recording is taking place. This may cause the patient to make movements which are not their natural movements. The recording may not be of the usual pattern for that movement and hence may not give an accurate diagnosis of the muscular problems for which the testing has been required [5].

The innovation of wireless surface electromyography (WsEMG) technology has greatly improved the ability to measure muscular activity in a more natural and unencumbered way.

1.3 Wireless Surface Electromyography (WsEMG)

Wireless networks are now part of daily lives through smart phones and tablet technology. Creating a wireless sensor network for equipment is feasible and gives the greatest amount of freedom and flexibility to use sEMG in a new free environment to analyse previously seriously restricted abilities.

Wireless technologies offer alternative design solutions for the transmission of complex data communication through such systems as Radio Frequency (RF), Bluetooth and ZigBee etc. In particular, the medical field and the sport and recreation industry stands to benefit widely by substituting wireless systems for wired measurement systems instead of continuing to use the more restricted wired systems.

The advantages of wireless technology is [6]:

1. ***Reliability and Mobility*** *– the units for wireless are usually in a singular enclosed unit so there are no moving parts.*
2. ***Easy Access and Comfort*** *– they are easy to use for both patient and clinician with few complicated instructions.*
3. ***Low-power consumption*** *– Most wireless units now come with advanced batteries or a power source so longer period of use is feasible before recharging is required.*
4. ***Real-time processing*** *–the recording of data can be completed on site and at the time for the testing without having to wait for this to be completed at a later stage.*
5. ***Small size and low-cost*** *– recent technology has reduced the sizes of these devises as well as the components used.*

This chapter has shown the development of electromyography from its early days to the current situation of the ability to use modern wireless technology for a medical procedure in some circumstances.

The next chapter will review the literature to show the development of wireless technology related to electromyography. This has led to the development of a new electrode unit which will enhance further the ability of the clinician to diagnose muscle function under set circumstances using this technology.

Chapter 2
Literature Review

This chapter will review the literature on the development of Wireless Surface Electromyography (WsEMG) electrodes and their systems that are used to collect signals from a subject's muscles that are being examined. These signals are then sent to the computer for further analysis at a later date.

As indicated in the first chapter Surface Electromyography (sEMG) is the non-invasive method used to measure the muscle's activity. This is a safe and easy way to record the bioelectrical signal of muscle activity. This has now becoming more widely used for research and clinical applications in many fields for purposes such as rehabilitation programmes, ergonomics and sports performance as well as neurophysiological research [7].

Overall wireless technology provides no wired connections, and is safe with flexible connectivity. It greatly improves resource sharing, is easy to install and has a high mobility factor [6, 8, 9]. The other advantage is that these systems usually use low power levels, thus can be used for a longer period of time before the power source requires renewal [6, 8, 9].

An intensive literature search was carried out, which found that there were a limited number of journal papers published on this topic. But the publications published were mainly found in recognised international conference papers explaining the development of the systems currently developed and used. The search carried out for papers were through recognised databases using the following keywords *'Wireless'* and *'Electromyography'* and limited to papers published since the year 2000. In total 165 papers were found of which 86 were journal papers and the rest were papers presented and then published from recognised conferences. After further extensive examination of these papers a large number were rejected for this literature review due to their unsuitability for the topic being researched i.e. they included using wireless technology for monitoring animal behaviour and many others elements.

The remaining papers used in this literature review were then classified in terms of the wireless protocol used. They were:

1. Radio frequency (RF) (11 papers)
2. Bluetooth (BT) (6 papers)
3. ZigBee (5 papers)

A number of questions were posed to gain the relevant information about each of the systems present in the papers, these were:

a) What electrode configuration was used i.e. type and material?
b) Which biosignals were collected with the system?
c) What amplification and filtering was used and where?
d) What was the bit resolution of analogue to digital converter (ADC) used?
e) What type of wireless link was used i.e. type and frequency?
f) What type of computer interface was used with the wireless system?
g) What was the sampling frequency used to acquire the sEMG signal?

2.1 Radio Frequency (RF) WsEMG

A radio frequency (RF) signal refers to a wireless electromagnetic signal used as a form of communication, for wireless electronics. Radio waves are a form of electromagnetic radiation identified with radio frequencies ranging from 3 kHz to 300 GHz. RF communication is used in many industries including television broadcasting, radar systems, computer and mobile platform networks, remote control, remote metering/monitoring, and many more such as medical devices.

After an intensive search of the papers only eleven papers were found to be relevant to this research all having being peered reviewed and presented at recognised international conferences. The summary of these papers are presented in Table 2.1 on pages 10 to 12.

Table 2.1 – Summary of the Literature Review for Radio Frequency WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
A Wireless Device for Measuring Hand-Applied Forces'	*Tam, W., et al., 2004 [10]*	*Conference*	*Not stated.*	*EMG*	*Instrumentation amplifier (variable gain). Band-pass filter (100 – 1 kHz).*	*16-bit*	*Linx Transceiver System.* *PCMCIA* card*	*1 kHz*
Design of Implantable Wireless Biomedical Signals Telemetry System	*Young-Ho, Y., et al., 2004 [11]*	*Conference*	*Not stated.*	*EMG, ECG***	*Not stated*	*16-bit*	*Infra-red (Carrier Frequency 37.9 kHz).* *Micro-processor*	*8.62 k Hz*
Microcontroller-based Wireless Recorder for Biomedical Signals	*Chien, C.N., et al., 2006[12]*	*Conference*	*Not stated.*	*EMG, ECG***	*Instrumentation amplifier (variable gain). Low-pass filter (variable) with optional High-pass filter.*	*10-bit*	*Microcontroller (Carrier Frequency 433.92 MHz).* *RS-232*** Serial Interface*	*1 kHz*
Development and Evaluation of a Wireless Interface for Inputting Characters Using Laplacian EMG'	*Miyazawa, K., et al., 2006 [13]*	*Conference*	*Laplacian*	*EMG*	*Instrumentation amplifier (variable gain). High-pass filter (f_c = 100 Hz).*	*Not stated*	*Not stated.* *Scanning communication system*	*Not stated*

PCMCIA is Personal Computer Memory Card International Association, ECG** is Electrocardiography, RS232*** is serial port for a personal computer*

Table 2.1 (continued) – Summary of the Literature Review for Radio Frequency WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
In situ measurement of playing children by wireless wearable electromyography	*Kawakami, G., Y. Nishida, and H. Mizoguchi, 2007 [14]*	*Conference*	*Pure active pure silver (Ag) electrode.*	*EMG*	*Differential Amplifier (Gain 600). Band-pass filter*	*10-bit*	*GFSK* Transceiver module 2.5-2.5 GHz using GSM** band.* *USB*** Interface.*	*1 kHz*
Wireless Vestibular Evoked Myogenic Potentials System	*Torfs, T., et al., 2007 [15]*	*Conference*	*Conventional Ag/AgCl electrodes*	*EMG*	*Instrumentation amplifier. High pass filter.*	*12-bit*	*Personal body area network (BAN)* *Not stated.*	*Not stated*
Wireless Transmission of EMG Signal and Analysis of Its Correlation with Simultaneously Acquired Carotid Pulse Wave Using Dual Channel System	*Bansal, D., M. Khan, and A.K. Salhan., 2010 [16]*	*Conference*	*Ag-AgCl**** electrodes.*	*EMG*	*Operational amplifier (gain 500) (100 – 1 kHz).*	*Not stated.*	*RF Frequency Modulation* *Sound port.*	*8 kHz*

GFSK is Gaussian Frequency-Shift Keying, GSM** is Global System for Mobile Communications, USB*** is Universal Serial Bus, Ag-AgCl**** is Silver/Silver Chloride*

Table 2.1 (continued) – Summary of the Literature Review for Radio Frequency WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
Rechargeable wireless EMG sensor for prosthetic control	*Lichter, P.A., et al., 2010 [17]*	*Conferenc e*	*Not stated.*	*EMG*	*Operational amplifier (gain 5)* *Band-pass filter.*	*20-bit*	*Not stated.* *USB Interface.*	*Not stated.*
Biomedical signal amplifier for EMG wireless sensor system	*Rendek, K., et al., 2010 [18]*	*Conference*	*Gold (Au) plated.*	*EMG*	*Instrumentation amplifier. Band-pass filter (15 – 1 kHz).*	*16-bit*	*RF* *USB Interface.*	*100 kHz*
A Pilot Study on Evaluating Recovery of the Post-Operative Based on Acceleration and sEMG	*Zhelong, W., et al., 2010[19]*	*Conference*	*Not stated.*	*EMG*	*Difference amplifier.* *Low pass filter, (f_c = 45Hz).*	*Not stated*	*Wireless transceiver modules (CC2420)* *USB Bluetooth dongle.*	*100 Hz*
A Wearable Wireless General Purpose Bio-signal Acquisition Prototype System for Home Healthcare'	*Junwei, D., et al., 2012 [20]*	*Conference*	*Ag-AgCl electrodes.*	*EMG, ECG, EEG*.*	*TI ADS1298 IC (Programmable gain 1-12)* *Notch filter (50 Hz)*	*24-bit*	*RFCC285 Transceiver modules.* *Serial port.*	*500 Hz*

EEG is Electroencephalography*

2.2 Bluetooth (BT) WsEMG

Bluetooth (BT) was based on the IEEE 802.15.1 standard for wireless personal area networks (WPANs), which are no longer maintained. The BT development and technology is now overseen by the Bluetooth Special Interest Group. This technology is designed to provide reliable, low-power wireless communications over short distances and uses short-wavelength radio transmissions in the Industrial, Scientific and Medical (ISM) band from 2.4 – 2.48 GHz. BT is best known as the primary technology for wirelessly connecting mobile phones with peripheral devices such as wireless headsets. However, BT can be an ideal choice for a wide range of designs such as medical devices.

Only six papers were found to be relevant to this research of which two were from peer review journals and the other four had been presented and published from recognised international conferences. The summary of these papers are presented in Table 2.2 on pages 14 to 16.

Table 2.2 – Summary of the Literature Review for Bluetooth WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
The tremor coherence analyzer (TCA): a portable tool to assess instantaneous inter-muscle coupling in tremor.	*Brunetti, F.J., et al., 2004 [21]*	*Conference*	*Electrodes using medical-grade stainless-steel.*	*EMG*	*Preamplifier with a gain of 20.*	*8-bit*	*Bluetooth modules (Blue giga Wrap Thor)* *Microcontroller*	*512 Hz*
Design and implementation of a wireless (Bluetooth) four channel bio-instrumentation amplifier and digital data acquisition device with user-selectable gain, frequency, and driven reference.	*Cosmanescu, A., et al., 2006[22]*	*Conference*	*Not stated.*	*EMG, EKG**	*Instrumentation amplifier (Gain 100, 500 and 1000). Band-pass filter (10 – 500 Hz).*	*10-bit*	*WBTV42 Bluetooth modules from Wintec Industries.* *RS232 serial port*	*2 kHz*

EKG is Electrocardiography*

Table 2.2 (continued) - Summary of the Literature Review for Bluetooth WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
Wireless esophageal catheter dedicated to respiratory diseases diagnostic.	*Desilets, T., M. Sawan, and F. Bellemare., 2006 [23]*	*Conference*	*Platinum ring electrodes.*	*EMG*	*Instrumentation amplifier (variable gain). Band-pass filter (35 – 1 kHz).*	*16-bit*	*Bluetooth wireless serial port adapter (OEMSPA13i).* *USB Bluetooth dongle.*	*1 kHz*
Development of a compact-size and wireless surface EMG measurement system.	*Wonkeun, Y. and K. Jung., 2009 [24]*	*Conference*	*Ag/AgCl electrodes.*	*EMG*	*Pre-amplified. Band-pass filter (10 – 500 Hz) and Band-rejection filter (60 Hz).*	*Not stated.*	*Bluetooth* *Not stated.*	*1024 Hz*
Analysis of Right Arm Biceps Brachii Muscle Activity with Varying the Electrode Placement on Three Male Age Groups During Isometric Contractions Using a Wireless EMG Sensor	*Ahamed, N.U., et al., 2012[25]*	*Journal*	*Active electrodes.*	*EMG*	*Pre-amplified. Band-pass filter (5 – 482 Hz).*	*Not stated*	*Bluetooth radio modules.* *SH-SHIM-KIT-004*	*100 Hz*

Table 2.2 (continued) - Summary of the Literature Review for Bluetooth WsEMG

Paper Title	***Authors/Year***	***Conference or Journal***	***Electrode Configuration (Type and Configuration)***	***Type of Biosignals Collected***	***Amplification and Filters***	***ADC (Bit Resolution)***	***Wireless link used and Computer Interface***	***Sampling Frequency***
A Wireless sEMG Recording System and Its Application to Muscle Fatigue Detection.	*Chang, K.-M., S.-H. Liu, and X.-H. Wu., 2012 [26]*	*Journal*	*Ag/AgCl electrodes.*	*EMG*	*Instrumentation amplifier (gain 20). Band-pass filter (30 – 1 kHz).*	*12-bit*	*Bluetooth modules using chip (BTM-204B) made by CSR Company.* *Serial port.*	*2 kHz*

2.3 ZigBee WsEMG

ZigBee is a specification for communication in wireless personal area networks (WPANs), like Bluetooth. This technology is designed to be low cost and low powered making it ideal for wireless sensor networks (WSNs) and other low power networks that span potentially large distances. ZigBee builds upon the IEEE 802.15.4 standard, adding extra features such as mesh networking capability with multi-hop functionality and a routing protocol. ZigBee technology does not compete with other technologies such as Bluetooth or Wi-Fi (IEEE 802.11). ZigBee is designed for applications where the data transfer rate is much less important than power efficiency, network size, and the capacity for ad hoc routing. Global operation is in the 2.4GHz frequency band according to IEEE 802.15.4, with regional operation in the 915 MHz (Americas) and 868 MHz (Europe).

After an intensive search of papers only five papers were found to be relevant to this research. One was published in a peer review journal and the other four were papers presented and published papers from recognised international conferences. The summary of these papers are presented in Table 2.3 on pages 18 to 19.

Table 2.3 – Summary of the Literature Review for ZigBee WsEMG

Paper Title	***Authors/Year***	***Conference or Journal***	***Electrode Configuration (Type and Configuration)***	***Type of Biosignals Collected***	***Amplification and Filters***	***ADC (Bit Resolution)***	***Wireless link used and Computer Interface***	***Sampling Frequency***
Wireless Head Cap for EOG and Facial EMG Measurements	*Vehkaoja, A.T., et al., 2006[27]*	*Conference*	*Ag coated reusable electrodes.*	*fEMG*, EOG***	*Instrumentation amplifier (gain 1000). Band-pass filter (10 – 400 Hz).*	*16-bit*	*Chipcon's CC2420 ZigBee compliant chip. RS-232 interface.*	*200 kHz*
Design of Wearable, Low Power, Single Supply Surface EMG Extractor Unit for Wireless Monitoring	*Sankar, K.A., M. Oishee, and B. Subhasis, 2011 [28]*	*Conference*	*Disposable electrodes.*	*EMG*	*Instrumentation amplifier (gain 1111). Band-pass filter (10 – 500 Hz).*	*10-bit*	*XBee® Digimesh 2.4 OEM RF modules. USB Interface.*	*1 kHz*
A portable wireless biometric multi-channel system	*Boquete, L., et al., 2012 [29]*	*Journal*	*Not stated.*	*EMG, ECG, EEG, EOG.*	*Instrumentation amplifier (gain 20). Band-pass filter (0.5 – 1.5 kHz).*	*12-bit*	*XBee® modules. USB Interface.*	*400 Hz*
A portable multi-channel behavioral state and physiological signal monitoring system	*Chung-Ping, Y., et al., 2012 [30]*	*Conference*	*Not stated.*	*EMG, ECG, EEG, EOG.*	*Not stated.*	*10-bit*	*CC2430 Modules. USB to RS-232 convertor.*	*Approx. 2.8 kHz*

fEMG is Facial Electromyography, EOG** is Electrooculography*

Table 2.3 (continued) - Summary of the Literature Review for ZigBee WsEMG

Paper Title	*Authors/Year*	*Conference or Journal*	*Electrode Configuration (Type and Configuration)*	*Type of Biosignals Collected*	*Amplification and Filters*	*ADC (Bit Resolution)*	*Wireless link used and Computer Interface*	*Sampling Frequency*
Development of a wearable ZigBee sensor system for upper limb rehabilitation robotics	*Cifuentes, C., et al., 2012 [31]*	*Conference*	*EMG active electrodes.*	*EMG*	*Instrumentation amplifier. Band-pass filter (2 – 500 Hz).*	*16-bit*	*ZigBee network consisting of two end devices and one coordinator.* *Signals stored on micro SD Card, then download to computer.*	*1 kHz*

2.4 Summary of Literature Review Comparison of RF with BT with ZigBee

Table 4 on page 22 shows the results of the seven important questions that were identified at the beginning of this chapter to assist in determining the design of the new wireless system developed in this research. It can be seen that there is little difference in the outcomes when comparing RF, Bluetooth and ZigBee wireless systems used for the collection of EMG signals.

The first factor - the configuration and material used for surface electrodes showed that no clear setup was found throughout all the papers examined. But from known wired setups the commonest setup for the electrodes used the single differential configuration with the electrodes themselves being either dry or pre-gelled made from Ag/AgCl material.

The second factor to be investigated was to identify any other biosignals collected at the same time with wireless systems and being developed in the papers reviewed. It was found that a wide range of biosignals along with EMG were collected which required the setup of the systems presented to be modified to incorporate the biosignals to be obtained. The aim of this research is just to collect sEMG signals and so the setup of the new wireless setup will not have any of the extra features required to collect different biosignals from the body.

The third factor examined was the amplification and filtering of the signals in the overall setup. The findings showed that the most common amplification used an instrumentation amplifier with the filtering of the signal carried out by using a band-pass filter. The band-pass consists of two filters one a low-pass and the other-high pass. There was a wide range of cut-off frequencies found, ranging from 0.5 Hz for high pass to 1.5 kHz for low pass. Also one of the papers showed a notch filter for 60 Hz. This was deemed to be unacceptable for use when examining the frequency content of EMG signals; as the main frequency of an EMG signal lies between 0 to 500 Hz, with the dominance being in the 50 to 150 Hz range [32]. The new design of a system presented in this research incorporated an instrumentation amplifier with a band-pass filter.

The fourth factor investigated was the bit-resolution of the analogue to digital conversion of the signal and it was found in the range from 8-bit to 24-bit. This factor is important as a low bit resolution will give a poor picture of the signal being collected whereas a higher bit resolution gives a better picture of the signal but is major problem in terms of the transfer rate of the signal being acquired. So a balance between the transfer rate and bit resolution of ADC needs to be found [33].

The fifth point examined in all the papers reviewed was the wireless transmission standard to use, whether to use RF, Bluetooth or ZigBee. The setup for this research proposed to use the ZigBee protocol as this was the fastest developing protocol used in the world of wireless transmission of data for miniaturised standalone wireless devices.

The sixth point reviewed was how the wireless system was connected to the computer for displaying information and the data storage of the signals being collected. It was found that this was achieved by either using the RS232 serial port using or a USB port. The wireless setup of the system being developed for this research will use a USB port with a newly developed dongle.

The last point reviewed from the papers examined was sampling the frequency of the systems used to acquire the EMG signals. The values of the sampling frequencies had a wide range from as low as 400 Hz and as high as 200 KHz. This required further research and examining the useful frequency content of EMG signals. It was found that the optimum frequency should be set up at a value no less than 1 kHz [34].

Table 2.4 – Comparison of the Three Wireless Systems Examined

Questions	Radio Frequency	Bluetooth	ZigBee
What electrode configuration was used i.e. type and material?	There was no clear common electrode configuration used and material used.	There was no clear common electrode configuration used or material.	There was no clear common electrode configuration used, or material used.
Which biosignals were collected with the system?	The other biosignals collected with systems were ECG and EEG.	The other biosignals collected with these systems were electrocardiography (EKG) signals.	The other biosignals collected with this system were fEMG, ECG, EEG and EOG.
What amplification and filtering was used and where?	Any amplification of the signals was commonly amplified by instrumentation amplifiers with band-pass filtering.	Any amplification of the signals was commonly amplified by instrumentation amplifiers with band-pass filtering.	Any amplification of the signals was commonly amplified by instrumentation amplifiers with band-pass filtering.
What was the bit resolution of analogue to digital converter (ADC) used?	The most commonly used bit resolution of the analogue digital conversion was 16-bit but was as low as 10-bit and as high as 24-bit.	The most commonly used bit resolution for the analogue digital conversion ranged from 8-bit to 16-bit.	The most commonly used bit resolution for the analogue digital conversion was as low as 10-bit and as high as 16-bit with 16-bit the most common.
What type of wireless link used i.e. type and frequency?	The type of wireless links using RF frequencies varied from infra-red links to sound waves.	The types of wireless links used were different commercially available Bluetooth transceiver modules.	The type of wireless link used was a ZigBee industry compliant transceiver such as the XBee® modules.
What type of computer interface was used with wireless system?	The most commonly used computer interface to the wireless system was the computer serial port or USB port.	The most commonly used computer interface used a RS232 serial port or the USB port with a Bluetooth dongle.	The most commonly used computer interface for this wireless system was serial RS232 port or a USB dongle.
What was the sampling frequency used to acquire the sEMG signal?	The sampling rate for the data collection of the signals varied greatly from 500 Hz up to several values in kHz's.	The sampling rate for the data collection of the signals varied greatly from 512 Hz up to 2 kHz.	The sampling rate for the data collection of the signals varied greatly from 400 Hz up to 2.8 kHz.

This chapter summarised the literature review for various types WsEMG technology such as (a) RF, (b) Bluetooth and (c) ZigBee that have been presented at conferences and then published as part of the conference papers; or published in journals. It has shown that the majority of papers published have been presented at conferences with very few published in journals. This has shown that WsEMG technology is in its infancy and has a long way to go before it can be recognised as a credible alternative technology that can be used in the data collection of sEMG signals.

The next chapter will present the methodology used in the design, development and creation of the new WsEMG electrodes used in this research.

Chapter 3
Methodology in the Development of Wireless Surface Electrodes

This chapter will discuss the methodology used for the design, development and building of the new Wireless Surface (WsEMG) Electrodes used in this research, and the data collection of sEMG signals from the *vastus lateralis* muscle of the quadriceps.

Chapter 2 in the literature review it was found that there were three main techniques used for the wireless link between sEMG electrodes and the computer. These were:

- RF
- Bluetooth
- ZigBee

For the purposes of this research ZigBee was chosen as the wireless link for the transmission of the sEMG signals between the electrodes and the laptop computer used for data storage purposes.

This chapter will discuss the methodology used in the design and development of the electrodes only from the initial concept to the final design and build of the WsEMG electrodes to be used.

3.1 Concept and Block Diagram of WsEMG Electrodes

The proposed block diagram for the system is shown in Figure 3.1 and incorporates two separate nodes. The sensor node will be placed on the subject's body and the other a USB dongle node is connected to the laptop computer for receiving and storing the data.

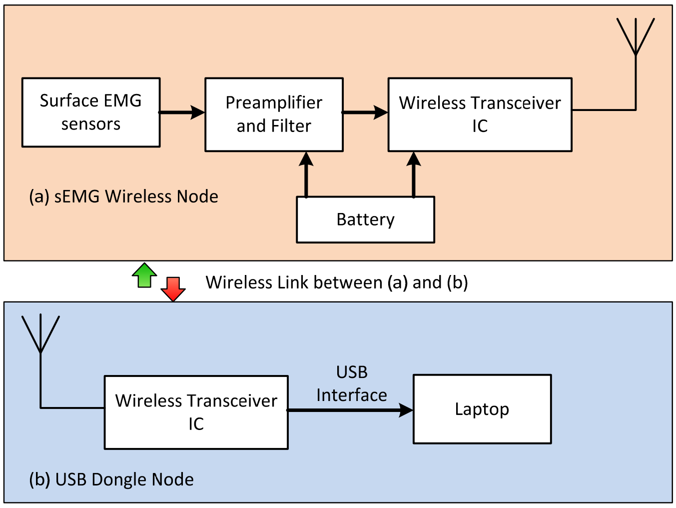


Figure 3.1 – The Proposed Block Diagram for the Design/Build of WsEMG Electrodes

The detail of the literature review and current trends in wireless technology influenced the design and development of the systems used for the WsEMG electrodes. The detailed block diagram Figure 3.2 shows the necessary components needed to be considered in the final system built. The main component used was the Cypress PSoC® chip, which incorporated a number of features necessary for the design of the WsEMG electrodes to be used in this research.

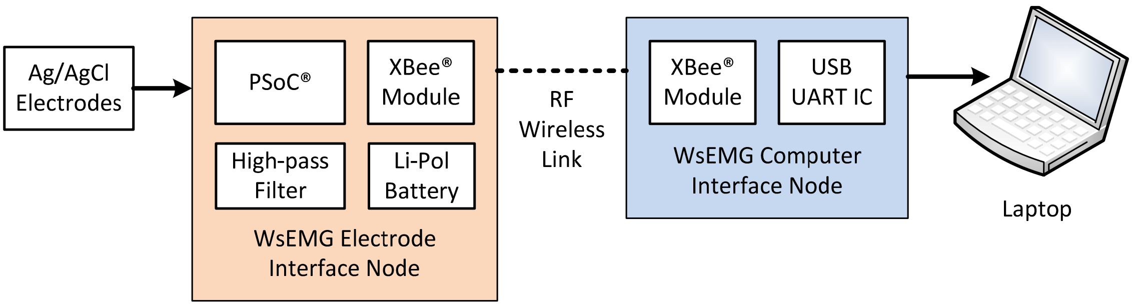


Figure 3.2 – The Components Used for the WsEMG Electrodes

This new WsEMG system has been split into two different modules and is covered in sections:

3.2 WsEMG electrode interface node

3.3 WsEMG laptop computer interface node

3.2 WsEMG Electrode Interface Node

The ***WsEMG electrode interface node*** made the connection between the surface Ag/AgCl surface electrode and the RF wireless link, which consists of four main components and will be covered in sections:

3.2.1 Programmable System-on-Chip (PSoC®)

3.2.2 High-pass Filter

3.2.3 XBee® Transceiver Module

3.2.4 Lithium-ion Polymer (Li-Pol) Battery and Charger

3.2.1 Programmable System-on-Chip (PSoC®)

The main component for the new WsEMG electrode system was the CY8C29466-24PVXA integrated circuit chip from the family of PSoC® 1 made by the Cypress, Semiconductor Corporation, USA, see Appendix A for the datasheet.

The PSoC® chip has integrating configurable analogue and digital peripheral functions which are supported by an integrated development environment (IDE) PSoC® Designer™ to programme the chip with the following functions:

Instrumentation Amplifier plus programmable gain amplifier

Low-pass Filter

Analogue Digital Convertor (ADC)

Universal Asynchronous Receiver/Transmitter (UART) interface to the XBee® transceiver module

The required configurable module layout box for the PSoC® integrated circuit chip for the WsEMG system is shown in Figure 3.3 inside the yellow shaded box.

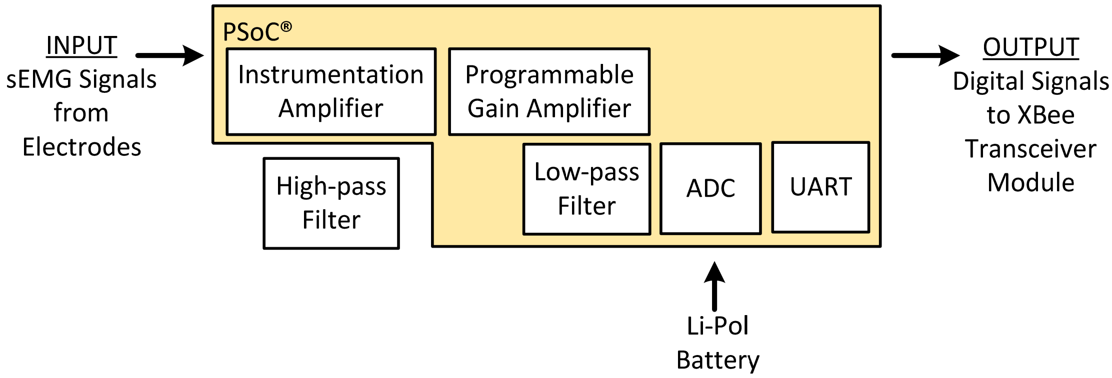


Figure 3.3 – The PSoC® Individual Modules that are required to be configured

Using the PSoC® chip has made the wireless electrode interface mode more flexible. The configuration for the gain and filtering is easily done in terms of coding and does not require any changes in the physical hardware components.

There are six modules which are required to be configured and coded on the PSoC® CY8C29466-24PVXA chip for the WsEMG electrode interface. These are covered in sections:

3.2.1.1 Instrumentation Amplifier
3.2.1.2 Programmable Gain Amplifier
3.2.1.3 Low Pass Filter
3.2.1.4 Analogue Digital Convertor (ADC)
3.2.1.5 UART
3.2.1.6 24-bit timer

To be able to configure the PSoC® chip as required for the WsEMG, PSoC® Designer™ software is required, which has its own Integrated Design Environment (IDE). The IDE allows the user to be able to customise the integrated circuit to meet specific application requirements. The PSoC® Designer™ has the following subsystems:

The PSoC® Designer™ IDE workspace shown in Figure 3.4 area has a number of active windows that differ depending on the functionality of the subsystem are in. These are:

- Chip-Level Editor
- Code Editor
- Build Manger
- Debugger

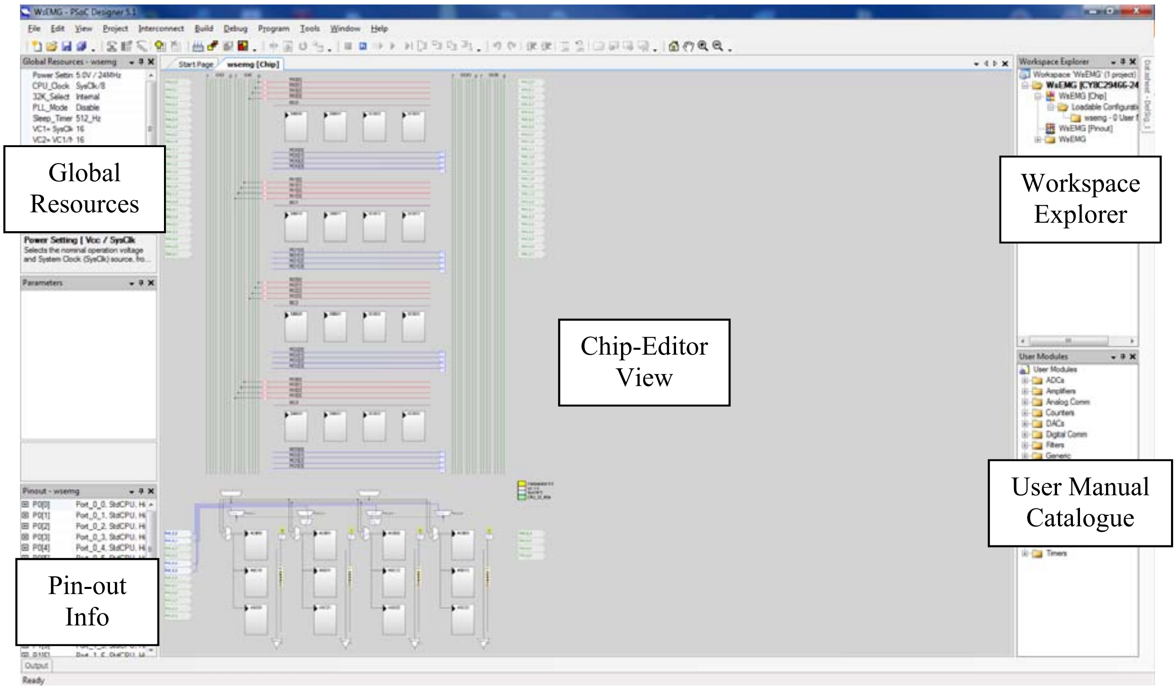


Figure 3.4 – The IDE Workspace for the PSoC® Designer™

The ***Chip-Level editor*** which is the main view of the IDE shows the diagram of the resources available on the CY8C29466-24PVXA chip to be selected and is shown in detail in Figure 3.5. The blocks types available are split into either digital or analogue and the interconnections to the pins of the chip.

The ***Code Editor*** is a full featured text editor designed for editing and assembling the C code in the project. The C code is the application code that is downloaded on the PSoC® chip for the modules selected from the Chip Editor.

The ***Build Manger*** is the utility that controls the various parts of the build process including the compiler, assembler and linker. It also manages the process of building the project and preparing the download to the PSoC® chip.

The ***Debugger*** this has multiple windows that allow interaction and observe the code execution on the PSoC® chip.

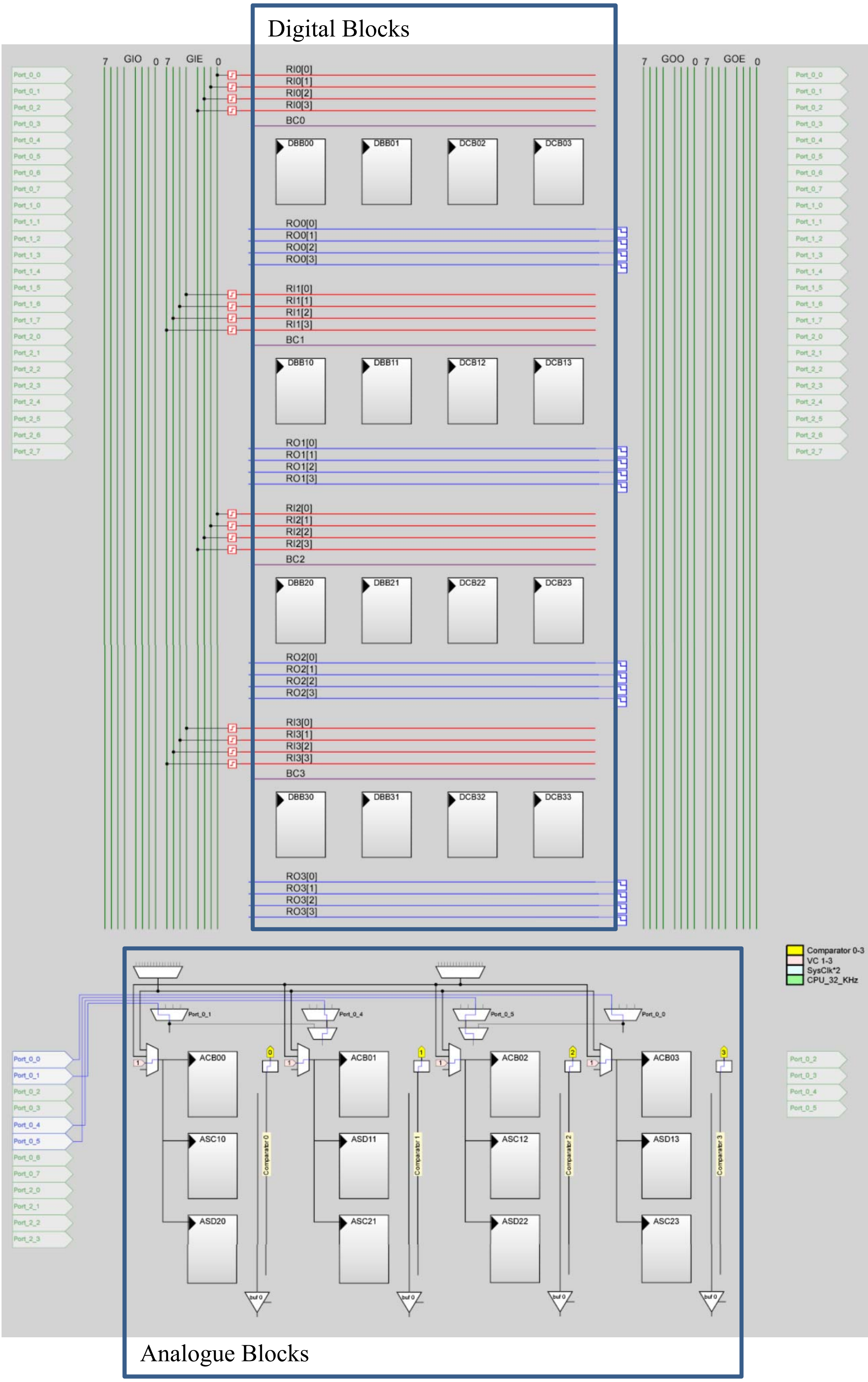


Figure 3.5 – The Detail View of the Chip Editor Window for CY8C29466-24PVXA chip of IDE Workspace

3.2.1.1 Configuration of Instrumentation Amplifier

The CY8C29466-24PVXA chip offers analogue module blocks for configuration of the instrumentation amplifier to collect the sEMG signals from the surface electrodes, and was selected for the following points:

- Low Noise
- Low Nonlinearity
- Simple Gain Selection
- Adequate Bandwidth

The instrumentation analogue module blocks on the PSoC® chip being used have the following features:

- User-programmable gain from 2 to 16 with a two op amp topology
- User-programmable gain up to 93 for the three op amp topology
- High impedance differential inputs
- Single-ended output
- Selectable reference with the two op amp topology

The instrumentation amplifier with the three op amp topology has been chosen as it had excellent common mode rejection ratio (CMRR) and a wide dynamic range. The schematic of the three op amp topology is shown in Figure 3.6.

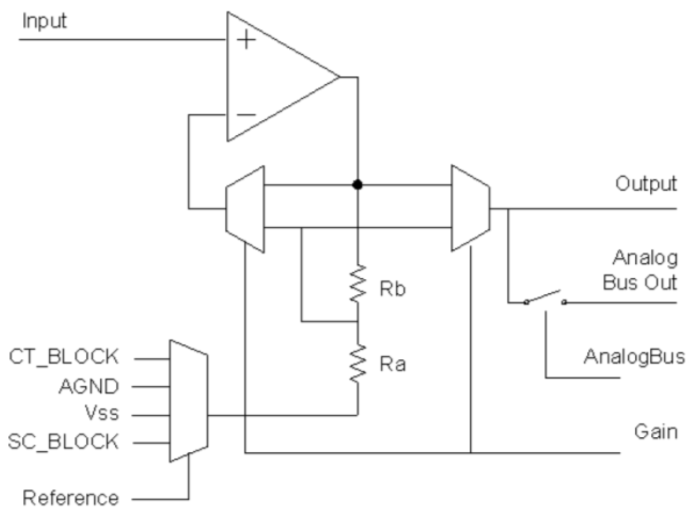


Figure 3.6 – Circuit diagram for the Instrumentation Amplifier (three op amp topology)

Three analogue block modules were required to implement the instrumentation amplifier on the IDE is shown in Figure 3.7 by three red coloured boxes, labelled as:

a. INSAMP NON_INV

b. INSAMP INV

c. INSAMP CONVERT

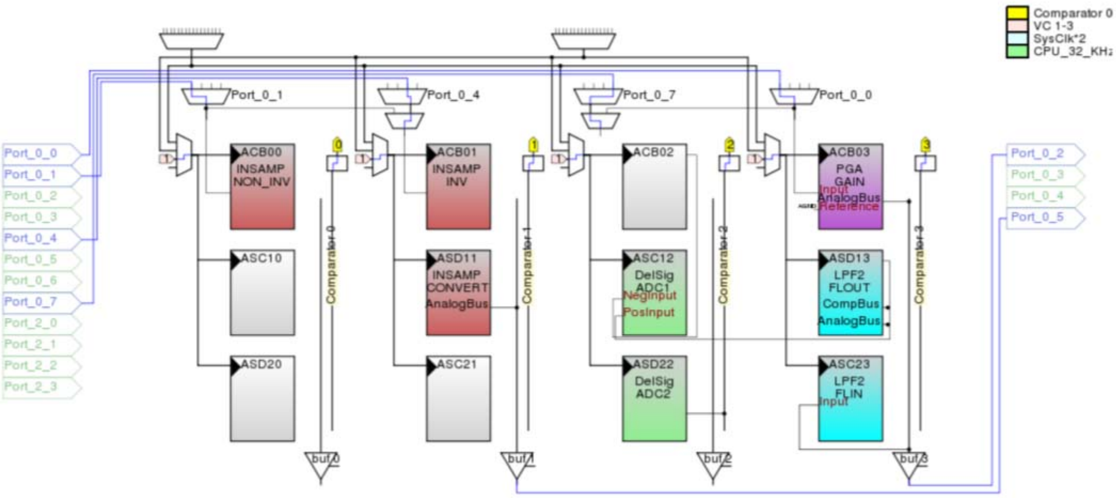


Figure 3.7 – The Analogue Modules used to configure Analogue Elements of the WsEMG System on the PSoC®

The output voltage of INV and NON_INV block are given by Equations 3.1 and 3.2 respectively.

$$V_{out\ INV} = V_{CM} + \left(1 + \frac{R_b}{R_a}\right)\left(\frac{V_{IN+} - V_{IN-}}{2}\right) \qquad \text{Equation 3.1}$$

$$V_{out\ NONINV} = V_{CM} - \left(1 + \frac{R_b}{R_a}\right)\left(\frac{V_{IN+} - V_{IN-}}{2}\right) \qquad \text{Equation 3.2}$$

From Figure 3.7 the output of block INV drives the capacitor C_b input of CONVERT and the output of block NON_INV drives the capacitor C_a input of CONVERT. The sign of the C_b input is fixed by block topology to be negative and the sign of the C_a input is set in the User Module firmware to be positive. The capacitors C_a and C_b have identical values; so the conversion of the continuous time block outputs is the differential and the output of CONVERT is given by Equation 3.3.

$$CONVERT = V_{AGND} + (V_{IN+} - V_{IN-})\left(1 + \frac{R_a}{R_b}\right)\frac{C_a}{C_b} \qquad \text{Equation 3.3}$$

The available resistor ratios for R_b and R_a set the useful gain range of the input stage to values between 1.0 and 48.0. Conversion gains in the switched capacitor block can be between 0.032 and 1.9375 (i.e. 1/32 to 31/16). This yields a large number of useful gain settings between 1.0 and 93. Differential Gain and Conversion Gain are set independently by the user as parameters in PSoC® Designer™ and may be changed at run time through the SetGain Application Programming Interface (API) function.

The input of the instrumentation INV and NON_INV inputs were connected to port_0_1 and port_0_4 respectively see Figure 3.7. The output of the instrumentation amplifier is placed on the analogue column output bus using the enable selection of the AnalogBus module parameter see Figure 3.7. The AnalogBus module parameter was set to the AnalogOutBus_1 and the other setting for the parameter was set in the API with the CommonModeout is set to No Connect. Figure 3.8 shows the setting of the module parameters.

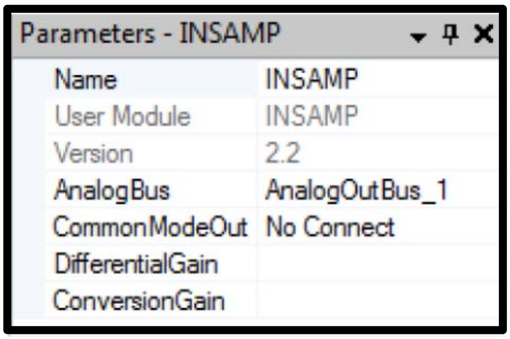


Figure 3.8 – The Setting of Instrumentation Amplifier in the API window

3.2.1.2 Configuration of Programmable Gain Amplifier

The Programmable Gain Amplifier used on the PSoC® has following features:

- Thirty-three user-programmable gain settings with a maximum gain of 48.0
- High impedance input
- Single-ended output with selectable reference

The Programmable Gain Amplifier circuit diagram is shown in Figure 3.9 and only required one analogue block module to be implemented on the IDE, shown in Figure 3.7 by the purple coloured box, labelled as PGA GAIN.

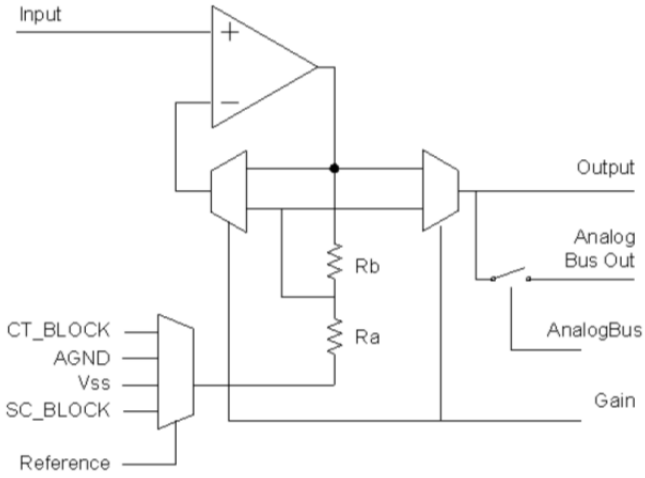


Figure 3.9 – Circuit diagram for the Programmable Gain Amplifier

This module amplified an internal or externally-applied signal. This signal could be referenced to the internal analogue ground, Vs or other selected references. The gain was set by programming the selectable tap in a resistor array and the feedback tap in a continuous time analogue PSoC® block. The output voltage was determined by using two equations. For a gain greater than or equal to one, the top resistor string was connected to the op-amp output and the resistor tap was connected to the inverting input of the op-amp. The gain was calculated using Equation 3.4.

$$V_{out} = (V_{IN} - V_{GND})\left(1 + \frac{R_b}{R_a}\right) + (V_{GND}) \qquad \text{Equation 3.4}$$

For the gain of less than one, the op-amp was set as a voltage follower and the user module output was selected at the resistor tap. The gain is calculated using Equation 3.5.

$$V_{out} = (V_{IN} - V_{GND})\left(\frac{R_a}{R_a + R_B}\right) + (V_{GND}) \qquad \text{Equation 3.5}$$

The input to the programmable gain amplifier were driven by the outputs of the adjacent PSoC® blocks and the analogue column input multiplexer and was set to AnalogColumn_InputMUX_3. The gain of the PGA was referenced to AGND (on-chip analogue ground). The AnalogBus parameter was set to AnalogOutBus_3, which was off pin_0_2. The API settings are shown in Figure 3.10.

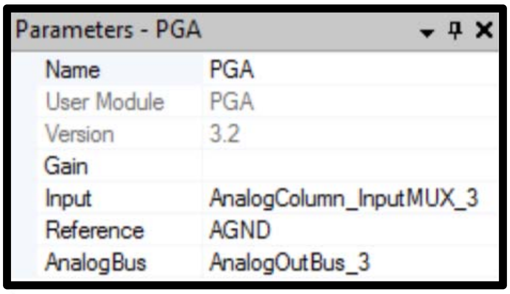


Figure 3.10 – The Setting of Programmable Gain Amplifier in the API window

3.2.1.3 Configuration of Low Pass Filter

The PSoC® CY8C29466-24PVXA only allowed for a two-pole low-pass filter to be configured using the IDE. So when a band pass filter was used for the WsEMG a high-pass filter needed to be used and configured alongside the chip as shown in Figure 3.3. This was required because there were no high-pass filter module available on the chip. The low-pass features on the PSoC® had the following attributes available:

- User-programmable gain
- User-programmable corner frequency and damping ratio with no external components
- Filter corner-frequency stability directly derived from clock accuracy
- Filter sampling rates to 1.0 MHz

This module implemented a general purpose second order state variable low-pass filter. The corner frequency and damping ratio are functions of the clock frequency and the ratios of the selected capacitor values. This could be implemented on any classical all-pole filter configuration (Butterworth, Bessel and Chebyshev). The corner frequency could be set very accurately or adjusted by controlling the sample rate clock.

The low-pass filter is shown in Figure 3.11 and it required only two analogue block modules to be implemented on the IDE, shown in Figure 3.7 by the light blue coloured box, labelled as:

a. LPF2 FLIN
b. LPF2 FLOUT

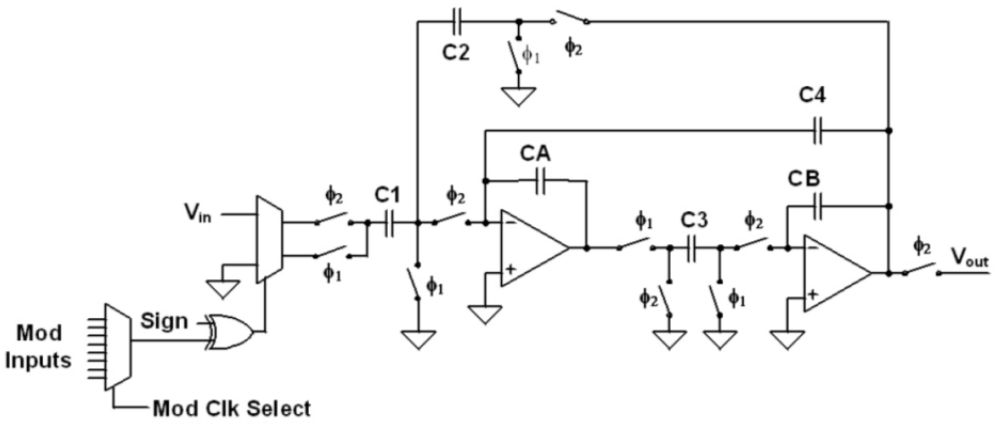


Figure 3.11 – Circuit diagram for Two-Pole Low Pass Filter

The PSoC® Designer™ provided a filter design wizard to automate the procedure for the two-pole filters show in Figure 3.12. In the wizard all that needed to be activated was to select the cut-off frequency and sampling rate of the frequency and filter type. It will then generate the required parameters for the research. The filter configuration for the WsEMG system was a Butterworth filter with a cut-off frequency of 1 kHz.

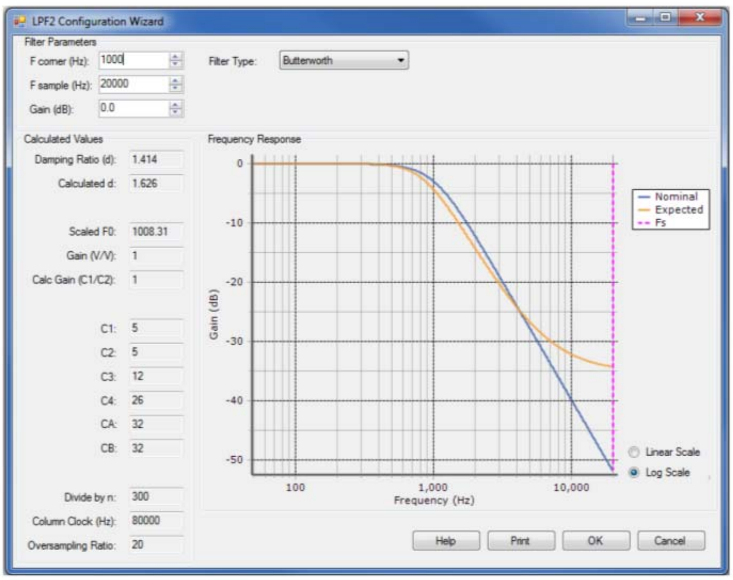
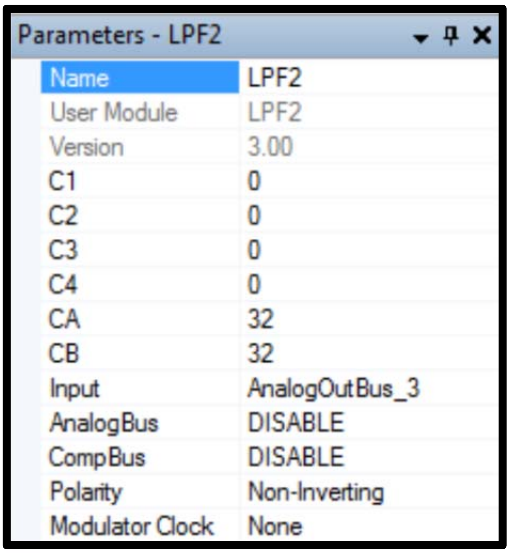


Figure 3.12 – The output from the Filter Design for a Butterworth Low-Pass Filter with a cut-off of 1 kHz

The inputs to the filter are driven by the output of the PGA module. The AnalogBus is was not been connected to this module. The CompBus which was a FLOUT block comparator output needed to be routed to the input bus of the digital PSoC® blocks or to an interrupt. This was also not connected for this module. Polarity is the parameter that determines the polarity of the output relative to the input, in this research it was been sets to Non-inverting. The Modulator Clock was used to connect the polarity control in the A input of the input block (FLIN). For this research it had been set to none. Figure 3.13 shows the API settings for the two-pole low-pass filter.



Parameters - LPF2	
Name	LPF2
User Module	LPF2
Version	3.00
C1	0
C2	0
C3	0
C4	0
CA	32
CB	32
Input	AnalogOutBus_3
AnalogBus	DISABLE
CompBus	DISABLE
Polarity	Non-Inverting
Modulator Clock	None

Figure 3.13 – The Two-Pole Low-Pass Filter settings in the API window

3.2.1.4 Analogue Digital Convertor (ADC)

The CY8C29466-24PVXA chip offers analogue and digital module blocks for the configuration of an ADC. The ADC used was a Delta Sigma (DΣ) ADC, which was ideal for converting analogue signals over a wide range of frequencies, from DC to several megahertz. Basically, these converters consisted of an oversampling modulator followed by a digital/decimation filter that together produced a high-resolution data-stream output.

The ADC on the PSoC® has the following features:

- 6-bit resolution with 32X oversampling to 14-bit resolution with 256X oversampling
- Data in unsigned or signed 2's complement formats
- Maximum sample rates of 65,500 sps at 6 bit resolution, 7812 sps at 14-bit resolution

The ADC circuit diagram is shown in Figure 3.14 and it required only two analogue block modules to activate the input to the ADC. This would need to be implemented on the IDE, and is shown in Figure 3.7 as green coloured boxes, labelled as:

a. DelSig_ADC1

b. DelSig_ADC2

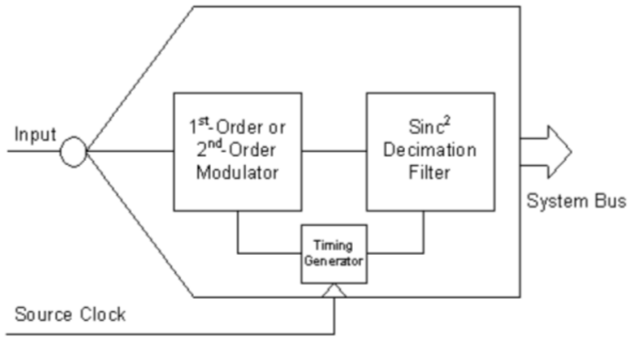


Figure 3.14 – Circuit diagram for the Delta Sigma (DΣ) ADC

Also two digital block modules to act as the output from the ADC were required to be implemented on the IDE. These are shown in Figure 3.15 as green coloured boxes, labelled as:

a. DelSig PWMLSB

b. DelSig PWMLSB Output

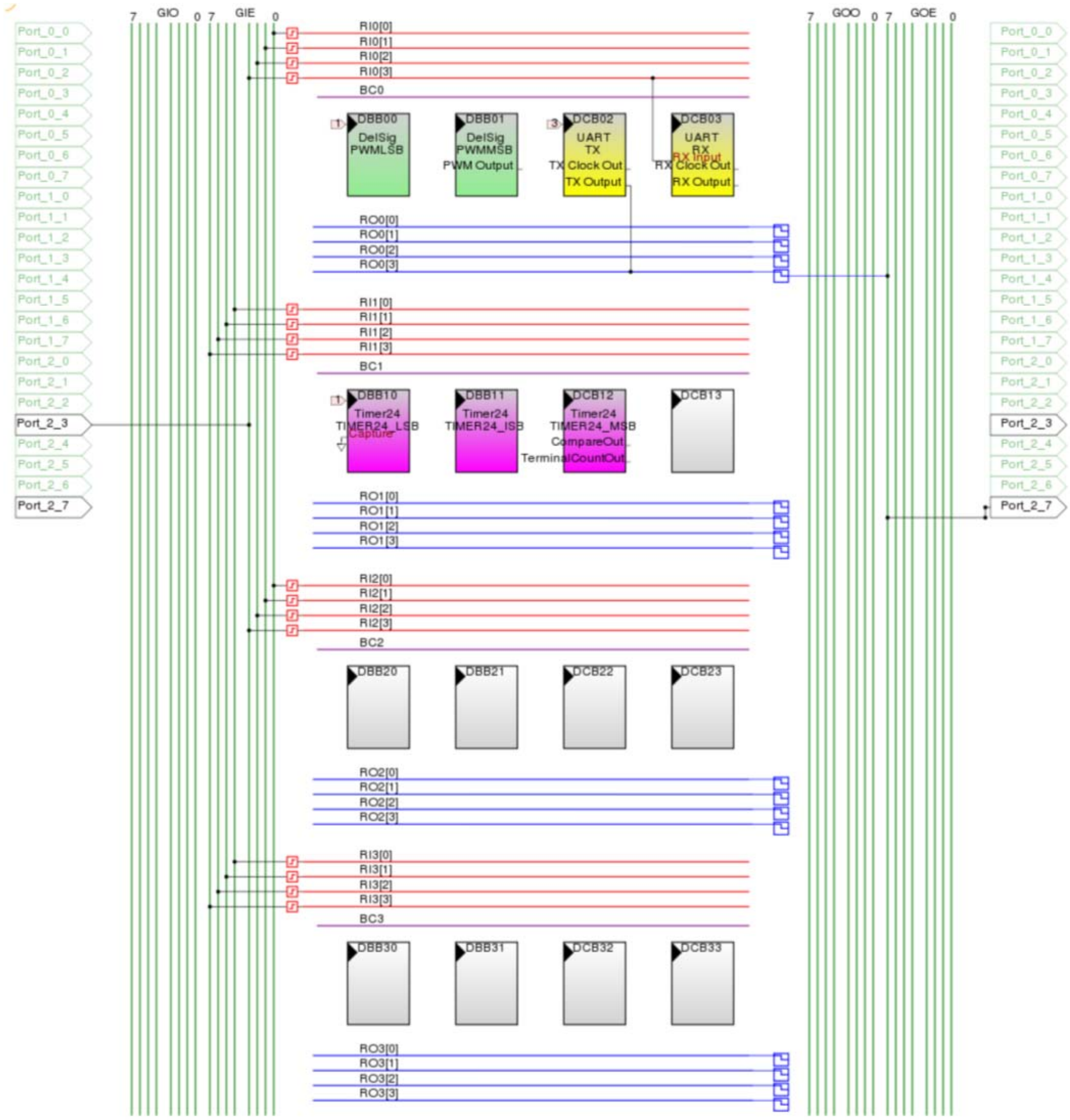


Figure 3.15 – The Digital Modules used to configure Digital Elements of the WsEMG System on the PSoC® on the IDE

The output rate was determined by dividing the data by 4 to get the 1-bit over sample rate and then divided by the decimation rate to get the final sample rate by using Equation 3.6.

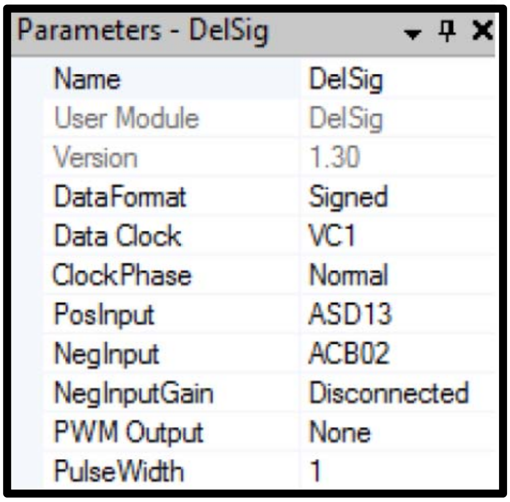
$$Sample\ Rate = \frac{Data\ Clock\ Frequency}{4 \times Decimation\ Rate}\ \text{samples/second} \qquad \text{Equation 3.6}$$

It would use a 12-bit DelSig ADC in the research. The decimation rate for the 12-bit ADC is 128. So if the research required 1000 samples per second, the data clock frequency could be calculated using Equation 3.7.

$$Data\ Clock\ Frequency = Sample\ Rate \times 4 \times Decimation\ Rate \qquad \text{Equation 3.7}$$
$$= 1000 \times 4 \times 128 = 0.512\ MHz$$

As the maximum range of the signals was required, so it was chosen to the RefMux parameter to (V_{DD}/2) ± (V_{DD}/2) with the range for input is from 0 to 3.3V. Since the 12-bit ADC was chosen, so total will be $2^{12} - 1$ which is 4095 samples, so each sample will be 0.00080586 V.

The data format parameter was set to signed data because it gave a range in the value from -2^{n-1} to $+2^{n-1} - 1$. The Data clock parameter was set to VC2 which had been set to 0.533 MHz. The sample rate work out was set at 1048 which is close to 1000 samples per second. The clock phase was set to normal. PosInput was set to the ASD13 block which was set to the output block of the low-pass filter. The NegInput was set to the ACB02 block since that block would have no module setting. The NegInputGain was set to disconnected, as this function would not be required. The PWM output was set to none. The Pulse Width was set to 1. The research would not be using the PWM and the NegInput so no settings were configured. Figure 3.16 shows the parameters settings.



Parameters - DelSig

Name	DelSig
User Module	DelSig
Version	1.30
DataFormat	Signed
Data Clock	VC1
ClockPhase	Normal
PosInput	ASD13
NegInput	ACB02
NegInputGain	Disconnected
PWM Output	None
PulseWidth	1

Figure 3.16 – The ADC settings in the API window

3.2.1.5 Universal Asynchronous Receiver/Transmitter (UART)

The UART module provided by the PSoC® has following features:

- Asynchronous receiver and transmitter
- Data-format compliant with RS-232 serial-data format
- Burst rates up to 6 M bits/second
- Data framing consists of start, optional parity, and stop bits

The UART module is 8-bit that supports data format serial communications over two wires. The received and transmitted data format includes a start bit, optional parity, and a stop bit; see Figure 3.17 for the block diagram of UART. Two digital block modules were required to be implemented on the IDE, and all shown in Figure 3.15 as the yellow coloured boxes, labelled as:

a. UART TX
b. UART RX

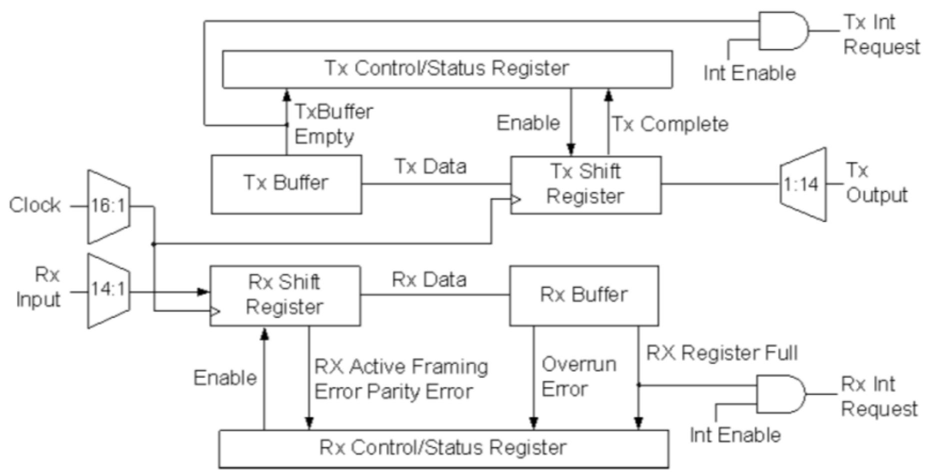


Figure 3.17 – Block diagram for the UART

The UART User Module implemented a serial transmitter and receiver. The UART mapped onto the two PSoC® blocks which were designated TX and RX. The TX PSoC® block gives transmitter functionality and the RX PSoC® block gives receiver functionality. The RX and TX blocks operate independently. Each had its own Control and Status register, programmable interrupts, I/O, Buffer register, and Shift register. They share the same enabled, clock, and data format. Setting the Enable bit in the RX Control and TX Control registers enables the UART to operate. Enabling and disabling was performed using the API provided functions. The UART User Module clock was shared by both the RX and TX components. The clock frequency selected had to be eight times the frequency of the required data bit rate. Each received or transmitted data bit requires eight input clock cycles. The data received and transmitted was a bit stream that consisted of a start bit, eight data bits, an optional parity bit, and a stop bit.

The clock setting for the UART module was set to VC3. Since the XBee® baud rate was set to 115200 bps, it needed to match the baud rate for the PSoC® UART module to 115200 bps as well. The clock rate was set to eight times the desired bit rate. One data bit was received or transmitted every eight clock cycles. The VC3 was set to the system clock to divide by 27 so the baud rate was found using Equation 3.8.

$$baud\ rate = \frac{24\ MHz}{27 \times 8} = 512\ kHz \qquad \text{Equation 3.8}$$

Only 2% tolerance of the clock is within the range of the PSoC® to enable it to talk to the XBee® properly. The RX Input used a global bus to connect the external pin. It was set to ROW_0_Input_3 which was connected to pin_2_3. The TX Output also used a global bus to connect the external pin as well. This is set to Row_0_Output_3 which was connected to pin_2_7. The TX Interrupt was set to TXRegEmpty which was best used to maximize the output of the transmitter. The ClockSync parameter was used to control the clock skew and ensure its accurate operation when reading and writing the PSoC® block register values. In the research it was set to sync to sysclk. The Command Terminator was where the parameters selected the characters that signalled the end of a command. When it receive data a flag was sent signalling that a complete command has been received. After this flag was set additional characters are not accepted until the cmdReset() function was called. This had been set to 13 which was a carriage return. Figure 3.18 shows the parameter settings.

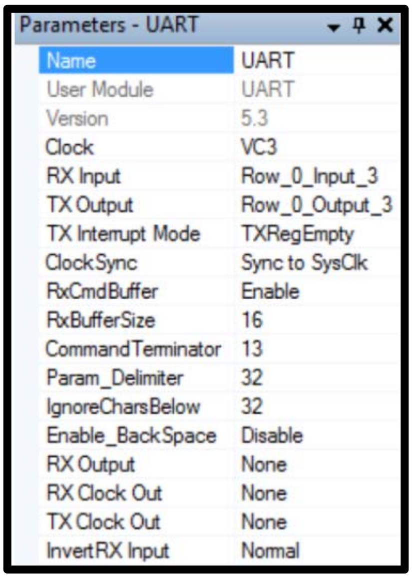


Figure 3.18 – The UART settings in the API window

3.2.1.6 24-bit Timer

The 24-bit Timer user module provided a down counter with programmable period and capture ability. The clock and enable signals could be selected from any system time base or external source. Once started, the timer operated continuously and reloaded its internal value from the period register upon reaching the terminal count. The output pulses high in the clock cycle following any terminal count. Events can capture the current Timer count value by asserting the edge-sensitive capture input signal. In each clock cycle, the Timer tested the count against the value of the compare register for either a "Less Than" or "Less Than or Equal To" condition. Interrupts may be generated based on terminal count and compare signals.

The 24-bit Timer block diagram is shown in Figure 3.19 and it required three digital block modules to be implemented on the IDE, shown in Figure 3.8 by the purple coloured box, labelled as:

a. TIMER24_LSB capture
b. TIMER24_LSB
c. TIMER24_MSB

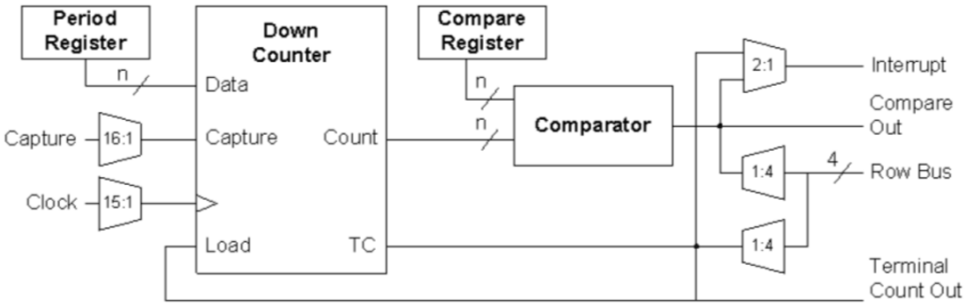


Figure 3.19 – The 24-bit Timer block diagram

Each digital block module contributed 8 bits to the total resolution. The consecutive blocks are linked so their internal carry, terminal count and the compare signals are synchronously chained. This concatenates the 8-bit Count, Period and Compare registers (Data registers DR0, DR1 and DR2, respectively) from block to block to provide the required resolution. The value of the timer period can be calculated using Equation 3.9.

$$Output\ Period = Source\ Clock\ period\ \times (Period\ Resgister\ Value + 1)$$

Equation 3.9

The output period required for the research was 1 second and the source clock was set at 8 MHz so the period register value, could be calculated using Equation 3.10.

$$Period\ Register\ Value = Output\ Period\ Source\ Clock\ Period - 1$$

$$= \frac{1}{8 \times 10^6} - 1 = 7{,}999$$

Equation 3.10

The clock parameter was selected for VC1 as the VC1 was set to 8 MHz. The capture parameter was set to low as the falling edge of the clock cycle caused the count register to be transferred to the compare register. The period of the timer was set to 7999999. The interrupt type parameter was set to the terminal to count events to trigger the interrupt. The clocksync parameter was set to sync to sysclk. The invert capture was set to normal which determined the sensitivity of the enable input signal to active-high. It would not be using the compare function, so this would not be used.

The API settings are:

- Timer24_EnableInt
- Timer24_Start
- Timer24_Stop

The most important feature was that when programmed the timer interrupt just does not write in the c code file, it also needs to set the assembly code file call: Timer24INT.asm which was the file content timer's interrupt service routine. Under _Timer24_ISR it needed to add a "limp_timercount" to tell the timer where the interrupt would go. Figure 3.20 shows the code that needed to be added.

```
_Timer24_ISR:

   ;@PSoC_UserCode_BODY@ (Do not change this line.)
   ;---------------------------------------------------
   ; Insert your custom assembly code below this banner
   ;---------------------------------------------------
   ;   NOTE: interrupt service routines must preserve
   ;   the values of the A and X CPU registers.
   ljmp _timecount
   ;---------------------------------------------------
   ; Insert your custom assembly code above this banner
   ;---------------------------------------------------
```

Figure 3.20 – Interrupt service routine for Timer24

3.2.2 High-pass Filter

The sEMG signals have a frequency range between 10 Hz to 1 kHz because the PSoC® could only configure a low pass filter. An external passive high-pass filter was designed cut the frequency which was around 10 Hz. This research used a passive RC high-pass. The reason for this was to ease the design as only two components are needed; a resistor with a capacitor, see Figure 3.21.

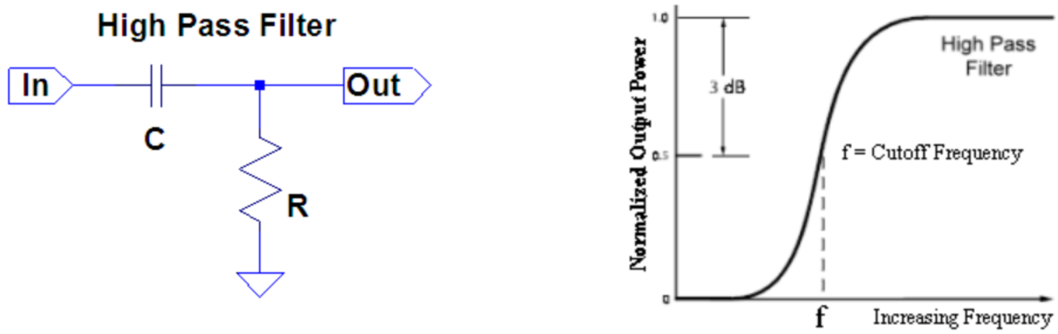


Figure 3.21 – RC Filter Circuit and Frequency Response Diagram

The RC filter was chosen as it was easy to configure and cheaper than an active filter, which would require more components. The value was chosen for the RC passive high filter at 68 kΩ and 0.22 uF, using Equation 3.11, the cut-off frequency was calculated to be at 9.6 Hz, which is very close to the 9.6 Hz required.

$$f_c = \frac{1}{2\pi RC} \qquad \text{Equation 3.11}$$

3.2.3 XBee® Transceiver Module

The wireless link chosen was an XBee® RF transceiver module, because this is commonly used in health devices and are easy to configure. These are available from Digi International, USA. XBee® modules are either Series 1 (802.15.4) or XBee® Series 2 (ZB) and are shown in Figure 3.22.

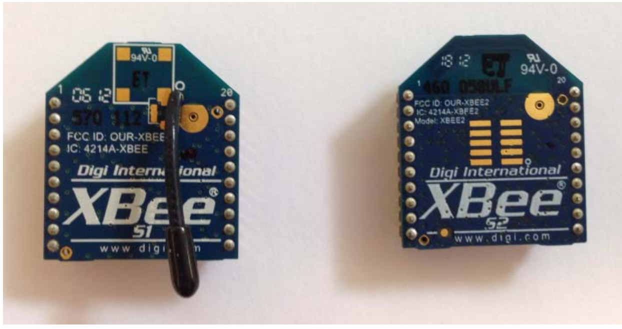


Figure 3.22 – XBee® modules: Series 1 on the left and Series 2 on the right.

Table 3 details the comparisons of a number of technical features extracted from the datasheets for XBee® Series 1 and XBee® Series 2.

Table 3.1: Product Comparison between XBee® Series 1 and XBee® Series 2.

Feature	XBee® ***Series 1***	XBee® ***Series 2***
Indoor/Urban range	up to 100 ft. (30m)	up to 133 ft. (40m)
Outdoor RF line-of-sight range	up to 300 ft. (100m)	up to 400 ft. (120m)
Transmit Power Output	1 mW (0dbm)	2 mW (+3dbm)
RF Data Rate	250 Kbps	250 Kbps
Receiver Sensitivity	-92dbm (1% PER)	-98dbm (1% PER)
Supply Voltage	2.8 - 3.4 V	2.8 - 3.6 V
Transmit Current (typical)	45 mA (@ 3.3 V)	40 mA (@ 3.3 V)
Idle/Receive Current (typical)	50 mA (@ 3.3 V)	40 mA (@ 3.3 V)
Power-down Current	10 uA	1 uA
Frequency	ISM 2.4 GHz	ISM 2.4 GHz
Dimensions	0.0960" x 1.087"	0.0960" x 1.087"
Operating Temperature	-40 to 85 C	-40 to 85 C
Antenna Options	PCB, Integrated Whip, U.FL, RPSMA	PCB, Integrated Whip, U.FL, RPSMA
Network Topologies	Point to point, Star, Mesh (with DigiMesh firmware)	Point to point, Star, Mesh
Number of Channels	16 Direct Sequence Channels	16 Direct Sequence Channels
Filtration Options	PAN ID, Channel & Source/Destination	PAN ID, Channel & Source/Destination

The selection of the XBee® transceiver module used for this research was initially determined to be the XBee® series 1 module as it was easier to setup for point to point connection. This was used to test the system to be tested and when this was found to be functioning reliably the XBee® Series 2 module was used for the research work on the subjects. The difference between the two is that the Series 2 modules are used for mesh networks and can test multiple patterns of movement.

The final development of the WsEMG electrodes used the series 2 transceivers. This would allow for expansion in the number electrode interfaces to be incorporated into a mesh network. By having more than one electrode interface it would be possible to collect EMG signals simultaneously from different sites on a muscle or muscles.

3.2.4 Lithium-ion Polymer (Li-Pol) Battery and Charger

For the WsEMG electrode node to function a battery which is rechargeable, small and light was required. This research used the lithium-ion polymer battery LP-402025-1S-3 as it was suitable for this wireless electrode interface node. The battery chosen required the designing of a suitable battery charger. This was designed as part of the research, see Appendix B for the datasheet.

This lithium-ion polymer battery will need to be charged at regular intervals, so a new charger was required. The battery charger chip used was a LTC4053-4.2 chip is manufactured by Linear Technology, see Appendix C for the datasheet. The reason for choosing this battery charger was because it is a standalone linear charger specially designed for charging the lithium-ion battery. It could be powered directly from a USB port; also it had a thermal regulator to automatically adjust the charge current to limit the battery temperature during charging and in different temperature conditions. The LTC4053-4.2 only needed to use one external resistor to program the charge current; so using Equation 3.12, the resistor value could be calculated.

$$R_{Prog} = \frac{1500\,V}{I_{Chg}} \qquad \text{Equation 3.12}$$

The battery capacity was 155 mAh so when charging the battery it needed the charge current to be very small. For the research the charge current was set to 20 mA. The external resistor value would be 75 kΩ.

3.3 WsEMG Computer Interface Node

The WsEMG computer interface node made the connection between the RF wireless link and the computer. This consists of two components and will be covered in sections:

3.3.1 XBee® transceiver module

3.3.2 USB UART chip

The XBee® transceiver and USB UART were combined to form the USB dongle. This would be plugged into a USB port of the laptop computer. The sEMG signals would be collected via the USB dongle and would be stored in the laptop for further processing, shown in Figure 3.23.

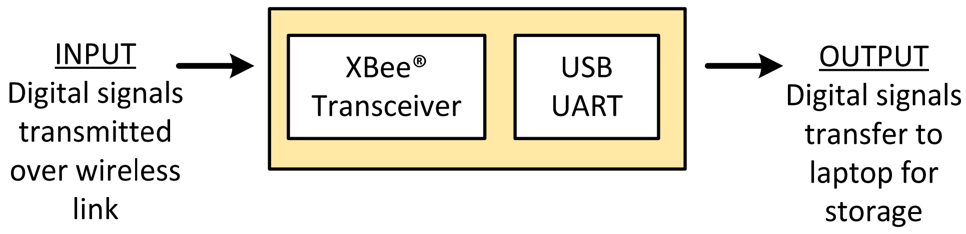


Figure 3.23 – The USB Dongle consisting of the XBee® Transceiver and USB UART chip

3.3.1 XBee® Transceiver Module

The XBee® transceiver attached to the laptop computer interface was the same as described in section 3.2.3. This would be attached to a new USB UART board so that digital signals could be received and transferred to the laptop computer.

3.3.2 USB UART

For the laptop computer to receive the signals from the XBee® transceiver a USB UART was included. A FT232R chip was used for the USB to serial UART with an optional clock generator output, and the new FTDIChip-ID™ security dongle manufactured by Future Technology Devices International Ltd (FTDI), UK, see Appendix D for the datasheet. This allowed the use of the WsEMG Computer Interface Node as this would need no external power supply as it would be powered via the USB port of the laptop computer. The following features were the main reasons for choosing the use of the interface chip:

- The entire USB protocol was handled on the chip. No USB specific firmware programming was required.
- The data transfer rates were from 300 baud rate to 3M baud rate.

- The UART interface support would be for 7 or 8 data bits; 1 or 2 stop bits and odd/even/mark/space/no parity.
- The USB 2.0 full speed compatible.

This chapter has presented the methodology used in the design and development of the new WsEMG electrodes used in this research. These consisted of two separate components. The detailed circuitry and new printed circuits boards for the final design of this research will be presented in the next chapter.

Chapter 4
Detail Circuit Diagrams and Printed Circuit Board of Wireless Surface Electrodes

This chapter will show the detailed circuitry and newly manufactured printed circuit boards (PCBs) that make up the components of the WsEMG electrodes system discussed in Chapter 3. These will consist of three main components and are covered in sections:

4.1 WsEMG Electrode Interface Node
4.2 WsEMG Computer Interface Node
4.3 Lithium-ion Polymer Battery Charger

4.1 WsEMG Electrode Interface Node

This node consists of the new main PCB, which has the Cypress PSoC® CY8C29466-24PVXA chip plus the necessary components related to it, along with the high-pass filter and the socket for XBee® transceiver module plus the three header pins. The header pins are to connect (a) the surface electrodes, (b) the lithium-ion polymer battery and a third (c) which was required only to initially allow the code for the PSoC® chip to be downloaded on the chip via the MiniPro1 programmer, which would not be required later when collecting the sEMG signals.

The overall circuit diagram for the main board WsEMG Electrode Interface Node can be found in Appendix E. Figure 4.1 shows the pin layout connections for the PSoC® CY8C29466-24PVXA chip along with the external crystal and the RC high pass filter.

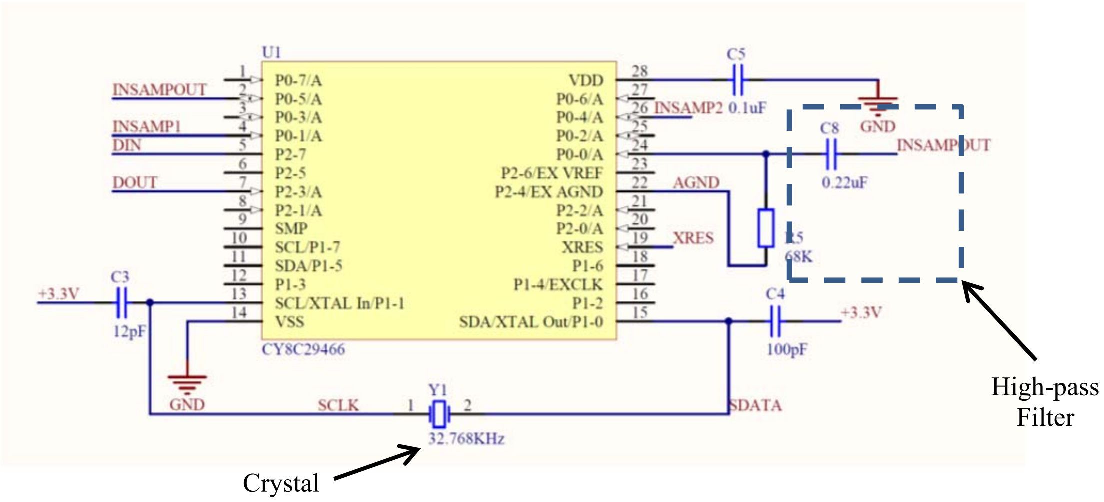


Figure 4.1 – Pin configuration for CY8C29466-24PVXA chip plus components.

The sEMG signals were very small in value with both positive and negative voltages, but the instrumentation amplifier module provided by the PSoC® chip could only accept positive voltages as an input. The input gain limit was symmetrical with the analogue ground, so that the input common mode voltage of 0.5V above the Vss (ground) had to have the same input limitation as the input common mode voltage 0.5V below the Vcc (supply). So a DC offset voltage was required for the sEMG signal to fit into this range. This is achieved by using a voltage divider biasing technique and is shown in Figure 4.2. The DC offset was applied to both inputs of the instrumentation amplifier and is 1.65 V (3.3 V/2) as all the resistors must had to have equal values.

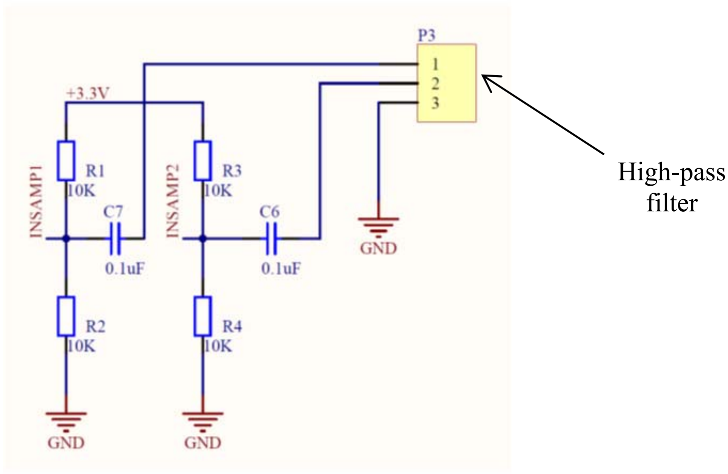


Figure 4.2 – sEMG signal DC offset configuration

The XBee® module on the PSoC® main board was needed to connect the DOUT pin to the RX pin in PSoC® chip; and the DIN pin was connected to TX pin in the PSoC® chip. The circuit schematic is shown in Figure 4.3.

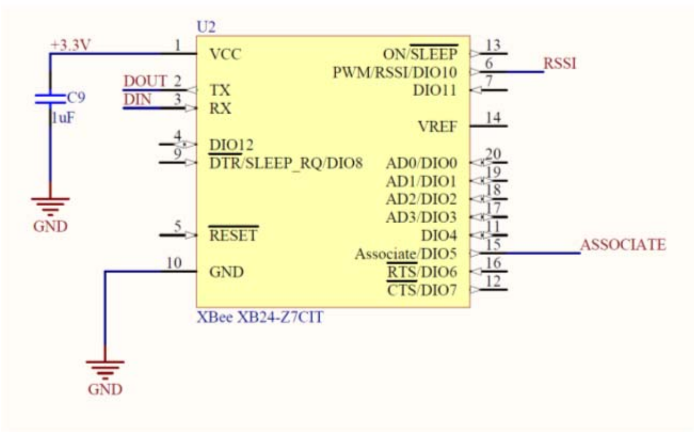


Figure 4.3 – Pin configuration and schematic diagram of XBee® module on main board of the WsEMG electrode interface node

The XBee® module would only work with a supply voltage of 3.3 V DC but the Lithium-ion polymer battery supplied 3.7 V DC so a DC voltage regulator was needed. The voltage regulator MIC5209-3.3 was a 500 mA low-noise load dropout voltage regulator manufactured by Micrel. A semiconductor was used to supply both the XBee® module and the PSOC® chip, see Appendix F for this datasheet. The voltage for small loads only required a 10 mV dropout and less than 500 mV at full load. The circuit configuration is shown in Figure 4.4.

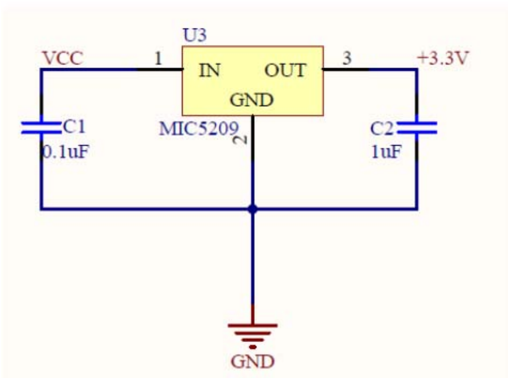


Figure 4.4 – Circuit configuration of MIC5209 voltage regulator for WsEMG electrode interface node

Figure 4.5 shows the components for the main board, the XBee® module, the lithium-ion polymer battery, the sEMG electrode leads and the MiniPro1 programmer.

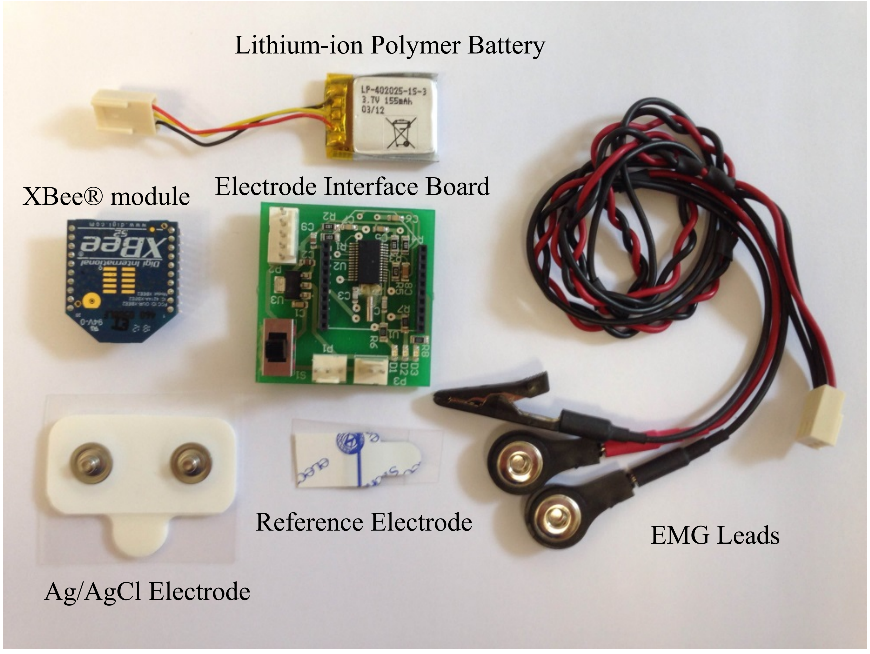


Figure 4.5 – The components that make up WsEMG electrode interface node assembly

Figure 4.6 show pictures of the WsEMG electrode interface node assembled for two different configurations: (a) the top picture shows the initial assembly for the programming of the PSoC® chip with the MiniPro1 programmer and (b) the bottom picture shows it when fully assembled for collection of the sEMG signals. The MiniPro1 programmer module allowed for the configuration of files plus the code that had been build and compiled in the PSoC® Designer™ which needed to be downloaded onto the PSoC® chip. The code for the WsEMG electrode system is found in Appendix G.

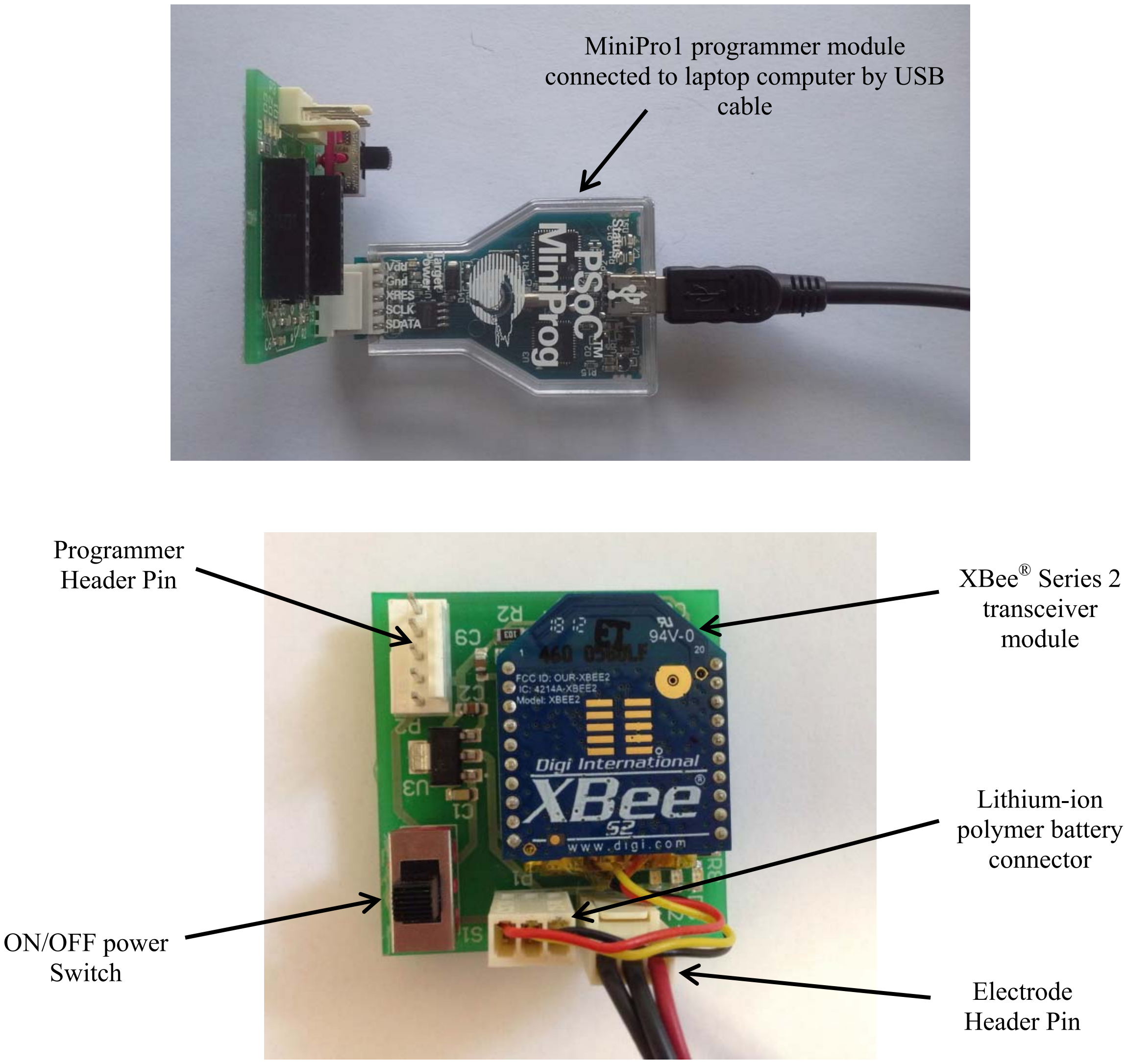


Figure 4.6 – The WsEMG Electrode Interface Node

Overall weight of the board with the XBee® module and battery is 17 grams and the overall dimension is: 42 mm x 41 mm x 20mm.

4.2 WsEMG Computer Interface Node

The overall circuit diagram for the main board WsEMG Computer Interface Node is found in Appendix H. This node consists of a PCB to act as a USB dongle to the laptop computer, which has a socket for the XBee® transceiver module and a PCB mounted USB Male Type A connector. The circuit configuration is shown in Figure 4.7.

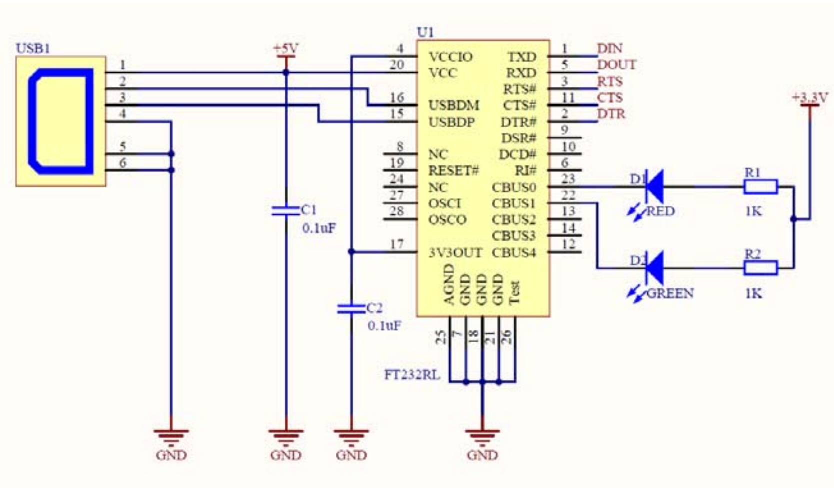


Figure 4.7– Pin configuration and schematic diagram of USB Dongle

The connection between the XBee® module and the FT232RL chip required 5 pins to be connected together. These are given in Table 4.1.

Table 4.1 – Shows the Pin Connections for the XBee® transceiver module on the USB dongle

FT232 RL Pin No	***XBee® Pin No***	***Name***	***Description***
1	3	DIN	Transmit Asynchronous data output
2	9	DTR	Data terminal ready control output
3	16	RTS	Request to send control output
5	2	DOUT	Receiving asynchronous data input
11	12	CTS	Clear to send control input

The XBee® transceiver module circuit diagram and pin configuration was different to the WsEMG electrode node and is shown in Figure 4.8.

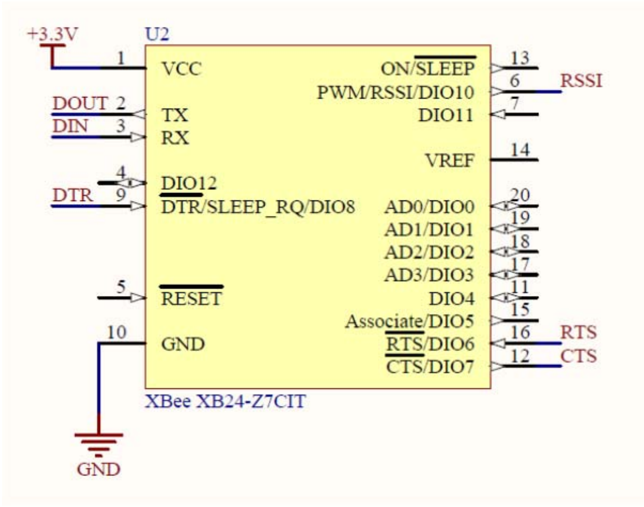


Figure 4.8 – Pin configuration and schematic diagram of XBee® module on USB dongle of the WsEMG computer interface node

The supply voltage for the USB dongle PCB was +5 V. The same voltage regulator MIC5209 was used to manage the 3.3 V to the XBee® transceiver on this node but with different components, see Figure 4.9.

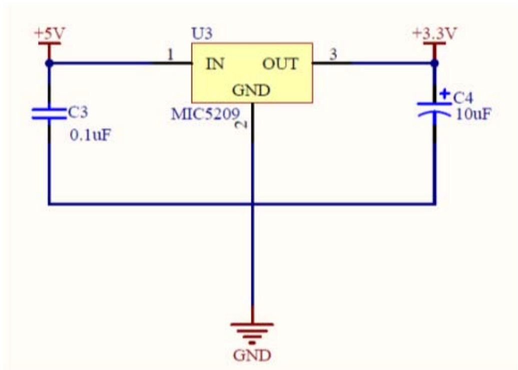


Figure 4.9 – Circuit configuration of MIC5209 voltage regulator for WsEMG computer interface node

Figure 4.10 shows the XBee® transceiver module and the new PCB board with the FT232RL chip and voltage before final assembly.

Figure 4.10 – The final PCB with XBee® module been attach on.

Figure 4.11 shows the new WsEMG computer interface node attached to a USB port of the laptop computer.

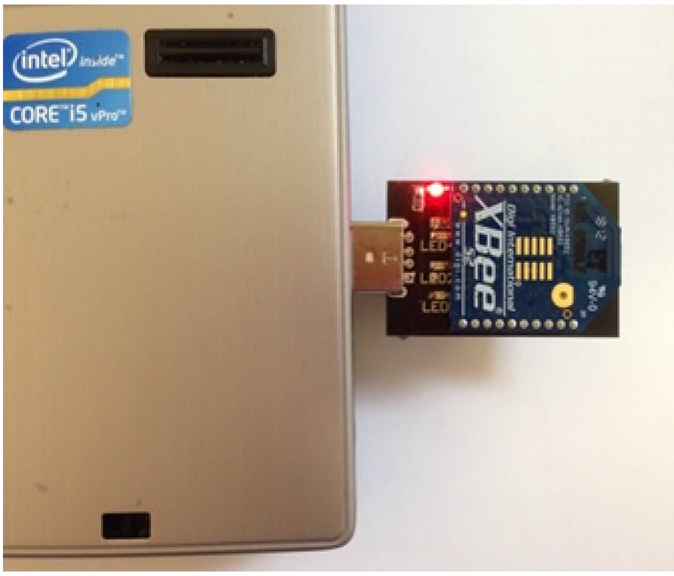


Figure 4.11 – The new WsEMG computer interface node attached to the laptop computer

4.3 Lithium-ion Polymer Battery Charger

The rechargeable lithium-ion polymer battery used for the WSEMG electrode interface node required a new board to be designed and manufactured so the battery could be recharged using the laptop computer USB port. The overall circuit diagram is shown in Appendix I. The circuit schematic for the charging of the LTC4053-4.2 chip used is shown in Figure 4.12. The three light emitting diodes (LEDs) in the circuit indicated the different states of the charger. At D3 the green LED indicated whether the Vcc had been supplied to the circuit or not. Table 4.2 shows LEDs D1 and D2 which indicated the different states whilst the battery was charging.

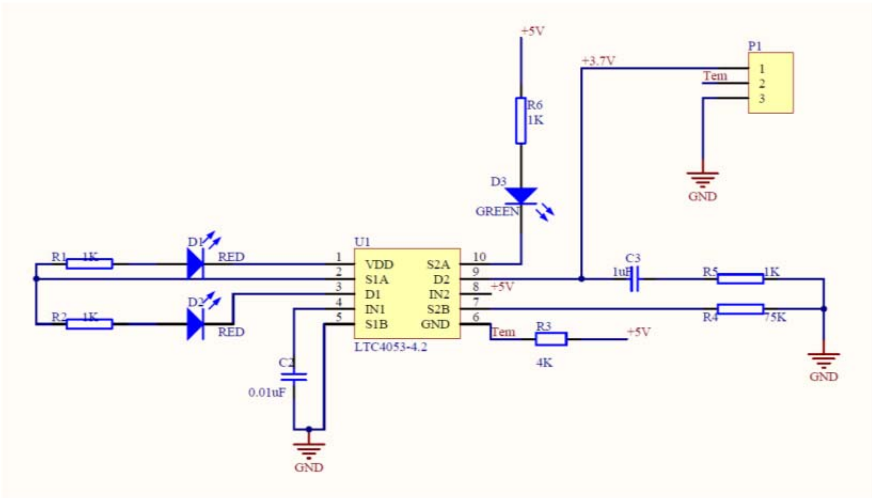


Figure 4.12 – Circuit schematic of battery charger

Table 4.2 – Different states of the Lithium-ion Polymer battery charger

LED D1	***LED D2***	***Description***
ON	OFF	Charge cycle has started
ON	ON	Error battery not at the right temperature condition
OFF	OFF	Normal timeout charging has been terminated
OFF	ON	Error battery has a bad cell which cannot be charged

The final layout of the new PCB for the battery charger for the lithium-ion polymer battery is shown in Figure 4.13.

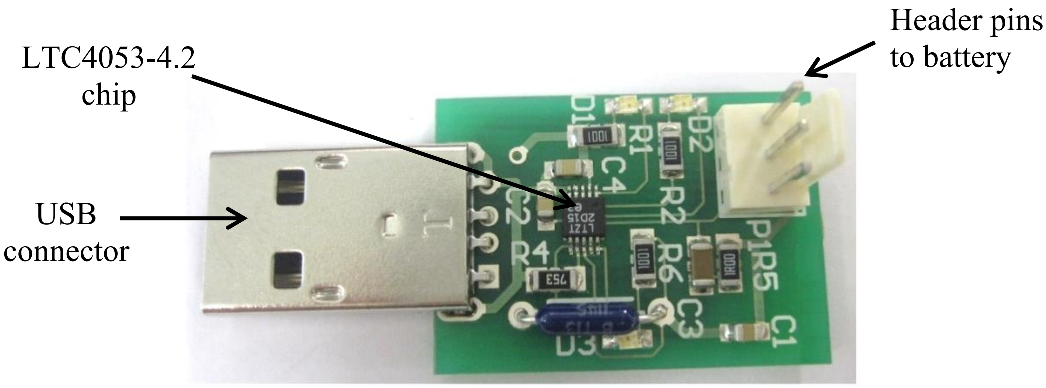


Figure 4.13 – The new Lithium-ion Polymer battery charger

4.4 XBee® Wireless Link Configuration

This research used the XBee® series 2 transceiver module with a build in antenna version as shown in Figure 4.14.

Figure 4.14 – XBee® Series 2 transceiver with build in antenna

XBee® transceiver modules came with default factory settings, which can be modified to improve the security of the data being transmitted. To configure the XBee® modules the USB dongle described in section 3.3.2 was used to configure both modules separately.

Digi International had customised software to interact with the firmware files found on Digi's wireless products, which had a simple graphical user interface which is called X-CTU. The X-CTU software only needed changes in three different areas, these were:

1. DL (Destination Address Low): was reset/to read the lower 32 bits of the 64 bit destination address. The DH register was set to zero. The DL was less

than 0xFFFF for transmitting using a 16 bit address 0x000000000000FFFF was the broadcast address for the PAN.

2. MY (16-bit Source Address): was set/to read the 16-bit source address for the modem. The MY = 0xFFFF was set to disable the reception of packets with 16-bit addresses. The 64-bit source address was the serial number and was always enabled.
3. BD (Interface Data Rate): was set/to read the serial interface baud rate for communication between the modem serial port and the host. The request for non-standard baud rates with values above 0x80 was used for the terminal window. The BD register had to be read to find the actual baud rate achieved.

Setting for both XBee® series 1 and 2 modules are shown below in Table 4.3.

Table 4.3 – Setting made in X-CTU software for XBee® Series 1 and 2

Setting	***XBee® Series 1***	***XBee® Series 2***
DL (Destination Address Low)	80	81
MY (16-bit Source Address)	81	80
BD (Interface Data Rate)	7 – 115200	7 – 115200

Figure 4.15 shows the screen shots of the setting made in X-CTU for both XBee® modules.

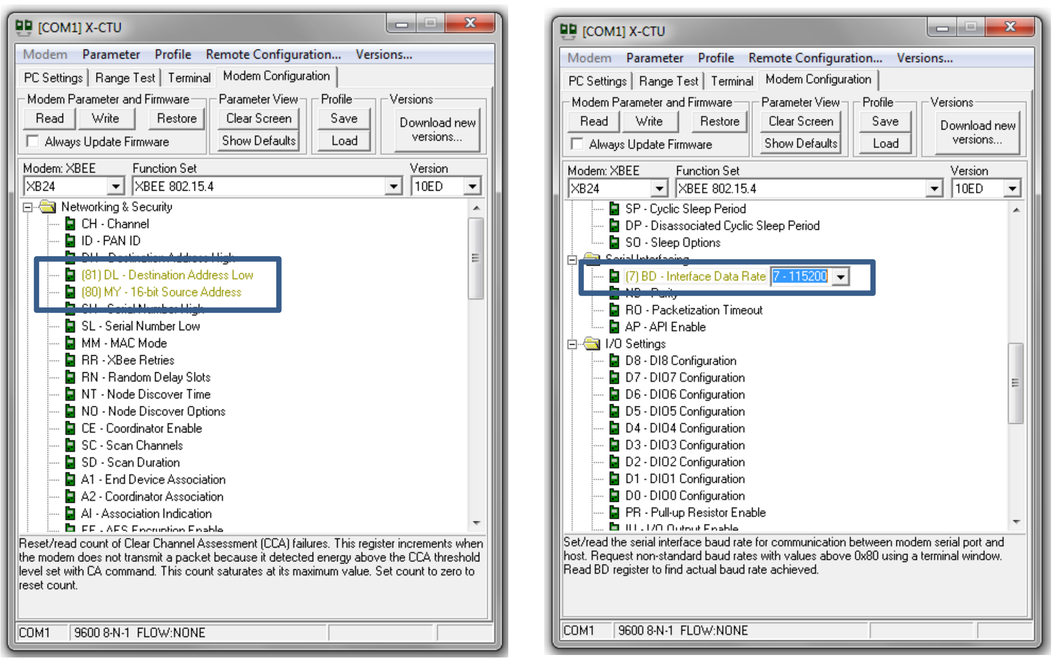


Figure 4.15 – Setting for the XBee® Series 2 modules

To test whether the two XBee® transceivers were communicating with each, two USB dongles were required with the modules configured. Two X-CTU windows were required to open separately and by typing a statement into one window it would appear in the other window. The other test used to show a certain message was sent by checking the response from the other module to show it had been received. These two tests indicated that the two modules were communicating with each other. This can be seen in Figure 4.16.

Figure 4.16 – The X-CTU window for one XBee® module sending a message (blue) with a response from the second XBee® module message (red)

4.5 Overall Setup of WsEMG Electrodes

Figure 4.17 shows the electrode interface and computer interface nodes with the surface electrodes connected to a laptop computer ready for the data collection of the sEMG signals from the subject's vastus lateralis muscle.

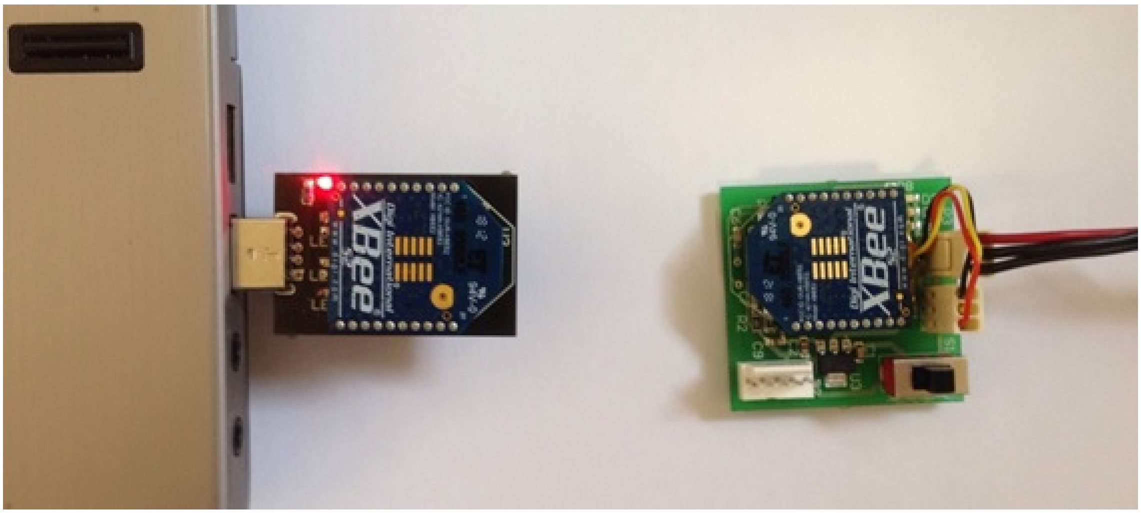


Figure 4.17 – Overall setup of WsEMG system

This chapter has presented the detailed circuitry and the new printed circuits boards for the two nodes that made up the WsEMG system and the battery charger.

The next chapter will present the necessary software that was required to connect the wireless system to the computer in order to collect and store the signals on the designated laptop.

Chapter 5
Graphical User Interface for WsEMG Data Recording

This chapter will discuss the data acquisition of the sEMG signals from the new Wireless Surface (WsEMG) electrode system developed for this research.

This research used LabVIEW software provided by National Instruments to collect the sEMG signals and analysed them. LabVIEW provided a graphical user interface programming code environment, which could be easily configured. There were a large number of functions available for data acquisition, signal conditioning and analysis in this software so it was invaluable for use in this system design.

The WsEMG computer interface node connected to the USB port of the laptop computer FT232RL chip used recognised a serial COM port. This serial COM port needed a software driver interface to connect to the LabVIEW and is called a Virtual Instrument Software Architecture (VISA) and was provided by National instruments. VISA is a standard for configuring, programming, and troubleshooting instrumentation systems comprising GPIB, VXI, PXI, Serial, Ethernet, and/or USB interfaces. Once the driver was installed the LabVIEW could connect to the XBee® transceiver module on the USB dongle.

LabVIEW programs are called 'Virtual Instruments (VI)' because their appearance and operation imitate physical instruments such as the waveform graph that was needed and used in this research. LabVIEW had a comprehensive set of tools for acquiring, analysing and storing data for the sEMG signals being collected. LabVIEW has two parts; its user interface called the Front Panel with the controls and indicators and the second the Block Diagram where the code is written graphically for the VI to work to analyse the data.

5.1 Main VI

The front panel and the block diagram of the VI for data acquisition for the sEMG system for collecting signals from the vastus lateralis muscle of the subject are shown in Figure 5.1. An enlarged copy of the block diagram is found in Appendix J.

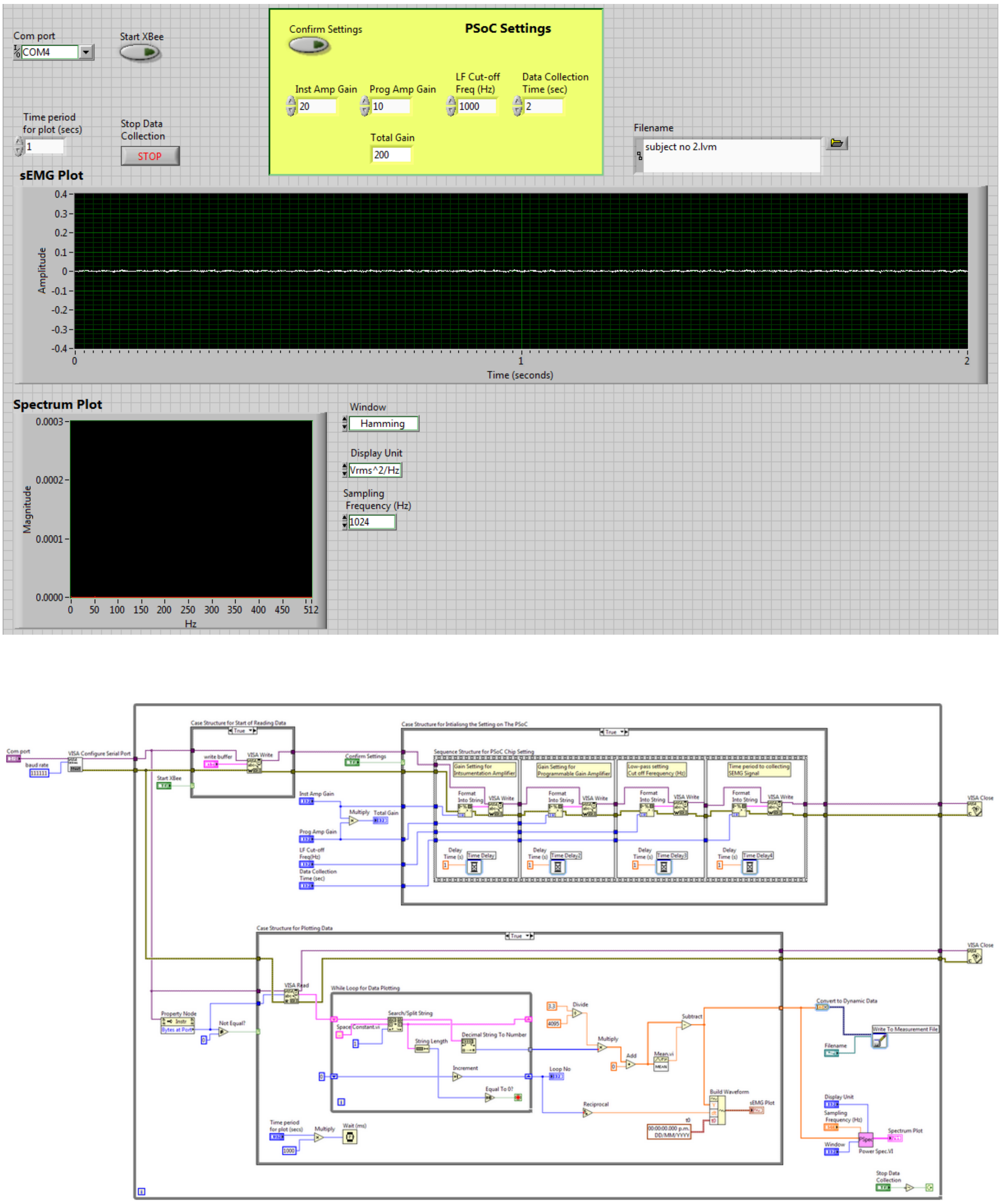


Figure 5.1 – Front Panel (top) and Block Diagram (bottom) of the LabVIEW VI used for data acquisition of sEMG signals.

The VI discussions in this chapter have been split into four sections as follows:

Section 5.2 The Initialisation of the VISA

Section 5.3 The Initial Settings of the PSoC®

Section 5.4 The Plotting of the sEMG signal

Section 5.5 The Power Spectrum of the sEMG signal

5.2 Initialisation of the VISA

To allow the XBee® modules on the dongle and main boards of the system to start sending data, the VISA configuration serial port function node had to be set. The two settings required were:

1. The setting of the *com port* from the USB dongle for the communications. This was done on the front panel of the VI.
2. The *baud rate* for XBee® module to communicate with the PSoC® chip.

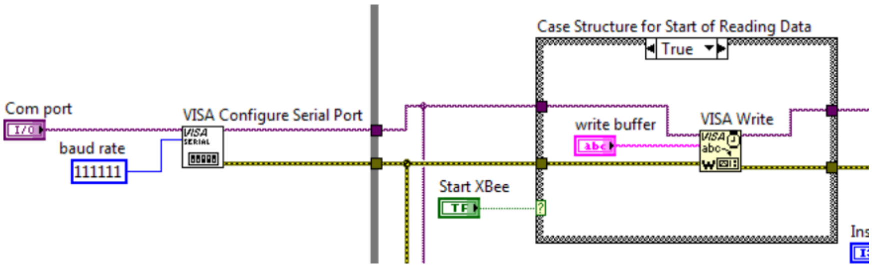


Figure 5.2 – Section of the VI block diagram for configuring the VISA function node of the main LabVIEW VI

Once the *com port* and *baud rate* had been set, the XBee® start control button on the front panel could be pressed to start the XBee® modules to communicate with the laptop computer.

5.3 Initial Settings of the PSoC®

The front panel instrumentation allowed different setting to be chosen for the parameters of the PSoC® chip. This is shown on Figure 5.3, these are:

1. The Instrumentation Amplifier gain
2. The Programmable Gain Amplifier
3. The Low-pass filter cut-off frequency
4. The Time setting of the PSoC® for collecting the data

These setting were made on the front panel of the VI and once the Confirm Settings control had been pressed each of the above setting were sent in sequence to the PSoC® chip to be set before the data was transferred to the laptop computer.

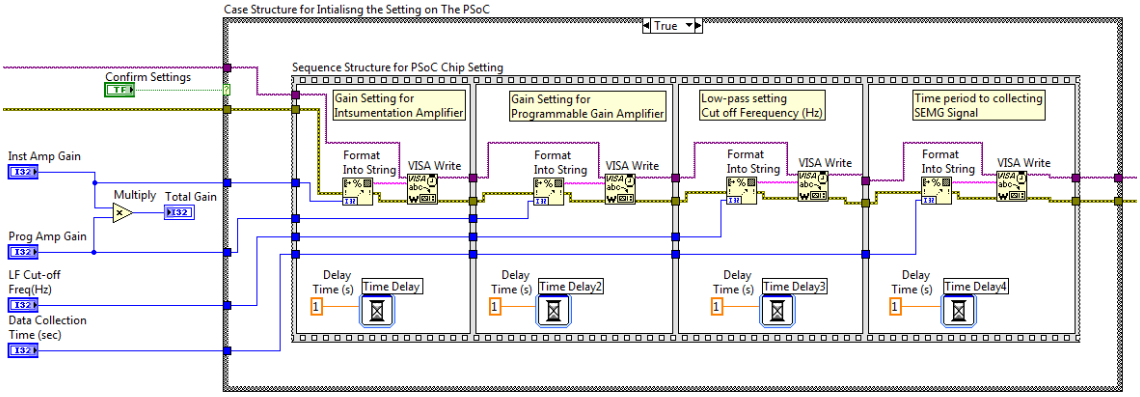


Figure 5.3 – Section of the VI block diagram for configuring the amplifiers, low-pas filter and time period on PSoC®

5.4 Plotting of the sEMG signal

Once the PSoC® transmitted the data via the XBee® transceiver modules it did so continuously. To display this on the front panel of the main VI the data had to be split into segments. The technique used to achieve this is shown in Figure 5.4.

The data from the VISA read function node on the block diagram was fed into the while loop to split the data stream into values which could then be plotted. This was done by identifying the spaces which separated the data into individual values ready for plotting.

The values that passed to the laptop computer were digital binary values that represent the amplified voltages which needed to be converted to plus or minus values which are shown inside the dotted box on Figure 5.3. The PSoC® Delta Sigma ADC was 12-bit, so the bit resolution is approximately 0.8 mV. These values were then plotted and displayed on a graph on the front panel and also passed to the Power Spectrum VI.

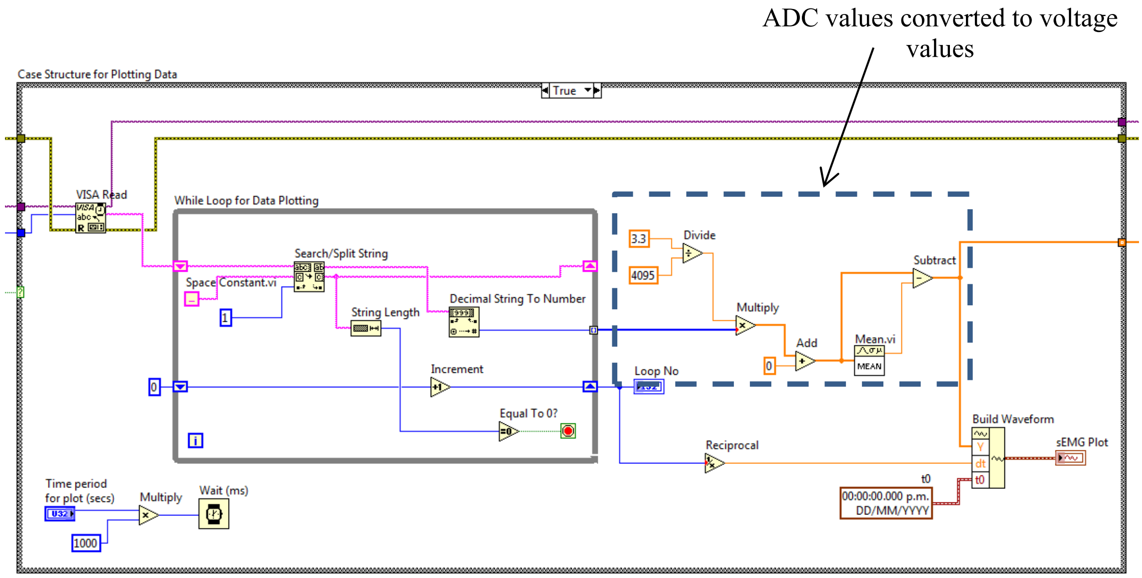


Figure 5.4 – Section of the VI block plotting the sEMG data

5.5 Power Spectrum of the sEMG signal

The Power Spectrum sub VI shown in Figure 5.5 takes the sEMG signal and performed a Fast Fourier Transform (FFT) to produce the Power Spectrum plot on the front panel of the main VI. The power spectrum was used to allow further analysis of the sEMG signals, and was not part of this research. This could show the power spectral changes of the sEMG signals under certain test conditions.

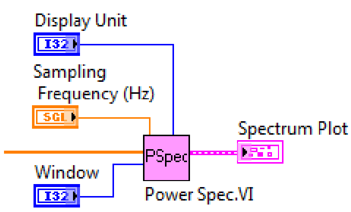


Figure 5.5 – Power Spectrum sub VI for analysis purposes of the sEMG signal

This chapter has presented the LabVIEW VI software that was developed for the data collection of sEMG signals for the new WsEMG electrode system developed for this research. The protocol for the collection of the sEMG signals plus a set of results taken a from the subject's vastus lateralis muscle using the new WsEMG electrodes will be presented in the next chapter.

Chapter 6
Testing Procedures and Results

This chapter will describe the testing protocol that was approved by the Auckland University of Technology (AUT) Ethics Committee. These are detailed in Appendix K. A single set of results was collected using the newly designed WsEMG electrodes with the newly VI developed using the LabVIEW software.

6.1 Testing Protocol

The following steps were taken in collecting the sEMG signals from the subjects who had volunteered to be part of this research.

6.1.1 Procedure

When potential participants made contact with the researcher they were screened using inclusion and exclusion criteria, this is detail in Appendix K. If the subject was deemed to be suitable to participate in the study, they received a verbal explanation of what would be involved. Prior to assessment, procedures were explained to the participant and time was given for each participant to have any remaining questions answered before their individual written consent was obtained.

6.1.2 Maximal Strength Test

Participants were expected to perform a five-minute generalised warm up that would include riding an exer-cycle at a self-selected pace and performing a range of motion exercises for the lower limbs.

After the general warm-up was completed, the participants were seated in the upright chair of the HUMAC®/NORM™ Testing and Rehabilitation System (Computer Sports Medicine, Inc) with the selected knee bent to 80 degrees and attached to a load cell that measured the voluntary isometric force of the quadriceps.

The upper body and upper thigh of the subject was securely strapped to the chair and the leg was also strapped to the load cell at mid-shin level, as shown in Figure 6.1. The subject was then asked to perform a specific warm-up and was familiarised with a series of four sets of short (5 seconds) sub-maximal isometric knee extensions. The intensity of the contractions was gradually increased against the resistance of the load cell and within the subject's own limits.

A one-minute rest followed each set of warm-up contractions. The subject was then rested for three minutes before the maximal voluntary isometric force (MVIF) of the quadriceps was measured. Three MVIF's were measured and recorded for a five-second period. There was then a two-minute rest period between each MVIF test and the highest MVIF was then selected for analysis.

Standardised verbal encouragement was given throughout the test from the force-to-failure point.

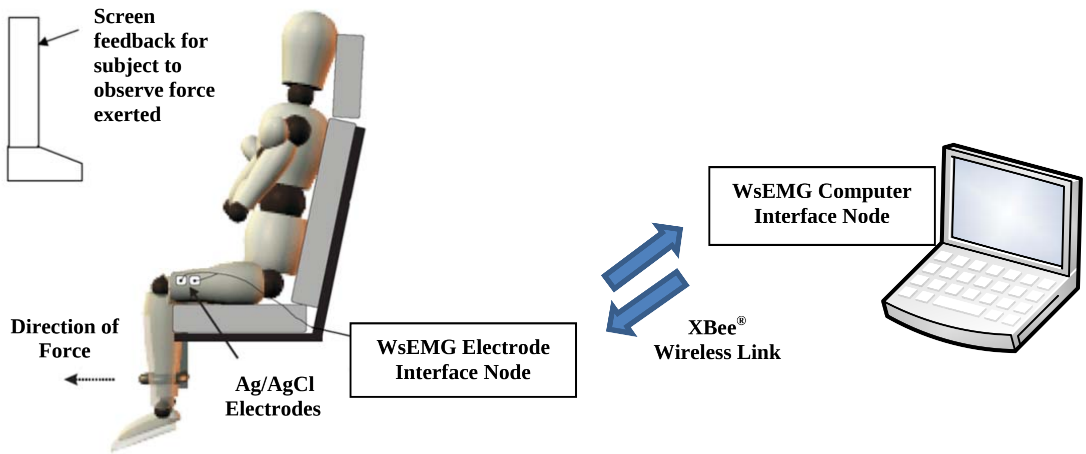


Figure 6.1 – Schematic diagram showing the equipment setup for data acquisition of sEMG signals.

6.1.3 Isometric Contraction Knee Extension Test

The subjects were rested for a further period of 20 minutes following the maximal strength test, before the subjects were again asked to maintain a sub-maximal contraction at 50% MVIF for a ten-second period. Subjects were also instructed prior to and during the tests to endure the contraction s required using standardised verbal encouragement.

6.1.4 Electromyography (EMG) Measures:

Muscle activity was recorded using the new WsEMG electrode system designed for this research. Following appropriate skin preparation (the skin was shaved, then gently abraded and cleaned with alcohol), the surface Ag/AgCl surface electrodes were then place on the skin surface overlying the vastus lateralis muscle of the thigh using standardised procedures.

6.2 Results

The new WsEMG was tested on five healthy volunteers with no previous history of knee or severe musculoskeletal injuries (five males, aged between 18-35 years) participated in this study.

Figure 6.2 shows placement of both the Ag/AgCl electrodes on the vastus lateralis muscle of the subjects and the reference electrode as per recommendations published by the Surface Electromyography for Non-invasive Assessment of Muscle[35].

Figure 6.2 – Placement of Electrodes on Subjects Leg

Figure 6.3 shows the Electrode Interface Node attached the surface electrodes on the subjects prior to testing.

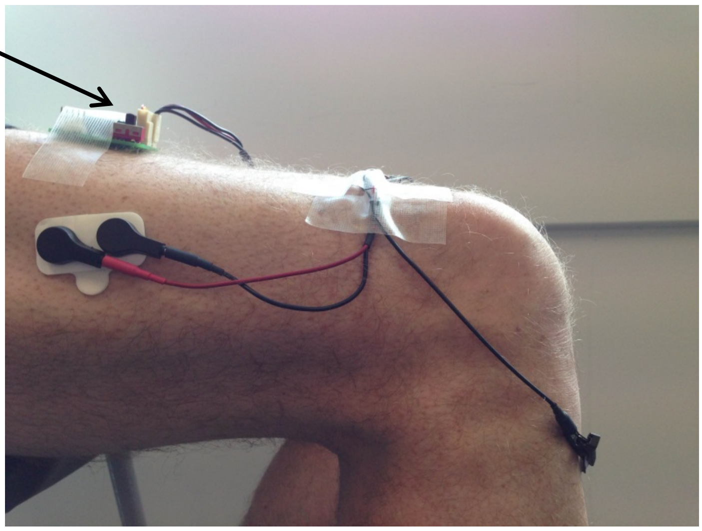


Figure 6.3 – Placement of Electrodes on Subjects Leg

Figure 6.4 shows a one second period of sEMG signal collected from Subject No. 2 vastus lateralis muscle performing 50% Maximum Voluntary Isometric Force (MVIF) contraction as per the testing protocol approved by the AUT Ethics Committee.

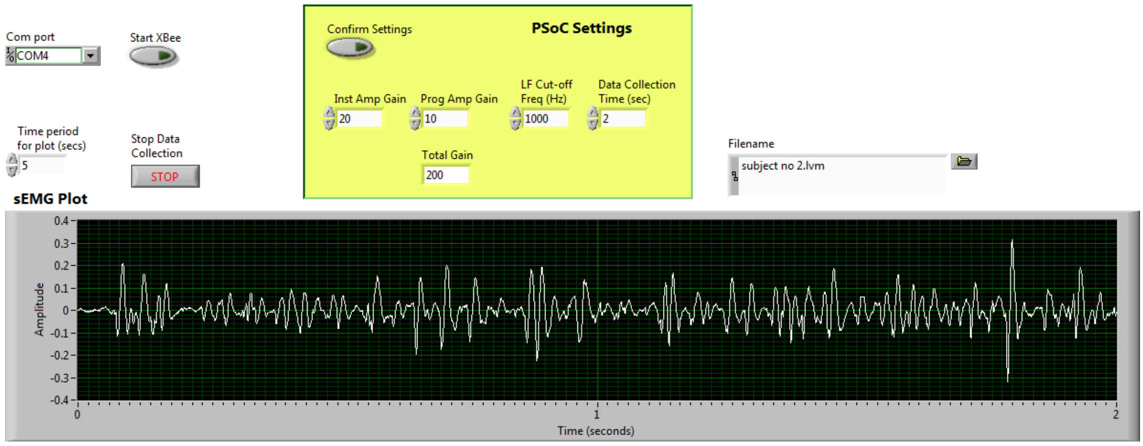


Figure 6.4 – sEMG signal at 50% MVIF from Subject No.2

Figure 6.5 shows the corresponding Power Spectrum plot for the sEMG signal shown in Figure 6.4

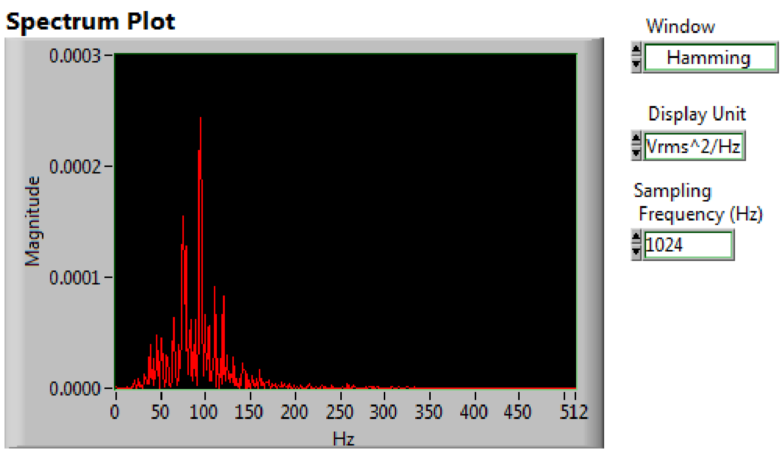


Figure 6.5 – Power Spectrum for sEMG shown in Figure 6.4

The outcome of this research showed that the new developed WsEMG electrode system using the PSoC® chip using XBee® series 2 transceivers modules with a new VI developed using LabVIEW code produce acceptable results in terms of the data collection of sEMG signals.

Chapter 7
Conclusion and Future Work

This research was designed to show the potential in building a new light and compact wireless electrode system for data acquisition of sEMG signals. The prototype system consisted of two parts (a) the electrode interface node and (b) the computer interface node. The XBee® series 2 transceiver modules were used for the wireless link between the two nodes.

The data acquisition and storage of the data on a laptop computer was achieved by developing a new virtual instrument using LabVIEW software. By using the PSoC® chip with LabVIEW it was possible to reconfigure a number of settings such as the overall gain and low-pass cut off frequency by using software without having to physically change the hardware components which made the system more flexible and easier to use.

The overall system acquired sEMG signals sampled at a sampling frequency of 1048 Hz with an overall gain of 200. The signals collected using human subjects after gaining the AUT Ethics Committee's approval gave acceptable results compared to wired electrodes in terms of signal quality. This research has shown that using the new WsEMG electrodes would enhance the ability of the clinician to collect sEMG signals without the need to put patients or subjects under unrealistic test conditions.

Future work is required to solve a number of issues, these are:

1. The present configuration of the XBee® transceiver modules had been configured using a point to point network. As the modules were series 2 which supports mesh networking, future work is required to understand how this would be implemented using more than one node on a muscle site or testing different muscles at the same time.

2. The prototype device at present requires both nodes to be handled with care. It requires some skill to place one on the subject's skin and the other on the USB interface. So new enclosures will be required to be designed. This will require greater consideration of the PCB layout and connectors.

3. The rechargeable battery needs to be removed from the electrode interface node when it needs to be recharged using an external battery charger. It would be more suitable to have the charger become part of the interface node board. This would then need a new circuit and PCB board to manage the battery charger circuit. This could still be on the same board as the PSoC® chip with the XBee® modules. This would still require this board to be light and compact.

Appendix A:

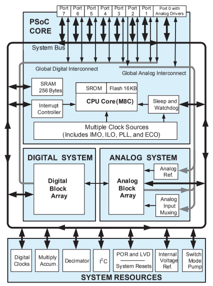
Datasheet for PSoC® CY8C29466-24PVXA Chip

Automotive PSoC® Programmable System-on-Chip™

Features

- Automotive Electronics Council (AEC) Q100 qualified
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - Two 8 × 8 multiply, 32-bit accumulate
  - Low power at high speed
  - Operating voltage: 3.0 V to 5.25 V
  - Automotive temperature range: –40 °C to +85 °C
- Advanced peripherals (PSoC® blocks)
  - 12 rail-to-rail analog PSoC blocks provide:
    - Up to 14-bit analog-to-digital converters (ADCs)
    - Up to 9-bit digital-to-analog converters (DACs)
    - Programmable gain amplifiers (PGAs)
    - Programmable filters and comparators
  - 16 digital PSoC blocks provide:
    - 8- to 32-bit timers, counters, and pulse width modulators (PWMs)
    - Cyclic redundancy check (CRC) and pseudo-random sequence (PRS) modules
    - Full- or half-duplex UART
    - SPI master or slave
    - Connectable to all general purpose I/O (GPIO) pins
  - Complex peripherals by combining blocks
- Precision, programmable clocking
  - Internal ±5% 24- and 48-MHz oscillator
  - High accuracy 24 MHz with optional 32.768 kHz crystal and phase-locked loop (PLL)
  - Optional external oscillator, up to 24 MHz
  - Internal low-speed, low-power oscillator for watchdog and sleep functionality
- Flexible on-chip memory
  - 32 KB flash program storage, 1000 erase/write cycles
  - 2 KB SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Programmable pin configurations
  - 25 mA sink, 10 mA drive on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open drain drive modes on all GPIOs
  - Up to 12 analog inputs on GPIOs[1]
  - Four 30 mA analog outputs on GPIOs
  - Configurable interrupt on all GPIOs
- Additional system resources
  - Inter-Integrated Circuit (I^2C™) slave, master, or multimaster operation up to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory

Logic Block Diagram



Note
1. There are eight standard analog inputs on the GPIO. The other four analog inputs connect from the GPIO directly to specific switched-capacitor block inputs. See the *PSoC Technical Reference Manual* for more details

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Contents

PSoC Functional Overview

The PSoC programmable system-on-chip family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in the Logic Block Diagram on page 1, is comprised of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global buses allow all the device resources to be combined into a complete custom system. The automotive PSoC CY8C29x66 family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included sleep timer and watchdog timer (WDT).

Memory includes 32 KB of flash for program storage and 2 KB of SRAM for data storage. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software intellectual property (IP) protection.

The PSoC device incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to ±5% over temperature and voltage. A low power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the 32.768-kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24-MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital resources, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt.

The Digital System

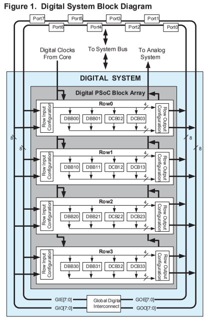
The digital system is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include those listed here.

- PWMs (8- to 32-bit)
- PWMs with deadband (8- to 24-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- Full- or half-duplex 8-bit UART with selectable parity
- SPI master and slave
- I^2C master, slave, or multimaster (implemented in a dedicated I^2C block)
- Cyclic redundancy checker/generator (16-bit)
- Infrared Data Association (IrDA)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Figure 1. Digital System Block Diagram



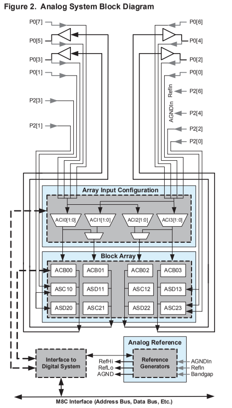
The Analog System

The analog system is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are as follows:

- ADCs (up to four, with 6- to 14-bit resolution, selectable as incremental, delta-sigma, or successive approximation register (SAR))
- Filters (two- and four-pole band pass, low pass, and notch)
- Amplifiers (up to four, with selectable gain up to 48x)
- Instrumentation amplifiers (up to two, with selectable gain up to 93x)
- Comparators (up to four, with 16 selectable thresholds)
- DACs (up to four, with 6- to 9-bit resolution)
- Multiplying DACs (up to four, with 6- to 9-bit resolution)
- High current output drivers (four with 30-mA drive)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, LVD, and power-on reset (POR). Brief statements describing the merits of each system resource are given below:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multiplier with 32-bit accumulate to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- The I^2C module provides 0 to 400 kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45[2]	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K
CY8C21x45[2]	up to 24	1	4	up to 24	0	4	6[3]	512	8 K
CY8C21x34[2]	up to 28	1	4	up to 28	0	2	4[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K
CY8C20x34[2]	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

The automotive CY8C29x66 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of digital I/O. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

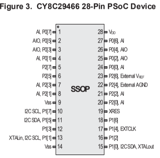
28-Pin Part Pinout

Table 2. 28-Pin Part Pinout (SSOP)

Pin No.	Type: Digital	Type: Analog	Pin Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection
10	I/O		P1[7]	I2C serial clock (SCL)
11	I/O		P1[5]	I2C serial data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal input (XTALin), I2C serial clock (SCL), ISSP-SCLK[5]
14	Power		V_{SS}	Ground connection
15	I/O		P1[0]	Crystal output (XTALout), I2C serial data (SDA), ISSP-SDATA[5]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional external clock (EXTCLK) input.
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External analog ground (AGND)
23	I/O		P2[6]	External voltage reference (V_{REF})
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I/O	P0[2]	Analog column mux input and column output
26	I/O	I/O	P0[4]	Analog column mux input and column output
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C29466 28-Pin PSoC Device



Note
5. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

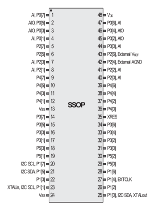
48-Pin Part Pinout

Table 3. 48-Pin Part Pinout (SSOP)

Pin No.	Type: Digital	Type: Analog	Pin Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	I/O		P4[7]	
10	I/O		P4[5]	
11	I/O		P4[3]	
12	I/O		P4[1]	
13	Power		V_{SS}	Ground connection
14	I/O		P3[7]	
15	I/O		P3[5]	
16	I/O		P3[3]	
17	I/O		P3[1]	
18	I/O		P5[3]	
19	I/O		P5[1]	
20	I/O		P1[7]	I2C serial clock (SCL)
21	I/O		P1[5]	I2C serial data (SDA)
22	I/O		P1[3]	
23	I/O		P1[1]	Crystal input (XTALin), I2C serial clock (SCL), ISSP-SCLK[6]
24	Power		V_{SS}	Ground connection
25	I/O		P1[0]	Crystal output (XTALout), I2C Serial Data (SDA), ISSP-SDATA[6]
26	I/O		P1[2]	
27	I/O		P1[4]	Optional external clock (EXTCLK) input
28	I/O		P1[6]	
29	I/O		P5[0]	
30	I/O		P5[2]	
31	I/O		P3[0]	
32	I/O		P3[2]	
33	I/O		P3[4]	
34	I/O		P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O		P4[0]	
37	I/O		P4[2]	
38	I/O		P4[4]	
39	I/O		P4[6]	
40	I/O	I	P2[0]	Direct switched capacitor block input
41	I/O	I	P2[2]	Direct switched capacitor block input
42	I/O		P2[4]	External analog ground (AGND)
43	I/O		P2[6]	External voltage reference (V_{REF})
44	I/O	I	P0[0]	Analog column mux input
45	I/O	I/O	P0[2]	Analog column mux input and column output
46	I/O	I/O	P0[4]	Analog column mux input and column output
47	I/O	I	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C29666 48-Pin PSoC Device



Note
6. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

Registers

Register Conventions

This section lists the registers of the automotive CY8C29x66 PSoC device. For detailed register information, refer to the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to '1', the user is in bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
	19		DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A		DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B		DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C		DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D		DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E		DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F		DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18		DCB32FN	58	RW	ASD22CR0	98	RW		D8	
	19		DCB32IN	59	RW	ASD22CR1	99	RW		D9	
	1A		DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C		DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
	1D		DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E		DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C29x66 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by visiting http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 21 on page 30 for the electrical specifications of the internal main oscillator (IMO) using slow IMO (SLIMO) mode.

Figure 5. Voltage versus CPU Frequency

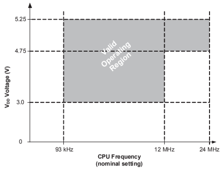
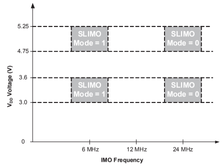


Figure 6. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 20 on page 29.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 41. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	See DC POR and LVD Specifications on page 28.
I_{DD}	Supply current	–	8	14	mA	Conditions are 5.25 V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are V_{DD} = 3.3 V, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode.	–	2	3	mA	Conditions are V_{DD} = 3.3 V, CPU = 3 MHz, 48 MHz disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active.	–	4	25	µA	Conditions are with internal low speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.
I_{SBXTL}	Sleep (mode) current with POR, LVD, sleep timer, WDT, ILO, and 32-kHz crystal oscillator active.	–	4	27	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C.
V_{REF}	Reference voltage (bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate V_{DD}.

DC General Purpose I/O Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin.
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High-level source current	10	–	–	mA	V_{OH} ≥ V_{DD} –1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low-level sink current	25	–	–	mA	V_{OL} ≤ 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25.

Table 10. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.

DC Operational Amplifier Specifications

Table 11 and Table 12 on page 18 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog CT PSoC blocks and the analog SC PSoC blocks. The guaranteed specifications are measured in the analog CT PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Power = high and Opamp bias = high settings are not allowed together for 3.3 V V_{DD} operation.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.6	10	mV	
TCV_{OSOA}	Average input offset voltage drift	–	4.0	23.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C.
V_{CMOA}	Common-mode voltage range All cases, except highest Power = high, Opamp bias = high	 0.0 0.5	 – –	 V_{DD} V_{DD} – 0.5	 V V	
$CMRR_{OA}$	Common-mode rejection ratio	60	–	–	dB	This specification is measured through the analog output buffer and therefore includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	67	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25)$ or $(V_{DD} - 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.4	10	mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	40.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C.
V_{CMOA}	Common-mode voltage range	0	–	V_{DD}	V	
$CMRR_{OA}$	Common-mode rejection ratio	60	–	–	dB	This specification is measured through the analog output buffer and therefore includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA –	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	54	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25)$ or $(V_{DD} - 1.25\ V) \le VIN \le V_{DD}$

DC Low-Power Comparator Specifications

Table 13 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 13. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

Table 14 and Table 15 on page 20 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value)	–	3.2	18	mV	
TCV_{OSOB}	Average input offset voltage drift	–	5.5	26.0	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 – –	 1 1	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (load = 32 Ω to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (load = 32 Ω to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 2 5	 mA mA	
$PSRR_{OB}$	Power supply rejection ratio	40	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Table 15. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low Power = high	 – –	 3.2 6.0	 20.0 25.0	 mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = low Power = high	 – –	 8.0 12.0	 32.0 41.0	 µV/°C µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 – –	 10 10	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (load = 1 kΩ to V_{DD}/2) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (load = 1 kΩ to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 1 5	 mA mA	
$PSRR_{OB}$	Power supply rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

DC Analog Reference Specifications

Table 16 and Table 17 on page 25 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog CT PSoC blocks. The power levels for AGND refer to the power of the analog CT PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog CT PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 16. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.228	V_{DD}/2 + 1.290	V_{DD}/2 + 1.352	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.078	V_{DD}/2 – 0.007	V_{DD}/2 + 0.063	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.336	V_{DD}/2 – 1.295	V_{DD}/2 – 1.250	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.224	V_{DD}/2 + 1.293	V_{DD}/2 + 1.356	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.056	V_{DD}/2 – 0.005	V_{DD}/2 + 0.043	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.338	V_{DD}/2 – 1.298	V_{DD}/2 – 1.255	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.226	V_{DD}/2 + 1.293	V_{DD}/2 + 1.356	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.057	V_{DD}/2 – 0.006	V_{DD}/2 + 0.044	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.337	V_{DD}/2 – 1.298	V_{DD}/2 – 1.256	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}/2 + Bandgap	V_{DD}/2 + 1.226	V_{DD}/2 + 1.294	V_{DD}/2 + 1.359	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.047	V_{DD}/2 – 0.004	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{DD}/2 – Bandgap	V_{DD}/2 – 1.338	V_{DD}/2 – 1.299	V_{DD}/2 – 1.258	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.085	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.055	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.077	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.032	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.009	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.061	V_{DD}/2 – 0.006	V_{DD}/2 + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.039	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.049	V_{DD}/2 – 0.005	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.054	V_{DD}/2 – 0.005	V_{DD}/2 + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.046	V_{DD}/2 – 0.004	V_{DD}/2 + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	2.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 + P2[6]	2.586 + P2[6]	2.657 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 + P2[6]	2.591 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 + P2[6]	2.592 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.594 + P2[6]	2.665 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

Table 17. 3.3-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}/2 + BandGap	V_{DD}/2 + 1.225	V_{DD}/2 + 1.292	V_{DD}/2 + 1.361	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.067	V_{DD}/2 – 0.002	V_{DD}/2 + 0.063	V
		V_{REFLO}	Ref Low	V_{DD}/2 – BandGap	V_{DD}/2 – 1.35	V_{DD}/2 – 1.293	V_{DD}/2 – 1.210	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}/2 + BandGap	V_{DD}/2 + 1.218	V_{DD}/2 + 1.294	V_{DD}/2 + 1.370	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.038	V_{DD}/2 – 0.001	V_{DD}/2 + 0.035	V
		V_{REFLO}	Ref Low	V_{DD}/2 – BandGap	V_{DD}/2 – 1.329	V_{DD}/2 – 1.296	V_{DD}/2 – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}/2 + BandGap	V_{DD}/2 + 1.221	V_{DD}/2 + 1.294	V_{DD}/2 + 1.366	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.050	V_{DD}/2 – 0.002	V_{DD}/2 + 0.046	V
		V_{REFLO}	Ref Low	V_{DD}/2 – BandGap	V_{DD}/2 – 1.331	V_{DD}/2 – 1.296	V_{DD}/2 – 1.260	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}/2 + BandGap	V_{DD}/2 + 1.226	V_{DD}/2 + 1.295	V_{DD}/2 + 1.365	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.028	V_{DD}/2 – 0.001	V_{DD}/2 + 0.025	V
		V_{REFLO}	Ref Low	V_{DD}/2 – BandGap	V_{DD}/2 – 1.329	V_{DD}/2 – 1.297	V_{DD}/2 – 1.262	V
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.06	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.05	V_{DD}/2 – 0.002	V_{DD}/2 + 0.040	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.009	Vss + 0.056	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.060	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.028	V_{DD}/2 – 0.001	V_{DD}/2 + 0.025	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.034	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.058	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.037	V_{DD}/2 – 0.002	V_{DD}/2 + 0.033	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.046	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.057	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.025	V_{DD}/2 – 0.001	V_{DD}/2 + 0.022	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.004	Vss + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + BandGap (P2[4] = V_{DD}/2)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap (P2[4] = V_{DD}/2)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + BandGap (P2[4] = V_{DD}/2)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap (P2[4] = V_{DD}/2)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + BandGap (P2[4] = V_{DD}/2)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap (P2[4] = V_{DD}/2)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + BandGap (P2[4] = V_{DD}/2)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – BandGap (P2[4] = V_{DD}/2)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V_{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V_{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF	

DC POR and LVD Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	–	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	–	V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[7]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[8]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
7. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
8. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	10	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[9, 10]	1,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[10, 11]	512,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	15	–	–	Years	

Notes
9. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
10. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
11. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	IMO frequency for 24 MHz	22.8[12]	24	25.2[12]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 14. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5[12]	6	6.5[12]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 14. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.089[12]	–	25.2[12]	MHz	4.75 V ≤ V_{DD} ≤ 5.25 V. SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.089[12]	–	12.6[12]	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V. SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V V_{DD} nominal)	0	–	50.4[12,13]	MHz	Refer to AC Digital Block Specifications on page 35.
F_{BLK33}	Digital PSoC block frequency (3.3 V V_{DD} nominal)	0	–	25.2[12,13]	MHz	Refer to AC Digital Block Specifications on page 35.
F_{32K1}	ILO frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{32K2}	ECO frequency	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	Refer to Figure 7 on page 31.
$t_{PLLSLEWLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	Refer to Figure 8 on page 31.
t_{OS}	ECO startup to 1%	–	250	500	ms	Refer to Figure 9 on page 31.
t_{OSACC}	ECO startup to 100 ppm	–	300	600	ms	The ECO frequency is within 100 ppm of its final value by the end of the t_{OSACC} period. Correct operation assumes a properly loaded 1-μW maximum drive level, 32.768-kHz crystal.
t_{XRST}	External reset pulse width	10	–	–	μs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	45.6 [12]	48.0	50.4 [12]	MHz	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.6[12]	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power up from 0 V.

Notes
12. Accuracy derived from IMO with appropriate trim for V_{DD} range.
13. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 21. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
t_{JIT_IMO}[14]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{JIT_PLL}[14]	PLL cycle-to-cycle jitter (RMS)	–	200	800	ps	
	PLL long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	PLL period jitter (RMS)	–	100	700	ps	

Figure 7. PLL Lock Timing Diagram

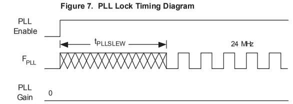


Figure 8. PLL Lock for Low Gain Setting Timing Diagram

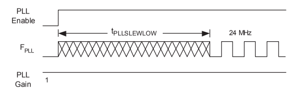
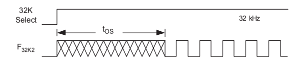


Figure 9. External Crystal Oscillator Startup Timing Diagram



Note
14. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

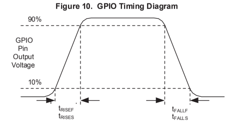
AC GPIO Specifications

Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6[15]	MHz	Normal strong mode
t_{RISEF}	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{FALLF}	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Figure 10. GPIO Timing Diagram



Note
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC Operational Amplifier Specifications

Table 23 and Table 24 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog CT PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 23. 5-V AC Operational Amplifier Specifications

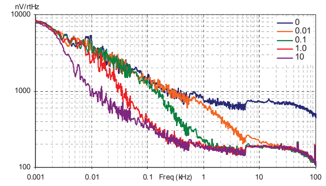
Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time to 0.1% for a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
t_{SOA}	Falling settling time to 0.1% for a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising slew rate (20% to 80%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling slew rate (80% to 20%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz	

Table 24. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time to 0.1% of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs	
t_{SOA}	Falling settling time to 0.1% of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs	
SR_{ROA}	Rising slew rate (20% to 80%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs	
SR_{FOA}	Falling slew rate (80% to 20%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs	
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz	

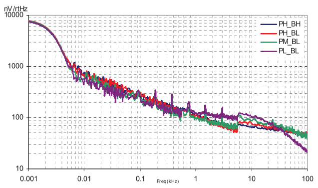
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 kΩ resistance and the external capacitor.

Figure 11. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 12. Typical Opamp Noise



AC Low-Power Comparator Specifications

Table 25 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 25. AC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

Table 26 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
	With capture	–	–	25.2[17]	MHz	
	Capture pulse width	50[16]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
	With enable input	–	–	25.2[17]	MHz	
	Enable input pulse width	50[16]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[16]	–	–	ns	
	Disable mode	50[16]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2[17]	MHz	
SPIM	Input clock frequency	–	–	8.4[17]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.2[17]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated between transmissions	50[16]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4[17]	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	

Notes

16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
17. Accuracy derived from IMO with appropriate trim for V_{DD} range.

Table 26. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4[18]	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2[18]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[18]	MHz	

AC Analog Output Buffer Specifications

Table 27 and Table 28 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1-V step, 100 pF load Power = low Power = high	 – –	 – –	 4 4	 µs µs	
t_{SOB}	Falling settling time to 0.1%, 1-V step, 100 pF load Power = low Power = high	 – –	 – –	 3.4 3.4	 µs µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1-V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1-V step, 100 pF load Power = low Power = high	 0.55 0.55	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz	

Table 28. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1-V step, 100 pF load Power = low Power = high	 – –	 – –	 4.7 4.7	 µs µs	
t_{SOB}	Falling settling time to 0.1%, 1-V step, 100 pF load Power = low Power = high	 – –	 – –	 4 4	 µs µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1-V step, 100 pF load Power = low Power = high	 0.36 0.36	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1-V step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz	

Note

18. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC External Clock Specifications

Table 29 and Table 30 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 29. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 30. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.093	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 31 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	40[19]	ms	
t_{WRITE}	Flash block write time	–	40	160[19]	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	V_{DD} > 3.6
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
t_{PRGH}	Total flash block program time (t_{ERASEB} + t_{WRITE}), hot	–	–	100[19]	ms	T_J ≥ 0 °C
t_{PRGC}	Total flash block program time (t_{ERASEB} + t_{WRITE}), cold	–	–	200[19]	ms	T_J < 0 °C

Note

19. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

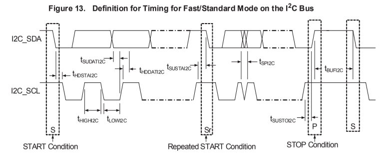
AC I^2C Specifications

Table 32 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 32. AC Characteristics of the I^2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100[20]	0	400[20]	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[21]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus-free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 13. Definition for Timing for Fast/Standard Mode on the I^2C Bus



Notes

20. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
21. A Fast-Mode I^2C-bus device can be used in a Standard-Mode I^2C-bus system, but the requirement $t_{SUDATI2C}$ ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SUDATI2C}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I^2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the automotive CY8C29x66 PSoC device, along with the thermal impedances and solder reflow for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 14. 28-Pin (210-Mil) SSOP

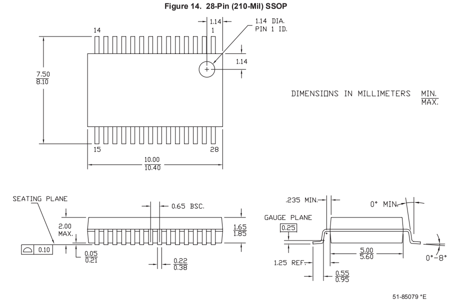
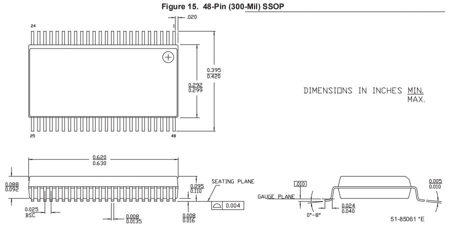


Figure 15. 48-Pin (300-Mil) SSOP



Thermal Impedances

Table 33. Thermal Impedances per Package

Package	Typical θ_{JA} [22]
28-pin SSOP	94 °C/W
48-pin SSOP	69 °C/W

Capacitance on Crystal Pins

Table 34. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF
48-pin SSOP	3.3 pF

Solder Reflow Specifications

Table 35 shows the solder reflow temperature limits that must not be exceeded.

Table 35. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SSOP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds

Note
22. $T_J = T_A + Power \times \theta_{JA}$.

Tape and Reel Information

Figure 16. 28-Pin SSOP Carrier Tape Drawing

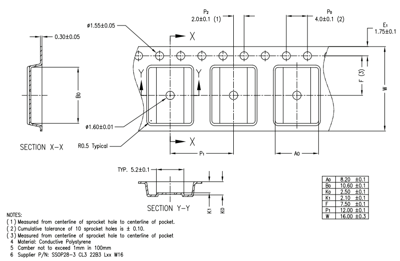


Figure 17. 48-Pin SSOP Carrier Tape Drawing

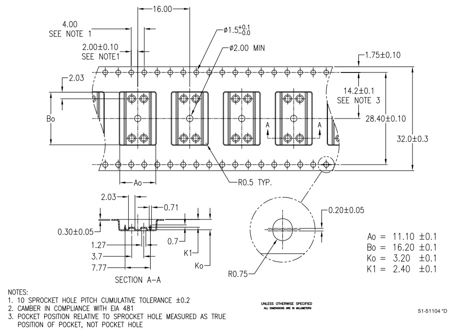


Table 36. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
28-Pin SSOP	13.3	7	42	25	1000
48-Pin SSOP	25.5	4	32	19	1000

Development Tool Selection

This section presents the development tools available for the CY8C29x66 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-pin PDIP emulation pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC device samples (two)
- PSoC Designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-pin CY8C29466-24PXI PDIP PSoC device sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-29X66 Evaluation Pod (EvalPod)

PSoC EvalPods are pods that connect to the ICE (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-29X66 provides evaluation of the CY8C29x66 PSoC device family.

Device Programmers

All device programmers can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 37. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[23]	Foot Kit[24]	Adapter[25]
CY8C29466-24PVXA	28-pin SSOP	CY3250-29XXX	CY3250-28SSOP-FK	AS-28-28-02SS-6ENP-GANG
CY8C29666-24PVXA	48-pin SSOP	CY3250-29XXX	CY3250-48SSOP-FK	AS-48-48-01SS-6-GANG

Notes
23. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
24. Foot kit includes surface mount feet that can be soldered to the target PCB.
25. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.

Ordering Information

The following table lists the automotive CY8C29x66 PSoC devices' key package features and ordering codes.

Table 38. CY8C29x66 Automotive PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	RAM (KB)	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (210-Mil) SSOP	CY8C29466-24PVXA	32	2	–40 °C to +85 °C	16	12	24	12[26]	4	Yes
28-pin (210-Mil) SSOP (tape and reel)	CY8C29466-24PVXAT	32	2	–40 °C to +85 °C	16	12	24	12[26]	4	Yes
48-pin (300-Mil) SSOP	CY8C29666-24PVXA	32	2	–40 °C to +85 °C	16	12	44	12[26]	4	Yes
48-pin (300-Mil) SSOP (tape and reel)	CY8C29666-24PVXAT	32	2	–40 °C to +85 °C	16	12	44	12[26]	4	Yes

Ordering Code Definitions

CY 8 C 29 xxx-SPxx

- Package type:
  - PX = PDIP Pb-free
  - SX = SOIC Pb-free
  - PVX = SSOP Pb-free
  - LFX/LTX = QFN Pb-free
  - AX = TQFP Pb-free
- Thermal Rating:
  - A = Automotive -40 °C to +85 °C
  - C = Commercial
  - E = Automotive Extended -40 °C to +125 °C
  - I = Industrial
- CPU speed: 24 MHz
- Part number
- Family code
- Technology code: C = CMOS
- Marketing code: 8 = PSoC
- Company ID: CY = Cypress

Note
26. There are eight standard analog inputs on the GPIO. The other four analog inputs connect from the GPIO directly to specific switched-capacitor block inputs. See the *PSoC Technical Reference Manual* for more details

Reference Information

Acronyms

The following table lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LVD	low-voltage detect
ADC	analog-to-digital converter	MAC	multiply accumulate
AEC	Automotive Electronics Council	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PDIP	plastic dual-in-line package
CRC	cyclic redundancy check	PGA	programmable gain amplifier
CT	continuous time	PLL	phase-locked loop
DAC	digital-to-analog converter	POR	power-on reset
DC	direct current	PPOR	precision POR
DTMF	dual-tone multi-frequency	PRS	pseudo-random sequence
ECO	external crystal oscillator	PSoC®	Programmable System-on-Chip
EEPROM	electrically erasable programmable read-only memory	PWM	pulse-width modulator
GPIO	general-purpose I/O	RTC	real time clock
I/O	input/output	SAR	successive approximation register
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
I^2C	inter-integrated circuit	SPI	serial peripheral interface
ILO	internal low-speed oscillator	SRAM	static random-access memory
IMO	internal main oscillator	SROM	supervisory read-only memory
IP	intellectual property	SSOP	shrink small-outline package
IrDA	infrared data association	UART	universal asynchronous receiver trans-mitter
ISSP	in-system serial programming	USB	universal serial bus
LCD	liquid crystal display	WDT	watchdog timer
LED	light-emitting diode	XRES	external reset
LPC	low power comparator		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Data Sheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Document Conventions

Units of Measure

The following table lists the units of measure that are used in this document.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibel	mVpp	millivolts peak-to-peak
°C	degree Celsius	nA	nanoampere
fF	femto-farad	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	ppm	parts per million
µA	microampere	%	percent
µs	microsecond	pF	picofarad
µV	microvolt	ps	picosecond
µW	microwatt	pA	pikoampere
mA	milliampere	rt-Hz	root hertz
mm	millimeter	V	volt
ms	millisecond	W	watt
mV	millivolt		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are in decimal format.

Glossary

active high
1. A logic signal having its asserted state as the logic 1 state.
2. A logic signal having the logic 1 state as the higher voltage of the two states.

analog blocks — The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.

analog-to-digital converter (ADC) — A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog converter (DAC) performs the reverse operation.

Application programming interface (API) — A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.

asynchronous — A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.

bandgap reference — A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.

bandwidth
1. The frequency range of a message or information processing system measured in hertz.
2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog converter (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital converter (ADC) performs the reverse operation.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at the V_{DD} supply voltage and pulled high with resistors. The bus operates up to100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the CPU receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitted data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power-on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied value.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a known state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-built, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level analog and digital PSoC blocks. User modules also provide high level *API (Application Programming Interface)* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain". The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
Document Title: CY8C29466, CY8C29666 Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-12899				
**	772096	HMT	See ECN	New silicon, new document (Revision **).
*A	2697720	VIVG/ PYRS	04/24/09	Updated template Content edits
*B	2769233	BTK	09/25/09	Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections for added clarity. Improved formatting of the register tables. Added clarifying comments to some electrical specifications. Changed T_{RAMP} specification per MASJ input. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Updated the Development Tool Selection section. Improved the bookmark structure. Edited F_{IMO6}, T_{ERASEB}, T_{WRITE}, T_{RSCLK}, T_{FSCLK}, V_{IHP}, V_{PPORxR}, and 5 V RefLo specifications according to MASJ input. Removed 'TM' from Programmable System-on-Chip in the title.
*C	2822792	BTK/ AESA	12/07/2009	Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the footnotes for the DC Programming Specifications table. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Added "Contents" on page 2.
*D	2888007	NJF	03/30/2010	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated Packaging Information. Updated Ordering Code Definitions. Removed Third Party Tools and Build a PSoC Emulator into your Board. Updated Development Kits and Evaluation Tools. Updated links in Sales, Solutions, and Legal Information.
*E	2987146	BTK	07/19/2010	Updated Pinouts section to add 48-pin package. Updated Packaging Information section to add 48-pin package. Updated Development Tool Selection section to add 48-pin package development tool information. Updated Ordering Information section to add new 48-pin package product. Moved Acronyms section to the end of the document. Added part number CY8C29666 to the title.
*F	3111512	BTK/NJF	07/25/2011	Updated I^2C timing diagram to improve clarity. Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarity. Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Updated PSoC Device Characteristics table. Updated the F_{32KU} electrical specification. Updated note for R_{PD} electrical specification. Updated note for the T_{STG} electrical specification to add more clarity. Added Tape and Reel Information section. Added C_L electrical specification. Updated Analog Reference specifications. Updated V_{OSOA}, TCV_{OSOA}, V_{OSOB}, and TCV_{OSOB} electrical specifications.
*G	3543452	KAUL	03/06/2012	Updated Tape and Reel Information under Packaging Information.

Sales, Solutions, and Legal Information

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Appendix B:

Datasheet for Lithium-ion Polymer Battery LP-402025-1S-3

File no.: 20120102
Edition: 1.0

Specification

of

Li-polymer Rechargeable Battery

Model No.: LP-402025-1S-3

Reported by: 陈声宇 Date: Jan,02,2012

Checked by: ______ Date：Jan,02,2012

Approved by: ______ Date: Jan,02,2012

1. Scope

This specification describes the definition, technical requirement, testing method, warning and caution of the Lithium ion polymer rechargeable battery. The specification only applies to DUBILIER'S Li-ion battery.

2. Product Model

Battery type: Rechargeable Lithium-ion Polymer Battery
Battery Model: LP-402025-1S-3

3. Ratings

3.1. Nominal Capacity[at 0.2C]: 155mAh (min); 165mAh (typical)
3.2. Nominal Voltage: 3.7V (average voltage at 0.2C discharge)
3.3. Charging Voltage: 4.20 ±0.05V
3.4. Max. Charging Current: 155mA
3.5. Charging Method: constant current constant voltage
Standard Charge: 78mA (constant current) charge to 4.20V, then 4.2V (constant voltage) for 3.5hr or 3mA(0.02C) cut off
Quick Charge: 155mA(constant current) charge to 4.20V, then 4.2V (constant voltage) for 3.0hr or 3mA (0.02C) cut off
3.6. Max. Continuous Discharge Current: 310mA
3.7. Discharge Cut-off Voltage: 2.75V
3.8. Battery Dimensions (Refer to the attached drawing)
Thickness: 3.8±0.3
(Measured with weighing 300gf at 25±2℃)
Width: 20±1
(Measured with weighing 300gf at 25±2℃)
Length: 26±1
3.9.Battery Weight: 4±0.2g
3.10. Operating Temperature
Discharge: -20℃ ～+60℃
Charging: 0℃ ～+45℃

Storage in a 50% charged state Temperature range	Duration	Typ. Capacity recovery
-20℃ - +80℃	10 days	50%(expected)
-20℃ - +60℃	1month	75%(expected)
-20℃ - +45℃	3months	70%(expected)
-20℃ - +25℃	1year	80%(expected)

4. Battery Performance

4.1. Visual Inspection
There shall be no such defects as remarkable scratches, cracks, leakage or deformations.
4.2. Test Condition
4.2.1.Standard Test Condition
Test new cells within one month after shipment from our factory and the cells shall not be cycled over five times before the tests.
All the tests in this specification shall be conducted in an ambient temperature of 25℃ ±5℃ under a humidity of 25% to 85%, unless otherwise specified.
4.2.2 Measuring Instrument or Apparatus
4.2.2.1. The dimension measurement shall be implemented by instruments with equal or more precision of 0.01mm.
4.2.2.2 Standard class specified in the national standard or more sensitive class having inner impedance more than 10kΩ/V.
4.2.2.3 Impedance shall be measured by a sinusoidal alternating current method (1kHz LCR meter).
4.2.2.4 The current measurement shall be implemented by instrument with equal to more precision scale of±0.1% and the constant voltage precision should be implemented with±0.5%, and the timing precision should be not below ±0.1%.
4.2.2.5 The temperature measurement shall be implemented by instrument with equal or more precision seal of ±0.5℃.
4.3 Electrical Characteristics
4.3.1 Standard Charge
The cell shall be charged at a constant current of 0.5C to 4.2V and then at constant voltage of 4.2V with a charging time of 3.5 hours or 0.02C cut off.
4.3.2 Rated Capacity (0.2C): 155mAh (minimum)
The capacity shall be measured at a discharge current of 0.2C and a cut-off voltage of 2.75V after the standard charge (Section 4.3.1.)
4.3.3 High Rate Discharge Capacity (1C): 85% (minimum) of Rated Capacity
The capacity shall be measured at a discharge current of 1C and a cut-off voltage of 2.75V after the standard charge (Section 4.3.1.)
4.3.4 Low Temperature Discharge Capacity (0℃): 80% (minimum) of Rated Capacity
The capacity shall be measured at a discharge current of 0.2C in an ambient temperature of 0℃±2℃ and a cut-off voltage of 2.75V after the standard charge (Section 4.3.1.)
4.3.5 Low Temperature Discharge Capacity (-10℃): 70% (minimum) of Rated Capacity
The capacity shall be measured at a discharge current of 0.2C in an ambient temperature of -10℃±2℃ and a cut-off voltage of 2.75V after the standard charge (Section 4.3.1.)
4.3.6 High Temperature Discharge Capacity (60℃): 100% (minimum) of Rated Capacity
The capacity shall be measured at a discharge current of 0.2C in an ambient temperature of 60℃±2℃ and a cut-off voltage of 2.75V after the standard charge (Section 4.3.1.)
4.3.7. Storage Characteristics (25℃)
Capacity Retention: 85% (minimum) of Rated Capacity
Capacity Recovery: 90% (minimum) of Rated Capacity
The capacity retention shall be measured at a discharge current of 0.2C and a cut-off voltage of 2.75V after standard charge (Section 4.3.1.) and being stored for 28 days at 25℃±5℃. Then, the capacity recovery shall be measured at a discharge current of 0.2C and a cut-off voltage of 2.75V after standard charge (Section 4.3.1.).
4.3.8. Storage Characteristics (45℃)
Capacity Retention: 60% (minimum) of Rated Capacity
Capacity Recovery: 70% (minimum) of Rated Capacity
The capacity retention shall be measured at a discharge current of 0.2C and a cut-off voltage of 2.75V after standard charge (Section 4.3.1.) and being stored for 28 days at 45℃±5℃. Then, the capacity recovery shall be measured at a discharge current Of 0.2C and a cut-off voltage of 2.75V after standard charge (Section 4.3.1.)
4.3.9 Internal Impedance: 255mΩ(type) ; 425mΩ(max)
The internal impedance shall be measured at a since wave alternative current process of 1kHz after the standard charge.
4.3.10. Cycle Life :
The cycle life shall be conducted as the following procedures：
Step 1: charge the cell with the standard charge (as of section 4.3.1);
Step 2: discharge the cell at 0.5C to 2.75V,
Step 3: repeat Step 1 and Step 2 for 500 times.
The capacity after 300 cycles is expected to be equal to or more than 80% of the rated capacity. The capacity after 500 cycles is expected to be equal to or more than 60% of the rated capacity.
4.3.11 Open Circuit Voltage: 3.6V ~ 4.1V as of shipment.
4.4 Mechanical Performance
4.4.1 Vibration Test: 95% (min) of Rated Capacity, No Leakage
After standard charge (Section 4.3.1.), the battery is vibrated with an amplitude of 0.8mm (1. 6mm total maximum excursion) for 60 minutes in three mutually perpendicular directions. The vibration is performed between 10Hz and 55Hz at a rate of 1Hz per minute After the completion of the vibration, the capacity shall be measured at a discharge current of 0.2C and a cut-off voltage of 2.75V
4.5 Environmental Performance
4.5.1 Thermal Shock Test: No Leakage, No Fire, No Explosion
The battery is stored at 75℃±5℃ for 48 hours, moved to a temperature of -20℃±5℃ within 5 minutes and stored for 6 hours after standard charge (Section 4.3.1.).
4.6 Safety Performance
4.6.1 Short Circuit Test: No Fire, No Explosion
After standard charge (Section 4.3.1.), the battery shall be subjected to a short-circuit condition with a wire of resistance less than50mΩfor 1 hour.
4.6.2 Overcharge Test: (with a PCM) No Fire, No Explosion
After standard charge (Section 4.3.1.), the battery shall be charged at 1C /12V For 2.5 hrs.
4.6.3 Thermal Exposure Test No Fire, No Explosion
After standard charge (Section 4.3.1.), the battery is placed in an oven and is heated up at a rate of 5℃ until the temperature reaches 130℃. The oven shall be maintained at 130℃ for 60 minutes.

5. Delivery Condition: about 50% charged.

6. Lithium Ion Polymer Battery Handling Guideline

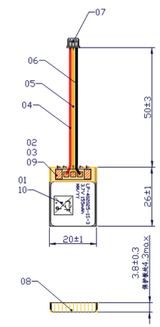
6.1 In case of contacting the materials from a damaged or ruptured cell or battery:
Eye contact: Washing immediately with plenty of water and soap or for at least 15 minutes. Get medical attention.
Skin Contact: Washing immediately with water and soap. Inhalation of Vented Gas: Remove to fresh air. Get medical attention. Ingestion: Get medical attention immediately.
6.2 Keep away batteries from children.
6.3 The cells/ batteries are requested to be stored within a proper temperature range specified in this specification.
6.4 Do not store batteries in a manner that allow s terminals to short circuit.
6.5 Do not place batteries near heating sources, nor exposed to direct sunlight for long periods. Elevated temperatures can result in reduced battery service life.
6.6 Charging Battery
Use only approved chargers and procedures. Improperly charging a cell or battery may cause the cell or battery to flame or damage.
Charge the battery using the "CC/CV" or constant current /constant voltage method.
Do not charge the battery with a current or voltage higher than the specified maximum value in this specification. The absolute maximum charging voltage is 4.25V per cell.
Prohibit reverse charging of the battery. The battery must be connected correctly.
6.7 Discharging Battery
Discharge battery at the max current specified in this specification. If you plan to discharge battery at a higher current than the max current, please consult us.
Avoid discharge the battery below 2.75V for each cell.
Do not over-discharge the battery. Over-discharging can damage the performance of the battery. It should be noted that the cell/battery would be at an over-discharged state by its self-discharge characteristics in case the cell is not used for long time. In order to prevent over-discharging, the cell/battery shall be charged periodically to maintain between 3.7V and 4.1V.
6.8 Operation Temperature
The battery shall be operated (stored, charged and discharged) in the temperature specified in This specification.
6.9 Cell/Battery Protection Circuit Module (PCM)
The cell/battery must be equipped with a PCM that protects the cell/battery from overcharging, over-discharging and over-current.
6.10 Battery Short Circuit
Do not short-circuit a battery. A short circuit can result in over-heating of the terminals and provide an ignition source. More than a momentary short circuit will generally reduce the cell or battery service life and can lead to ignition of surrounding materials or materials within the cell or battery if the seal integrity is damaged. Extended short-circuiting creates high temperature in the cell and at the terminals. Physical contact to high temperatures can cause skin burns. In addition, extended short-circuit may cause the cell or battery to flame.
6.11 Prohibit reversing cell polarity within a battery assembly.
6.12 The cell edge of the heat seal zone is electrically conductive. Avoid the edge cross battery terminals, PCB, or conductive surfaces.
6.13 Do not bend, fold or fall the battery or part of the battery. It may cause the battery be damaged and result in the battery swelling, leaking, explosion or ignition
6.14 Do not open or manipulate the folded cell edge.
6.15 Do not bend or fold the sealing edge. And do not tear off the sealing film.
6.16 Battery Pack Design
The battery housing should have sufficient mechanical strength.
No sharp edge components shall be inside the battery housing. The sharp edge may destroy the cell packaging.
No cell movement is allowed in the battery housing.
The ultrasonic head shall not directly/ or indirectly pressed the cell if you need to enclose the battery housing by ultrasonic method. Please consult us for designing the ultrasonic head. Avoid designing airtight battery housing.
6.17 Battery Assembly
We recommend ultrasonic welding or spot welding to connect battery with PCM or other parts. If you employ manual solder method to connect tab with PCM, please pay attention to the followings:
Use a solder with temperature controlled and ESD.
Soldering temperature should not exceed 300℃.
Soldering time should not be longer than 3s.
Soldering times should not exceed 5 times.
Keep battery tab cold down before next time soldering.
Do not directly heat cell body. It may cause the battery be damaged by heat above 90℃
6.18 Battery Disassembly
Never disassemble a battery.
Should a battery unintentionally be crushed, thus releasing its contents, rubber gloves must be used to handle all battery components. Avoid inhalation of any vapors that may be emitted.
6.19 Do not mixed Batteries and Types. Avoid to use old and new cells or cells of different sizes, different chemistry or types in the same battery assembly.
6.20 Other Warnings
Do not heat or dispose the battery into fire, water or other liquids.
Do not put the battery into microwave, washing machine or drying machine.
Do not use a damaged battery.
6.21 Others
Dubilier shall make no liability for problems that occur when the above specifications are not followed.

7. Remarks

If any matter with this specification arises, it shall be revised by mutual agreements.

8. Drawing

序号	部件名称	型号	数量
01	电芯/Cell	402025P	1
02	保护板/PCM	308NB 2.5V截止电压/cut-off	1
03	热敏电阻/NTC	25°C 10K±1%	1
04	红线/Red Wire(+)	UL1061#28	1
05	黄线/Yellow Wire(N)	UL1061#28	1
06	黑线/Black Wire(-)	UL1061#28	1
07	插头/connector	51201-3P正向/Positive	1
08	绝缘胶布/Insulating Tape	橙色/orange	1
09	绝缘胶布/Insulating Tape	橙色/orange	2
10	贴纸/Label	00-787([illegible]8*8)	1



Data sheet for protect circuit board

1. Type and Model

2. Type: Protection Module for Li Ion/Li-Polymer Battery Pack

3.1 Absolute Maximum Ratings (for Ricoh R5402N205KD)
3.2 Supply Voltage: -0.3V to 12 V
3.3 Operating Temperature: -40℃ to 85℃
3.4 Storage Temperature: -55℃ to 125℃

4. Electrical Characteristics (for Ricoh R5402N204KD)(T=25℃)

The followings is referring to the specs of R5402N204KD of Ricoh (for details, see R5402N204KD). These specs are guaranteed by design not by production tests.

4-A.1 Input Voltage: 1.5V (min) 5.0V(max)

4-A.2 Overcharge Detection : 4.175V (min) 4.200V(Typ) 4.225V(max)

4-A.3 Output Delay of Overcharge: 0.7s (min) 1.0s(Typ.) 1.3s (max)

4-A.4 Overcharge Release : 3.85V(min) 3.90V(Typ) 3.95V(max)

4-A.4 Over-discharge Detection : 2.438V (min) 2.500V(Typ) 2.562V(max)

4-A.5 Output Delay of Over-discharge: 14ms (min) 20ms(Typ.) 26ms(max)

4-A.6 Over-discharge Release : 2.925V (min) 3.000V(Typ) 3. 075V(max)

4-A.7 Over Discharge-Current Detection : 0.185V (min) 0.20V(Typ) 0.225V(max)

4-A.8Overcharge-Current Detection : 0.17V (min) 0.20V(Typ) 0.23V(max)
4-A.9 Over Discharge-Current Value: 3.0A(min) 4.0A(Typ) 7.0A (max)

4-A.10 Over charge-Current Value: 3.0A(min) 4.0A(Typ) 7.0A (max)

4-A.11 Output Delay of Over-Discharge-Current 8ms (min) 12ms(Typ.) 16ms (max)

4-A.12 Output Delay of Over-charge-Current: 5ms (min) 8ms(Typ.) 11ms (max)

4-A.13 Short Protection Voltage: 0.55V (min) 0.8 V (Typ) 1.0V (max)

4-A.14 Output Delay of Short Protection: 230(Min) 300 µs(Typ) 500µs(max)

4-A.15 Supply Current (active status): 4.0µA (Typ) 8.0µA (max)

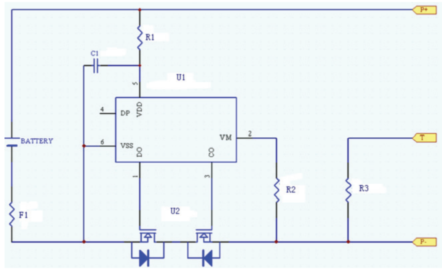
4-A.16 Supply Current (Standby): 1.2µA (Typ) 2.00µA (max)

4-A.17 PCM Resistance : 35mΩ(min) 50mΩ(Typ) 60mΩ(max)

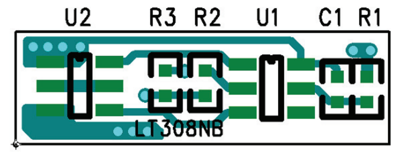
5. Part List

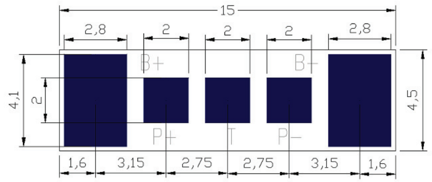
Part Number	Part Name	Qty	Remark
Ricoh R5402N204KD or Equivalent	Control IC	1	U1
SMS8205 or STS8205 or SMS2017or Equivalent	MOSFET	1	U2
330Ω(0603)	Resister	1	R1
1kΩ(0603)	Resister	1	R2
10kΩ(0603)	NTC	1	R3
SMD200F(1812)	PTC	1	F1
0.1uF(0603)	Capacitor	1	C1

6. PCM Circuit Diagram (R5402N204KD or Equivalent)



7. PCB layout(R5402N204KD OR Equivalent)PCM308NB





Appendix C:

Datasheet for Battery Charger LTC4053-4.2 Chip

LTC4053-4.2

USB Compatible Lithium-Ion Battery Charger with Thermal Regulation

FEATURES

- **Charges Single-Cell Li-Ion Batteries Directly from USB Port**
- **Thermal Regulation Maximizes Charge Rate without Risk of Overheating***
- **Programmable Charge Current with ±7% Accuracy**
- **Low Dropout Operation**
- **No External MOSFET, Sense Resistor or Blocking Diode Required**
- Programmable Charge Termination Timer
- Preset Charge Voltage with ±1% Accuracy
- C/10 Charge Current Detection Output
- AC Present Logic Output
- 25µA Supply Current in Shutdown Mode
- Automatic Recharge
- Charge Current Monitor Useful for Gas Gauging
- Thermistor Input for Temperature Qualified Charging
- Available in 10-pin thermally enhanced MSOP and low profile (0.75mm) 3mm × 3mm DFN packages

APPLICATIONS

- Cellular Telephones
- Handheld Computers
- Charging Docks and Cradles
- MP3 Players
- Digital Cameras

DESCRIPTION

The LTC®4053 is a standalone linear charger for lithium-ion batteries that can be powered directly from a USB port. The IC contains an on-chip power MOSFET and eliminates the need for an external sense resistor and blocking diode. Thermal regulation automatically adjusts charge current to limit die temperature during high power or high ambient temperature conditions. This feature protects the end product and the LTC4053 from thermal stress while the IC charges the battery at maximum rate without interruption.

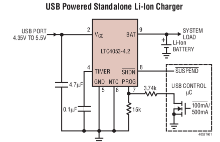
The charge current and charge time can be set externally with a single resistor and capacitor, respectively. When the input supply (wall adapter or USB supply) is removed, the LTC4053 automatically enters a low current sleep mode, dropping the battery drain current to less than 5µA.

The LTC4053 also includes NTC temperature sensing, C/10 detection circuitry, AC present logic, low battery charge conditioning (trickle charging) and shutdown (25µA supply current).

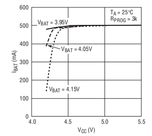
The LTC4053 is available in 10-pin thermally enhanced MSOP and low profile (0.75mm) DFN packages.

TYPICAL APPLICATION

USB Powered Standalone Li-Ion Charger



Charge Current vs Input Voltage



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{CC}) 7V
BAT 7V
NTC, SHDN, TIMER, PROG .... –0.3V to V_{CC} + 0.3V
CHRG, FAULT, ACPR .... –0.3V to 7V
BAT Short-Circuit Duration .... Continuous
BAT Current (Note 2) 1.3A
PROG Current (Note 2) 1.3mA
Junction Temperature .... 125°C
Operating Temperature Range (Note 3) ... –40°C to 85°C
Storage Temperature Range
MSE .... –65°C to 150°C
DD .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSE .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW: CHRG 1, VCC 2, FAULT 3, TIMER 4, GND 5 / 10 ACPR, 9 BAT, 8 SHDN, 7 PROG, 6 NTC; 11. DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN. T_{JMAX} = 125°C, θ_{JA} = 40°C/W (NOTE 4). EXPOSED PAD (PIN 11) IS GND (MUST BE SOLDERED TO PCB)	ORDER PART NUMBER	TOP VIEW: CHRG 1, VCC 2, FAULT 3, TIMER 4, GND 5 / 10 ACPR, 9 BAT, 8 SHDN, 7 PROG, 6 NTC; 11. MSE EXPOSED PAD PACKAGE 10-LEAD PLASTIC MSOP. T_{JMAX} = 125°C, θ_{JA} = 40°C/W (NOTE 4). EXPOSED PAD (PIN 11) IS GND (MUST BE SOLDERED TO PCB)	ORDER PART NUMBER
	LTC4053EDD-4.2		LTC4053EMSE-4.2
	DD PART MARKING		MSE PART MARKING
	LBQC		LTZT

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Supply Voltage		●	4.25		6.5	V
I_{CC}	V_{CC} Supply Current	Charger On; Current Mode; R_{PROG} = 30k (Note 5) Shutdown Mode; $V_{\overline{SHDN}}$ = 0V Sleep Mode $V_{CC} < V_{BAT}$ or $V_{CC} \le 4V$	● ● ●		1 25 25	2 50 50	mA µA µA
V_{BAT}	V_{BAT} Regulated Float Voltage		●	4.158	4.2	4.242	V
I_{BAT}	Battery Pin Current	R_{PROG} = 3k; Current Mode R_{PROG} = 15k; Current Mode Shutdown Mode; $V_{\overline{SHDN}}$ = 0V Sleep Mode $V_{CC} < V_{BAT}$ or $V_{CC} < (V_{UV} - \Delta V_{UV})$	● ●	465 93	500 100 ±1 ±1	535 107 ±3 ±3	mA mA µA µA
I_{TRIKL}	Trickle Charge Current	V_{BAT} < 2V; R_{PROG} = 3k	●	35	50	65	mA
V_{TRIKL}	Trickle Charge Trip Threshold	V_{BAT} Rising			2.48		V
ΔV_{TRIKL}	Trickle Charge Trip Hysteresis				100		mV
V_{UV}	V_{CC} Undervoltage Lockout Voltage	V_{CC} Rising	●		4	4.25	V
ΔV_{UV}	V_{CC} Undervoltage Lockout Hysteresis				200		mV
V_{MSD}	Manual Shutdown Threshold Voltage	SHDN Pin Voltage		0.6		1.3	V
V_{ASD}	Automatic Shutdown Threshold Voltage	(V_{CC} - V_{BAT}) High to Low (V_{CC} - V_{BAT}) Low to High			35 70		mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PROG}	PROG Pin Voltage	R_{PROG} = 3k, I_{PROG} = 500µA			1.5		V
$I_{\overline{CHRG}}$	CHRG Pin Weak Pulldown Current	$V_{\overline{CHRG}}$ = 1V		15	30	50	µA
$V_{\overline{CHRG}}$	CHRG Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			0.35	0.6	V
$V_{\overline{ACPR}}$	ACPR Pin Output Low Voltage	$I_{\overline{ACPR}}$ = 5mA			0.35	0.6	V
$V_{\overline{FAULT}}$	FAULT Pin Output Low Voltage	$I_{\overline{FAULT}}$ = 5mA			0.35	0.6	V
$I_{C/10}$	End of Charge Indication Current Level	R_{PROG} = 3k		44	50	56	mA
t_{TIMER}	TIMER Accuracy	C_{TIMER} = 0.1µF			10		%
V_{RECHRG}	Recharge Battery Voltage Threshold	Battery Voltage Falling			4.035		V
$V_{NTC-HOT}$	NTC Pin Hot Threshold Voltage	V_{NTC} Falling			2.5		V
$V_{HOT-HYS}$	NTC Pin Hot Hysteresis Voltage				80		mV
$V_{NTC-COLD}$	NTC Pin Cold Threshold Voltage	V_{NTC} Rising			4.375		V
$V_{COLD-HYS}$	NTC Pin Cold Hysteresis Voltage				80		mV
$V_{NTC-DIS}$	NTC Pin Disable Threshold Voltage	V_{NTC} Rising			100		mV
$V_{DIS-HYS}$	NTC Pin Disable Hysteresis Voltage				10		mV
T_{LIM}	Junction Temperature in Constant-Temperature Mode				105		°C
R_{ON}	Power MOSFET "ON" Resistance				375		mΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The Absolute Maximum BAT Current Rating of 1.3A is guaranteed by design and current density calculations. The Absolute Maximum PROG Current Rating is guaranteed to be 1/1000 of BAT current rating by design.

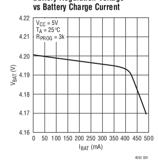
Note 3: The LTC4053E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 4: Failure to solder the exposed backside of the package to the PC board will result in a thermal resistance much higher than 40°C/W.

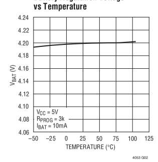
Note 5: Supply current includes PROG pin current (approximately 50µA) but does not include any current delivered to the battery through the BAT pin (approximately 50mA).

TYPICAL PERFORMANCE CHARACTERISTICS

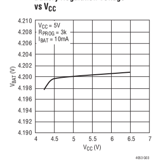
Battery Regulation Voltage vs Battery Charge Current



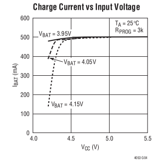
Battery Regulation Voltage vs Temperature



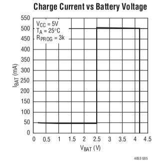
Battery Regulation Voltage vs V_{CC}



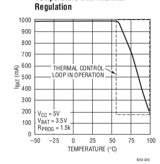
Charge Current vs Input Voltage



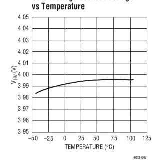
Charge Current vs Battery Voltage



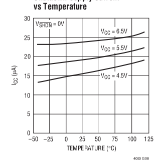
Charge Current vs Ambient Temperature with Thermal Regulation



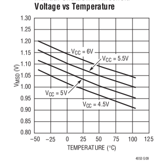
Undervoltage Lockout Voltage vs Temperature



Shutdown Supply Current vs Temperature

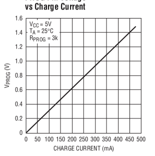


Manual Shutdown Threshold Voltage vs Temperature

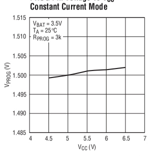


TYPICAL PERFORMANCE CHARACTERISTICS

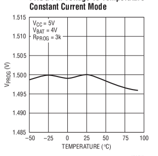
PROG Pin Voltage vs Charge Current



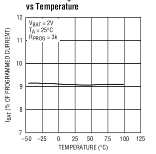
PROG Pin Voltage vs V_{CC} Constant Current Mode



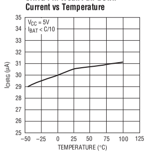
PROG Pin Voltage vs Temperature Constant Current Mode



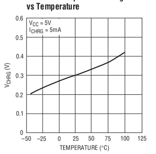
Trickle Charge Current vs Temperature



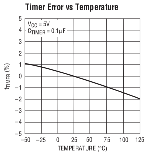
CHRG Pin Weak Pull-Down Current vs Temperature



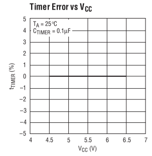
CHRG Pin Output Low Voltage vs Temperature



Timer Error vs Temperature



Timer Error vs V_{CC}



PIN FUNCTIONS

CHRG: Open-Drain Charge Status Output. When the battery is being charged, the CHRG pin is pulled low by an internal N-channel MOSFET. When the charge current drops to 10% of the full-scale current, the N-channel MOSFET latches off and a 30µA current source is connected from the CHRG pin to ground. The C/10 latch can be cleared by grounding the SHDN pin, momentarily, or toggling V_{CC}. When the timer runs out or the input supply is removed, the current source is disconnected and the CHRG pin is forced high impedance.

V_{CC}: Positive Input Supply Voltage. When V_{CC} is within 35mV of V_{BAT} or less than the undervoltage lockout threshold, the LTC4053 enters sleep mode, dropping I_{BAT} to less than 3µA. V_{CC} can range from 4.25V to 6.5V. Bypass this pin with at least a 4.7µF ceramic capacitor to ground.

FAULT: Open-Drain Fault Status Output. The FAULT open-drain logic signal indicates that the charger has timed out under trickle charge conditions or the NTC comparator is indicating an out-of-range battery temperature condition. If V_{BAT} is less that 2.48V, trickle charging begins whereby the charge current drops to one tenth of its programmed value and the timer period is reduced by a factor of four. When one fourth of the timing period has elapsed, if V_{BAT} is still less than 2.48V, trickle charging stops and the FAULT pin latches to ground. The fault can be cleared by toggling V_{CC}, momentarily grounding the SHDN pin or pulling the BAT pin above 2.48V. If the NTC comparator is indicating an out-of-range battery temperature condition, the FAULT pin will pull to ground until the temperature returns to the acceptable range.

TIMER: Timer Capacitor. The timer period is set by placing a capacitor, C_{TIMER}, to ground. The timer period is:

$$\text{Time (Hours)} = (C_{TIMER} \bullet 3\ \text{hr})/(0.1\mu F)$$

Short the TIMER pin to ground to disable the internal timer function.

GND: Ground. The exposed backside of the package is also ground and must be soldered to the PC board for maximum heat transfer.

NTC: Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit. With an external 10kΩ NTC thermistor to ground and a 1% resistor to V_{CC}, this pin can sense the temperature of the battery pack and stop charging when it is out of range. When the voltage at this pin drops below (0.5)•(V_{CC}) at hot temperatures or rises above (0.875)•(V_{CC}) at cold, charging is suspended and the internal timer is frozen. The CHRG pin output status is not affected in this hold state. The FAULT pin will be pulled to ground, but not latched. When the temperature returns to an acceptable range, charging will resume and the FAULT pin will be released. The NTC feature can be disabled by grounding the NTC pin.

PROG: Charge Current Program and Charge Current Monitor Pin. The charge current is programmed by connecting a resistor, R_{PROG} to ground. When in constant-current mode, the LTC4053 servos the PROG pin voltage to 1.5V. In all modes the voltage on the PROG pin can be used to measure the charge current as follows:

$$I_{BAT} = (V_{PROG}/R_{PROG}) \bullet 1000.$$

SHDN: Shutdown Input Pin. Pulling the SHDN pin to ground will put the LTC4053 into standby mode where the BAT drain current is reduced to less than 3µA, and the supply current is reduced to less than 25µA. For normal operation, pull the SHDN pin up to V_{CC}.

BAT: Charge Current Output. A bypass capacitor of at least 1µF with a 1Ω series resistor is required to keep the loop stable when the battery is not present. A precision internal resistor divider sets the final float potential on this pin. The internal resistor divider is disconnected in sleep and shutdown mode.

ACPR: Open-Drain Power Supply Status Output. When V_{CC} is greater than the undervoltage lockout threshold and at least 35mV above V_{BAT}, the ACPR pin will pull to ground. Otherwise, the pin is high impedance.

SIMPLIFIED BLOCK DIAGRAM

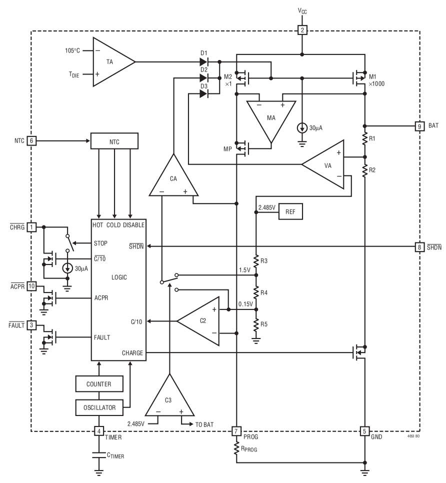


Figure 1

OPERATION

The LTC4053 is a linear battery charger designed primarily for charging single cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1.25A with a final float voltage accuracy of ±1%. No blocking diode or sense resistor is required thus dropping the external component count to three for the basic charger circuit. The CHRG, ACPR, and FAULT open-drain status outputs provide information regarding the status of the LTC4053 at all times. An NTC thermistor input provides the option of charge qualification using battery temperature.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC4053 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4053 or the external components. Another benefit of the LTC4053 thermal limit is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The charge cycle begins when the voltage at the V_{CC} pin rises above the UVLO level, a program resistor is connected from the PROG pin to ground, and the SHDN pin is pulled above the shutdown threshold. At the beginning of the charge cycle, if the battery voltage is below 2.48V, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.48V. In constant-current mode, the charge current is set by R_{PROG}.

When the battery approaches the final float voltage, the charge current begins to decrease as the LTC4053 enters the constant-voltage mode. When the current drops to 10% of the full-scale charge current, an internal comparator latches off the MOSFET on the CHRG pin and connects a weak current source to ground (30µA) to indicate a near end-of-charge (C/10) condition. The C/10 latch can be cleared by grounding the SHDN pin momentarily, or momentarily removing and reapplying V_{CC}.

An external capacitor on the TIMER pin sets the total charge time. When this time elapses, the charge cycle terminates and the CHRG pin assumes a high impedance state. To restart the charge cycle, remove the input voltage and reapply it, or momentarily force the SHDN pin to 0V. The charge cycle will also restart if the BAT pin voltage falls below the recharge threshold.

For lithium-ion and similar batteries that require an accurate final float voltage, the internal reference, voltage amplifier and the resistor divider provide regulation with ±1% (max) accuracy.

When the input voltage is not present, the charger goes into a sleep mode, dropping battery drain current, I_{BAT}, to less than 5µA. This greatly reduces the current drain on the battery and increases the standby time. The charger can be shut down (I_{CC} = 25µA) by forcing the SHDN pin to 0V.

APPLICATIONS INFORMATION

Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until V_{CC} rises above the undervoltage lockout threshold. The UVLO circuit has a built-in hysteresis of 150mV. Furthermore, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if V_{CC} falls to within 35mV of the battery voltage. If the UVLO comparator is tripped, the charger will not come out of shutdown until V_{CC} rises 70mV above the battery voltage.

Trickle Charge And Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below 2.48V) the charger goes into trickle charge reducing the charge current to 10% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated, the $\overline{CHRG}$ pin output assumes a high impedance state, and the $\overline{FAULT}$ pin pulls low. The fault can be cleared by toggling V_{CC}, temporarily forcing the $\overline{SHDN}$ pin to 0V, or temporarily forcing the BAT pin voltage above 2.48V.

Shutdown

The LTC4053 can be shut down (I_{CC} = 25µA) by pulling the $\overline{SHDN}$ pin to 0V. For normal operation, pull the $\overline{SHDN}$ pin above the manual shutdown threshold voltage level. Do not leave this pin open. In shutdown the internal linear regulator is turned off, and the internal timer is reset.

Programming Charge Current

The formula for the battery charge current (see Figure 1) is:

$$I_{CHG} = (I_{PROG}) \bullet 1000$$
$$= (1.5V / R_{PROG}) \bullet 1000 \text{ or}$$
$$R_{PROG} = 1500V/I_{CHG}$$

where R_{PROG} is the total resistance from the PROG pin to ground. Under trickle charge conditions, this current is reduced to 10% of the full-scale value.

For example, if 500mA charge current is required, calculate:

$$R_{PROG} = 1500V/0.5A = 3k\Omega$$

For best stability over temperature and time, 1% metal-film resistors are recommended.

If the charger is in constant-temperature or constant-voltage mode, the battery current can be monitored by measuring the PROG pin voltage as follows:

$$I_{CHG} = (V_{PROG} / R_{PROG}) \bullet 1000$$

USB and Wall Adapter Power

Although the LTC4053 allows charging from a USB port, a wall adapter can also be used to charge Li-Ion batteries. Figure 2 shows an example of how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conducting into the USB port when a wall adapter is present and Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

Typically a wall adapter can supply significantly more current than the 500mA-limited USB port. Therefore, an N-channel MOSFET, MN1 and an extra 3k program resistor can be used to increase the charge current to 1A when the wall adapter is present.

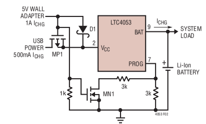


Figure 2. Combining Wall Adapter and USB Power

APPLICATIONS INFORMATION

Programming The Timer

The programmable timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin. The total charge time is:

$$\text{Time (Hours)} = (3 \text{ Hours}) \bullet (C_{TIMER}/0.1\mu F) \text{ or}$$
$$C_{TIMER} = 0.1\mu F \bullet \text{Time (Hours)}/3 \text{ (Hours)}$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied and the $\overline{SHDN}$ pin is greater than the manual shutdown threshold voltage level. After a time-out occurs, the charge current stops, and the $\overline{CHRG}$ output assumes a high impedance state to indicate that the charging has stopped. Connecting the TIMER pin to ground disables the timer function.

Recharge

After a charge cycle has terminated, if the battery voltage drops below the recharge threshold of 4.05V a new charge cycle will begin. The recharge circuit integrates the BAT pin voltage for a few milliseconds to prevent a transient from restarting the charge cycle.

If the battery voltage remains below 2.48V during trickle charge for 1/4 of the programmed time, the battery may be defective and the charge cycle will end. In addition, the recharge comparator is disabled and a new charge cycle will not begin unless the input voltage is toggled off-then-on, the $\overline{SHDN}$ pin is momentarily pulled to ground, or the BAT pin is pulled above the 2.48V trickle charge threshold.

Open-Drain Status Outputs

The LTC4053 has three open-drain status outputs: $\overline{ACPR}$, $\overline{CHRG}$ and $\overline{FAULT}$. The $\overline{ACPR}$ pin pulls low when an input voltage greater than the undervoltage lockout threshold is applied and becomes high impedance when power ($V_{IN} < V_{UV}$) is removed. $\overline{CHRG}$ and $\overline{FAULT}$ work together to indicate the status of the charge cycle. Table 1 describes the status of the charge cycle based on the $\overline{CHRG}$ and $\overline{FAULT}$ outputs.

Table 1.

$\overline{FAULT}$	$\overline{CHRG}$	Description
High	Low	Charge cycle has started, C/10 has not been reached and charging is proceeding normally.
Low	Low	Charge cycle has started, C/10 has not been reached, but the charge current and timer have been paused due to an NTC out-of-temperature condition.
High	30µA pull-down	C/10 has been reached and charging is proceeding normally.
Low	30µA pull-down	C/10 has been reached but the charge current and timer have paused due to an NTC out-of-temperature condition.
High	High	Normal timeout (charging has terminated).
Low	High	If $\overline{FAULT}$ goes low and $\overline{CHRG}$ goes high impedance simultaneously, then the LTC4053 has timed out due to a bad cell (V_{BAT} < 2.48V after one-quarter the programmed charge time). If $\overline{CHRG}$ goes high impedance first, then the LTC4053 has timed out normally (charging has terminated), but NTC is indicating an out-of-temperature condition.

$\overline{CHRG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. When the charge current drops to 10% of the full-scale current (C/10), the N-channel MOSFET is latched off and a weak 30µA current source to ground is connected to the $\overline{CHRG}$ pin. After a time-out occurs, the pin assumes a high impedance state. By using two different value pull-up resistors a microprocessor can detect three states from this pin (charging, C/10 and time-out). See Figure 3.

When the LTC4053 is in charge mode, the $\overline{CHRG}$ pin is pulled low by the internal N-channel MOSFET. To detect this mode, force the digital output pin, OUT, high and measure the voltage at the $\overline{CHRG}$ pin. The N-channel MOSFET will pull the pin low even with the 2k pull-up resistor. Once the charge current drops to 10% of the

APPLICATIONS INFORMATION

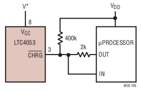


Figure 3. Microprocessor Interface

full-scale current (C/10), the N-channel MOSFET is turned off and a 30µA current source is connected to the $\overline{CHRG}$ pin. The IN pin will then be pulled high by the 2k pull-up. By forcing the OUT pin to a high impedance state, the current source will pull the pin low through the 400k resistor. When the internal timer has expired, the $\overline{CHRG}$ pin will assume a high impedance state and the 400k resistor will then pull the pin high to indicate that charging has terminated.

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 4. To use this feature, connect a 10k NTC thermistor between the NTC pin and ground and a resistor (R_{HOT}) from the NTC pin to V_{CC}. R_{HOT} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 50°C (this value is 4.1k for a Vishay NTHS0603N02N1002J thermistor). The LTC4053 goes into hold mode when the resistance of the NTC thermistor drops below 4.1k which should be approximately 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4053 is designed to go into hold mode when the value of the NTC thermistor increases to seven times the value of R_{HOT}. For a Vishay NTHS0603N02N1002J thermistor, this value is 28.7k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 2°C of hysteresis to prevent oscillation about the trip point. The NTC function can be disabled by grounding the NTC pin.

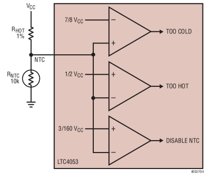


Figure 4

Thermistors

The LTC4053 NTC trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 2". The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Futhermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of R_{COLD} to R_{HOT} of 2.816/0.4086 = 6.9).

NTC Layout Considerations

It is important that the NTC thermistor not be in close thermal contact with the LTC4053. Because the LTC4053 package can reach temperatures in excess of the 50°C trip point, the NTC function can cause a hysteretic oscillation which turns the charge current on and off according to the package temperature rather than the battery temperature. This problem can be eliminated by thermally coupling the NTC thermistor to the battery and not to the LTC4053.

Furthermore, it is essential that the V_{CC} connection to R_{HOT} is made according to standard Kelvin sense techniques. Since V_{CC} is a high current path into the LTC4053, it is essential to minimize voltage drops between the V_{CC} input pin and the top of R_{HOT}.

APPLICATIONS INFORMATION

NTC Trip Point Errors

When a 1% resistor is used for R_{HOT}, the major error in the 50°C trip point is determined by the tolerance of the NTC thermistor. A typical 10k NTC thermistor has a ±10% tolerance. By looking up the temperature coefficient of the thermistor at 50°C, the tolerance error can be calculated in degrees centigrade. Consider the Vishay NTHS0603N02N1002J thermistor which has a temperature coefficient of –3.3%/°C at 50°C. Dividing the tolerance by the temperature coefficient, ±10%/(3.3%/°C) = ±3°C, gives the temperature error of the hot trip point.

The cold trip point is a little more complicated because its error depends on the tolerance of the NTC thermistor and the degree to which the ratio of its value at 0°C and its value at 50°C varies from 7 to 1. Therefore, the cold trip point error can be calculated using the tolerance, TOL, the temperature coefficient of the thermistor at 0°C, TC (in %/°C), the value of the thermistor at 0°C, R_{COLD}, and the value of the thermistor at 50°C, R_{HOT}. The formula is:

$$\text{Temperature Error (°C)} = \frac{\left(\frac{1+TOL}{7} \bullet \frac{R_{COLD}}{R_{HOT}} - 1\right) \bullet 100}{TC}$$

For example, the Vishay NTHS0603N02N1002J thermistor with a tolerance of ±10%, TC of –4.5%/°C, and R_{COLD}/R_{HOT} of 6.89, has a cold trip point error of:

$$\text{Temperature Error (°C)} = \frac{\left(\frac{1 \pm 0.10}{7} \bullet 6.89 - 1\right) \bullet 100}{-4.5}$$

$$= -1.8°C, +2.5°C$$

If a thermistor with a tolerance less than ±10% is used, the trip point errors begin to depend on errors other than thermistor tolerance including the input offset voltage of the internal comparators of the LTC4053 and the effects of internal voltage drops due to high charging currents.

Constant-Current/Constant-Voltage/Constant-Temperature

The LTC4053 uses a unique architecture to charge a battery in a constant-current, constant-voltage, constant-temperature fashion. Figure 1 shows a simplified block diagram of the LTC4053. Three of the amplifier feedback loops shown control the constant-current, CA, constant-voltage, VA, and constant-temperature, TA modes. A fourth amplifier feedback loop, MA, is used to increase the output impedance of the current source pair, M1 and M2 (note that M1 is the internal P-channel power MOSFET). It ensures that the drain current of M1 is exactly 1000 times greater than the drain current of M2.

Amplifiers CA, TA, and VA are used in three separate feedback loops to force the charger into constant-current, temperature, or voltage mode, respectively. Diodes, D1, D2, and D3 provide priority to whichever loop is trying to reduce the charge current the most. The outputs of the other two amplifiers saturate low which effectively removes their loops from the system. When in constant-current mode, CA servos the voltage at the PROG pin to be precisely 1.50V (or 0.15V when in trickle-charge mode). TA limits the die temperature to approximately 105°C when in constant-temperature mode and the PROG pin voltage gives an indication of the charge current as discussed in "Programming Charge Current". VA servos its inverting input to precisely 2.485V when in constant-voltage mode and the internal resistor divider made up of R1 and R2 ensures that the battery voltage is maintained at 4.2V. Again, the PROG pin voltage gives an indication of the charge current.

In typical operation, the charge cycle begins in constant-current mode with the current delivered to the battery equal to $1500V/R_{PROG}$. If the power dissipation of the LTC4053 results in the junction temperature approaching 105°C, the amplifier (TA) will begin decreasing the charge current to limit the die temperature to approximately 105°C. As the battery voltage rises, the LTC4053 either returns to constant-current mode or it enters constant-voltage mode straight from constant-temperature mode.

APPLICATIONS INFORMATION

Regardless of mode, the voltage at the PROG pin is proportional to the current being delivered to the battery.

Power Dissipation

The conditions that cause the LTC4053 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the IC. For high charge currents, the LTC4053 power dissipation is approximately:

$$P_D = (V_{CC} - V_{BAT}) \bullet I_{BAT}$$

where P_D is the power dissipated, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage, and I_{BAT} is the battery charge current. It is not necessary to perform any worst-case power dissipation scenarios because the LTC4053 will automatically reduce the charge current to maintain the die temperature at approximately 105°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105°C - P_D\theta_{JA}$$
$$T_A = 105°C - (V_{CC} - V_{BAT}) \bullet I_{BAT} \bullet \theta_{JA}$$

Example: Consider an LTC4053 operating from a 5V wall adapter providing 1.2A to a 3.75V Li-Ion battery. The ambient temperature above which the LTC4053 will begin to reduce the 1.2A charge current is approximately:

$$T_A = 105°C - (5V - 3.75V) \bullet 1.2A \bullet 40°C/W$$
$$T_A = 105°C - 1.5W \bullet 40°C/W = 105°C - 60°C = 45°C$$

The LTC4053 can be used above 45°C, but the charge current will be reduced below 1.2A. The approximate charge current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{105°C - T_A}{(V_{CC} - V_{BAT}) \bullet \theta_{JA}}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{105°C - 55°C}{(5V - 3.75V) \bullet 40°C/W} = \frac{50°C}{50°C/A} = 1A$$

Furthermore, the voltage at the PROG pin will change proportionally with the charge current as discussed in the Programming Charge Current section.

It is important to remember that LTC4053 applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 105°C.

Board Layout Considerations

The ability to deliver maximum charge current under all conditions require that the exposed metal pad on the backside of the LTC4053 package be soldered to the PC board ground. Correctly soldered to a 2500mm^2 double-sided 1oz. copper board the LTC4053 has a thermal resistance of approximately 40°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 40°C/W. As an example, a correctly soldered LTC4053 can deliver over 1250mA to a battery from a 5V supply at room temperature. Without a backside thermal connection, this number could drop to less than 500mA.

V_{CC} Bypass Capacitor

Many types of capacitors can be used for input bypassing. However, caution must be exercised when using multi-layer ceramic capacitors. Because of the self resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a hot power source. For more information refer to Application Note 88.

Stability

The constant-voltage mode feedback loop is stable without any compensation provided that a battery is connected. However, a 1µF capacitor with a 1Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

In the constant-current mode it is the PROG pin that is in the feedback loop and not the battery. The constant-current mode stability is affected by the impedance at the

APPLICATIONS INFORMATION

PROG pin. With no additional capacitance on the PROG pin, stability is acceptable with program resistor values as high as 50k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 500kHz. Therefore, if the PROG pin is loaded with a capacitance, C, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} < 1/(6.283 \bullet 5 \times 10^5 \bullet C)$$

Average, rather than instantaneous, battery current may be of interest to the user. For example, if a switching power supply operating in low-current mode is connected in parallel with the battery the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses. In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current as shown in Figure 5. A 10k resistor is added between the PROG pin and the filter capacitor and monitoring circuit to ensure stability.

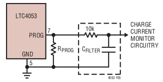
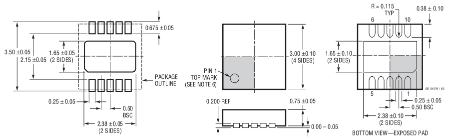


Figure 5. Isolating Capacitive Load on PROG Pin and Filtering

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

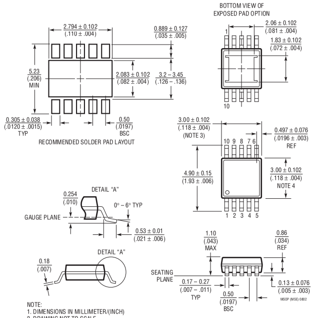


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

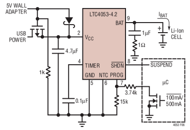
MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1663)



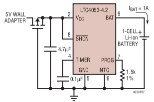
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATIONS

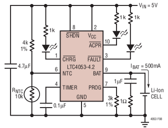
USB/Wall Adapter Power Li-Ion Battery Charger



Li-Ion Battery Charger with Reverse Polarity Input Protection



Full Featured Single Cell Li-Ion Charger



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1571	200kHz/500kHz Switching Battery Charger	Up to 1.5A Charge Current; Preset and Adjustable Battery Voltages
LTC1729	Lithium-Ion Battery Charger Termination Controllers	Time or Charge Current Termination, Preconditioning 8-Lead MSOP
LTC1730	Lithium-Ion Battery Pulse Charger	No Blocking Diode Required, Current Limit for Maximum Safety
LTC1731	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Features Preset Voltages, C/10 Charger Detection and Programmable Timer
LTC1732	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Features Preset Voltages, C/10 Charger Detection and Programmable Timer, Input Power Good Indication
LTC1733	Monolithic Lithium-Ion Linear Battery Charger	Standalone Charger with Programmable Timer, Up to 1.5A Charge Current
LTC1734	Lithium-Ion Linear Battery Charger in ThinSOT™	Simple ThinSOT Charger, No Blocking Diode, No Sense Resistor Needed
LTC1734L	Lithium-Ion Linear Battery Charger Controller	50mA to 180mA, No Blocking Diode, No Sense Resistor Needed
LTC4050	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Thermistor Input for Battery Temperature Sensing
LTC4052	Lithium-Ion Linear Battery Pulse Charger	Fully Integrated, Standalone Pulse Charger, Minimal Heat Dissipation, Overcurrent Protection
LTC4054	Standalone Lithium-Ion Linear Battery Charger in ThinSOT	Up to 800mA Charge Current, Thermal Regulation, USB Compatible, Charge Termination
LTC4056	Standalone Lithium-Ion Linear Battery Charger Controller in ThinSOT	Up to 700mA Charge Current, Charge Termination, Continuous Charging with Poorly Regulated or High Impedance Input Supplies

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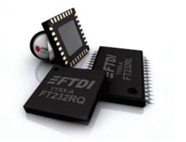
Appendix D:

Datasheet for FT232R Chip

Future Technology Devices International Ltd.

FT232R USB UART IC



The FT232R is a USB to serial UART interface with the following advanced features:

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 1024 bit EEPROM storing device descriptors and CBUS I/O configuration.
- Fully integrated USB termination resistors.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- Data transfer rates from 300 baud to 3 Mbaud (RS422, RS485, RS232) at TTL levels.
- 128 byte receive buffer and 256 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Unique USB FTDIChip-ID™ feature.
- Configurable CBUS I/O pins.
- Transmit and receive LED drive signals.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity
- FIFO receive and transmit buffers for high data throughput.
- Synchronous and asynchronous bit bang interface options with RD# and WR# strobes.
- Device supplied pre-programmed with unique USB serial number.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- Integrated +3.3V level converter for USB I/O.
- Integrated level converter on UART and CBUS for interfacing to between +1.8V and +5V logic.
- True 5V/3.3V/2.8V/1.8V CMOS drive output and TTL input.
- Configurable I/O pin output drive strength.
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- UART signal inversion option.
- +3.3V (using external oscillator) to +5.25V (internal oscillator) Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).

1 Typical Applications

- USB to RS232/RS422/RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU/PLD/FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader and Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software and Hardware Encryption Dongles

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32,64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS 8/9, OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32,64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT232RQ-xxxx	32 Pin QFN
FT232RL-xxxx	28 Pin SSOP

Note: Packing codes for xxxx is:

- Reel: Taped and Reel, (SSOP is 2,000pcs per reel, QFN is 6,000pcs per reel).

- Tube: Tube packing, 47pcs per tube (SSOP only)

- Tray: Tray packing, 490pcs per tray (QFN only)

For example: FT232RQ-Reel is 6,000pcs taped and reel packing

1.3 USB Compliant

The FT232R is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40680004 (Rev B) and 40770018 (Rev C).

2 FT232R Block Diagram

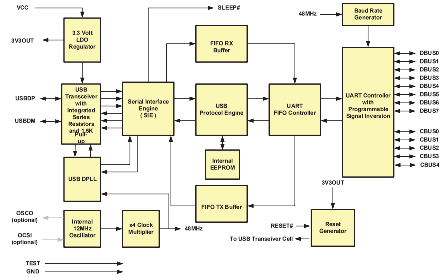


Figure 2.1 FT232R Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 28-LD SSOP Package

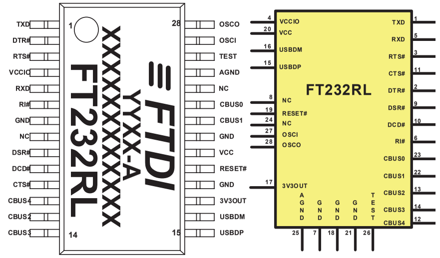


Figure 3.1 SSOP Package Pin Out and Schematic Symbol

3.2 SSOP Package Pin Out Description

Note: The convention used throughout this document for active low signals is the signal name followed by a #

Pin No.	Name	Type	Description
15	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V.
16	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.

Table 3.1 USB Interface Group

Pin No.	Name	Type	Description
4	VCCIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect this pin to 3V3OUT pin to drive out at +3.3V levels, or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply in order to drive outputs at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
7, 18, 21	GND	PWR	Device ground supply pins

Pin No.	Name	Type	Description
17	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The main use of this pin is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
20	VCC	PWR	+3.3V to +5.25V supply to the device core. (see Note 1)
25	AGND	PWR	Device analogue ground supply for internal clock multiplier

Table 3.2 Power and Ground Group

Pin No.	Name	Type	Description
8, 24	NC	NC	No internal connection
19	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCC.
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation. (see Note 2)
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used. (see Note 2)

Table 3.3 Miscellaneous Signal Group

Pin No.	Name	Type	Description
1	TXD	Output	Transmit Asynchronous Data Output.
2	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
3	RTS#	Output	Request to Send Control Output / Handshake Signal.
5	RXD	Input	Receiving Asynchronous Data Input.
6	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend.
9	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
10	DCD#	Input	Data Carrier Detect Control Input.
11	CTS#	Input	Clear To Send Control Input / Handshake Signal.
12	CBUS4	I/O	Configurable CBUS output only Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 3.9.
13	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 3.9.

Pin No.	Name	Type	Description
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 3.9. PWREN# should be used with a 10kΩ resistor pull up.
22	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 3.9.
23	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 3.9.

Table 3.4 UART Interface and CUSB Group (see note 3)

Notes:

1. The minimum operating voltage VCC must be +4.0V (could use VBUS=+5V) when using the internal clock generator. Operation at +3.3V is possible using an external crystal oscillator.
2. For details on how to use an external crystal, ceramic resonator, or oscillator with the FT232R, please refer Section 7.6
3. When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

3.3 QFN-32 Package

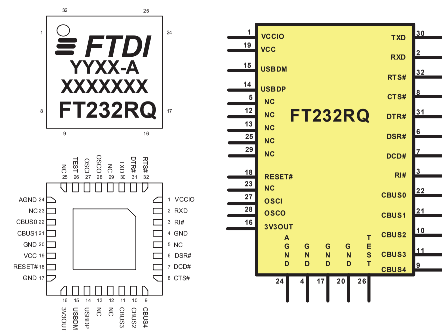


Figure 3.2 QFN-32 Package Pin Out and schematic symbol

3.4 QFN-32 Package Signal Description

Pin No.	Name	Type	Description
14	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to +3.3V.
15	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.

Table 3.5 USB Interface Group

Pin No.	Name	Type	Description
1	VCCIO	PWR	+1.8V to +5.25V supply for the UART Interface and CBUS group pins (2, 3, 6,7,8,9,10 11, 21, 22, 30,31,32). In USB bus powered designs connect this pin to 3V3OUT to drive out at +3.3V levels, or connect to VCC to drive out at +5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
4, 17, 20	GND	PWR	Device ground supply pins.

Pin No.	Name	Type	Description
16	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The purpose of this output is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
19	VCC	PWR	+3.3V to +5.25V supply to the device core. (See Note 1).
24	AGND	PWR	Device analogue ground supply for internal clock multiplier.

Table 3.6 Power and Ground Group

Pin No.	Name	Type	Description
5, 12, 13, 23, 25, 29	NC	NC	No internal connection. Do not connect.
18	RESET#	Input	Active low reset. Can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCC.
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation. (See Note 2).
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used. (See Note 2).

Table 3.7 Miscellaneous Signal Group

Pin No.	Name	Type	Description
30	TXD	Output	Transmit Asynchronous Data Output.
31	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
32	RTS#	Output	Request to Send Control Output / Handshake Signal.
2	RXD	Input	Receiving Asynchronous Data Input.
3	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend.
6	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
7	DCD#	Input	Data Carrier Detect Control Input.
8	CTS#	Input	Clear To Send Control Input / Handshake Signal.
9	CBUS4	I/O	Configurable CBUS output only Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 3.9.
10	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 3.9.

Pin No.	Name	Type	Description
11	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 3.9. PWREN# should be used with a 10kΩ resistor pull up.
21	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 3.9.
22	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 3.9.

Table 3.8 UART Interface and CBUS Group (see note 3)

Notes:

1. The minimum operating voltage VCC must be +4.0V (could use VBUS=+5V) when using the internal clock generator. Operation at +3.3V is possible using an external crystal oscillator.
2. For details on how to use an external crystal, ceramic resonator, or oscillator with the FT232R, please refer to Section 7.6.
3. When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

3.5 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. CBUS signal options are common to both package versions of the FT232R. These options can be configured in the internal EEPROM using the software utility FT_PPROG or MPROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 8.

CBUS Signal Option	Available On CBUS Pin	Description
TXDEN	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Enable transmit data for RS485
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*
TXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Transmit data LED drive: Data from USB Host to FT232R. Pulses low when transmitting data via USB. See Section 7.5 for more details.
RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Receive data LED drive: Data from FT232R to USB Host. Pulses low when receiving data via USB. See Section 7.5 for more details.
TX&RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	LED drive – pulses low when transmitting or receiving data via USB. See Section 7.5 for more details.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK48	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	48MHz ±0.7% Clock output. **
CLK24	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	24 MHz Clock output.**
CLK12	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	12 MHz Clock output.**
CLK6	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	6 MHz ±0.7% Clock output. **
CBitBangI/O	CBUS0, CBUS1, CBUS2, CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal EEPROM. A separate application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BitBangWRn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBangRDn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.

Table 3.9 CBUS Configuration Control

* PWREN# must be used with a 10kΩ resistor pull up.

**When in USB suspend mode the outputs clocks are also suspended.

4 Function Description

The FT232R is a USB to serial UART interface device which simplifies USB to serial designs and reduces external component count by fully integrating an external EEPROM, USB termination resistors and an integrated clock circuit which requires no external crystal, into the device. It has been designed to operate efficiently with a USB host controller by using as little as possible of the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated EEPROM, USB termination resistors, clock generation, AVCC filtering, POR and LDO regulator.

Configurable CBUS I/O Pin Options. The fully integrated EEPROM allows configuration of the Control Bus (CBUS) functionality, signal inversion and drive strength selection. There are 5 configurable CBUS I/O pins. These configurable options are

1. **TXDEN** - transmit enable for RS485 designs.
2. **PWREN#** - Power control for high power, bus powered designs.
3. **TXLED#** - for pulsing an LED upon transmission of data.
4. **RXLED#** - for pulsing an LED upon receiving data.
5. **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data.
6. **SLEEP#** - indicates that the device going into USB suspend mode.
7. **CLK48 / CLK24 / CLK12 / CLK6** - 48MHz, 24MHz, 12MHz, and 6MHz clock output signal options.

The CBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins which are available during normal operation. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

The CBUS lines can be configured with any one of these output options by setting bits in the internal EEPROM. The device is supplied with the most commonly used pin definitions pre-programmed - see Section 8 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strobes. The FT232R supports FTDI's previous chip generation bit-bang mode. In bit-bang mode, the eight UART lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scaler). With the FT232R device this mode has been enhanced by outputting the internal RD# and WR# strobes signals which can be used to allow external logic to be clocked by accesses to the bit-bang I/O bus. This option will be described more fully in a separate application note available from FTDI website (www.ftdichip.com).

Synchronous Bit Bang Mode. The FT232R supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

FTDIChip-ID™. The FT232R also includes the new FTDIChip-ID™ security dongle feature. This FTDIChip-ID™ feature allows a unique number to be burnt into each device during manufacture. This number cannot be reprogrammed. This number is only readable over USB and forms a basis of a security dongle which can be used to protect any customer application software being copied. This allows the possibility of using the FT232R in a dongle for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT232R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note, AN232R-02, available from FTDI website (www.ftdichip.com) describes this feature.

The FT232R is capable of operating at a voltage supply between +3.3V and +5V with a nominal operational mode current of 15mA and a nominal USB suspend mode current of 70µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the UART interface allows the FT232R to interface to UART logic running at +1.8V, 2.5V, +3.3V or +5V.

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT232R. Please refer to the block diagram shown in Figure 2.1

Internal EEPROM. The internal EEPROM in the FT232R is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The internal EEPROM is also used to configure the CBUS pin functions. The FT232R is supplied with the internal EEPROM pre-programmed as described in Section 8. A user area of the internal EEPROM is available to system designers to allow storing additional data. The internal EEPROM descriptors can be programmed in circuit, over USB without any additional voltage requirement. It can be programmed using the FTDI utility software called MPROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com).

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates the internal USB series termination resistors on the USB data lines and a 1.5kΩ pull up resistor on USBDP.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz, 24MHz, 12MHz and 6MHz reference clock signals. The 48Mz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the UART in accordance with the USB 2.0 specification chapter 9.

FIFO RX Buffer (128 bytes). Data sent from the USB host controller to the UART via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer. Data is removed from the buffer to the UART transmit register under control of the UART FIFO controller. (Rx relative to the USB interface).

FIFO TX Buffer (256 bytes). Data from the UART receive register is stored in the TX buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

UART FIFO Controller. The UART FIFO controller handles the transfer of data between the FIFO RX and TX buffers and the UART transmit and receive registers.

UART Controller with Programmable Signal Inversion and High Drive. Together with the UART FIFO Controller the UART Controller handles the transfer of data between the FIFO RX and FIFO TX buffers and the UART transmit and receive registers. It performs asynchronous 7 or 8 bit parallel to serial and serial to parallel conversion of the data on the RS232 (or RS422 or RS485) interface.

Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. The UART Controller also provides a transmitter enable control signal pin option (TXDEN) to assist with interfacing to RS485 transceivers. RTS/CTS, DSR/DTR and XON / XOFF handshaking options are also supported. Handshaking is handled in hardware to ensure fast response times. The UART interface also supports the RS232 BREAK setting and detection conditions.

Additionally, the UART signals can each be individually inverted and have a configurable high drive strength capability. Both these features are configurable in the EEPROM.

Baud Rate Generator - The Baud Rate Generator provides a 16x clock input to the UART Controller from the 48MHz reference clock. It consists of a 14 bit pre-scaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction or "sub-integer"). This determines the baud rate of the UART, which is programmable from 183 baud to 3 Mbaud.

The FT232R supports all standard baud rates and non-standard baud rates from 183 Baud up to 3 Mbaud. Achievable non-standard baud rates are calculated as follows -

Baud Rate = 3000000 / (n + x)

where 'n' can be any integer between 2 and 16,384 (= 2^{14}) and 'x' can be a sub-integer of the value 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, x = 0, i.e. baud rate divisors with values between 1 and 2 are not possible.

This gives achievable baud rates in the range 183.1 baud to 3,000,000 baud. When a non-standard baud rate is required simply pass the required baud rate value to the driver as normal, and the FTDI driver will calculate the required divisor, and set the baud rate. See FTDI application note AN232B-05 on the FTDI website (www.ftdichip.com) for more details.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT232R.

RESET# can be tied to VCC or left unconnected if not being used.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT232R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT232RL	11162037	hours
MTTF FT232RQ	4464815	hours
VCC Supply Voltage	-0.5 to +6.00	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.8	V
DC Input Voltage – High Impedance Bidirectionals	-0.5 to + (VCC +0.5)	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCC +0.5)	V
DC Output Current – Outputs	24	mA
DC Output Current – Low Impedance Bidirectionals	24	mA
Power Dissipation (VCC = 5.25V)	500	mW

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCC Operating Supply Voltage	4.0	---	5.25	V	Using Internal Oscillator
VCC1	VCC Operating Supply Voltage	3.3	---	5.25	V	Using External Crystal
VCC2	VCCIO Operating Supply Voltage	1.8	---	5.25	V	
Icc1	Operating Supply Current	---	15	---	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	μA	USB Suspend
3V3	3.3v regulator output	3.0	3.3	3.6	V	

Table 5.2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.3 UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.4 UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.5 UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.32	1.62	1.8	V	I source = 0.2mA
Vol	Output Voltage Low	0.06	0.1	0.18	V	I sink = 0.5mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.6 UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.7 UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.8 UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.9 UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.35	1.67	1.8	V	I source = 0.4mA
Vol	Output Voltage Low	0.12	0.18	0.35	V	I sink = 3mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.10 UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, High Drive Level)

** Only input pins have an internal 200KΩ pull-up resistor to VCCIO

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 5.11 RESET# and TEST Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15KΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15KΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	See Note 1

Table 5.12 USB I/O Pin (USBDP, USBDM) Characteristics

5.3 EEPROM Reliability Characteristics

The internal 1024 Bit EEPROM has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Read / Write Cycle	10,000	Cycles

Table 5.13 EEPROM Characteristics

5.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 5.14 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	

Table 5.15 OSCI, OSCO Pin Characteristics – see Note 1

Note1: When supplied, the FT232R is configured to use its internal clock oscillator. These characteristics only apply when an external oscillator or crystal is used.

6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT232R. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT232RL and FT232RQ package options.

All USB power configurations illustrated apply to both package options for the FT232R device. Please refer to Section 3 for the package option pin-out and signal descriptions.

6.1 USB Bus Powered Configuration

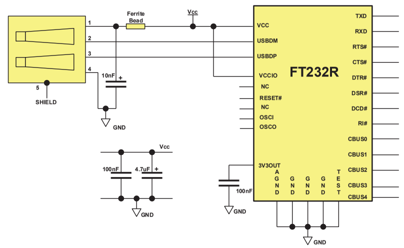


Figure 6.1 Bus Powered Configuration

Figure 6.1 Illustrates the FT232R in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus power devices are as follows –

i) On plug-in to USB, the device should draw no more current than 100mA.
ii) In USB Suspend mode the device should draw no more than 2.5mA.
iii) A bus powered high power USB device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
iv) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
v) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal EEPROM of the FT232R should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT232R and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Steward (www.steward.com), for example Steward Part # MI0805K400R-10.

Note: If using PWREN# (available using the CBUS) the pin should be pulled to VCCIO using a 10kΩ resistor.

6.2 Self Powered Configuration

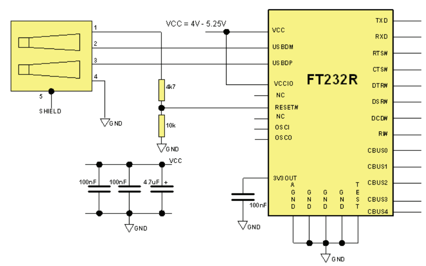


Figure 6.2 Self Powered Configuration

Figure 6.2 illustrates the FT232R in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

i) A self powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self powered device can be used with any USB host, a bus powered USB hub or a self powered USB hub.

The power descriptor in the internal EEPROM of the FT232R should be programmed to a value of zero (self powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the RESET# pin of the FT232R device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V (generated using the 4K7 and 10k resistor network), thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, RESET# will be low and the FT232R is held in reset. Since RESET# is low, the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 6.2 illustrates a self powered design which has a +4V to +5.25V supply.

Note:

1. When the FT232R is in reset, the UART interface I/O pins are tri-stated. Input pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.
2. When using internal FT232R oscillator the VCC supply voltage range must be +4.0V to 5.25V.
3. When using external oscillator the VCC supply voltage range must be +3.3V to 5.25V
Any design which interfaces to +3.3 V or +1.8V would be having a +3.3V or +1.8V supply to VCCIO.

6.3 USB Bus Powered with Power Switching Configuration

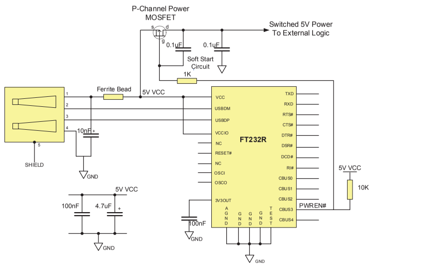


Figure 6.3 Bus Powered with Power Switching Configuration

A requirement of USB bus powered applications, is when in USB suspend mode, the application draws a total current of less than 2.5mA. This requirement includes external logic. Some external logic has the ability to power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT232R provides a simple but effective method of turning off power during the USB suspend mode.

Figure 6.3 shows an example of using a discrete P-Channel MOSFET to control the power to external logic. A suitable device to do this is an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1μF capacitor is used to limit the current surge when the MOSFET turns on. Without the soft start circuit it is possible that the transient power surge, caused when the MOSFET switches on, will reset the FT232R or the USB host/hub controller. The soft start circuit example shown in Figure 6.3 powers up with a slew rate of approximaely12.5V/ms. Thus supply voltage to external logic transitions from GND to +5V in approximately 400 microseconds.

As an alternative to the MOSFET, a dedicated power switch IC with inbuilt "soft-start" can be used. A suitable power switch IC for such an application is the Micrel (www.micrel.com) MIC2025-2BM or equivalent.

With power switching controlled designs the following should be noted:

i) The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.

ii) Set the Pull-down on Suspend option in the internal FT232R EEPROM.

iii) One of the CBUS Pins should be configured as PWREN# in the internal FT232R EEPROM, and used to switch the power supply to the external circuitry. This should be pulled high through a 10 kΩ resistor.

iv) For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FT232R EEPROM. A high-power bus powered application uses the descriptor in the internal FT232R EEPROM to inform the system of its power requirements.

v) PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

6.4 USB Bus Powered with Selectable External Logic Supply

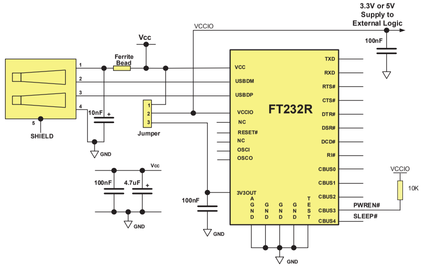


Figure 6.4 USB Bus Powered with +3.3V or +5V External Logic Power Supply

Figure 6.4 illustrates a USB bus power application with selectable external logic supply. The external logic can be selected between +3.3V and +5V using the jumper switch. This jumper is used to allow the FT232R to be interfaced with a +3.3V or +5V logic devices. The VCCIO pin is either supplied with +5V from the USB bus (jumper pins1 and 2 connected), or from the +3.3V output from the FT232R 3V3OUT pin (jumper pins 2 and 3 connected). The supply to VCCIO is also used to supply external logic.

With bus powered applications, the following should be noted:

i) To comply with the 2.5mA current supply limit during USB suspend mode, PWREN# or SLEEP# signals should be used to power down external logic in this mode. If this is not possible, use the configuration shown in Section 6.3.

ii) The maximum current sourced from the USB bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 6.3) should be used.

Another possible configuration could use a discrete low dropout (LDO) regulator which is supplied by the 5V on the USB bus to supply between +1.8V and +2.8V to the VCCIO pin and to the external logic. In this case VCC would be supplied with the +5V from the USB bus and the VCCIO would be supplied from the output of the LDO regulator. This results in the FT232R I/O pins driving out at between +1.8V and +2.8V logic levels.

For a USB bus powered application, it is important to consider the following when selecting the regulator:

i) The regulator must be capable of sustaining its output voltage with an input voltage of +4.35V. An Low Drop Out (LDO) regulator should be selected.

ii) The quiescent current of the regulator must be low enough to meet the total current requirement of <= 2.5mA during USB suspend mode.

A suitable series of LDO regulators that meets these requirements is the MicroChip/Telcom (www.microchip.com) TC55 series of devices. These devices can supply up to 250mA current and have a quiescent current of under 1μA.

7 Application Examples

The following sections illustrate possible applications of the FT232R. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT232RL and FT232RQ package options.

7.1 USB to RS232 Converter

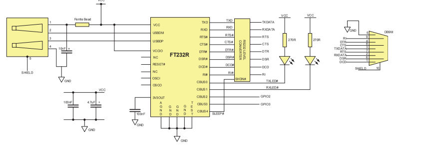


Figure 7.1 Application Example showing USB to RS232 Converter

An example of using the FT232R as a USB to RS232 converter is illustrated in Figure 7.1. In this application, a TTL to RS232 Level Converter IC is used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS232 levels. This level shift can be done using the popular "213" series of TTL to RS232 level converters. These "213" devices typically have 4 transmitters and 5 receivers in a 28-LD SSOP package and feature an in-built voltage converter to convert the +5V (nominal) VCC to the +/- 9 volts required by RS232. A useful feature of these devices is the SHDN# pin which can be used to power down the device to a low quiescent current during USB suspend mode.

A suitable level shifting device is the Sipex SP213EHCA which is capable of RS232 communication at up to 500k baud. If a lower baud rate is acceptable, then several pin compatible alternatives are available such as the Sipex SP213ECA, the Maxim MAX213CAI and the Analogue Devices ADM213E, which are all suitable for communication at up to 115.2k baud. If a higher baud rate is required, the Maxim MAX3245CAI device is capable of RS232 communication rates up to 1Mbaud. Note that the MAX3245 is not pin compatible with the 213 series devices and that the SHDN pin on the MAX device is active high and should be connect to PWREN# pin instead of SLEEP# pin.

In example shown, the CBUS0 and CBUS1 have been configured as TXLED# and RXLED# and are being used to drive two LEDs.

7.2 USB to RS485 Coverter

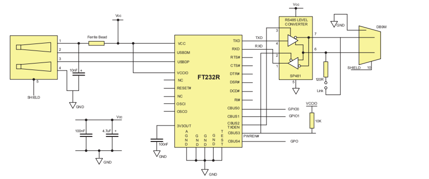


Figure 7.2 Application Example Showing USB to RS485 Converter

An example of using the FT232R as a USB to RS485 converter is shown in Figure 7.2. In this application, a TTL to RS485 level converter IC is used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS485 levels.

This example uses the Sipex SP481 device. Equivalent devices are available from Maxim and Analogue Devices. The SP481 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN signal CBUS pin option on the FT232R is provided for exactly this purpose and so the transmitter enable is wired to CBUS2 which has been configured as TXDEN. Similarly, CBUS3 has been configured as PWREN#. This signal is used to control the SP481's receiver enable. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode. CBUS2 = TXDEN and CBUS3 = PWREN# are the default device configurations of the FT232R pins.

RS485 is a multi-drop network; so many devices can communicate with each other over a two wire cable interface. The RS485 cable requires to be terminated at each end of the cable. A link (which provides the 120Ω termination) allows the cable to be terminated if the SP481 is physically positioned at either end of the cable.

In this example the data transmitted by the FT232R is also present on the receive path of the SP481.This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT232R it is possible to do this entirely in hardware by modifying the example shown in Figure 7.2 by logically OR'ing the FT232R TXDEN and the SP481 receiver output and connecting the output of the OR gate to the RXD of the FT232R.

Note that the TXDEN is activated 1 bit period before the start bit. TXDEN is deactivated at the same time as the stop bit. This is not configurable.

7.3 USB to RS422 Converter

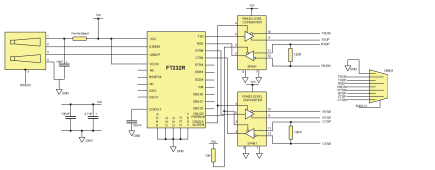


Figure 7.3 USB to RS422 Converter Configuration

An example of using the FT232R as a USB to RS422 converter is shown in Figure 7.3. In this application, two TTL to RS422 Level Converter ICs are used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS422 levels. There are many suitable level converter devices available. This example uses Sipex SP491 devices which have enables on both the transmitter and receiver. Since the SP491 transmitter enable is active high, it is connected to a CBUS pin in SLEEP# configuration. The SP491 receiver enable is active low and is therefore connected to a CBUS pin PWREN# configuration. This ensures that when both the SP491 transmitters and receivers are enabled then the device is active, and when the device is in USB suspend mode, the SP491 transmitters and receivers are disabled. If a similar application is used, but the design is USB BUS powered, it may be necessary to use a P-Channel logic level MOSFET (controlled by PWREN#) in the VCC line of the SP491 devices to ensure that the USB standby current of 2.5mA is met.

The SP491 is specified to transmit and receive data at a rate of up to 5 Mbaud. In this example the maximum data rate is limited to 3 Mbaud by the FT232R.

7.4 USB to MCU UART Interface

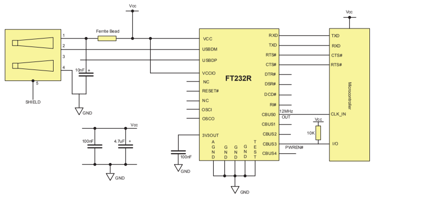


Figure 7.4 USB to MCU UART Interface

An example of using the FT232R as a USB to Microcontroller (MCU) UART interface is shown in Figure 7.4. In this application the FT232R uses TXD and RXD for transmission and reception of data, and RTS# / CTS# signals for hardware handshaking. Also in this example CBUS0 has been configured as a 12MHz output to clock the MCU.

Optionally, RI# could be connected to another I/O pin on the MCU and used to wake up the USB host controller from suspend mode. If the MCU is handling power management functions, then a CBUS pin can be configured as PWREN# and would also be connected to an I/O pin of the MCU.

7.5 LED Interface

Any of the CBUS I/O pins can be configured to drive an LED. The FT232R has 3 configuration options for driving LEDs from the CBUS. These are TXLED#, RXLED#, and TX&RXLED#. Refer to Section 3.5 for configuration options.

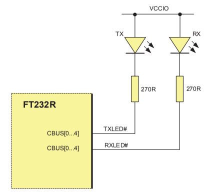


Figure 7.5 Dual LED Configuration

An example of using the FT232R to drive LEDs is shown in Figure 7.5. In this application one of the CBUS pins is used to indicate transmission of data (TXLED#) and another is used to indicate receiving data (RXLED#). When data is being transmitted or received the respective pins will drive from tri-state to low in order to provide indication on the LEDs of data transfer. A digital one-shot is used so that even a small percentage of data transfer is visible to the end user.

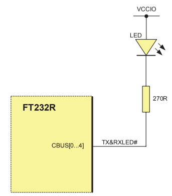


Figure 7.6 Single LED Configuration

Another example of using the FT232R to drive LEDs is shown in Figure 7.6. In this example one of the CBUS pins is used to indicate when data is being transmitted or received by the device (TX&RXLED). In this configuration the FT232R will drive only a single LED.

7.6 Using the External Oscillator

The FT232R defaults to operating using its own internal oscillator. This requires that the device is powered with VCC(min)=+4.0V. This supply voltage can be taken from the USB VBUS. Applications which require using an external oscillator, VCC= +3.3V, must do so in the following order:

1. When device powered for the very first time, it must have VCC > +4.0V. This supply is available from the USB VBUS supply = +5.0V.
2. The EEPROM must then be programmed to enable external oscillator. This EEPROM modification cannot be done using the FTDI programming utility, MPROG. The EEPROM can only be re-configured from a custom application. Please refer to the following applications note on how to do this:

   http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

3. The FT232R can then be powered from VCC=+3.3V and an external oscillator. This can be done using a link to switch the VCC supply.

The FT232R will fail to operate when the internal oscillator has been disabled, but no external oscillator has been connected.

8 Internal EE□RO□ Configuration

Following a power-on reset or a USB reset the FT232R will scan its internal EEPROM and read the USB configuration descriptors stored there. The default factory programmed values of the internal EEPROM are shown in Table □1.

□arameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6001h	FTDI default PID (hex)
Serial Number Enabled□	□es	
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN□ is high).
Manufacturer Name	FTDI	
Product Description	FT232R USB UART	
Max Bus Power Current	□mA	
Power Source	Bus Powered	
Device Type	FT232R	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 □gh Speed device (4□Mb/s).
Remote Wake Up	Enabled	Taking RI□ low will wake up the USB host controller from suspend in approximately 20 ms.
□gh Current I/Os	Disabled	Enables the high drive level on the UART and CBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
CBUS0	TXLED□	Default configuration of CBUS0 – Transmit LED drive.
CBUS1	RXLED□	Default configuration of CBUS1 – Receive LED drive.
CBUS2	TXDEN	Default configuration of CBUS2 – Transmit data enable for RS4□5
CBUS3	PWREN□	Default configuration of CBUS3 – Power enable. Low after USB enumeration, high during USB suspend mode.

□arameter	Value	Notes
CBUS4	SLEEP□	Default configuration of CBUS4 – Low during USB suspend mode.
Invert TXD	Disabled	Signal on this pin becomes TXD□ if enable.
Invert RXD	Disabled	Signal on this pin becomes RXD□ if enable.
Invert RTS□	Disabled	Signal on this pin becomes RTS if enable.
Invert CTS□	Disabled	Signal on this pin becomes CTS if enable.
Invert DTR□	Disabled	Signal on this pin becomes DTR if enable.
Invert DSR□	Disabled	Signal on this pin becomes DSR if enable.
Invert DCD□	Disabled	Signal on this pin becomes DCD if enable.
Invert RI□	Disabled	Signal on this pin becomes RI if enable.

Ta□le 8.1 Default Internal EE□RO□ Configuration

The internal EEPROM in the FT232R can be programmed over USB using the FTDI utility program MPROG. MPROG can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com). Version 2.□a or later is required for the FT232R chip. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI support for this service.

□ □ac□age □arameters

The FT232R is available in two different packages. The FT232RL is the SSOP-2□option and the FT232R□ is the □FN-32 package option. The solder reflow profile for both packages is described in Section □5.

□1 SSO□28 □ac□age Dimensions

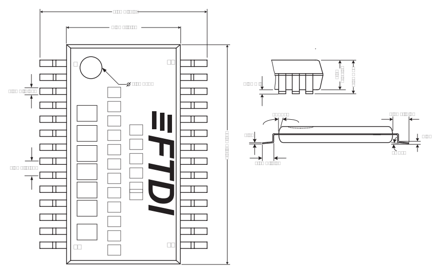


Figure □1 SSO□28 □ac□age Dimensions

The FT232RL is supplied in a Ro□S compliant 2□pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 5.30mm x 10.20mm body (7.□mm x 10.20mm including pins). The pins are on a 0.65 mm pitch. The above mechanical drawing shows the SSOP-2□package.

All dimensions are in millimetres.

The date code format is □□□□where XX = 2 digit week number, □□= 2 digit year number. This is followed by the revision number.

The code □□□□□□□□□□□□is the manufacturing LOT code. This only applies to devices manufactured after April 200□

□2 □FN□32 □ac□age Dimensions

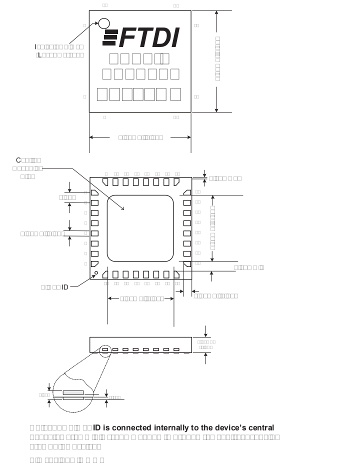


Figure □2 □FN□32 □ac□age Dimensions

The FT232R□ is supplied in a Ro□S compliant leadless □FN-32 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 5.00mm x 5.00mm. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the □FN-32 package. All dimensions are in millimetres.

The centre pad on the base of the FT232R□ is not internally connected, and can be left unconnected, or connected to ground (recommended).

The date code format is □□□□where XX = 2 digit week number, □□= 2 digit year number.

The code □□□□□□□is the manufacturing LOT code. This only applies to devices manufactured after April 200□

□3 □FN□32 □ac□age T□□ical □a□La□out

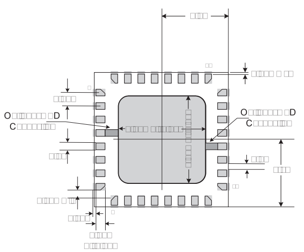


Figure □3 T□□ical □a□La□out for □FN□32 □ac□age

□.□ □FN□32 □ac□age T□□ical Sol□er □aste Diagram

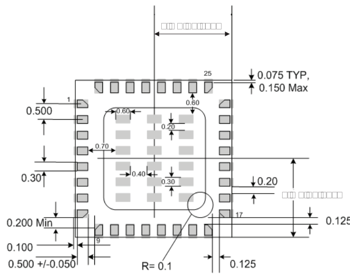


Figure □.□ T□□ical Sol□er □aste Diagram for □FN□32 □ac□age

□5 Sol□er Reflo□ □rofile

The FT232R is supplied in Pb free 2□LD SSOP and □FN-32 packages. The recommended solder reflow profile for both package options is shown in Figure □5.

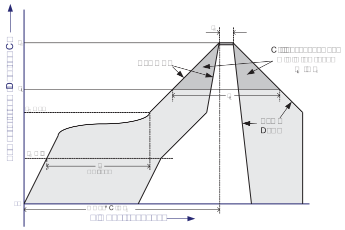


Figure □5 FT232R Sol□er Reflo□ □rofile

The recommended values for the solder reflow profile are detailed in Table □1. Values are shown for both a completely Pb free solder process (i.e. the FT232R is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT232R is used with non-Pb free solder).

□rofile Feature	□□Free Sol□er □rocess	Non□□□Free Sol□er □rocess
Average Ramp Up Rate (T_s to T_p)	3□C / second Max.	3□C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	150□C 200□C 60 to 120 seconds	100□C 150□C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	217□C 60 to 150 seconds	1□3□C 60 to 150 seconds
Peak Temperature (T_p)	260□C	240□C
Time within 5□C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6□C / second Max.	6□C / second Max.
Time for T= 25□C to Peak Temperature, T_p	□minutes Max.	6 minutes Max.

Ta□le □1 Reflo□ □rofile □arameter Values

10 Contact Information

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E-Mail (Support): cn.support□ftdichip.com
E-Mail (General Enquiries): cn.admin1□ftdichip.com

□e□Site URL: htt□□□□□□.ft□chi□.com

Distri□utor an□Sales Re□resentati□es

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

A□□en□ix A – References

Useful A□□lication Notes

http://www.ftdichip.com/Documents/AppNotes/AN232R-01_FT232RBitBangModes.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_107_AdvancedDriverOptions_AN_000073.pdf

http://www.ftdichip.com/Documents/AppNotes/AN232R-02_FT232RChipID.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_121_FTDI_Device_EEPROM_User_Area_Usage.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_120_Aliasing_VCP_Baud_Rates.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

http://www.ftdichip.com/Resources/Utilities/AN_126_User_Guide_For_FT232_Factory□20test□20utility.pdf

http://www.ftdichip.com/Documents/AppNotes/AN232B-05_BaudRates.pdf

http://www.ftdichip.com/Documents/InstallGuides.htm

Appendix B – List of Figures and Tables

List of Figures

List of Tables

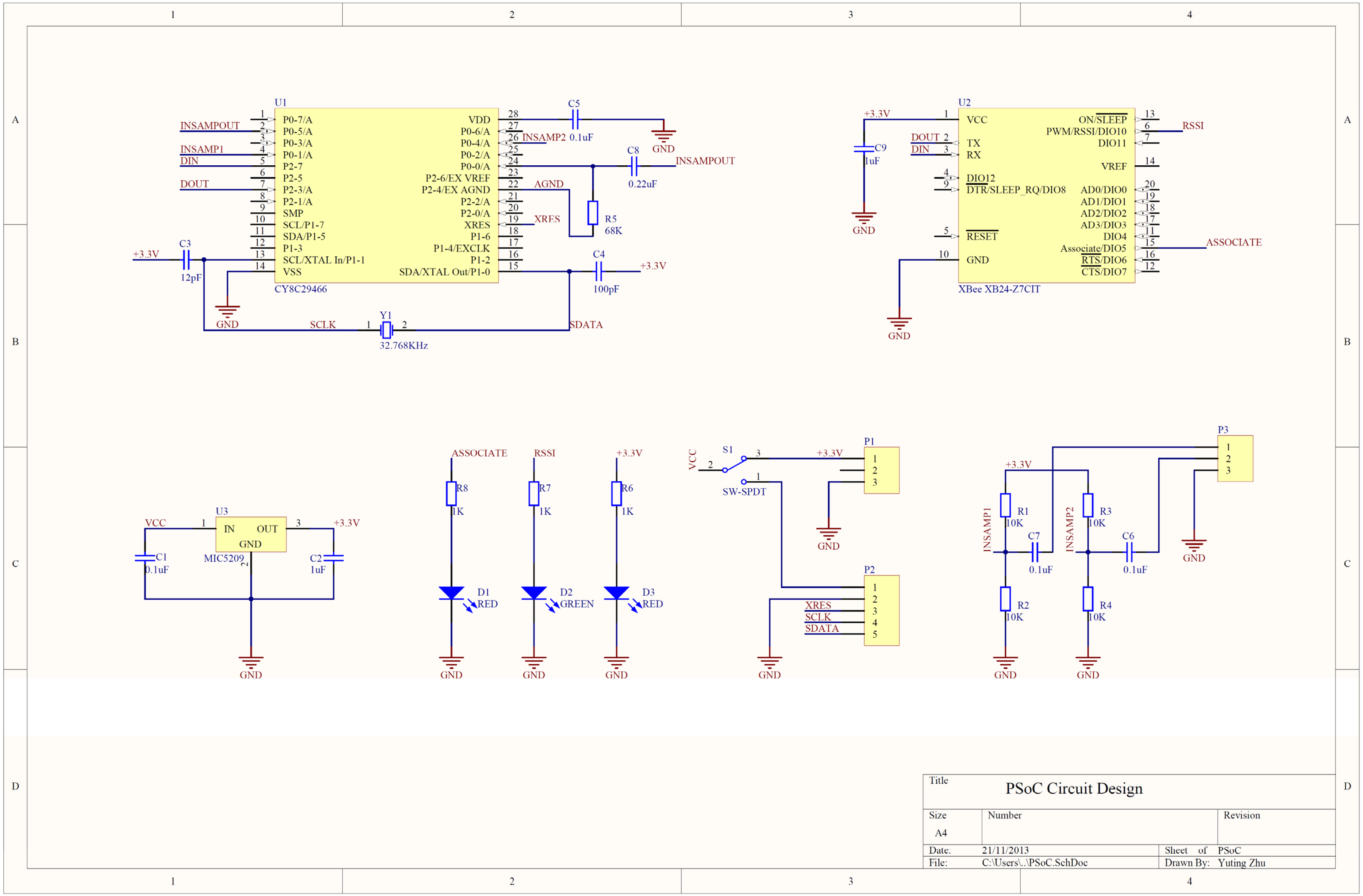
Appendix C – Revision History

Document Title: USB UART IC FT232R
Document Reference No.: FT_000053
Clearance No.: FTDI# 3□
Product Page: http://www.ftdichip.com/FTProducts.htm
Document Feedback: Send Feedback

Version 0.□0	Initial Datasheet Created	August 2005
Version 0.□6	Revised Pre-release datasheet	October 2005
Version 1.00	Full datasheet released	December 2005
Version 1.02	Minor revisions to datasheet	December 2005
Version 1.03	Manufacturer ID added to default EEPROM configuration; Buffer sizes added	January 2006
Version 1.0□	QFN-32 Pad layout and solder paste diagrams added	January 2006
Version 2.00	Reformatted, updated package info, added notes for 3.3V operation;	June 200□
	Part numbers, TID; added UART and CBUS characteristics for +1.□V;	
	Corrected RESET#; Added MTTF data;	
	Corrected the input switching threshold and input hysteresis values for VCCIO=5V	
Version 2.01	Corrected pin-out number in table3.2 for GND pin1□	
	Improved graphics on some Figures.	
	Add packing details. Changed USB suspend current spec from 500uA to 2.5mA	
	Corrected Figure □2 QFN dimensions.	August 200□
Version 2.02	Corrected Tape and Reel quantities.	
	Added comment "PWREN# should be used with a 10kΩ resistor pull up".	
	Replaced TXDEN# with TXDEN since it is active high in various places.	
	Added lot number to the device markings.	
	Added 3V3 regulator output tolerance.	
	Clarified VCC operation and added section headed "Using an external Oscillator"	
	Updated company contact information.	April 200□
Version 2.03	Corrected the RX/TX buffer definitions to be relative to the USB interface	June 200□
Version 2.0□	Additional dimensions added to QFN solder profile	June 200□
Version 2.05	Modified package dimensions to 5.0 x 5.0 +/-0.075mm.	December 200□
	and Solder paste diagram to 2.50 x 2.50 +/-0.0375mm	
	Added Windows 7 32, 64 bit driver support	
	Added FT_PROG utility references	
	Added Appendix A-references.Figure 2.1 updated.	
	Updated USB-IF TID for Rev B	
Version 2.06	Updated section 6.2, Figure 6.2 and the note,	May 2010
	Updated section 5.3, Table 5.13, EEPROM data retention time	
Version 2.07	Added USB Certification Logos	July 2010
Version 2.08	Updated USB-IF TID for Rev C	April 2011
Version 2.0□	Corrected Rev C TID number	April 2011
Version 2.10	Table 3.□ added clock output frequency within □0.7□	March 2012
	Edited Table 3.□ TXLED# and TXLED# Description	
	Added feedback links	

Appendix E:

Circuit Diagram for the WsEMG Electrode Interface Node

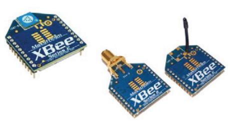

U1
CY8C29466
P0-7/A
P0-5/A
P0-3/A
P0-1/A
P2-7
P2-5
P2-3/A
P2-1/A
SMP
SCL/P1-7
SDA/P1-5
P1-3
SCL/XTAL In/P1-1
VSS
VDD
P0-6/A
P0-4/A
P0-2/A
P0-0/A
P2-6/EX VREF
P2-4/EX AGND
P2-2/A
P2-0/A
XRES
P1-6
P1-4/EXCLK
P1-2
SDA/XTAL Out/P1-0
INSAMPOUT
INSAMP1
DIN
DOUT
INSAMP2
AGND
C5 0.1uF
C8 0.22uF
R5 68K
C3 12pF
C4 100pF
Y1 32.768KHz
SCLK
SDATA
U2
XBee XB24-Z7CIT
VCC
TX
RX
DIO12
DTR/SLEEP_RQ/DIO8
RESET
GND
ON/SLEEP
PWM/RSSI/DIO10
DIO11
VREF
AD0/DIO0
AD1/DIO1
AD2/DIO2
AD3/DIO3
DIO4
Associate/DIO5
RTS/DIO6
CTS/DIO7
RSSI
ASSOCIATE
C9 1uF
U3 MIC5209
IN OUT GND
VCC
C1 0.1uF
C2 1uF
R8 1K
R7 1K
R6 1K
D1 RED
D2 GREEN
D3 RED
S1 SW-SPDT
P1
P2
P3
XRES
SCLK
SDATA
INSAMP1
INSAMP2
R1 10K
R2 10K
R3 10K
R4 10K
C7 0.1uF
C6 0.1uF
+3.3V
GND
Title PSoC Circuit Design
Size A4
Number
Revision
Date: 21/11/2013
File: C:\Users\..\PSoC.SchDoc
Sheet of PSoC
Drawn By: Yuting Zhu

Appendix F:

Datasheet for XBee® Series 2 Module

XBee™ Series 2 OEM RF Modules

XBee Series 2 OEM RF Modules
ZigBee™ Networks
RF Module Operation
RF Module Configuration
Appendices



Product Manual v1.x.1x - *ZigBee* Protocol
For OEM RF Module Part Numbers: XB24-BxIT-00x

ZigBee OEM RF Modules by MaxStream, Inc. - a Digi International brand

Firmware Versions: 1.0xx - Coordinator, Transparent Operation
1.1xx - Coordinator, API Operation
1.2xx - Router, End Device, Transparent Operation
1.3xx - Router, End Device, API Operation

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90000866_A
2007.06.01

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Contents

1. XBee Series 2 OEM RF Modules

The XBee Series 2 OEM RF Modules were engineered to operate within the ZigBee protocol and support the unique needs of low-cost, low-power wireless sensor networks. The modules require minimal power and provide reliable delivery of data between remote devices.

The modules operate within the ISM 2.4 GHz frequency band.

1.1. Key Features

High Performance, Low Cost

- Indoor/Urban: up to 133' (40 m)
- Outdoor line-of-sight: up to 400' (120 m)
- Transmit Power: 2 mW (+3 dBm)
- Receiver Sensitivity: -95 dBm

RF Data Rate: 250,000 bps

Advanced Networking & Security

Retries and Acknowledgements

DSSS (Direct Sequence Spread Spectrum)

Each direct sequence channel has over 65,000 unique network addresses available

Point-to-point, point-to-multipoint and peer-to-peer topologies supported

Self-routing, self-healing and fault-tolerant mesh networking

Low Power

XBee Series 2

- TX Current: 40 mA (@3.3 V)
- RX Current: 40 mA (@3.3 V)
- Power-down Current: < 1 µA @ 25°C

Easy-to-Use

No configuration necessary for out-of box RF communications

AT and API Command Modes for configuring module parameters

Small form factor

Extensive command set

Free X-CTU Software (Testing and configuration software)

Free & Unlimited Technical Support

1.1.1. Worldwide Acceptance

FCC Approval (USA) Refer to Appendix A [p50] for FCC Requirements. Systems that contain XBee Series 2 RF Modules inherit MaxStream Certifications.

ISM (Industrial, Scientific & Medical) **2.4 GHz frequency band**

Manufactured under **ISO 9001:2000** registered standards

XBee Series 2 RF Modules are optimized for use in **US**, **Canada**, **Australia, Israel and Europe** (contact MaxStream for complete list of agency approvals).

1.2. Specifications

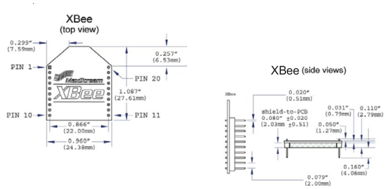
Table 1-01. Specifications of the XBee Series 2 OEM RF Module (PRELIMINARY)

Specification	XBee Series 2
Performance	
Indoor/Urban Range	up to 133 ft. (40 m)
Outdoor RF line-of-sight Range	up to 400 ft. (120 m)
Transmit Power Output (software selectable)	2mW (+3dBm)
RF Data Rate	250,000 bps
Serial Interface Data Rate (software selectable)	1200 - 230400 bps (non-standard baud rates also supported)
Receiver Sensitivity	-95 dBm (1% packet error rate)
Power Requirements	
Supply Voltage	2.8 – 3.4 V
Operating Current (Transmit)	40mA (@ 3.3 V)
Operating Current (Receive)	40mA (@ 3.3 V)
Power-down Current	< 1 uA @ 25°C
General	
Operating Frequency Band	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)
Operating Temperature	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip, RPSMA, or U.FL Connector
Networking & Security	
Supported Network Topologies	Point-to-point, Point-to-multipoint, Peer-to-peer & Mesh
Number of Channels (software selectable)	16 Direct Sequence Channels
Addressing Options	PAN ID and Addresses, Cluster IDs and Endpoints (optional)
Agency Approvals	
United States (FCC Part 15.247)	Pending
Industry Canada (IC)	Pending
Europe (CE)	Pending

Antenna Options: The ranges specified are typical when using the integrated Whip (1.5 dBi) and Dipole (2.1 dBi) antennas. The Chip antenna option provides advantages in its form factor; however, it typically yields shorter range than the Whip and Dipole antenna options when transmitting outdoors. For more information, refer to the "XBee Series 2 Antenna" application note located on MaxStream's web site http://www.maxstream.net/support/knowledgebase/article.php?kb=153

1.3. Mechanical Drawings

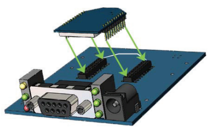
Figure 1-01. Mechanical drawings of the XBee Series 2 OEM RF Modules (antenna options not shown)



1.4. Mounting Considerations

The XBee Series 2 RF Module (through-hole) was designed to mount into a receptacle (socket) and therefore does not require any soldering when mounting it to a board. The XBee Series 2 Development Kits contain RS-232 and USB interface boards which use two 20-pin receptacles to receive modules.

Figure 1-02. XBee Series 2 Module Mounting to an RS-232 Interface Board.



The receptacles used on MaxStream development boards are manufactured by Century Interconnect. Several other manufacturers provide comparable mounting solutions; however, MaxStream currently uses the following receptacles:

- Through-hole single-row receptacles - Samtec P/N: MMS-110-01-L-SV (or equivalent)
- Surface-mount double-row receptacles - Century Interconnect P/N: CPRMSL20-D-0-1 (or equivalent)
- Surface-mount single-row receptacles - Samtec P/N: SMM-110-02-SM-S

MaxStream also recommends printing an outline of the module on the board to indicate the orientation the module should be mounted.

1.5. Pin Signals

Figure 1-03. XBee Series 2 RF Module Pin Number
(top sides shown - shields on bottom)

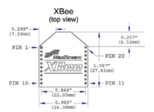


Table 1-02. Pin Assignments for the XBee Series 2 Modules
(Low-asserted signals are distinguished with a horizontal line above signal name.)

Pin #	Name	Direction	Description
1	VCC	-	Power supply
2	DOUT	Output	UART Data Out
3	DIN / CONFIG	Input	UART Data In
4	DIO8	Either	Digital I/O 8
5	RESET	Input	Module Reset (reset pulse must be at least 200 ns)
6	PWM0 / RSSI / DIO10	Output	PWM Output 0 / RX Signal Strength Indicator / Digital IO
7	PWM / DIO11	Either	Digital I/O 11
8	[reserved]	-	Do not connect
9	DTR / SLEEP_RQ/ DI8	Input	Pin Sleep Control Line or Digital Input 8
10	GND	-	Ground
11	DIO4	Either	Digital I/O 4
12	CTS / DIO7	Either	Clear-to-Send Flow Control or Digital I/O 7
13	ON / SLEEP	Output	Module Status Indicator
14	[reserved]	-	Do not connect
15	Associate / DIO5	Either	Associated Indicator, Digital I/O 5
16	RTS / DIO6	Either	Request-to-Send Flow Control, Digital I/O 6
17	AD3 / DIO3	Either	Analog Input 3 or Digital I/O 3
18	AD2 / DIO2	Either	Analog Input 2 or Digital I/O 2
19	AD1 / DIO1	Either	Analog Input 1 or Digital I/O 1
20	AD0 / DIO0	Either	Analog Input 0 or Digital I/O 0

Design Notes:

- Minimum connections: VCC, GND, DOUT & DIN
- Minimum connections to support firmware upgrades: VCC, GND, DIN, DOUT, RTS & DTR
- Signal Direction is specified with respect to the module
- Module includes a 30k Ohm resistor attached to RESET
- Several of the input pull-ups can be configured using the PR command
- Unused pins should be left disconnected

1.6. Electrical Characteristics

Table 1-03. DC Characteristics of the XBee Series 2 (VCC = 2.8 - 3.4 VDC)

Symbol	Parameter	Condition	Min	Typical	Max	Units
VIL	Input Low Voltage	All Digital Inputs	-	-	0.2 * VCC	V
V_{IH}	Input High Voltage	All Digital Inputs	0.8 * VCC	-	0.18* VCC	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, VCC >= 2.7 V	-	-	0.18*VCC	V
V_{OH}	Output High Voltage	I_{OH} = -2 mA, VCC >= 2.7 V	0.82*VCC	-	-	V
II_{IN}	Input Leakage Current	V_{IN} = VCC or GND, all inputs, per pin	-	-	0.5uA	uA
TX	Transmit Current	VCC = 3.3 V	-	45	-	mA
RX	Receive Current	VCC = 3.3 V	-	50	-	mA
PWR-DWN	Power-down Current	SM parameter = 1	-	< 10	-	uA

2. RF Module Operation

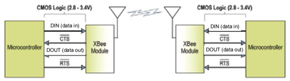
2.1. Serial Communications

The XBee Series 2 OEM RF Modules interface to a host device through a logic-level asynchronous serial port. Through its serial port, the module can communicate with any logic and voltage compatible UART; or through a level translator to any serial device (For example: Through a MaxStream proprietary RS-232 or USB interface board).

2.1.1. UART Data Flow

Devices that have a UART interface can connect directly to the pins of the RF module as shown in the figure below.

Figure 2-01. System Data Flow Diagram in a UART-interfaced environment
(Low-asserted signals distinguished with horizontal line over signal name.)

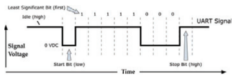


Serial Data

Data enters the module UART through the DIN (pin 3) as an asynchronous serial signal. The signal should idle high when no data is being transmitted.

Each data byte consists of a start bit (low), 8 data bits (least significant bit first) and a stop bit (high). The following figure illustrates the serial bit pattern of data passing through the module.

Figure 2-02. UART data packet 0x1F (decimal number "31") as transmitted through the RF module
Example Data Format is 8-N-1 (bits - parity - # of stop bits)



The module UART performs tasks, such as timing and parity checking, that are needed for data communications. Serial communications depend on the two UARTs to be configured with compatible settings (baud rate, parity, start bits, stop bits, data bits).

2.1.2. Serial Buffers

The XBee Series 2 modules maintain small buffers to collect received serial and RF data. The serial receive buffer collects incoming serial characters and holds them until they can be processed. The serial transmit buffer collects data that is received via the RF link that will be transmitted out the UART.

Serial Receive Buffer

When serial data enters the RF module through the DIN Pin (3 pin), the data is stored in the serial receive buffer until it can be processed.

Hardware Flow Control (CTS). When the serial receive buffer is 17 bytes away from being full, by default, the module de-asserts CTS (high) to signal to the host device to stop sending data [refer to D7 (DIO7 Configuration) parameter]. CTS is re-asserted after the serial receive buffer has 34 bytes of memory available.

Cases in which the serial receive buffer may become full and possibly overflow:

1. If the module is receiving a continuous stream of RF data, any serial data that arrives on the DIN pin is placed in the serial receive buffer. The data in the serial receive buffer will be transmitted over-the-air when the module is no longer receiving RF data in the network.
2. When data is ready to be transmitted, the module may need to discover a Network Address and/or a Route in order to reach the destination node. Discovery overhead may delay packet transmission.
   Refer to the ZigBee Networks --> Mesh Routing sections for more information.

Serial Transmit Buffer

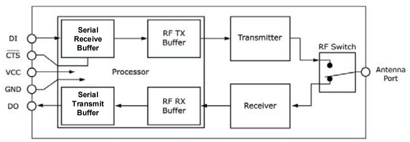
When RF data is received, the data is moved into the serial transmit buffer and is sent out the serial port. If the serial transmit buffer becomes full enough such that all data in a received RF packet won't fit in the serial transmit buffer, the entire RF data packet is dropped.

Hardware Flow Control (RTS). If RTS is enabled for flow control (D6 (DIO6 Configuration) Parameter = 1), data will not be sent out the serial transmit buffer as long as RTS (pin 16) is de-asserted.

Cases in which the serial transmit buffer may become full resulting in dropped RF packets

1. If the RF data rate is set higher than the interface data rate of the module, the module could receive data faster than it can send the data to the host.
2. If the host does not allow the module to transmit data out from the serial transmit buffer because of being held off by hardware flow control.

Figure 2-03. Internal Data Flow Diagram



2.1.3. Transparent Operation

RF modules that contain the following firmware versions will support Transparent Mode: 1.0xx (coordinator) and 1.2xx (router/end device).

When operating in Transparent Mode, modules are configured using AT Commands and API operation is not supported. The modules act as a serial line replacement - all UART data received through the DIN pin is queued up for RF transmission. Data is sent to a module as defined by the DH (Destination Address High) and DL (Destination Address Low) parameters.

When RF data is received by a module, the data is sent out the DOUT pin.

Serial-to-RF Packetization

Data is buffered in the serial receive buffer until one of the following causes the data to be packetized and transmitted:

1. No serial characters are received for the amount of time determined by the RO (Packetization Timeout) parameter. If RO = 0, packetization begins when a character is received.
2. Maximum number of characters that will fit (72) in an RF packet is received.
3. The Command Mode Sequence (GT + CC + GT) is received. Any character buffered in the serial receive buffer before the sequence is transmitted.

2.1.4. API Operation

API (Application Programming Interface) Operation is an alternative to the default Transparent Operation. The frame-based API extends the level to which a host application can interact with the networking capabilities of the module. RF modules that contain the following firmware versions will support API operation: 1.1xx (coordinator) and 1.3xx (router/end device).

When in API mode, all data entering and leaving the module is contained in frames that define operations or events within the module.

Transmit Data Frames (received through the DIN pin (pin 3)) include:

- RF Transmit Data Frame
- Command Frame (equivalent to AT commands)

Receive Data Frames (sent out the DOUT pin (pin 2)) include:

- RF-received data frame
- Command response
- Event notifications such as reset, associate, disassociate, etc.

The API provides alternative means of configuring modules and routing data at the host application layer. A host application can send data frames to the module that contain address and payload information instead of using command mode to modify addresses. The module will send data frames to the application containing status packets; as well as source, and payload information from received data packets.

The API operation option facilitates many operations such as the examples cited below:

-> Transmitting data to multiple destinations without entering Command Mode
-> Receive success/failure status of each transmitted RF packet
-> Identify the source address of each received packet

To implement API operations, refer to the API Operation chapter 6.

2.2. Modes of Operation

2.2.1. Idle Mode

When not receiving or transmitting data, the RF module is in Idle Mode. During Idle Mode, the RF module is also checking for valid RF data. The module shifts into the other modes of operation under the following conditions:

- Transmit Mode (Serial data in the serial receive buffer is ready to be packetized)
- Receive Mode (Valid RF data is received through the antenna)
- Sleep Mode (End Devices only)
- Command Mode (Command Mode Sequence is issued)

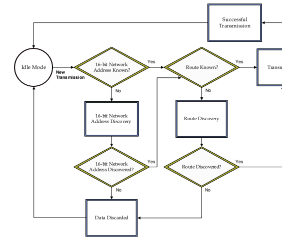
2.2.2. Transmit Mode

When serial data is received and is ready for packetization, the RF module will exit Idle Mode and attempt to transmit the data. The destination address determines which node(s) will receive the data.

Prior to transmitting the data, the module ensures that a 16-bit Network Address and route to the destination node have been established.

If the 16-bit Network Address is not known, Network Address Discovery will take place. If a route is not known, route discovery will take place for the purpose of establishing a route to the destination node. If a module with a matching Network Address is not discovered, the packet is discarded. The data will be transmitted once a route is established. If route discovery fails to establish a route, the packet will be discarded.

Figure 2-04. Transmit Mode Sequence



When data is transmitted from one node to another, a network-level acknowledgement is transmitted back across the established route to the source node. This acknowledgement packet indicates to the source node that the data packet was received by the destination node. If a network acknowledgement is not received, the source node will re-transmit the data. See Data Transmission and Routing in chapter 3 for more information.

2.2.3. Receive Mode

If a valid RF packet is received and its address matches the RF module's MY (16-bit Source Address) parameter, the data is transferred to the serial transmit buffer.

2.2.4. Command Mode

To modify or read RF Module parameters, the module must first enter into Command Mode - a state in which incoming serial characters are interpreted as commands. Refer to the API Mode section for an alternate means of configuring modules.

AT Command Mode

To Enter AT Command Mode:

Send the 3-character command sequence "+++" and observe guard times before and after the command characters. [Refer to the "Default AT Command Mode Sequence" below.]

Default AT Command Mode Sequence (for transition to Command Mode):

- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]
- Input three plus characters ("+++") within one second [CC (Command Sequence Character) parameter = 0x2B.]
- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]

All of the parameter values in the sequence can be modified to reflect user preferences.

NOTE: Failure to enter AT Command Mode is most commonly due to baud rate mismatch. Ensure the 'Baud' setting on the "PC Settings" tab matches the interface data rate of the RF module. By default, the BD parameter = 3 (9600 bps).

To Send AT Commands:

Send AT commands and parameters using the syntax shown below.

Figure 2-05. Syntax for sending AT Commands

"AT" Prefix + **ASCII Command** + **Space** (Optional) + **Parameter** (Optional, HEX) + **Carriage Return**

Example: ATDL 1F<CR>

To read a parameter value stored in the RF module's register, omit the parameter field.

The preceding example would change the RF module Destination Address (Low) to "0x1F". To store the new value to non-volatile (long term) memory, subsequently send the WR (Write) command.

For modified parameter values to persist in the module's registry after a reset, changes must be saved to non-volatile memory using the WR (Write) Command. Otherwise, parameters are restored to previously saved values after the module is reset.

System Response. When a command is sent to the module, the module will parse and execute the command. Upon successful execution of a command, the module returns an "OK" message. If execution of a command results in an error, the module returns an "ERROR" message.

To Exit AT Command Mode:

1. Send the ATCN (Exit Command Mode) command (followed by a carriage return).
   [OR]
2. If no valid AT Commands are received within the time specified by CT (Command Mode Timeout) Command, the RF module automatically returns to Idle Mode.

For an example of programming the RF module using AT Commands and descriptions of each configurable parameter, refer to the "RF Module Configuration" chapter.

2.2.5. Sleep Mode

Sleep modes are supported on end devices only. Router and coordinator devices participate in routing data packets and are intended to be mains powered. End devices must be joined to a parent (router or coordinator) before they can participate on a ZigBee network. The parent device does not track when an end device is awake or asleep. Instead, the end device must inform the parent when it is able to receive data. The parent must be able to buffer incoming data packets destined for the end device until the end device can awake and receive the data. When an end device is able to receive data, it sends a poll command to the parent. When the parent router or coordinator receives the poll command, it will transmit any buffered data packets for the end device. Routers and coordinators are capable of buffering one broadcast transmission for sleeping end device children.

The SM, ST, SP, and SN commands are used to configure sleep mode operation.

Data Management

The SP command on the parent determines how long the parent will buffer a packet. It should be set to match the maximum SP value on any end device that may join to it. SP can be set up to 28 seconds (0xAF0).

End Device Sleep Modes

Pin Sleep

Setting SM=1 or SM=2 configures a device as a pin-sleep enabled end device. When operating in this mode, an end device monitors the Sleep_Request pin for a high state. When Sleep_Request goes high, the module enters sleep mode once any pending transmissions have finished. The module remains in a low power state until the Sleep_Request pin goes low.

When the module wakes from pin sleep, it sends a poll request to the parent to see if any data is pending for the end device. Since routers and coordinators can only buffer data up to 30 seconds, end devices should not remain in pin sleep longer than about 28 seconds if incoming data packets must be received. Using pin sleep for more than 28 seconds is recommended only if incoming data packets are not expected.

When the module wakes from a pin sleep mode, the CTS line goes low, and On/Sleep goes high.

Cyclic Sleep

Cyclic sleep allows the end device to sleep for a specified period of time. The period of time is specified by SP. Since routers and coordinators can only buffer data packets for up to 30 seconds, SP on end devices can be set up to 28 seconds (0xAF0). The module will wake after SP time and send a poll request to the parent to check for data. If any serial or RF data is received, the ST time is restarted. Once ST time has expired with no serial or RF activity, the end device will resume cyclic sleep operation.

When the module wakes, CTS goes low allowing the application to send serial data to the module if necessary. The On/Sleep indicator will be set high to alert the application that the end device has awakened. If serial or RF data is received, the ST timer will be reset, otherwise, the end device will resume low power operation.

Off board peripherals may wish to sleep longer than the maximum SP time of the end device. The SN command can be used to not wake off board peripherals for longer than SP time.

For example, if SP=28 seconds, and SN=5, the end device will wake up every 28 seconds and poll the parent for data. If no data is pending, the end device will return to sleep. In this example, if the parent has no data for the end device, On/Sleep will go high after 140 seconds, assuming the parent never has data for the end device. If the parent has data for the end device, On/Sleep will go high and the SN counter will reset.

3. ZigBee Networks

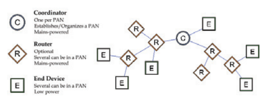
3.1. ZigBee Network Formation

A ZigBee Personal Area Network (PAN) consists of one coordinator and one or more routers and/or end devices. A ZigBee Personal Area Network (PAN) is created when a coordinator selects a channel and PAN ID to start on. Once the coordinator has started a PAN, it can allow router and end device nodes to join the PAN.

When a router or end device joins a PAN, it receives a 16-bit network address and can transmit data to or receive data from other devices in the PAN. Routers and the coordinator can allow other devices to join the PAN, and can assist in sending data through the network to ensure data is routed correctly to the intended recipient device. When a router or coordinator allows an end device to join the PAN, the end device that joined becomes a child of the router or coordinator that allowed the join.

End devices, however can transmit or receive data but cannot route data from one node to another, nor can they allow devices to join the PAN. End devices must always communicate directly to the parent they joined to. The parent router or coordinator can route data on behalf of an end device child to ensure it reaches the correct destination. End devices are intended to be battery powered and can support low power modes.

Figure 3-01. Node Types / Sample of a Basic ZigBee Network Topology



The network address of the PAN coordinator is always 0. When a router joins a PAN, it can also allow other routers and end devices to join to it. Joining establishes a parent/child relationship between two nodes. The node that allowed the join is the parent, and the node that joined is the child. The parent/child relationship is not necessary for routing data.

3.1.1. Starting a ZigBee Coordinator

When a coordinator first comes up, it performs an energy scan on mulitple channels (frequencies) to select an unused channel to start the PAN. After removing channels with high detected energy levels, the coordinator issues an 802.15.4 beacon request command on the remaining, low energy level channels. Any routers or coordinators respond to the beacon request frame with a small beacon transmission that indicates the PAN identifier (PAN ID) that they are operating on, and whether or not they are allowing joining.The coordinator will attempt to start on an unused PAN ID and channel. After starting, the coordinator may allow other devices to join its PAN.

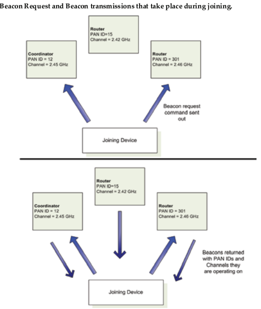
3.1.2. Joining a Router

When a router first comes up, it must locate and join a ZigBee PAN. To do this, it issues an 802.15.4 beacon request command on multiple channels to locate nearby PANs. Nearby routers and coordinators respond to the beacon request frame with a small beacon transmission, indicating which channel and PAN ID they are operating on. The router listens on each channel for these beacon frames, and determines which device it should join. If a valid PAN is found from one of the received beacons, the router issues a join request to the device that sent the beacon. If joining succeeds, the router will then receive a join confirmation from the device, indicating the join was successful. Once the router joins the PAN, it can communicate with other devices on the PAN and allow new devices to join to it.

3.1.3. Joining an End Device

When an end device first comes up, it must also locate and join a PAN. End devices follow the same process as a router to join a PAN. Once the end device has successfully joined a PAN, it can communicate with other devices on the PAN. However, since end devices cannot route data, it must always communicate directly with its parent and allow the parent to route data in its behalf.

Figure 3-02. Demonstration of Beacon Request and Beacon transmissions that take place during joining.



3.2. ZigBee Network Communications

Zigbee supports device addressing and application layer addressing. Device addressing specifies the destination address of the device a packet is destined to. Application layer addressing indicates a particular application recipient, known as a Zigbee endpoint, along with message type fields called cluster IDs.

3.2.1. ZigBee Device Addressing

The 802.15.4 protocol upon which the ZigBee protocol is built specifies two address types:

- 16-bit Network Addresses
- 64-bit Addresses

16-bit Network Addresses

A 16-bit Network Address is assigned to a node when the node joins a network. The Network Address is unique to each node in the network. However, Network Addresses are not static - it can change.

The following two conditions will cause a node to receive a new Network Address:

1. If an end device cannot communicate with its parent it may need to leave the network and rejoin to find a new parent.
2. If the device type changes from router to end device, or vice-versa, the device will leave the network and rejoin as the new device type.

ZigBee requires that data be sent to the 16-bit network address of the destination device. This requires that the 16-bit address be discovered before transmitting data. See 3.2.3 Network Address Discovery for more information.

64-bit Addresses

Each node contains a unique 64-bit address. The 64-bit address uniquely identifies a node and is permanent.

3.2.2. ZigBee Application-layer Addressing

The ZigBee application layers define endpoints and cluster identifiers (cluster IDs) that are used to address individual services or applications on a device. An endpoint is a distinct task or application that runs on a ZigBee device, similar to a TCP port. Each ZigBee device may support one or more endpoints. Cluster IDs define a particular function or action on a device. Cluster IDs in the ZigBee home controls lighting profile, for example, would include actions such as "TurnLightOn", "TurnLightOff", "DimLight", etc.

Suppose a single radio controls a light dimmer and one or more light switches. The dimmer and switches could be assigned to different endpoint values. To send a message to the dimmer, a remote radio would transmit a message to the dimmer endpoint on the radio. In this example, the radio might support cluster IDs to "TurnLightOn", "TurnLightOff", or "DimLight". Thus, for radio A to turn off a light on radio B, radio A would send a transmission to the light switch endpoint on radio B, using cluster ID "TurnLightOff". This is shown in the figure below.

Figure 3-03. ZigBee Data Transmission Higher Layer Addressing Fields

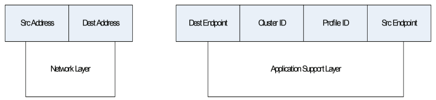
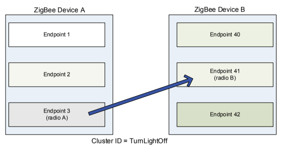


Figure 3-04. ZigBee Layer-Addressing Example



3.2.3. Data Transmission and Routing

All data packets are addressed using both device and application layer addressing fields. Data can be sent as a broadcast, multicast, or unicast transmission.

Broadcast Transmissions

Broadcast transmissions within the ZigBee protocol are intended to be propagated throughout the entire network such that all nodes receive the transmission. To accomplish this, all devices that receive a broadcast transmission will retransmit the packet 3 times. Each node that transmits the broadcast will also create an entry in a local broadcast transmission table. This entry is used to keep track of each received broadcast packet to ensure the packets are not endlessly transmitted. Each entry persists for 8 seconds. The broadcast transmission table holds 8 entries.

Since broadcast transmissions are retransmitted by each device in the network, broadcast messages should be used sparingly.

Multicast Transmissions

Multicast transmissions operate similar to broadcast transmissions. Data packets are broadcast throughout the network in a similar fashion. However, only devices that are part of the multicast group will receive the data packets.

Unicast Transmissions

Unicast ZigBee transmissions are always addressed to the 16-bit address of the destination device. However, only the 64-bit address of a device is permanent; the 16-bit address can change. Therefore, ZigBee devices may employ network address discovery to identify the current 16-bit

address that corresponds to a known 64-bit address. Once the 16-bit address is known, a route to the destination device must be discovered. ZigBee employs mesh routing using the Ad-hoc On-demand Distance Vector routing (AODV) protocol to establish a route between the source device and the destination.

Network Address Discovery

Data transmissions are always sent to the 16-bit network address of the destination device. However, since the 64-bit address is unique to each device and is generally known, ZigBee devices must discover the network address that was assigned to a particular device when it joined the PAN before they can transmit data.

To do this, the device initiating a transmission sends a broadcast network address discovery transmission throughout the network. This packet contains the 64-bit address of the device the initiator needs to send data to. Devices that receive this broadcast transmission check to see if their 64-bit address matches the 64-bit address contained in the broadcast transmission. If the addresses match, the device sends a response packet back to the initiator, providing the network address of the device with the matching 64-bit address. When this response is received, the initiator can then transmit data.

Mesh Routing

Mesh routing allows data packets to traverse multiple nodes (hops) in a network to route data from a source to a destination. The route a packet can take in a mesh network is independent of the parent/child relationships established during joining. Before transmitting a data packet from source to destination nodes, a route must be established. Route discovery is based on the AODV (Ad-hoc On-demand Distance Vector routing) protocol.

AODV (Ad-hoc On-demand Distance Vector) Routing Algorithm

Routing under the AODV protocol is accomplished using tables in each node that store in the next hop (intermediary node between source and destination nodes) for a destination node. If a next hop is not known, route discovery must take place in order to find a path. Since only a limited number of routes can be stored on a Router, route discovery will take place more often on a large network with communication between many different nodes.

When a source node must discover a route to a destination node, it sends a broadcast route request command. The route request command contains the source Network Address, the destination Network Address and a Path Cost field (a metric for measuring route quality). As the route request command is propagated through the network (refer to the Broadcast Transmission), each node that re-broadcasts the message updates the Path Cost field and creates a temporary entry in its route discovery table.

When the destination node receives a route request, it compares the 'path cost' field against previously received route request commands. If the path cost stored in the route request is better than any previously received, the destination node will transmit a route reply packet to the node that originated the route request. Intermediate nodes receive and forward the route reply packet to the Source Node (the node that originated route request).

Retries and Acknowledgments

ZigBee includes acknowledgment packets at both the Mac and Application Support (APS) layers. When data is transmitted to remote device, it may traverse multiple hops to reach the destination. As data is transmitted from one node to its neighbor, an acknowledgment packet (Ack) is transmitted in the opposite direction to indicate that the transmission was successfully received. If the Ack is not received, the transmitting device will retransmit the data, up to 4 times. This Ack is called the Mac layer acknowledgment.

In addition, the device that originated the transmission expects to receive an acknowledgment packet (Ack) from the destination device. This Ack will traverse the same path that the data traversed, but in the opposite direction. If the originator fails to receive this Ack, it will retransmit the data, up to 2 times until an Ack is received. This Ack is called the ZigBee APS layer acknowledgment.

Refer to the ZigBee specification for more details.

4. XBee Series 2 Network Formation

4.1. XBee Series 2 Network Formation

To create a ZigBee network, a coordinator must be started on a channel and PAN ID. Once the coordinator has started, routers and end device can join the network. Routers and coordinator devices can support up to 8 end device children each. Network formation is governed by the SC (Scan Channels), ID (PAN ID), SD (Scan Duration), and NJ (Node Join Time) commands. The SC and ID settings must be written using the WR command to affect network formation and joining.

4.1.1. Starting an XBee Series 2 Coordinator

In order to form a network, a coordinator must select an unused operating channel and PAN ID on behalf of its network. To do this, the coordinator first performs an energy scan on all channels specified by its SC (Scan Channels) parameter. The scan time on each channel is determined by the SD (Scan Duration) parameter. Once the energy scan is completed, the coordinator sends a beacon request on each of the SC channels and listens for any beacons. The information from the energy scan and the beacon scan (active scan) is used to select an unused channel and PAN ID. If the ID (PAN ID) parameter is set to 0xFFFF, the coordinator will select a random PAN ID. Otherwise, the coordinator will start on the PAN ID specified by its ID parameter.

After the coordinator has started, it will allow nodes to join to it for a time based on its NJ (Node Join Time) parameter. If the Associated LED function is enabled (D5 (DIO5 Configuration) command), the Associate pin (pin 15) will toggle its output state 1x per second after the coordinator stated. At this point, the operating channel and PAN ID can be read using the CH (Operating Channel) and ID (PAN ID) commands. The 16-bit address of the coordinator is always 0. If API is enable (AP parameter > 0): The API modem status "coordinator Started" frame is sent out the UART. The AI (Association Indication) command can be used at any point during the coordinator startup routine to determine the status of the startup operation.

4.1.2. Joining an XBee Series 2 Router to an existing PAN

Before a router can participate in a ZigBee network, the router must locate a coordinator or another router that has already joined a PAN, and attempt to join to it. To do this, it sends a beacon request frame on each of the SC channels and listens for beacon frames. The scan duration on each channel is determined by the SD parameter. The joining router will evaluate the received beacons to find a coordinator or router that is allowing joins on a valid PAN ID, and attempt to join to that device. If ID = 0xFFFF, the router will attempt to join to a device on any PAN ID. Otherwise, the router will only attempt joining with a device that operates on the PAN ID specified by the ID parameter. If a valid router/ coordinator is found, the router will attempt to join to that node. If the join succeeds, the Router has successfully started.

After the Router has started, it will allow nodes to join to it for a time based on the NJ (Node Join Time) parameter. If the Associated LED function is enabled(D5 (DIO5 Configuration) command) the Associate pin (pin 15) will toggle its output state 2x per second after the router has joined. At this point, the operating channel and PAN ID can be read using the CH (Operating Channel) and ID (PAN ID) commands. The 16-bit Network Address of the router can be read using the MY (16-bit Source Address) command. If API is enabled (AP parameter > 0): The API modem status "Joined" is sent out the UART. The AI (Association Indication) command can be used at any point during the router join routine to know the status of the startup operation.

4.1.3. Joining an XBee Series 2 End Device to an Existing PAN

Joining an end device to a PAN is similar to joining a router. Once the end device joins a PAN, however, the end device cannot allow other devices to join to it. If the Associate LED function is enabled (D5 (DIO5 Configuration) command), the Associate pin (pin 15) will toggle its output state 2x per second after the end device has joined. At this point, the operating channel and PAN ID can be read using the CH (Operating Channel) and ID (PAN ID) commands. The 16-bit network

address of the end device can be read using the MY (16-bit Source Address) command. If API is enabled (AP parameter > 0), the API modem status "Joined" is sent out the UART. The AI (Association Indication) command can be used at any point during the end device join routine to know the status of the startup operation.

4.1.4. Network Reset

Once a coordinator has started, or a router or end device has joined the network, the device will continue operating on that channel and PAN ID unless one of the following occurs:

1. The ID parameter changes, and is saved using the WR command
2. The SC parameter changes and is saved using the WR command, such that the current operating channel is not included in the new SC parameter
3. The NR command is issued with either 0 or 1 as a parameter

If any of the above occurs on a coordinator, the coordinator will attempt to restart on a channel and PAN ID based on the new saved ID and SC commands. On a router or end device, the above conditions will cause the device to leave the network (if previously joined) and attempt to join a new PAN using the saved ID and SC parameters.

4.2. XBee Series 2 Addressing

XBee modules support both ZigBee device addressing and application-layer addressing.

4.2.1. Device Addressing

All XBee/XBee-Pro modules can be identified by their unique 64-bit adresses or a user-configurable ASCII string identifier The 64-bit address of a module can read using the SH and SL commands. The ASCII string identifier is configured using the NI command. To transmit using device addressing, only the destination address must be configured. The destination address can be specified using either the destination device's 64-bit address or its NI-string. The XBee modules also support coordinator and broadcast addressing modes. Device addressing in the AT firmware is configured using the DL, DH, or DN commands. In the API firmware, the ZigBee Transmit Request API frame (0x10) can be used to specify destination addresses.

64-Bit Addressing

To address a node by its 64-bit address, the destination 64-bit address must be set to match the 64-bit address of the remote. In the AT firmware, the DH and DL commands set the destination 64-bit address. In the API firmware, the destination 64-bit address is set in the ZigBee Transmit Request frame. The coordinator can be addressed by either setting the destination address to 0 or by setting it to match the coordinator's 64-bit address. Broadcast transmissions can be sent by setting the 64-bit address to 0x000000000000FFFF.

To send a packet to an RF module using its 64-bit Address (Transparent Mode)

> Set the DH (Destination Address High) and DL (Destination Address Low) parameters of the source node to match the 64-bit Address (SH (Serial Number High) and SL (Serial Number Low) parameters) of the destination node.

To send a packet to an RF module using its 64-bit Address (API Mode)

> Use the ZigBee Transmit Request API frame to set the DH (Destination Address High) and DL (Destination Address Low) parameters of the source node to match the 64-bit Address (SH (Serial Number High) and SL (Serial Number Low) parameters) of the destination node.
>
> If the 16-bit address of the destination node is not known, set 16-bit Destination Network Address to 0xFFFE (refer to the 'API Addressing section below).

Since the ZigBee protocol relies on the 16-bit Network Address for routing, the 64-bit address must be converted into a 16-bit Network Address prior to transmitting data. If a module does not know the 16-bit Network Address for a given 64-bit address, it will transmit a broadcast Network Address Discovery command. The module with a matching 64-bit address will transmit its 16-bit network address back. Once the network address is discovered, the data will be transmitted.

The modules maintain a table that can store up to seven 64-bit addresses and their corresponding 16-bit Network Addresses.

API Addressing

API Mode provides the ability to store and maintain 16-bit Network Address tables on an external processor. The 16-bit Network Address information is provided to the application through the following:

- The ZigBee Transmit Status Frame
  (contains the current 16-bit Network Address of the remote)
- The ND and DN commands
  (return 64-bit and 16-bit Network Addresses of remote nodes)

With this information, a table can be built in an application that maps a 64-bit Address to the corresponding 16-bit Network Address.

The ZigBee Transmit Request API frame specifies the 64-bit Address and the Network Address (if known) that the packet should be sent to. By supplying both addresses, the module will forego Network Address Discovery and immediately attempt to route the data packet to the remote. If the Network Address of a particular remote changes, Network Address and route discovery will

take place to establish a new route to the correct node. Upon successful packet delivery, the TX Status Frame will indicate the correct Network Address of the remote.

Table 4-01. Sample table mapping 64-bit Addresses to 16-bit Network Addresses

Index	64-bit Address	16-bit Network Address
0	0013 4000 4000 0001	1234
1	0013 4000 4000 0002	5678
2	0013 4000 4000 01A0	A479
3	0013 4000 4000 0220	1F70

NI-String Addressing

The NI string can alternatively be used to address a remote module.

To send a packet to an RF module using its NI-string (Transparent Mode)

> Issue the DN (Destination Node) command using the NI (Node Identifier)-string of the destination node as the parameter.

To send a packet to an RF module using its NI-string (API Mode)

> Issue the DN command as stated above using the AT Command API frame.

When the DN command is issued, a broadcast transmission is sent across the network to discover the module that has a matching NI (Node Identifier) parameter. If a module is discovered with a matching NI-string, the DH and DL parameters will be configured to address the destination node and the command will return both the 64-bit Address and the 16-bit Network Address of the discovered node. Data can be transmitted after the DN (Destination Node) command finishes.

the AO command. See "API Frames" section for details.

Coordinator Addressing

A Coordinator can be addressed using its 64-bit address or NI string as described in the "NI-String Addressing" section. Alternatively, since the ZigBee Coordinator has a Network Address of "0", it can be addressed by its 16-bit Network Address.

To send a transmission to a Coordinator using its 16-bit Network Address:

> Set the Destination Addresses of the transmitting module as shown below:
> DL (Destination Low Address) = 0
> DH (Destination High Address) = 0

Broadcast Addressing

Broadcast transmissions are sent using a 64-bit address of 0x0000FFFF. Any RF module in the PAN will accept a packet that contains a broadcast address. When configured to operate in Broadcast Mode, receiving modules do not send ACKs (Acknowledgements).

To send a broadcast packet to all modules

> Set the Destination Addresses of the transmitting module as shown below:
> DL (Destination Low Address) = 0x0000FFFF
> DH (Destination High Address) = 0x00000000

NOTE: When programming the module, parameters are entered in hexadecimal notation (without the "0x" prefix). Leading zeros may be omitted.

Refer to the "Broadcast Transmissions" for more information.

4.2.2. Application-layer Addressing

Application-layer addressing allows the application to specify endpoint and cluster ID values for each transmission. Addressing multiple endpoints and cluster IDs can be accomplished by explicitly setting these values as needed.

In AT firmware, application-layer addressing must be enabled using the ZA command. When application-layer addressing is enabled, the DE and SE commands specify the source and destination endpoints, and the CI command sets the cluster ID that will be used in the transmission.

In API firmware, the Explicit Addressing ZigBee Command frame (0x11) can be used to configure the endpoint and cluster ID addressing parameters as needed. The destination device can indicate application-layer addressing information if the Explicit Receive API frame is addressing information using either the explicit receive indicator or the binding receive API frames. The receive RF data frame is set using Binding Table Addressing

The XBee Series 2 modules maintain several entries in a binding table. The binding table contains a destination 64-bit address, a type field, and endpoints for each transmission. Non-broadcast transmissions make use of the binding table to specify the addressing values for the transmission. Some entries in the binding table are reserved by MaxStream for special purposes. Binding table entries can be accessed by setting the BI command to a valid index in AT firmware, or by using the Binding Table API Command frame in the API firmware. The binding table entries are organized as follows.

Table 4-02.

Binding Table Index	Name	Access
0	Coordinator Binding	Read-Write
1	Tx-Aggregation Binding	Read-Only
2	Tx-Explicit Binding	Read-Write
3-4	Command Binding	Read-Only
5-8	Received Data Bindings	Read-Only
9	User Bindings.	Read-Write

Coordinator Binding

The coordinator binding contains the 64-bit address of the coordinator. This table entry is populated when the device joins the network.

Tx-Aggregation Binding

This binding table entry contains the 64-bit address of the aggregate (sink) node if one exists. Data can be sent to the aggregate node by addressing this index in the binding table.

Tx-Explicit Binding

The Tx-Explicit binding table entry contains the destination address and endpoint information from the last explicit transmission that was issued. This entry is modified whenever explicit addressing is used in either the AT or API firmware as described in the "XBee Series 2 Addressing" section.

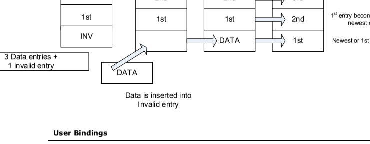
Command Binding

If a remote command request is received, the command binding entry stores information from the device that initiated the command. For example, if the ND or DN command is issued, this binding table entry would contain the source address of the device that sent the ND command.

Received Data Bindings

The received data bindings contain addressing information for the last three received data packets. The fourth entry is marked invalid. When a data packet is received, the address and endpoint information is stored into the invalid entry. Then, the oldest entry is made invalid. Thus, once an entry is created in the Received Data binding indexes, it will remain valid until three more RF data packets are received.

Figure 4-05. Demonstration of how entries in the received data bindings are replaced when an RF data packet is received.



User Bindings

These entries can be created and maintained by the application if needed. The following commands can be used to modify the user bindings. See the command descriptions for formatting details.

Table 4-03.

Command	Name	Description
B+	Add Binding	Creates a binding table entry at a specified User Binding index.
B-	Remove Binding	Removes a binding from a specified User Binding index.
BV	View Binding	Views one or more bindings in the binding table.
WB	Write Binding	Writes the binding table to non-volatile memory.

Multicast Addressing

Multicast addressing sends a broadcast message that will only be received by devices who subscribe to a multicast group. The binding table is used to subscribe to a multicast group. To send a multicast transmission, a binding table entry must exist where the type field is set to the multicast type value. The 64-bit address in this entry becomes a multicast group address. Only remote devices with a matching 64-bit multicast group will receive multicast transmissions. Once the binding table is configured with a multicast binding entry, the binding table index can be specified for a transmission using the BI command (AT firmware), or the Binding Table API Command Frame (API firmware). See the XBee Binding Table section for details.

Endpoint Addressing

The ZigBee specification, Ember stack, and MaxStream application have reserved some endpoints for different uses. Some of these endpoints are not accessible. Applications that will support custom endpoints should select endpoints not already used by ZigBee, Ember, or MaxStream.

The cluster ID used by MaxStream on the serial data endpoint for serial data transmissions is 0x11.

4.2.3. XBee Series 2 Endpoint Table

The XBee Series 2 modules maintain a table of supported endpoints. If an endpoint will be used as the source endpoint in a data transmission, the endpoint must first be defined in the endpoint table.

The XBee Series 2 endpoint table operates similar to the binding table. Entries may be added, removed, or viewed using the E+, E-, and EV commands respectively. Some table entries are reserved for special purposes

Table 4-04.

Endpoint Table Index	Name	Access
0	Command Endpoint	Read-Only
1	Data Endpoint	Read-Only
2	Tx-Explicit Endpoint	Read-Write
3- 4	User Endpoints	Read-Write

Command Endpoint

The command endpoint is used to send or reply to various commands. This endpoint must exist in the application.

Data Endpoint

This endpoint is used to send serial data to other XBee Series 2 modules. It must always exist in the application.

Tx-Explicit Endpoint

This entry is used as needed to define the source endpoint that must be defined for a data transmission. If a transmit request is made, and the specified source endpoint does not exist, it will be created temporarily at this endpoint table index.

User Endpoints

User endpoints are controlled entirely by the application. These endpoints may be added, removed, or viewed in the API firmware using the following commandsSee the command descriptions for command formatting details. At present, changes to the endpoint table are saved to non-volatile memory when WR is issued..

Table 4-05. ZigBee Data Transmissions Addressing Fields

Command	Name	Description
E+	Add Endpoint	Creates an endpoint entry at a specified user endpoint index.
E-	Remove Endpoint	Removes an endpoint entry from a specified user endpoint index.
EV	View Endpoint	Views one or more endpoints in the endpoint table.

4.3. Advanced Network Features

Network Mapping

Network mapping has provisions to identify all devices on a PAN.There are currently two ways to do this either through the Node Discover (ND) Command or the API Child Joined Indicator. Both are explained below.

Node Discover (ND) Command

Issuing the ND command on a device sends a broadcast node discovery command throughout the PAN. All devices that receive the command will send a response that includes the device's 64-bit and 16-bit addresses, along with the NI-string and other information.

API Child Joined Indicator

Routers and end devices can be configured to send a transmission after joining to alert the coordinator, or the entire network, that the device has joined the network. When this message is transmitted, the receiving device(s), if running API firmware, will send an advanced modem status indicator out the UART to indicate the 64-bit and 16-bit addresses of the joining device.

4.4. I.O. Line Configuration

The XBee Series 2 modules support both analog input and digital IO line modes on several configurable pins.

Configuring A/D and Digital Lines

The following table lists the pin functions supported on the modules

.

Table 4-06.

Module Pin Names	Module Pin Numbers	Configuration Command
CD/DIO12	4	P2
PWM0/RSSI/DIO10	6	P0
PWM/DIO11	7	P1
SLEEP_RQ/DIO8	9	IO Configuration not supported
DIO4	11	D4
CTS/DIO7	12	D7
ON_SLEEP/DIO9	13	IO Configuration not supported
ASSOC/DIO5	15	D5
RTS/DIO6	16	D6
AD3/DIO3	17	D3
AD2/DIO2	18	D2
AD1/DIO1	19	DI
AD0/DIO0	20	D0

Setting the configuration command that corresponds to a particular pin will configure the pin. Parameters for the pin configuration commands typically include the following:

.

Table 4-07.

Pin Command Parameter	Description
0	Unmonitored digital input
1	Reserved for pin-specific alternate functionalities
2	Analog input, single ended (A/D pins only)
3	Digital input, monitored
4	Digital output, default low
5	Digital output, default high
6-9	Alternate functionalities, where applicable
0	Unmonitored digital input
1	Reserved for pin-specific alternate functionalities
2	Analog input, single ended (A/D pins only)
3	Digital input, monitored
4	Digital output, default low
5	Digital output, default high

See the command table for more information. Pullup resistors for each digital input can be enabled using the PR command.

Sampling A/D and Digital Input Lines

The IS command can be used to read the current value of all enabled A/D and digital input lines. The format for the IS response is shown below. At the time, only one sample set is supported in this frame.

Bytes	Name	Description
1	Sample sets in packet	Number of sample sets in the packet
2	Digital Channel Mask	Each bit in the digital channel mask corresponds to one digital IO line. The bits, from LSB to MSB, correspond to DOI0-DOI5 on the module. For example a digital channel mask of 0x002F means DIO0,1,2,3, and 5 are enabled as digital input lines.
1	Analog Channel Mask	Each bit in the analog channel mask corresponds to one analog channel. The bits from LSB to MSB correspond to AIN0-AIN7 on the module. For example, if the analog channel mask is 0x06, AINI and AIN3 are enabled as analog input lines.
Var	Sampled Data Set	A sample set consisting of 1 sample for each enabled ADC and/or DIO channel. If any digital input lines are enabled, the first two bytes indicate the state of all enabled digital input lines. Each bit in these two bytes corresponds to one digital IO line, similar to the way each bit in the diglossia channel mask corresponds. Note: only the digital input line that are enabled in the detail channel mask have valid readings. Channels that are not enabled as digital input lines will return a 0 in the sampled data set. If no pins are configured as digital inputs, these 2 bytes will be omitted. Following the digital input data, if any, each enabled analog channel will return 2 bytes (10bits). The analog data is scaled such that 0 represents 0V, and 0x3FF=1.2V. The analog input lines cannot measure more than 1.2V. Information for each enabled analog channel is returned in order, starting with AIN0 and finishing with AIN4. Only enabled analog input channels will return data.

The AT firmware returns a carriage return delimited list containing the above-listed fields. The API firmware returns an AT command response API frame with the IO data included in the command data portion of the packet.

Example	Sample AT Response
0x01\r	[1 sample set]
0x0C0C\r	[Digital Inputs: DIO 2, 3, 10, 11 low]
0x03\r	[Analog Inputs: ADOP 0, 1]
0x0408\r	[Digital input states: DIO 3, 10 high, DIO 2, 11 low]
0x03D0\r	[Analog input ADIO 0= 0x3D0]
0x0124\r	[Analog input ADIO 1=0x120]

To convert the A/D reading to mV, do the following:

AD(mV)= (ADIO reading/0x3FF)*1200mV

The reading in the sample frame represent voltage inputs of 1144.9 and 342.5mV for ADIO0 and ADIO1 respectively.

5. XBee Series 2 Command Reference Tables

Special

Table 5-08. Special Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
WR	**Write**. Write parameter values to non-volatile memory so that parameter modifications persist through subsequent resets. Note: Once WR is issued, no additional characters should be sent to the module until after the "OK\r" response is received.	CRE	--	–
WB	**Write Binding Table:** Writes the current binding table to non-volative memory.	CRE	--	--
RE	**Restore Defaults**. Restore module parameters to factory defaults. RE command does not reset the ID parameter.	CRE	--	–
FR	**Software Reset**. Reset module. Responds immediately with an "OK" then performs a reset ~2 seconds later. Use of the FR command will cause a network layer restart on the node if SC or ID were modified since the last reset.	CRE	--	–
NR	**Network Reset**. Reset network layer parameters on one or more modules within a PAN. Responds immediately with an "OK" then causes a network restart. All network configuration and routing information is consequently lost. *If NR = 0*: Resets network layer parameters on the node issuing the command. *If NR = 1*: Sends broadcast transmission to reset network layer parameters on all nodes in the PAN.	CRE	0 - 1	–

Node types that support the command: C = Coordinator, R = Router, E = End Device

Addressing

Table 5-09. Addressing Commands (Sub-categories designated within {brackets})

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
DH[2]	**Destination Address High**. Set/Get the upper 32 bits of the 64-bit destination address. When combined with DL, it defines the destination address used for transmission. 0x000000000000FFFF is the broadcast address for the PAN. DH is not supported in API Mode. 0x0000000000000000 is the Coordinator's 16-bit Network Address.	CRE	0 - 0xFFFFFFFF	0
DL[2]	**Destination Address Low**. Set/Get the lower 32 bits of the 64-bit destination address. When combined with DH, DL defines the destination address used for transmission. 0x000000000000FFFF is the broadcast address for the PAN. DL is not supported in API Mode. 0x0000000000000000 is the Coordinator's 16-bit Network Address.	CRE	0 - 0xFFFFFFFF	0xFFFF(Coordinator) 0 (Router/End Device)
ZA[2]	**ZigBee Application Layer Addressing**. Set/read the Zigbee application layer addressing enabled attribute. If enabled, data packets will use the SE, DE, and CI commands to address Zigbee application layer source and destination endpoints, and the cluster ID fields in all data transmissions. ZA is only supported in the AT firmware.	CRE	0 - 1	0
SE[2]	**Source Endpoint**. Set/read the ZigBee application layer source endpoint value. If ZigBee application layer addressing is enabled (ZA command), this value will be used as the source endpoint for all data transmissions. SE is only supported in AT firmware.The default value (0xE8) is the MaxStream data endpoint	CRE	1 - 0xEF	0xE8
DE[2]	**Destination Endpoint**. Set/read Zigbee application layer destination ID value. If ZigBee application layer addressing is enabled (ZA command), this value will be used as the destination endpoint all data transmissions. DE is only supported in AT firmware.The default value (0xE8) is the MaxStream data endpoint.	CRE	0 - 0xEF	0xE8
CI[2]	**Cluster Identifier**. Set/read Zigbee application layer cluster ID value. If ZigBee application layer addressing is enabled (ZA command), this value will be used as the cluster ID for all data transmissions. CI is only supported in AT firmware.The default value (0x11) is the MaStream transparent data cluster ID.	CRE	0 - 0xFF	0x11
BI[2]	**Binding Table Index**. Set/read the binding table index value. If this value is set to a valid binding table index, the addressing information at that index in the binding table will be used for all data transmissions. BI is only supported in AT firmware	CRE	0 - 0xFF	0xFF
MY	**16-bit Network Address.** Get the 16-bit Network Address of the module.	CRE	0 - 0xFFFE [read-only]	0xFFFE
MP	**16-bit Parent Network Address.** Get the 16-bit parent Network Address of the module.	E	0 - 0xFFFE [read-only]	0xFFFE
SH	**Serial Number High**. Read high 32 bits of the RF module's unique IEEE 64-bit address. 64-bit source address is always enabled.	CRE	0 - 0xFFFFFFFF [read-only]	factory-set
SL	**Serial Number Low**. Read low 32 bits of the RF module's unique IEEE 64-bit address. 64-bit source address is always enabled.	CRE	0 - 0xFFFFFFFF [read-only]	factory-set

Table 5-09. Addressing Commands (Sub-categories designated within {brackets})

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
NI	**Node Identifier.** Stores a string identifier. The register only accepts printable ASCII data. In AT Command Mode, a string can not start with a space. A carriage return ends the command. Command will automatically end when maximum bytes for the string have been entered. This string is returned as part of the ND (Node Discover) command. This identifier is also used with the DN (Destination Node) command.	CRE	20-Byte printable ASCII string	--

1. Node types that support the command: C=Coordinator, R=Router, E=End Device
2. Command supported by modules using AT Command firmware only

Networking & Security

Table 5-010. Networking Commands (Sub-categories designated within {brackets})

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
CH	**Operating Channel**. Read the channel number used for transmitting and receiving between RF modules. Uses 802.15.4 channel numbers.	CRE	0, 0x0B-0x1A *(XBee)*	0
ID	**PAN ID**. Set/Get the PAN (Personal Area Network) ID. *Coordinator* - Set the preferred Pan ID. Set (ID = 0xFFFF) to auto-select. *Router / End Device* - Set the desired Pan ID. When the device searches for a Coordinator, it attempts to only join to a parent that has a matching Pan ID. Set (ID = 0xFFFF) to join a parent operating on any Pan ID. Changes to ID should be written to non-volatile memory using the WR command. ID changes are not used until the module is reset (FR, NR or power-up).	CRE	0 - 0x3FFF, 0xFFFF	0x0234 (291d)
BH	**Broadcast Hops.** Set/Read the maximum number of hops for each broadcast data transmission. Setting this to 0 will use the maximum number of hops.	CRE	0 - 0x0F	--
NT	**Node Discover Timeout.** Set/Read the amount of time a node will spend discovering other nodes when ND or DN is issued.	CRE	0 - 0xFC [x 100 msec]	0x3C (60d)
ND	**Node Discover.** Discovers and reports all RF modules found. The following information is reported for each module discovered. MY<CR> SH<CR> SL<CR> NI<CR> (Variable length) PARENT_NETWORK ADDRESS (2 Bytes)<CR> DEVICE_TYPE<CR> (1 Byte: 0=Coord, 1=Router, 2=End Device) STATUS<CR> (1 Byte: Reserved) PROFILE_ID<CR> (2 Bytes) MANUFACTURER_ID<CR> (2 Bytes) <CR> After (NT * 100) milliseconds, the command ends by returning a <CR>. ND also accepts a Node Identifier (NI) as a parameter (optional). In this case, only a module that matches the supplied identifier will respond. If ND is sent through the API, each response is returned as a separate AT_CMD_Response packet. The data consists of the above listed bytes without the carriage return delimiters. The NI string will end in a "0x00" null character.	CRE	optional 20-Byte NI or MY value	--
DN	**Destination Node.** Resolves an NI (Node Identifier) string to a physical address (case-sensitive). The following events occur after the destination node is discovered: <AT Firmware> 1. DL & DH are set to the extended (64-bit) address of the module with the matching NI (Node Identifier) string. 2. OK (or ERROR)\r is returned. 3. Command Mode is exited to allow immediate communication <API Firmware> 1. The 16-bit network and 64-bit extended addresses are returned in an API Command Response frame. If there is no response from a module within (NT * 100) milliseconds or a parameter is not specified (left blank), the command is terminated and an "ERROR" message is returned. In the case of an ERROR, Command Mode is not exited.	CRE	up to 20-Byte printable ASCII string	--
JN	**Join Notification**. Set/read the join notification value. If enabled, the device will send a transmission after joining a PAN identifying itself to other devices in the PAN.	CRE	0 - Join notification disabled 1 - Send notification only to coordinator after joining PAN 2 - Send notification as broadcast transmission after joining PAN	0

Table 5-010. Networking Commands (Sub-categories designated within {brackets})

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
SC	**Scan Channels**. Set/Read the list of channels to scan. *Coordinator* - Bit field list of channels to choose from prior to starting network. *Router/End Device* - Bit field list of channels that will be scanned to find a Coordinator/ Router to join. Changes to SC should be written using WR command. SC changes are not used until the module is reset (FR, NR or power-up). Bit (Channel): 0 (0x0B) 4 (0x0F) 8 (0x13) 12 (0x17) 1 (0x0C) 5 (0x10) 9 (0x14) 13 (0x18) 2 (0x0D) 6 (0x11) 10 (0x15) 14 (0x19) 3 (0x0E) 7 (0x12) 11 (0x16) 15 (0x1A)	CRE	1 - 0xFFFF[bitfield]	0x1FFE
SD	**Scan Duration**. Set/Read the scan duration exponent. Changes to SD should be written using WR command. *Coordinator* - Duration of the Active and Energy Scans (on each channel) that are used to determine an acceptable channel and Pan ID for the Coordinator to startup on. *Router / End Device* - Duration of Active Scan (on each channel) used to locate an available Coordinator / Router to join during Association. Scan Time is measured as:(# Channels to Scan) * (2 ^ SD) * 15.36ms - The number of channels to scan is determined by the SC parameter. The XBee can scan up to 16 channels (SC = 0xFFFF). Sample Scan Duration times (13 channel scan): If SD = 0, time = 0.200 sec SD = 2, time = 0.799 sec SD = 4, time = 3.190 sec SD = 6, time = 12.780 sec	CRE	0 - 7 [exponent]	3
NJ	**Node Join Time**. Set/Read the time that a Coordinator/Router allows nodes to join. This value can be changed at run time without requiring a Coordinator or Router to restart. The time starts once the Coordinator or Router has started. The timer is reset on power-cycle or when NJ changes.	CR	0 – 0x40, 0xFF [x 1 sec]	0xFF (always allows joining)
AR	**Aggregate Routing Notification**. Set/read time between consecutive aggregate route broadcast messages. If used, AR should be set on only one device to enable many-to-one routing to the device. Setting AR to 0 only sends one broadcast	CR	0 - 0xFF	0xFF
AI	**Association Indication**. Read information regarding last node join request: 0x00 - Successful completion - Coordinator started or Router/End Device found and joined with a parent. 0x21 - Scan found no PANs 0x22 - Scan found no valid PANs based on current SC and ID settings 0x23 - Valid Coordinator or Routers found, but they are not allowing joining (NJ expired) 0x27 - Node Joining attempt failed 0x2A - Coordinator Start attempt failed' 0xFF - Scanning for a Parent	CRE	0 - 0xFF [read-only]	--

RF Interfacing

Table 5-011. RF Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
PL	**Power Level**. Select/Read the power level at which the RF module transmits conducted power.	CRE	0 - 4 (XBee) 0 = -10 / 10 dBm 1 = -6 / 12 dBm 2 = -4 / 14 dBm 3 = -2 / 16 dBm 4 = 0 / 18 dBm	4
PM	**Power Mode**. Set/read the power mode of the device. Enabling boost mode will improve the receive sensitivity by 1dB and increase the transmit power by 2dB	CRE	0-1, 0=-Boost mode disabled, 1= Boost mode enabled.	1

1. Node types that support the command: C = Coordinator, R = Router, E = End Device

Serial Interfacing (I/O)

Table 5-012. Serial Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
AP[2]	**API Enable**. Enable API Mode. The AP parameter is only applicable when using modules that contain the following firmware versions:1.1xx (coordinator), 1.3xx (router/end device)	CRE	1 - 2 1 = API-enabled 2 = API-enabled (w/escaped control characters)	1

Table 5-012. Serial Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
AO[2]	**API Options**. Configure options for API. Current options select the type of API RF data receive frame that is used.	CRE	0 - ZigBee Rx data indicator enabled (0x90) 1 - Explicit Rx data indicator API frame enabled (0x91) 2 - Binding Rx data indicator API frame enabled (0x92)	0
BD	**Interface Data Rate**. Set/Read the serial interface data rate for communication between the module serial port and host. Any value above 0x07 will be interpreted as an actual baud rate. When a value above 0x07 is sent, the closest interface data rate represented by the number is stored in the BD register.	CRE	0 - 7 (standard baud rates) 0 = 1200 bps 1 = 2400 2 = 4800 3 = 9600 4 = 19200 5 = 38400 6 = 57600 7 = 115200 0x80 - 0x38400 (non-standard rates)	3
RO	**Packetization Timeout**. Set/Read number of character times of inter-character silence required before packetization. Set (RO=0) to transmit characters as they arrive instead of buffering them into one RF packet.	CRE	0 - 0xFF [x character times]	3
D7	**DIO7 Configuration**. Select/Read options for the DIO7 line of the RF module.	CRE	0 - 1 0 = Disabled 1 = CTS Flow Control 3 = Digital input 4 = Digital output, low 5 = Digital output, high 6 = RS-485 transmit enable (low enable) 7 = RS-485 transmit enable (high enable)	1
D6	**DIO6 Configuration.** Configure options for the DIO6 line of the RF module.	CRE	0 - Disabled 1 - RTS Flow Control	0
D5	**DIO5 Configuration**. Configure options for the DIO5 line of the RF module. Options include: Associated LED indicator (LED blinks 1x/sec when the module is powered and 2x/sec when module is associated to a Coordinator.).	CRE	0 - 1 0 = Disabled 1 = Associated indication LED 3 = Digital input 4	1

1. Node types that support the command: C = Coordinator, R = Router, E = End Device
2. Command supported by modules using API firmware only

I/O Commands

Table 5-013. Serial Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
P0	**PWM0 Configuration**. Select/Read function for PWM0.	CRE	0 - 1 0 = Disabled 1 = RSSI PWM	1
P1	**DIO11 Configuration**. Configure options for the DIO11 line of the RF module.	CRE	0 - Unmonitored digital input 3- Digital input, monitored 4- Digital output, default low 5- Digital output, default low	0
P2	**DIO12 Configuration**. Configure options for the DIO12 line of the RF module.	CRE	0 - Unmonitored digital input 3- Digital input, monitored 4- Digital output, default low 5- Digital output, default low	0

Table 5-013. Serial Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
RP	**RSSI PWM Timer.** Time RSSI signal will be output after last transmission. When RP = 0xFF, output will always be on.	CRE	0 - 0xFF [x 100 ms]	0x28 (40d)
IS	**Force Sample** Forces a read of all enabled digital and analog input lines.	CRE	–	--
D0	**AD0/DIO0 Configuration**. Select/Read function for AD0/DIO0.	CRE	0, 2-5 0 – Disabled 2 - Analog input, single ended 3 – Digital input 4 – Digital output, low 5 – Digital output, high	0
D1	**AD1/DIO1 Configuration**. Select/Read function for AD1/DIO1.	CRE	0, 2-5 0 – Disabled 2 - Analog input, single ended 3 – Digital input 4 – Digital output, low 5 – Digital output, high	0
D2	AD2/DIO2 Configuration. Select/Read function for AD2/DIO2.	CRE	0, 2-5 0 – Disabled 2 - Analog input, single ended 3 – Digital input 4 – Digital output, low 5 – Digital output, high	0
D3	AD3/DIO3 Configuration. Select/Read function for AD3/DIO3.	CRE	0, 2-5 0 – Disabled 2 - Analog input, single ended 3 – Digital input 4 – Digital output, low 5 – Digital output, high	0
D4	DIO4 Configuration. Select/Read function for DIO4.	CRE	0, 3-5 0 – Disabled 3 – Digital input 4 – Digital output, low 5 – Digital output, high	0

Diagnostics

Table 5-014. Diagnostics Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
VR	**Firmware Version**. Read firmware version of the module.	CRE	0 - 0xFFFF [read-only]	Factory-set
HV	**Hardware Version**. Read hardware version of the module.	CRE	0 - 0xFFFF [read-only]	Factory-set

1. Node types that support the command:C = Coordinator, R = Router, E = End Device

AT Command Options

Table 5-015. AT Command Options Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
CT[2]	**Command Mode Timeout.** Set/Read the period of inactivity (no valid commands received) after which the RF module automatically exits AT Command Mode and returns to Idle Mode.	CRE	2 - 0x028F [x 100 ms]	0x64 (100d)
CN[2]	**Exit Command Mode.** Explicitly exit the module from AT Command Mode.	CRE	--	--
GT[2]	**Guard Times**. Set required period of silence before and after the Command Sequence Characters of the AT Command Mode Sequence (GT + CC + GT). The period of silence is used to prevent inadvertent entrance into AT Command Mode.	CRE	1 - 0x0CE4 [x 1 ms] (max of 3.3 decimal sec)	0x3E8 (1000d)

Table 5-015. AT Command Options Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
CC[2]	**Command Sequence Character**. Set/Read the ASCII character value to be used between Guard Times of the AT Command Mode Sequence (GT + CC + GT). The AT Command Mode Sequence enters the RF module into AT Command Mode. CC command is only applicable when using modules that contain the following "AT Command" firmware versions: 8.0xx (Coordinator), 8.2xx (Router), 8.4xx (End Device)	CRE	0 - 0xFF	0x2B ('+' ASCII)

1. Node types that support the command: C = Coordinator, R = Router, E = End Device
2. Command supported by modules using AT Command firmware only

Sleep Commands

Table 5-016. Sleep Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
SM	**Sleep Mode** Sets the sleep mode on the RF module	RE	0-Sleep disabled 1-Pin sleep enabled 4-Cyclic sleep enabled Note: When SM=0, the device operates as a router. When SM changes to a non-zero value, the router leaves the network and rejoins as an end device. **Only end devices can sleep**	0
SN	**Number of Sleep Periods.** Sets the number of sleep periods to not assert the On/Sleep pin on wakeup if no RF data is waiting for the end device. This command allows a host application to sleep for an extended time if no RF data is present	RE	1-0xFF	1
SP	**Sleep Period.** This value determines how long the end device will sleep at a time, up to 28 seconds. (The sleep time can effectively be extended past 28 seconds using the SN command.) On the parent, this value determines how long the parent will buffer a message for the sleeping end device. It should be set at least equal to the longest SP time of any child end device.	CRE	0x20 - 0xAF0 x 10ms (Quarter second resolution)	0x7D0 (20 seconds)
ST	**Time Before Sleep** Sets the time before sleep timer on an end device.The timer is reset each time serial or RF data is received. Once the timer expires, an end device may enter low power operation. Applicable for cyclic sleep end devices only.	RE	1 - 0xFFFE (x 1ms)	0x1388 (5 seconds)

6. API Operation

As an alternative to Transparent Operation, API (Application Programming Interface) Operations are available. API operation requires that communication with the module be done through a structured interface (data is communicated in frames in a defined order). The API specifies how commands, command responses and module status messages are sent and received from the module using a UART Data Frame.

6.0.1. API Frame Specifications

Two API modes are supported and both can be enabled using the AP (API Enable) command. Use the following AP parameter values to configure the module to operate in a particular mode:

- AP = 1: API Operation
- AP = 2: API Operation (with escaped characters)

API Operation (AP parameter = 1)

When this API mode is enabled (AP = 1), the UART data frame structure is defined as follows:

Figure 6-06. UART Data Frame Structure:

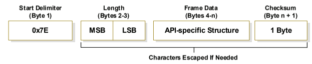
MSB = Most Significant Byte, LSB = Least Significant Byte

Any data received prior to the start delimiter is silently discarded. If the frame is not received correctly or if the checksum fails, the module will reply with a module status frame indicating the nature of the failure.

API Operation - with Escape Characters (AP parameter = 2)

When this API mode is enabled (AP = 2), the UART data frame structure is defined as follows:

Figure 6-07. UART Data Frame Structure - with escape control characters:



MSB = Most Significant Byte, LSB = Least Significant Byte

Escape characters. When sending or receiving a UART data frame, specific data values must be escaped (flagged) so they do not interfere with the data frame sequencing. To escape an interfering data byte, insert 0x7D and follow it with the byte to be escaped XOR'd with 0x20.

Data bytes that need to be escaped:

- 0x7E – Frame Delimiter
- 0x7D – Escape
- 0x11 – XON
- 0x13 – XOFF

Example - Raw UART Data Frame (before escaping interfering bytes):
0x7E 0x00 0x02 0x23 0x11 0xCB

0x11 needs to be escaped which results in the following frame:
0x7E 0x00 0x02 0x23 0x7D 0x31 0xCB

Note: In the above example, the length of the raw data (excluding the checksum) is 0x0002 and the checksum of the non-escaped data (excluding frame delimiter and length) is calculated as: 0xFF - (0x23 + 0x11) = (0xFF - 0x34) = 0xCB.

Checksum

To test data integrity, a checksum is calculated and verified on non-escaped data.

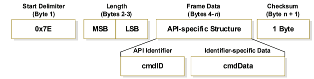
To calculate: Not including frame delimiters and length, add all bytes keeping only the lowest 8 bits of the result and subtract the result from 0xFF.

To verify: Add all bytes (include checksum, but not the delimiter and length). If the checksum is correct, the sum will equal 0xFF.

6.0.2. API Types

Frame data of the UART data frame forms an API-specific structure as follows:

Figure 6-08. UART Data Frame & API-specific Structure:

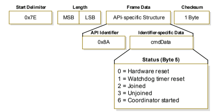


The cmdID frame (API-identifier) indicates which API messages will be contained in the cmdData frame (Identifier-specific data). Refer to the sections that follow for more information regarding the supported API types. Note that multi-byte values are sent big endian.

Modem Status

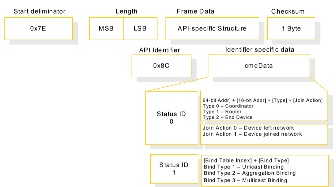
API Identifier: 0x8A
RF module status messages are sent from the module in response to specific conditions.

Figure 6-09. Modem Status Frames



Advanced Modem Status Frame (0x8C)

API Identifier Name: Advanced Modem Status Frame
API Identifier Value: 0x8C
Product support: XBEE Series 2



AT Command

API Identifier Value: 0x08
Allows for module parameter registers to be queried or set.

Figure 6-10. AT Command Frames

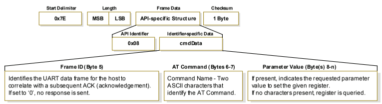


Figure 6-11. Example: API frames when reading the NJ parameter value of the module.

Byte 1	Bytes 2-3		Byte 4	Byte 5	Bytes 6-7		Byte 8
0x7E	0x00	0x04	0x08	0x52 (R)	0x4E (N)	0x4A (J)	0x0D
Start Delimiter	Length*		API Identifier	Frame ID**	AT Command		Checksum

* Length [Bytes] = API Identifier + Frame ID + AT Command
** "R" value was arbitrarily selected.

Figure 6-12. Example: API frames when modifying the NJ parameter value of the module.

Byte 1	Bytes 2-3		Byte 4	Byte 5	Bytes 6-7		Byte 8	Byte 9
0x7E	0x00	0x05	0x08	0x4D (M)	0x4E (N)	0x4A (J)	0x40	0xD2
Start Delimiter	Length*		API Identifier	Frame ID**	AT Command		Parameter Value	Checksum

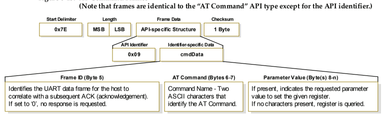
* Length [Bytes] = API Identifier + Frame ID + AT Command + Parameter Value
** "M" value was arbitrarily selected.

A string parameter used with the NI (Node Identifier), ND (Node Discover) and DH (Destination Address High) command is terminated with a 0x00 character.

AT Command - Queue Parameter Value

API Identifier Value: 0x09
This API type allows module parameters to be queried or set. In contrast to the "AT Command" API type, new parameter values are queued and not applied until either the "AT Command" (0x08) API type or the AC (Apply Changes) command is issued. Register queries (reading parameter values) are returned immediately.

Figure 6-13. AT Command Frames
(Note that frames are identical to the "AT Command" API type except for the API identifier.)

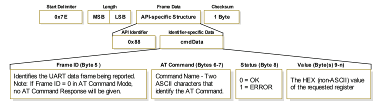


AT Command Response

API Identifier Value: 0x88
Response to previous command.

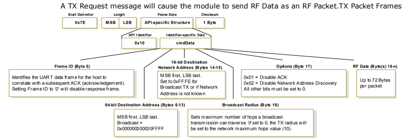
In response to an AT Command message, the module will send an AT Command Response message. Some commands will send back multiple frames (for example, the ND (Node Discover) command). These commands will end by sending a frame with a status of ATCMD_OK and no cmdData.

Figure 6-14. AT Command Response Frames.



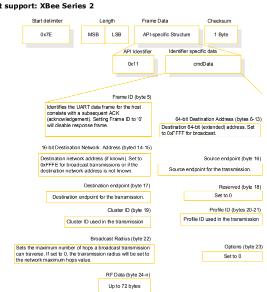
ZigBee Transmit Request

API Identifier Value: 0x10
A TX Request message will cause the module to send RF Data as an RF Packet.TX Packet Frames



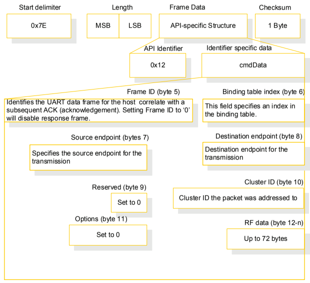
Explicit Addressing ZigBee Command Frame (0x11)

API Identifier Name: Explicit Addressing ZigBee Command Frame
API Identifier Value: 0x11
Product support: XBee Series 2



Binding Table ZigBee Command Frame (0x12)

API Identifier Name: Binding Table ZigBee Command Frame
API Identifier Value: 0x12
Product support: XBee Series 2

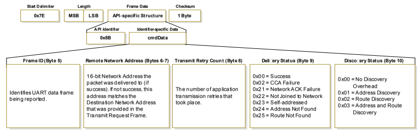


ZigBee Transmit Status

API Identifier Value: 0x8B

When a TX Request is completed, the module sends a TX Status message. This message will indicate if the packet was transmitted successfully or if there was a failure.

Figure 6-15. TX Status Frames

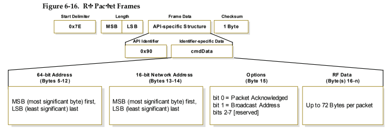


ZigBee Receive Packet

API Identifier Value: 0x90

When the module receives an RF packet, it is sent out the UART using this message type.

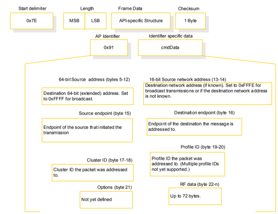
Figure 6-16. RX Packet Frames



ZigBee Explicit Rx Indicator (0x91)

API Identifier Name: ZigBee Explicit RX Indicator
API Identifier Value: 0x91
Product support: XBee Series 2

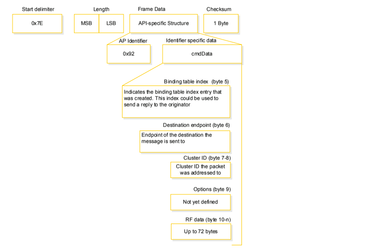
When the modem receives a ZigBee RF packet it is sent out the UART using this message type if the EXPLICIT_RECEIVE_OPTION bit is set in AO.



ZigBee Binding Rx Indicator (0x92)

API Identifier Name: ZigBee Binding RX Indicator
API Identifier Value: 0x92
Product support: XBee Series 2

When the modem receives a ZigBee RF packet it is sent out the UART using this message type if the BINDING_TABLE_INDEX_RECEIVE_OPTION bit is set in AO.



7. Examples

7.1. Starting an XBee Network

Start the coordinator

1. Determine the operating channels list using the SC (Scan Channels) command and the PAN ID to operate using the ID (PAN ID) command. The default SD (Scan Duration) parameter value should suffice. If these values are changed from the defaults, they must be written to non-volatile memory using the WR (Write) command.
2. The Associate LED, if enabled using the D5 (DIO5 Configuration) parameter, will start blinking 1x per second once the coordinator has started.
   If API is enabled (AP parameter > 0): The API Modem Status "Coordinator Started" is sent out the UART.
3. The AI (Association Indication) parameter will be 0 signifying a successful startup.
4. The MY (16-bit Source address) attribute is 0 (the 16-bit network address of a ZigBee coordinator).
5. After startup, the coordinator will allow joining based on its NJ (Node Join Time) value.
6. It is recommended that the coordinator be configured with an NI-String identifier. This NI-String identifier should be written to non-volatile memory using the WR (Write) command to be preserved through power-loss.

Adding a Child (router)

1. Determine the operating channel list (SC) and the desired PAN ID to join (ID) (0xFFFF - join any Pan). The default SD parameter should suffice. If these values are changed from the defaults, they must be written to non-volatile memory using the WR (Write) command.
2. The router, on power-up, will attempt to locate a parent to join according to its SC and ID parameters.
3. Once the router has joined a parent, the Associate LED, if enabled (D5), will start blinking 2x per second. The ID and CH parameters will reflect the operating PAN ID and Channel. The MY parameter will reflect the 16-bit network address of the router. The MP command returns the 16-bit network address of the router's parent (node it joined to).
   If API is enabled (AP parameter > 0): The API Modem Status "Joined" is sent out the UART.
4. If the router is not joining as expected, the AI (Association Indication) parameter can be read to determine the cause of failure.
   Verify the PAN contains a coordinator or nearby joined router that has matching Channel (SC, CH) and PAN ID (ID) settings and is allowing nodes to join to it (NJ parameter).
5. Once the router has joined a PAN, the router will allow joining based on the NJ parameter.
6. It is recommended that the router be configured with a unique NI-String identifier. This NI-String identifier should be written to non-volatile memory using the WR (Write) command to be preserved through power-loss.

Transmit Data

1. Start a coordinator (refer to instructions above).
2. Add one or more Child router(s) to the coordinator (refer to instructions above).
3. Once the coordinator has started, all routers and End Devices should join to a parent and their Associate LED should blink 2x per second.
4. If any nodes have not joined, read the AI command to determine why.
5. Issue the ATND command on the coordinator to get a list of all nodes on the network.
6. Use the 'Terminal' tab of the X-CTU Software to send serial data between nodes. The data should be transmitted from the source to the destination node as specified by the DH + DL parameters.
7. (Optional) Change the Destination address on any node to one of the 64-bit addresses discovered using the ND command in step 5 (DH, DL Commands, or in the ZigBee Transmit Request API Frame). Then repeat step 6 to transmit data.

7.2. AT Command Programming Examples

Refer to the 'X-CTU' section of the Development Guide [Appendix B] for more information regarding the X-CTU configuration software.

Setup

The programming examples in this section require the installation of MaxStream's X-CTU Software and a serial connection to a PC. (MaxStream stocks RS-232 and USB boards to facilitate interfacing with a PC.)

1. Install MaxStream's X-CTU Software to a PC by double-clicking the "setup_X-CTU.exe" file. (The file is located on the MaxStream CD and under the 'Software' section of the following web page: www.maxstream.net/support/downloads.php)
2. Mount the RF module to an interface board, then connect the module assembly to a PC.
3. Launch the X-CTU Software and select the 'PC Settings' tab. Verify the baud and parity settings of the Com Port match those of the RF module.

NOTE: Failure to enter AT Command Mode is most commonly due to baud rate mismatch. Ensure the 'Baud' setting on the 'PC Settings' tab matches the interface data rate of the RF module. By default, the BD parameter = 3 (which corresponds to 9600 bps).

Sample Configuration: Modify RF Module Destination Address

Example: Utilize the X-CTU "Terminal" tab to change the RF module's DL (Destination Address Low) parameter and save the new address to non-volatile memory.

After establishing a serial connection between the RF module and a PC [refer to the 'Setup' section above], select the "Terminal" tab of the X-CTU Software and enter the following command lines ('CR' stands for carriage return):

Method 1 (One line per command)

Send AT Command	System Response
+++	OK <CR> (Enter into Command Mode)
ATDL <Enter>	{current value} <CR> (Read Destination Address Low)
ATDL1A0D <Enter>	OK <CR> (Modify Destination Address Low)
ATWR <Enter>	OK <CR> (Write to non-volatile memory)
ATCN <Enter>	OK <CR> (Exit Command Mode)

Method 2 (Multiple commands on one line)

Send AT Command	System Response
+++	OK <CR> (Enter into Command Mode)
ATDL <Enter>	{current value} <CR> (Read Destination Address Low)
ATDL1A0D,WR,CN <Enter>	OK<CR> OK<CR> OK<CR>

Sample Configuration: Restore RF Module Defaults

Example: Utilize the X-CTU "Modem Configuration" tab to restore default parameter values.

After establishing a connection between the module and a PC [refer to the 'Setup' section above], select the "Modem Configuration" tab of the X-CTU Software.

1. Select the 'Read' button.
2. Select the 'Restore' button.

8. Manufacturing Support

8.1. Interoperability with other EM250 Devices

The XBee module may integrate functionality to some extent with other EM250 based devices. The following should be considered when communicating between a MaxStream XBee module and another EM250-based device.

8.1.1. XBee Data Transmission and Reception

The XBee firmware inserts 8 bytes at the beginning of the data payload that represent the 64-bit address of the source module. Custom devices that transmit to an XBee or receive data from an XBee should make provisions to manage these 8 address bytes in the payload. Data packets destined for an XBee module should include the source address of the sending device with the most significant byte copied first.

8.1.2. Customizing XBee Default Parameters

Once module parameters are determined, MaxStream can manufacture modules with specific customer-defined configurations. These custom configurations can lock in a firmware version or set command values when the modules are manufactured, eliminating the need for customers to adjust module parameters on arrival. Contact MaxStream to create a custom configuration.

8.1.3. XBee Series 2 Custom Bootloader

XBee Series 2 modules use a modified version of Ember's boot loader. This version supports a custom entry mechanism. To invoke the boot loader, do the following:

1. Set DTR low (TTL 0V) and RTS high.
2. Send a serial break to the DIN pin and power cycle or reset the module.
3. When the module powers up, DTR and DIN should be low (TTL 0V) and RTS should be high.
4. Terminate the serial break and send a carriage return at 115200bps to the module.
5. If successful, the module will send the Ember boot loader menu out the DOUT pin at 115200bps.
6. Commands can be sent to the boot loader at 115200bps.

Programming XBee Series 2 Modules

Firmware on the XBee Series 2 modules can be upgraded using the MaxStream x-CTU program to interface with the DIN and DOUT serial lines, or with an InSight programmer device via InSight header.

Appendix A:Definitions

Definitions

Table A-01. Terms and Definitions

ZigBee Node Types	
Coordinator	A node that has the unique function of forming a network. The coordinator is responsible for establishing the operating channel and PAN ID for an entire network. Once established, the coordinator can form a network by allowing routers and end devices to join to it. Once the network is formed, the coordinator functions like a router (it can participate in routing packets and be a source or destination for data packets). -- One coordinator per PAN -- Establishes/Organizes PAN -- Can route data packets to/from other nodes -- Can be a data packet source and destination -- Mains-powered Refer to the XBee Series 2 coordinator section for more information.
Router	A node that creates/maintains network information and uses this information to determine the best route for a data packet. A router must join a network before it can allow other routers and end devices to join to it. A router can participate in routing packets and is intended to be a mains-powered node. -- Several routers can operate in one PAN -- Can route data packets to/from other nodes -- Can be a data packet source and destination -- Mains-powered Refer to the XBee Series 2 router section for more information.
End device	End devices must always interact with their parent to receive or transmit data. (See 'joining definition.) They are intended to sleep periodically and therefore have no routing capacity. An end device can be a source or destination for data packets but cannot route packets. End devices can be battery-powered and offer low-power operation. -- Several end devices can operate in one PAN -- Can be a data packet source and destination -- All messages are relayed through a coordinator or router -- Lower power modes
ZigBee Protocol	
PAN	Personal Area Network - A data communication network that includes a coordinator and one or more routers/end devices.

Table A-01. Terms and Definitions

Joining	The process of a node becoming part of a ZigBee PAN. A node becomes part of a network by joining to a coordinator or a router (that has previously joined to the network). During the process of joining, the node that allowed joining (the parent) assigns a 16-bit address to the joining node (the child).
Network Address	The 16-bit address assigned to a node after it has joined to another node. The coordinator always has a network address of 0.
Operating Channel	The frequency selected for data communications between nodes. The operating channel is selected by the coordinator on power-up.
Energy Scan	A scan of RF channels that detects the amount of energy present on the selected channels. The coordinator uses the energy scan to determine the operating channel.
Route Request	Broadcast transmission sent by a coordinator or router throughout the network in attempt to establish a route to a destination node.
Route Reply	Unicast transmission sent back to the originator of the route request. It is initiated by a node when it receives a route request packet and its address matches the Destination Address in the route request packet.
Route Discovery	The process of establishing a route to a destination node when one does not exist in the Routing Table. It is based on the AODV (Ad-hoc On-demand Distance Vector routing) protocol.
ZigBee Stack	ZigBee is a published specification set of high-level communication protocols for use with small, low-power modules. The ZigBee stack provides a layer of network functionality on top of the 802.15.4 specification. For example, the mesh and routing capabilities available to ZigBee solutions are absent in the 802.15.4 protocol.

Appendix B: Migrating from the 802.15.4 Protocol

This following are some of the differences in the ZigBee firmware assuming familiarity with the 802.15.4 application:

- ZigBee Command Set
- Address Assignment
- API / AT Firmware Versions

Also, refer to the "Getting Started" section for more information.

ZigBee Command Set

Modified Commands

- CH - Read Only command that displays the operating channel that was selected from SC.
- MY - Read Only command that displays the assigned 16-bit Network Address of the device.
- AI - ZigBee definitions added to this command. See documentation.
- A1, A2 and CE commands are not supported.

New Commands

- NJ (Node Join Time) - This value determines how long a Coordinator or Router will allow other devices to join to it. This command is supported on Coordinators & Routers only.
- MP (16-bit Parent Network Address). This value represents the 16-bit parent Network Address of the module.
- BH (Broadcast Hops). This value sets the maximum number of hops for each broadcast data transmission. Setting this to 0 will use the maximum number of hops.

API & AT Firmware Versions

The 802.15.4 firmware supports the AP command for setting the module into No API (AP=0), API without escaping (AP=1), or API with escaping (AP=2) modes. The first digit in the 802.15.4 firmware versions is a '1'.

The ZigBee firmware comes in different versions to support the API interface (AP 1, 2 modes) or the AT command set (AP 0 mode). The first digit in the ZigBee firmware versions is an '8'.

The following is a list of firmware versions:

- 1.0xx - Coordinator, AT Command support (Transparent Mode)
- 1.1xx - Coordinator, API support (AP 1, 2)
- 1.2xx - Router, End Device, AT Command support (Transparent Mode)
- 1.3xx - Router, End Device, API support (AP 1, 2)

Appendix C: Agency Certifications

FCC, IC, and ETSI approvals pending.

Appendix D: Development Guide

XBee Series 2 Development Kits

The XBee Series 2 Professional Development Kit includes the hardware and software needed to rapidly create long range wireless data links between nodes (XBee Series 2 Starter Kits that contain fewer modules and accessories are also available).

Table D-01. Items Included in the Development Kit

Item	Qty.	Description	Part #
XBee Series 2 Module	5	(1) OEM RF Module, AT Coordinator with wire antenna (1) OEM RF Module, AT Router/End Device with wire antenna (1) OEM RF Module, AT Router/End Device with U.FL antenna (1) OEM RF Module, AT Router/End Device with chip antenna (1) OEM RF Module, AT Router/End Device with SMA antenna	XB24-BWIt-002 XB24-BWIT-004 XB24-BUIT-004 XB24-BCIT-004 XB24-BSIT-004
RS-232 Development Board	4	Board for interfacing between modules and RS-232 nodes (Converts signal levels, displays diagnostic info, & more)	XBIB-R
USB Development Board	1	Board for interfacing between modules & USB nodes (Converts signal levels, displays diagnostic info, & more)	XBIB-U
RS-232 Cable (6', straight-through)	1	Cable for connecting RS-232 interface board with DTE nodes (nodes that have a male serial DB-9 port - such as most PCs)	JD2D3-CDS-6F
USB Cable (6')	1	Cable for connecting USB interface board to USB nodes	JU1U2-CSB-6F
Serial Loopback Adapter	1	[Red] Adapter for configuring the module assembly (module + RS-232 interface board) to function as a repeater for range testing	JD2D3-CDL-A
NULL Modem Adapter (male-to-male)	1	[Black] Adapter for connecting the module assembly (module + RS-232 interface board) to other DCE (female DB-9) nodes	JD2D2-CDN-A
NULL Modem Adapter (female-to-female)	1	[Gray] Adapter for connecting serial nodes. It allows users to bypass the radios to verify serial cabling is functioning properly.	JD3D3-CDN-A
Power Adapter (9VDC, 1 A)	1	Adapter for powering the RS-232 development board	JP5P2-9V11-6F
Battery Clip (9V)	1	Clip for remotely powering the RS-232 board w/ a 9V battery	JP2P3-C2C-4I
RPSMA Antenna	2	RPSMA half-wave dipole antenna (2.4 GHz, 2.1 dB)	A24-HASM-450
RF Cable Assembly	2	Adapter for connecting RPSMA antenna to U.FL connector	JF1R6-CR3-4I
CD	1	Documentation and Software	MD0030
Quick Start Guide	1	Step-by-step instruction on how to create wireless links & test range capabilities of the modules	MD0026

Interfacing Options

The development kit includes RS-232 and USB interface boards. The boards provide a connection to PC ports and therefore give access to the RF module registries. Parameters stored in the registry allow OEMs and integrators to customize the modules to suite the needs of their data radio systems.

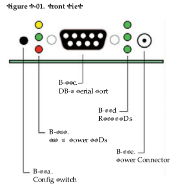
The following sections illustrate how to use the interface boards for development purposes. The MaxStream Interface board provides means for connecting the module to any node that has an available RS-232 or USB connector. Since the module requires signals to enter at TTL voltages, one of the main functions of the interface board is to convert signals between TTL levels and RS-232 and USB levels.

Note: In the following sections, an OEM RF Module mounted to an interface board will be referred to as a "Module Assembly".

RS-232 Development Board

External Interface

Figure D-01. Front View



B-01a. Reset Switch

The Reset Switch is used to reset (re-boot) the RF module. This switch only applies when using the configuration tabs of MaxStream's X-CTU Software.

B-01b. I/O & Power LEDs

LEDs indicate RF module activity as follows:

Yellow (top LED) = Serial Data Out (to host)
Green (middle) = Serial Data In (from host)
Red (bottom) = Power/Association Indicator (Refer to the D5 (DIO5 Configuration) parameter)

B-01c. Serial Port

Standard female DB-9 (RS-232) connector.

B-01d. RSSI LEDs

RSSI LEDs indicate the amount of fade margin present in an active wireless link. Fade margin is defined as the difference between the incoming signal strength and the module's receiver sensitivity.

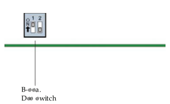
3 LEDs ON = Very Strong Signal (> 30 dB fade margin)
2 LEDs ON = Strong Signal (> 20 dB fade margin)
1 LED ON = Moderate Signal (> 10 dB fade margin)
0 LED ON = Weak Signal (< 10 dB fade margin)

B-01e. Power Connector

5-14 VDC power connector

B-02a. DIP Switch

Figure D-02. Back View



DIP Switch functions are not supported in this release. Future downloadable firmware versions will support DIP Switch configurations.

RS-232 Pin Signals

Figure D-03. Pins used on the female RS-232 (DB-9) Serial Connector

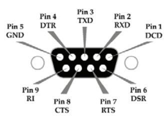


Table D-02. Pin Assignments and Implementations

DB-9 Pin	RS-232 Name	Description	Implementation*
1	DCD	Data-Carrier-Detect	Connected to DSR (pin6)
2	RXD	Receive Data	Serial data exiting the module assembly (to host)
3	TXD	Transmit Data	Serial data entering into the module assembly (from host)
4	DTR	Data-Terminal-Ready	Can enable Power-Down on the module assembly
5	GND	Ground Signal	Ground
6	DSR	Data-Set-Ready	Connected to DCD (pin1)
7	RTS / CMD	Request-to-Send / Command Mode	Provides RTS flow control or enables Command Mode
8	CTS	Clear-to-Send	Provides CTS flow control
9	RI	Ring Indicator	Optional power input that is connected internally to the positive lead of the front power connector

* Functions listed in the implementation column may not be available at the time of release.

Wiring Diagrams

Figure D-04. DTE node (RS-232 male connector) wired to a DCE Module Assembly (female connector)

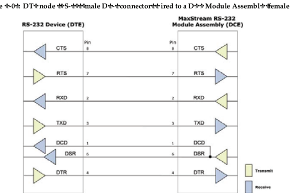
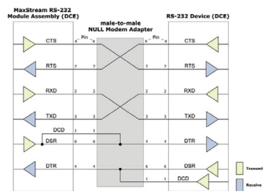
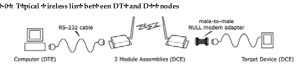


Figure D-05. DCE Module Assembly (female connector) wired to a DCE node (RS-232 male connector)



Sample Wireless Connection: DTE <--> DCE <--> DCE <--> DCE

Figure D-06. Typical wireless link between DTE and DCE nodes



Adapters

The development kit includes several adapters that support the following functions:

- Performing Range Tests
- Testing Cables
- Connecting to other RS-232 DCE and DTE nodes
- Connecting to terminal blocks or RJ-45 (for RS-485/422 nodes)

NULL Modem Adapter (male-to-male)

Part Number: JD2D2-CDN-A (Black, DB-9 M-M) The male-to-male NULL modem adapter is used to connect two DCE nodes. A DCE node connects with a straight-through cable to the male serial port of a computer (DTE).

Figure D-07. Male NULL modem adapter and pinouts

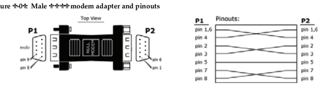
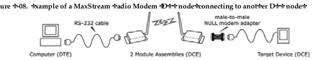


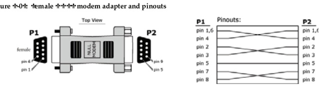
Figure D-08. Example of a MaxStream Radio Modem (DCE node) connecting to another DCE node



NULL Modem Adapter (female-to-female)

Part Number: JD3D3-CDN-A (Gray, DB-9 F-F) The female-to-female NULL modem adapter is used to verify serial cabling is functioning properly. To test cables, insert the female-to-female NULL modem adapter in place of a pair of module assemblies (RS-232 interface board + XTend Module) and test the connection without the modules in the connection.

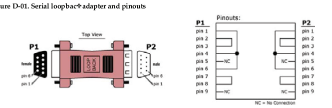
Figure D-09. Female NULL modem adapter and pinouts



Serial Loopback Adapter

Part Number: JD2D3-CDL-A (Red, DB-9 M-F) The serial loopback adapter is used for range testing. During a range test, the serial loopback adapter configures the module to function as a repeater by looping serial data back into the radio for retransmission.

Figure D-01. Serial loopback adapter and pinouts



USB Development Board

External Interface

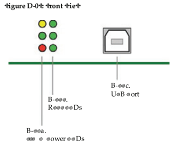


Figure D-0: Front View

B-11a. I/O & Power LEDs

LEDs indicate RF module activity as follows:

Yellow (top LED) = Serial Data Out (to host)
Green (middle) = Serial Data In (from host)
Red (bottom) = Power/Association Indicator (Refer to the D5 (DIO5 Configuration) parameter)

B-11b. RSSI LEDs

RSSI LEDs indicate the amount of fade margin present in an active wireless link. Fade margin is defined as the difference between the incoming signal strength and the module's receiver sensitivity.

3 LEDs ON = Very Strong Signal (> 30 dB fade margin)
2 LEDs ON = Strong Signal (> 20 dB fade margin)
1 LED ON = Moderate Signal (> 10 dB fade margin)
0 LED ON = Weak Signal (< 10 dB fade margin)

B-11c. USB Port

Standard Type-B OEM connector is used to communicate with OEM host and power the RF module.

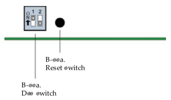


Figure D-0: Back View

B-12a. DIP Switch

DIP Switch functions are not supported in this release. Future downloadable firmware versions will support the DIP Switch configurations.

B-12b. Reset Switch

The Reset Switch is used to reset (re-boot) the RF module.

USB Pin Signals

Table D-0: USB signals and their implantations on the XBee/XBee-PRO RF Module

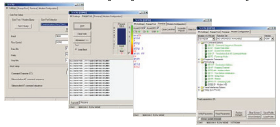
Pin	Name	Description	Implementation
1	VBUS	Power	Power the RF module
2	D-	Transmitted & Received Data	Transmit data to and from the RF module
3	D+	Transmitted & Received Data	Transmit data to and from the RF module
4	GND	Ground Signal	Ground

X-CTU Software

X-CTU is a MaxStream-provided software program used to interface with and configure MaxStream RF Modules. The software application is organized into the following four tabs:

- PC Settings tab - Setup PC serial ports for interfacing with an RF module
- Range Test tab - Test the RF module's range and monitor packets sent and received
- Terminal tab - Set and read RF module parameters using AT Commands
- Modem Configuration tab - Set and read RF module parameters

Figure D-0: X-CTU User Interface (PC Settings, Range Test, Terminal and Modem Configuration tabs)



NOTE: PC Setting values are visible at the bottom of the Range Test, Terminal and Modem Configuration tabs. A shortcut for editing PC Setting values is available by clicking on any of the values.

Install

Double-click the "setup_X-CTU.exe" file and follow prompts of the installation screens. This file is located in the 'software' folder of the MaxStream CD and also under the 'Downloads' section of the following web page: www.maxstream.net/support/downloads.php

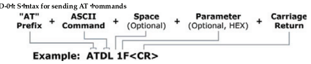
Setup

To use the X-CTU software, a module assembly (An RF module mounted to an interface Board) must be connected to a serial port of a PC. The interface data rate and parity settings of the serial port ("PC Settings" tab) must match those of the module (BD (Baud Rate) and NB (Parity) parameters).

Serial Communications Software

A terminal program is built into the X-CTU Software. Other terminal programs such as "HyperTerminal" can also be used. When issuing AT Commands through a terminal program interface, use the following syntax:

Figure D-0: Syntax for sending AT Commands



NOTE: To read a parameter value stored in a register, leave the parameter field blank.

The example above issues the DL (Destination Address Low) command to change destination address of the module to "0x1F". To save the new value to the module's non-volatile memory, issue WR (Write) command after modifying parameters.

Appendix E: Additional Information

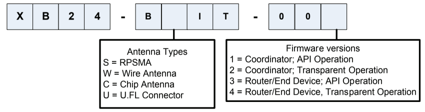
1-Year Warranty

XBee Series 2 RF Modules from MaxStream, Inc. (the "Product") are warranted against defects in materials and workmanship under normal use, for a period of 1-year from the date of purchase. In the event of a product failure due to materials or workmanship, MaxStream will repair or replace the defective product. For warranty service, return the defective product to MaxStream, shipping prepaid, for prompt repair or replacement.

The foregoing sets forth the full extent of MaxStream's warranties regarding the Product. Repair or replacement at MaxStream's option is the exclusive remedy. THIS WARRANTY IS GIVEN IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, AND MAXSTREAM SPECIFICALLY DISCLAIMS ALL WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL MAXSTREAM, ITS SUPPLIERS OR LICENSORS BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, FOR ANY LOSS OF USE, LOSS OF TIME, INCONVENIENCE, COMMERCIAL LOSS, LOST PROFITS OR SAVINGS, OR OTHER INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW. SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES. THEREFORE, THE FOREGOING EXCLUSIONS MAY NOT APPLY IN ALL CASES. This warranty provides specific legal rights. Other rights which vary from state to state may also apply.

Ordering Information

Figure E-01. Divisions of the XBee/XBee-PRO RF Module Part Numbers



Contact MaxStream

Free and unlimited technical support is included with every MaxStream Radio Modem sold. For the best in wireless data solutions and support, please use the following resources:

Documentation: www.maxstream.net/support/downloads.php

Technical Support: Phone. (866) 765-9885 toll-free U.S.A. & Canada
(801) 765-9885 Worldwide

Live Chat. www.maxstream.net

E-Mail. rf-xperts@maxstream.net

MaxStream office hours are 8:00 am - 5:00 pm [U.S. Mountain Standard Time]

Appendix G:

PSoC® Designer™ Code for the WsEMG Electrode System

PSoC C code

```
//
// Wireless Electrode Code for PSoC
//
// Written by Yuting Zhu
//
// 2013
//

//----------------------------------------------------------------------------
// C main line
//----------------------------------------------------------------------------

#include <m8c.h>      // part specific constants and macros
#include "PSoCAPI.h"  // PSoC API definitions for all User Modules
#include "stdlib.h"
#include "delay.h"
#include "string.h"
#pragma interrupt_handler timecount
char *command;
int ADC_Output;
int *status;
int *status1;
int run;
int INSAMPIN;
int INSAMPOUT1;
int INSAMPOUT2;
int x=0;
char start[] = "start";
char stop[] = "stop";
char F1000[] = "F1000";
char F900[] = "F900";
char F800[] = "F800";
char F700[] = "F700";
char F600[] = "F600";
char F500[] = "F500";
char PGA0_5[]="PGA0_5";
char PGA1[]="PGA1";
char PGA2[]="PGA2";
char PGA4[]="PGA4";
char PGA8[]="PGA8";
char PGA16[]="PGA16";
char PGA24[]="PGA24";
char PGA48[]="PGA48";
char INSAMP0_5[]="INSAMP0_5";
char INSAMP1[]="INSAMP1";
char INSAMP2_5[]="INSAMP2_5";
char INSAMP5[]="INSAMP5";
char INSAMP10[]="INSAMP10";
char INSAMP20[]="INSAMP20";
char INSAMP30[]="INSAMP30";
char INSAMP60[]="INSAMP60";
char INSAMP93[]="INSAMP93";
char S10[]="S10";
char S20[]="S20";
char S30[]="S30";
```

```c
char S60[]="S60";
char S90[]="S90";
char S120[]="S120";
char S180[]="S180";
char S240[]="S240";
char S300[]="S300";
int time;

void startpro(void)
{
	INSAMP_Start(INSAMP_HIGHPOWER);
	PGA_Start(PGA_HIGHPOWER);
	LPF2_Start(LPF2_HIGHPOWER);
	DelSig_Start(DelSig_HIGHPOWER);
	DelSig_StartAD();
	Delay10msTimes(10);
	Timer24_Start();
	Timer24_EnableInt();
}

void stoppro(void)
{
	INSAMP_Stop();
	PGA_Stop();
	LPF2_Stop();
	DelSig_Stop();
	DelSig_StopAD();
	Timer24_Stop();
}

void initial(void)
{
	run=0;
	LPF2_SetC1(5);
	LPF2_SetC2(5);
	LPF2_SetC3(12);
	LPF2_SetC4(26);
	LPF2_SetCA(LPF2_FEEDBACK_32);
	LPF2_SetCB(LPF2_FEEDBACK_32);
	PGA_SetGain(PGA_G1_00);
	INSAMP_Set2StageGain(INSAMP_INGAIN_1, INSAMP_OUTGAIN_1_00);
	time=10;
	stoppro();
}

void main(void)
{
	UART_CmdReset();
	UART_IntCntl(UART_ENABLE_RX_INT);
	UART_Start(UART_PARITY_NONE);

  // Uncomment this line to enable Global Interrupts
  M8C_EnableGInt;

  // Insert your main routine code here.
	initial();
	while(1)
	{
```

```
if(UART_bCmdCheck())              // Wait for command
{
	if(command = UART_szGetParam()) // When the command is sent to uC
	{
		if(!strcmp(command,start))
		{
			startpro();
			run=1;
		}
		else if(!strcmp(command,stop)) // command:
		{
			stoppro();
			run=0;
		}
		else if(!strcmp(command,F1000))
		{
			LPF2_SetC1(5);
			LPF2_SetC2(5);
			LPF2_SetC3(12);
			LPF2_SetC4(26);
		}
		else if(!strcmp(command,F900))
		{
			LPF2_SetC1(4);
			LPF2_SetC2(4);
			LPF2_SetC3(13);
			LPF2_SetC4(23);
		}
		else if(!strcmp(command,F800))
		{
			LPF2_SetC1(4);
			LPF2_SetC2(4);
			LPF2_SetC3(11);
			LPF2_SetC4(25);
		}
		else if(!strcmp(command,F700))
		{
			LPF2_SetC1(4);
			LPF2_SetC2(4);
			LPF2_SetC3(9);
			LPF2_SetC4(28);
		}
		else if(!strcmp(command,F600))
		{
			LPF2_SetC1(2);
			LPF2_SetC2(2);
			LPF2_SetC3(14);
			LPF2_SetC4(16);
		}
		else if(!strcmp(command,F500))
		{
			LPF2_SetC1(3);
			LPF2_SetC2(3);
			LPF2_SetC3(7);
			LPF2_SetC4(29);
		}
		else if(!strcmp(command,PGA0_5))
		{
```

```
        PGA_SetGain(PGA_G0_50);
}
else if(!strcmp(command,PGA1))
{
        PGA_SetGain(PGA_G1_00);
}
else if(!strcmp(command,PGA2))
{
        PGA_SetGain(PGA_G2_00);
}
else if(!strcmp(command,PGA4))
{
        PGA_SetGain(PGA_G4_00);
}
else if(!strcmp(command,PGA8))
{
        PGA_SetGain(PGA_G8_00);
}
else if(!strcmp(command,PGA16))
{
        PGA_SetGain(PGA_G16_0);
}
else if(!strcmp(command,PGA24))
{
        PGA_SetGain(PGA_G24_0);
}
else if(!strcmp(command,PGA48))
{
        PGA_SetGain(PGA_G48_0);
}
else if(!strcmp(command,INSAMP0_5))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_1,
                INSAMP_OUTGAIN_0_50);
}
else if(!strcmp(command,INSAMP1))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_1,
                INSAMP_OUTGAIN_1_00);
}
else if(!strcmp(command,INSAMP2_5))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_2,
                INSAMP_OUTGAIN_1_25);
}else if(!strcmp(command,INSAMP5))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_4,
                INSAMP_OUTGAIN_1_25);
}else if(!strcmp(command,INSAMP10))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_8,
                INSAMP_OUTGAIN_1_25);
}else if(!strcmp(command,INSAMP20))
{
        INSAMP_Set2StageGain(INSAMP_INGAIN_16,
                INSAMP_OUTGAIN_1_25);
}else if(!strcmp(command,INSAMP30))
{
```

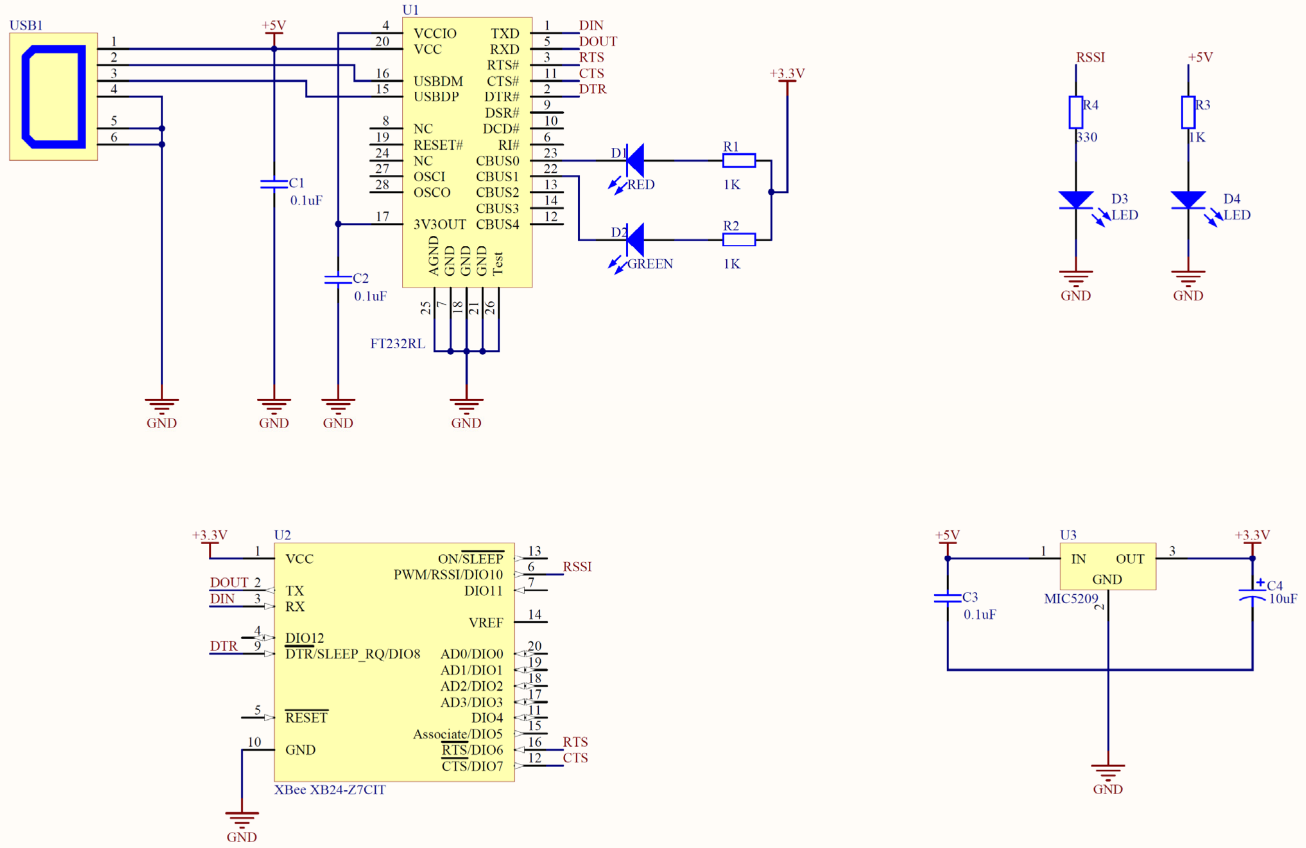
```
				INSAMP_Set2StageGain(INSAMP_INGAIN_24,
					INSAMP_OUTGAIN_1_25);
			}
			else if(!strcmp(command,INSAMP60))
			{
				INSAMP_Set2StageGain(INSAMP_INGAIN_48,
					INSAMP_OUTGAIN_1_25);
			}
			else if(!strcmp(command,INSAMP93))
			{
				INSAMP_Set2StageGain(INSAMP_INGAIN_48,
					INSAMP_OUTGAIN_1_94);
			}
			else if(!strcmp(command,S10))
			{
				time=10;
			}
			else if(!strcmp(command,S20))
			{
				time=20;
			}
			else if(!strcmp(command,S30))
			{
				time=30;
			}
			else if(!strcmp(command,S60))
			{
				time=60;
			}
			else if(!strcmp(command,S90))
			{
				time=90;
			}
			else if(!strcmp(command,S120))
			{
				time=120;
			}
			else if(!strcmp(command,S180))
			{
				time=180;
			}
			else if(!strcmp(command,S240))
			{
				time=240;
			}
			else if(!strcmp(command,S300))
			{
				time=300;
			}
		}
		UART_CmdReset();
	}
	if(run==1)
	{
		while(DelSig_fIsDataAvailable()== 0);
		ADC_Output=DelSig_iGetDataClearFlag();
		UART_PutString(ftoa((float)ADC_Output,status));
		UART_CPutString(" ")
```

```
		}
	}
}

void timecount(void)
{
	x++;
	if(x==time)
	{
		stoppro();
		run=0;
		x=0;
	}
	return;
}
```

Appendix H:

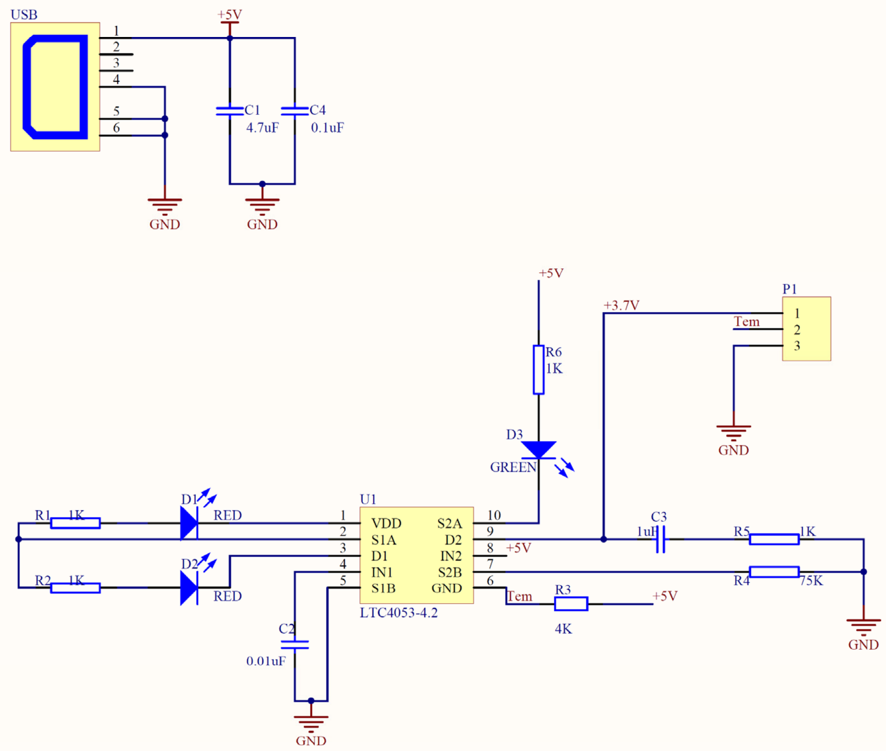
Circuit Diagram for the WsEMG Electrode Interface Node



Title	XBee Dougle Circuit Design		
Size A4	Number		Revision
Date:	22/11/2013	Sheet of	XBee Dougle
File:	C:\Users\..\XBee Dougle.SchDoc	Drawn By:	Yuting Zhu

Appendix I:

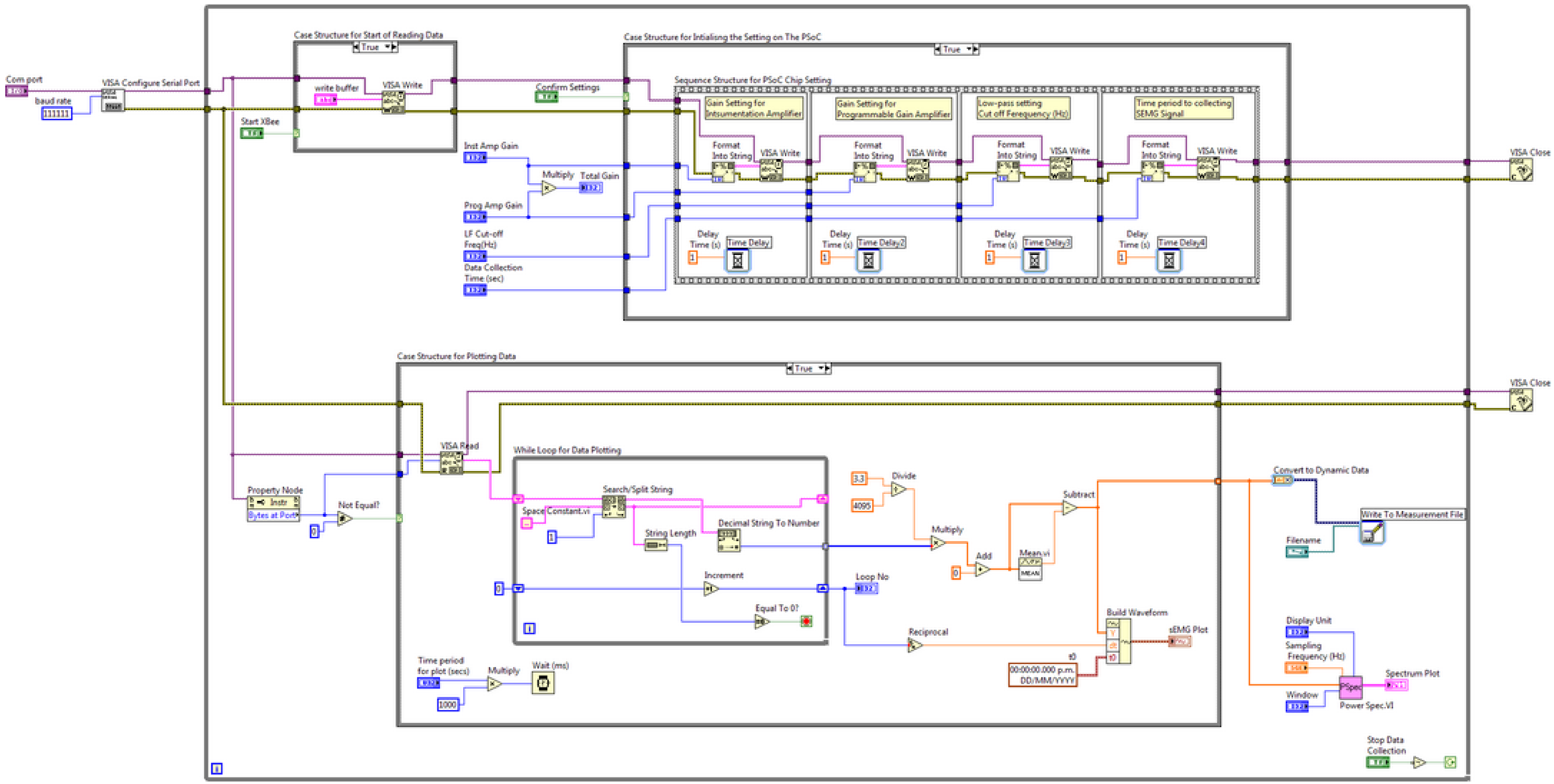
Circuit Diagram for Lithium-ion Polymer Battery Charger



Title	Battery Charger Circuit Design		
Size: A4	Number		Revision
Date: 22/11/2013		Sheet of	Battery Charger
File: C:\Users\..\Battery.SchDoc		Drawn By:	Yuting Zhu

Appendix J:

LabVIEW Block Diagram for Data Acquisition


Com port
baud rate
111111
VISA Configure Serial Port
Case Structure for Start of Reading Data
True
write buffer
VISA Write
Start XBee
Confirm Settings
Case Structure for Intialising the Setting on The PSoC
Sequence Structure for PSoC Chip Setting
Gain Setting for Intsumentation Amplifier
Gain Setting for Programmable Gain Amplifier
Low-pass setting Cut off Ferequency (Hz)
Time period to collecting SEMG Signal
Format Into String
VISA Write
Inst Amp Gain
Multiply
Total Gain
Prog Amp Gain
LF Cut-off Freq(Hz)
Data Collection Time (sec)
Delay Time (s)
Time Delay
Time Delay2
Time Delay3
Time Delay4
VISA Close
Case Structure for Plotting Data
VISA Read
While Loop for Data Plotting
Property Node
Instr
Bytes at Port
Not Equal?
Search/Split String
Space Constant.vi
String Length
Decimal String To Number
Increment
Equal To 0?
Loop No
Divide
3.3
4095
Multiply
Add
Mean.vi
Subtract
Reciprocal
Build Waveform
sEMG Plot
00:00:00.000 p.m. DD/MM/YYYY
Time period for plot (secs)
Multiply
1000
Wait (ms)
Convert to Dynamic Data
Write To Measurement File
Filename
Display Unit
Sampling Frequency (Hz)
Window
Power Spec.VI
Spectrum Plot
Stop Data Collection

Appendix K:

Ethics Approval

MEMORANDUM

Auckland University of Technology Ethics Committee (AUTEC)

To: Jeffrey Kilby
From: **Dr Rosemary Godbold** Executive Secretary, AUTEC
Date: 15 May 2012
Subject: Ethics Application Number 12/48 **Wireless electrodes for the collection of surface electromyography signals.**

Dear Jeffrey

Thank you for providing written evidence as requested. I am pleased to advise that it satisfies the points raised by the Auckland University of Technology Ethics Committee (AUTEC) at their meeting on 12 March 2012 and I have approved your ethics application. This delegated approval is made in accordance with section 5.3.2.3 of AUTEC's *Applying for Ethics Approval: Guidelines and Procedures* and is subject to endorsement at AUTEC's meeting on 28 May 2012.

Your ethics application is approved for a period of three years until 15 May 2015.

I advise that as part of the ethics approval process, you are required to submit the following to AUTEC:

- A brief annual progress report using form EA2, which is available online through http://www.aut.ac.nz/research/research-ethics/ethics. When necessary this form may also be used to request an extension of the approval at least one month prior to its expiry on 15 May 2015;
- A brief report on the status of the project using form EA3, which is available online through http://www.aut.ac.nz/research/research-ethics/ethics. This report is to be submitted either when the approval expires on 15 May 2015 or on completion of the project, whichever comes sooner;

It is a condition of approval that AUTEC is notified of any adverse events or if the research does not commence. AUTEC approval needs to be sought for any alteration to the research, including any alteration of or addition to any documents that are provided to participants. You are reminded that, as applicant, you are responsible for ensuring that research undertaken under this approval occurs within the parameters outlined in the approved application.

Please note that AUTEC grants ethical approval only. If you require management approval from an institution or organisation for your research, then you will need to make the arrangements necessary to obtain this.

To enable us to provide you with efficient service, we ask that you use the application number and study title in all written and verbal correspondence with us. Should you have any further enquiries regarding this matter, you are welcome to contact me by email at ethics@aut.ac.nz or by telephone on 921 9999 at extension 6902. Alternatively you may contact your AUTEC Faculty Representative (a list with contact details may be found in the Ethics Knowledge Base at http://www.aut.ac.nz/research/research-ethics/ethics).

On behalf of AUTEC and myself, I wish you success with your research and look forward to reading about it in your reports.

Yours sincerely

Dr Rosemary Godbold
Executive Secretary
Auckland University of Technology Ethics Committee

Cc: Yuting Zhu yuting.zhu@aut.ac.nz

Auckland University of Technology Ethics Committee (AUTEC)

EA1

APPLICATION FOR ETHICS APPROVAL FOR RESEARCH PROJECTS

Comprehensive information about AUT's ethics approval processes may be found online at http://www.aut.ac.nz/research/research-ethics/ethics. Please read the notes at the end of the form before submitting this application.

A. General Information

A.1. Project Title

If you will be using a different title in documents to that being used as your working title, please provide both, clearly indicating which title will be used for what purpose.

Wireless Electrodes for the Collection of Surface Electromyography Signals

A.2. Applicant Name and Qualifications

When the researcher is a student (including staff who are AUT students), the applicant is the principal supervisor. When the researcher is an AUT staff member undertaking research as part of employment or a staff member undertaking research as part of an external qualification, the applicant is the researcher. Staff should refer to Section 11.4 of Applying for Ethics Approval: Guidelines and Procedures *to check requirements for ethics approval where they are studying at another institution.*

Jeffrey Kilby, Master of Engineering (Honours)

A.3. Applicant's School/Department/Academic Group/Centre

School of Engineering/Department of Electrical and Electronics/ Signal and Systems Group

A.4. Applicant's Faculty

Design and Creative Technologies

A.5. Student Details

Please complete this section only if the research is being undertaken by a student as part of an AUT qualification.

A.5.1. Student Name(s):

Yuting Zhu

A.5.2. Student ID Number(s):

0000531

A.5.3. Completed Qualification(s):

Bachelor of Engineering Technology in Computer Systems
Post Diploma in Engineering

A.5.4. E-mail address:

yuting.zhu@aut.ac.nz

A.5.5. School/Department/Academic Group/Centre

School of Sport and Recreation

A.5.6. Faculty

Health and Environmental Sciences

A.5.7. Name of the qualification for which this research is being undertaken:

MPhil

A.5.8. Research Output

Please state whether your research will result in a thesis or dissertation or a research paper or is part of coursework requirements.

Thesis

A.6. Details of Other Researchers or Investigators

Please complete this section only if other researchers, investigators or organisations are involved in this project. Please also specify the role any other researcher(s), investigator(s) or organisation(s) will have in the research.

A.6.1. Individual Researcher(s) or Investigator(s)

Please provide the name of each researcher or investigator and the institution in which they research.

A.6.2. Research or Investigator Organisations

Please provide the name of each organisation and the city in which the organisation is located.

A.7. Are you applying concurrently to another ethics committee?

If your answer is yes, please provide full details, including the meeting date, and attach copies of the full application and approval letter if it has been approved.

No

A.8. Declaration

The information supplied is, to the best of my knowledge and belief, accurate. I have read the current Guidelines, published by the Auckland University of Technology Ethics Committee, and clearly understand my obligations and the rights of the participant, particularly with regard to informed consent.

Signature of Applicant   Date

(*In the case of student applications the signature must be that of the Supervisor*)

Signature of Student   Date

(*If the research is a student project, both the signature of the Supervisor, as the applicant, and the student are required*)

A.9. Authorising Signature

Signature of Head   Name of Faculty/Programme/School/Centre   Date

B. General Project Information

B.1. Project Duration

B.1.1. Approximate Start Date of Primary Data Collection

April 2012 (Once AUTEC approval is granted)

B.1.2. Approximate Finish Date of Complete Project

August 2012

B.2. Are funds being obtained specifically for this project?

If your answer is yes, then you must complete section G of this Application Form.

No

B.3. Types of persons participating as participants

Please indicate clearly every one of the following categories that applies to those participating in your research.

B.3.1. Researcher's students

No

B.3.2. Adults (20 years and above)

Yes

B.3.3. Legal minors (16 to 20 years old)

Yes

B.3.4. Legal minors (under 16 years old)

No

B.3.5. Members of vulnerable groups

e.g. persons with impairments, limited understanding, etc. If your answer is yes, please provide a full description.

No

B.3.6. Hospital patients

No

B.3.7. Prisoners

No

B.4. Does this research involve use of human remains, tissue or body fluids which does not require submission to a Regional Ethics Committee?

e.g. finger pricks, urine samples, etc. (please refer to section 13 of the AUTEC Guidelines). If your answer is yes, please provide full details of all arrangements, including details of agreements for treatment, how participants will be able to request return of their samples in accordance with right 7 (9) of the Code of Health and Disability Services Consumers' Rights, *etc.*

No

B.5. Does this research involve potentially hazardous substances?

e.g. radioactive materials (please refer to section 15 of the AUTEC Guidelines). If your answer is yes, please provide full details.

No

B.6. Research Instruments

B.6.1. Does the research include the use of a written or electronic questionnaire or survey?

If your answer is yes, please attach to this application form a copy of the finalised questionnaire or survey in the format that it will be presented to participants.

Yes included on the Consent Form.

B.6.2. Does the research involve the use of focus groups or interviews?

If the answer is yes, please indicate how the data will be recorded (e.g. audiotape, videotape, note-taking). When interviews or focus groups are being recorded, you will need to make sure there is provision for explicit consent on the Consent Form and attach to this Application Form examples of indicative questions or the full interview or focus group schedule.

No

B.6.3. Does the research involve the use of observation?

If the answer is 'Yes', please attach to this application a copy of the observation protocol that will be used.

No

B.6.4. Does the research involve the use of other research instruments such as performance tests?

If the answer is yes, please attach to this application a copy of the protocols for the instruments and the instruments that will be used to record results.

Yes

B.6.5. Who will be transcribing or recording the data?

If someone other than the researcher will be transcribing the interview or focus group records or taking the notes, you need to provide a confidentiality agreement with this Application Form.

Yuting Zhu

B.7. How does the design and practice of this research implement each of the three principles of the Treaty of Waitangi (Partnership, Participation and Protection) in the relationships between the researcher and other participants?

Please refer to Section 2.5 of AUTEC's Applying for Ethics Approval: Guidelines and Procedures *(accessible in the Ethics Knowledge Base (http://www.aut.ac.nz/research/research-ethics/ethics) and to the relevant Frequently Asked Questions section in the Ethics Knowledge Base.*

The participants for this research will represent a wide cross-section of race and culture. While there will be a dedicated partnership between the participants and researcher. The research will include a commitment to the Treaty of Waitangi with the encouragement of a partnership, participation and protection with a respect for the different values, practices and beliefs of all cultures.

The partnership will be between the researcher and the participant where a copy of the participant results would be available at the end of the completed research if requested.

The participation in this research provides the participants with information in both a written and verbal format to allow individuals to make an informed decision on whether they would like to take part.

The protection of the participant's data collect from the consent form and the electrodes will be to ensure the participant that it is to be securely held in the researcher's office for ten years after which time it will be destroyed.

B.8. Does this research target Maori participants?

No

B.8.1. If 'Yes", what consultation has been undertaken when designing the research?

Please identify the group(s) with whom consultation has occurred and provide evidence of their support and any impact this consultation had on the design of the research. Researchers are advised to read the Health Research Council's Guidelines for researchers on health research involving Maori, *available via the Ethics Knowledge Base.*

B.9. Does this research target participants of particular cultures or social groups?

Please refer to Section 2.5 of AUTEC's Applying for Ethics Approval: Guidelines and Procedures *(accessible in the Ethics Knowledge Base (http://www.aut.ac.nz/research/research-ethics/ethics) and to the relevant Frequently Asked Questions section in the Ethics Knowledge Base.*

No

B.9.1. If 'Yes" please identify which cultures or social groups are being targeted and how their cultures or social groups are being considered in the research design.

B.9.2. If your answer to B.9 was 'Yes", what consultation has occurred with these cultures or social groups in the design of the research?

Please identify the group(s) with whom consultation has occurred and provide evidence of their support and any impact this consultation had on the design of the research.

B.10. Is there a need for translation or interpreting?

If your answer is 'Yes', please provide copies of any translations with this application and any Confidentiality Agreement required for translators or interpreters.

No

C. Project Details

Please describe the project details in language which is, as far as possible, free from jargon and comprehensible to lay people.

C.1. Aim of project:

Please explain the broad scope and purpose of the project and state concisely how the type of information being sought will achieve the project's aims. Please give the specific hypothesis(es), if any, to be tested.

To collect surface electromyography from newly developed wireless electrodes from 20 subjects.

This project is part research that enhances a field of research presently being carried out at AUT University that has a potential for further research in the field of surface electromyography (EMG) signals.

This research is being done in collaboration with the Department in Sports and Recreation within the Faculty of Health and School of Engineering within the Faculty of Creative and Design Technologies at AUT University is the Sports Performance Research Institute New Zealand (SPRINZ).

C.2. Why are you proposing this research?

(ie what are its potential benefits to participants, researcher, wider community, etc?)

Research benefits are to establish and more suitable more accurate analysis or technique in detecting muscles activity for sports and recreation applications. This will widen and develop future research opportunities within the Performance Research Institute New Zealand (SPRINZ) at AUT University.

C.3. Background:

Please provide sufficient information, including relevant references, to place the project in perspective and to allow the project's significance to be assessed. Where appropriate, provide one or two references to the applicant's (or supervisor's) own published work in the relevant field.

Electromyography (EMG) research is based on measuring and studying the electrical activity that is produced by skeletal muscles of interest during movement or muscle contraction [1]. The study of EMG shows that muscles are electrically silent at rest [1-4]. However, when the muscle is active during contraction, it produces force that causes an electrical current to generate microvolt level electrical signals [1-4]. These signals can be measured at the surface of the body. There are two methods known for collecting EMG signals. One method is by penetrating into the muscle using needle sensors or electrodes. This is called needle EMG and is referred as an invasive technique [1, 5]. The other method is by placing the sensory electrodes on the surface of the skin without penetrating it. This technique is called Surface Electromyography (sEMG) and is a non-invasive technique [1, 5-7].

Traditionally sEMG data collection systems employ skin mounted sensors that transmit data to the computer via a cable which also supplies power the sensors electronic components [6, 8]. A typical sEMG analysis requires multiple sensors with each representing a unique data channel position on the subject's body [6, 8]. As the number of sensors increases, the subject's freedom of mobility decreases due to the lengthy cables linked to each sensor. A purpose wireless sensor system to be developed for this research using ZigBee technology would offer an attractive alternative to traditionally wired sEMG sensors and so the subject's mobility would be less compromised when collecting data.

Wireless sensors are being used increasing in the automotive industry, agricultural, industrial monitoring and many other areas. This technology provides no connectors, safe/flexible connectivity, improves resource sharing, easy installation and mobility [9-11]. The other advantage is the system uses low power levels, thus it can last for a longer period of time [9-11]. Two major protocols are used in wireless networking, IEE 802.15.4 and ZigBee stack.

The ZigBee stack sits on top of IEEE 802.15.4 standard medium access control and physical layers. Both layers define the RF and communication components between other devices. The ZigBee stack contains the network layer, an application layer and security service provider [9-11].

C.4. Procedure:

C.4.1. Explain the philosophical and/or methodological approach taken to obtaining information and/or testing the hypothesis(es).

Procedures

When potential participants make contact with the researcher they will be screened for inclusion and exclusion criteria. If appropriate to participate in the study, they will receive a verbal explanation of what is involved. Prior to assessment, procedures will be explained to the participant and time will be given for the participant to have any remaining questions answered before written consent is obtained.

C.4.2. State in practical terms what research procedures or methods will be used.

Maximal strength test:

Participants will perform a five-minute generalised warm up that will include riding an exer-cycle at a self selected pace and performing range of motion exercises for the lower limbs. After the general warm-up is completed, participants will be seated in the upright chair of the HUMAC®/NORM™ Testing and Rehabilitation System (Computer Sports Medicine, Inc) with their knee bent to 80 degrees and attached to load cell that measures voluntary isometric force of the quadriceps. The upper body and upper thigh of the subject will be securely strapped to the chair and the leg will be strapped to the load cell at mid-shin level. The subject will then perform a specific warm-up and familiarisation of a series of 4 sets of short (5 seconds) sub-maximal isometric knee extensions. The intensity of the contractions will be gradually increased against the resistance of the load cell and within the subject's own limits. A one-minute rest will follow each set of warm-up contractions. The subject will then rest for 3 minutes before the maximal voluntary isometric force (MVIF) of the quadriceps is measured. Three MVIF's will be measured and recorded for a 5 second period. There will be a two-minute rest period between each MVIF test and the highest MVIF will be selected for analysis. Standardised verbal encouragement will be given throughout the test from the force-to-failure point.

Ramped isometric knee extension test:

Following the Maximal strength test participants, will perform the ramped force production test. Force data from the maximal strength test will be transferred to a computer software programme that will calculate individual force values for 50% of maximal force. The force data for 50% level of MVIF will be displayed on the screen for feedback to the participant. The participant will then be required to perform and sustained isometric contraction of the knee for a given force level for a period of 10 seconds.

Electromyography (EMG) Measures:

Muscle activity will be recorded using new developed wireless surface electrodes plus amplifier. The equipment is electrically isolated and all cables are specifically shielded and grounded for human use. There is no risk of electric shock to the researcher or subject. Following appropriate skin preparation (the skin is shaved, then gently abraded and cleaned with alcohol) the new wireless surface electrodes will be place on the skin surface overlying vastus lateralis muscles of the thigh using standardised procedures.

C.4.3. State how information will be gathered and processed.

The EMG signal from an available the new wireless surface electrode will be amplified with a gain of either of the following values 10, 100 or 1000, bandwidth filtered between 5 and 500 Hz. Raw analogue signals will then be converted to digital data and recorded via National Instrument LabVIEW data acquisition software program at a frequency of 2048 Hz, for a period of 10 seconds for each muscle contraction.

C.4.4. State how your data will be analysed.

The data will then be transferred to MathWorks MATLAB software using standard signal processing analysis technique to analyse the frequency component and characteristics of the EMG signals.

C.4.5. Provide the statistical or methodological justification for this.

Fast Fourier Transform (FFT) and Short Time Fourier Transform (STFT) standard signal processing techniques will be used to analyse the collected data using MathWorks MATLAB software.

C.5. References

Please include the references for your responses to this section in the standard format used in your discipline.

1. Basmajian, J.V. and C.J. De Luca, *Muscles alive: their functions revealed by electromyography*. 5th ed. 1985, Baltimore: Williams and Wilkins.
2. Keynes, R.D. and D.J. Aidley, *Nerve and Muscle*. Third ed. 2001, Cambridge, United Kingdom: Cambridge University Press. 118-120.
3. Winter, D.A., *Biomechanics and Motor Control of Human Movement*. Third ed. 2005, Hoboken, New Jersey: John Wiley & Sons.
4. Jones, D., J. Round, and A. de Haan, *Skeletal Muscle From Molecules to Movement*. First ed. 2004, Philadelphia, U.S.: Churchill Livingstone.
5. Merletti, R. and P. Parker, *Electromyography Physiology, Engineering and Noninvasive Applications*. First ed. 2004, Hoboken, New Jersey: John Wiley & Sons.
6. Merletti, R., et al., *Technology and instrumentation for detection and conditioning of the surface electromyographic signal: State of the art*. Clinical Biomechanics, 2009. **24**(2): p. 122-134.
7. Cram, J.R., G.S. Kasman, and J. Holtz, *Introduction to Surface Electromyography*. 1998, Gaithersburg, Maryland, USA: Aspen Publishers. 49.
8. Carr, J.J. and J.M. Other Authors: Brown, *Introduction to biomedical equipment technology*. 4th ed. 2000, Upper Saddle River, N.J.
9. Gianluigi Ferrari, e., *Sensor networks : where theory meets practice*. 2010: Heidelberg : Springer, c2010.
10. Gislason, D., *Zigbee Wireless Networking* 2008, Oxford ;New York :.
11. Mauri Kuorilehto, M.K., Jukka Suhonen, Panu Hämäläinen, Marko Hännikäinen, Timo D. Hamalainen *Ultra-Low Energy Wireless Sensor Networks in Practice: Theory, Realization and Deployment* December 2007: WILEY.

D. Participants

D.1. Who are the participants?

Twenty subjects with no previous history of knee or severe musculoskeletal injury will participate in the study. Subjects will be students recruited from the North Shore Campus. Request notices will be posted on notice boards. Subjects will be male or female between the ages of 18 and 35 with no history of knee injury within the last year.

D.1.1. What criteria are to be used in recruiting the participants?

Subjects will be male or female between the ages of 18 and 35 with no history of knee injury within the last year.

D.1.2. What criteria are to be used for selecting participants from those recruited?

None

D.1.3. Are there any potential participants who will be excluded?

If your answer is yes, please detail the criteria for exclusion.

Yes.

Individuals will be excluded if they have had a knee injury within the last year, had any previous knee surgery, and have any current cardiovascular, neurological, cognitive or musculoskeletal ailments.

People with knee injury or leg muscles or any form of medication that may seem relevant to give an unsatisfactory result related to this research.

D.2. Are there any potential conflicts of interest or possible coercive influences in the professional, social, or cultural relationships between the researcher and the participants (e.g. dependent relationships such as teacher/student; parent/child; employer/employee; pastor/congregation etc.)?

No

D.2.1. If your answer was 'Yes', please identify the nature of the relationships concerned and provide full information about the processes being incorporated into the research design to mitigate any adverse affects that may arise from them.

D.3. How many participants will be selected?

10 for first which is development phase.

10 for second which is for verification.

D.3.1. What is the reason for selecting this number?

A small number is required in the development phase to ensure the wireless is performing correctly to the theoretical calculations. Then after any modifications that may be need after the in the development stage testing a similar small number is need to verify any changes made in the development phase are working satisfactory.

D.3.2. Provide a statistical justification where applicable, if you have not already provided one in C.4 5. above.

Not applicable

D.3.3. Is there a control group?

If your answer is yes, please describe and state how many are in the control group.

No

D.4. Describe in detail the recruitment methods to be used.

If you will be recruiting by advertisement or email, please attach a copy to this Application Form

This will be achieved by placing advertising posters at AUT North Shore campus asking for volunteers to participate in this research project.

D.5. How will information about the project be given to participants?

(e.g. in writing, verbally). A copy of information to be given to prospective participants is to be attached to this Application Form. If written information is to be provided to participants, you are advised to use the Information Sheet exemplar.

Information about the project will be given to participants in writing.

D.6. Will the participants have difficulty giving informed consent on their own behalf?

Consider physical or mental condition, age, language, legal status, or other barriers. If the answer is yes, please provide full details.

No

D.6.1. If participants are not competent to give fully informed consent, who will consent on their behalf?

D.6.2. Will these participants be asked to provide assent to participation?

If the answer is yes, please attach a copy of the assent form which will be used. Please note that assent is not the same as consent (please refer to the Glossary in Appendix A of the AUTEC Guidelines and Procedures.

D.7. Will consent of participants be gained in writing?

If the answer is yes, please attach a copy of the Consent Form which will be used. If the answer is No, please provide the reasons for this.

Yes

D.8. Will the participants remain anonymous to the researcher?

Please note that anonymity and confidentiality are different. If the answer is yes, please state how, otherwise, if the answer is no, please describe how participant privacy issues and confidentiality of information will be preserved.

At the time of data collection, participants will not be anonymous to the researcher as both will be interacting. However, no participants will be individually identified in the writing up of the research results. All written consent forms and personal data on external data storage devices will be held in secure location in the Yuting Zhu's office at AUT University for ten years.

D.9. In the final report will there be any possibility that individuals or groups could be identified?

If the answer is yes, please explain how and why this will happen.

No

D.10. Will feedback or findings be disseminated to participants (individuals or groups)?

If the answer is yes, please explain how this will occur and ensure that this information is included in the Information Sheet.

Yes

D.11. Will the findings of this study be of particular interest to specific cultures or social groups?

If your answer is 'Yes', please identify how the findings will be made available to them.

No

E. Other Project Details

E.1. Where will the project be conducted?

Please provide the name/s of the Institution/s, town/s, city or cities, region or country that best answers this question.

The testing of the participants will be carried out at North Shore Campus of AUT University, Auckland.

E.2. Who is in charge of data collection?

Yuting Zhu

E.3. Who will interact with the participants?

Yuting Zhu

E.4. What ethical risks are involved for participants in the proposed research?

Please consider the possibility of moral, physical, psychological or emotional risks to participants, including issues of confidentiality and privacy. Researchers are urged to consider this issue from the perspective of the participants, and not only from the perspective of someone familiar with the subject matter and research practices involved.

Minimum risk

E.4.1. Are the participants likely to experience any discomfort, embarrassment (physical, psychological, social) or incapacity as a result of the research's procedures?

To prepare participants for data collection, the subject's left and right legs will be shaven around the areas of the intended muscles. This is to ensure good skin-electrode contact. It will next be gently abraded with skin preparation cleanser (Green Prep), then cleansed with 70% alcoholic swab and let to dry before attaching the newly developed wireless surface electrodes. These surface electrodes are the main sensory contacts attached to the subject for muscle activity. They are disposable or one-off use as surfaces are self-adhesive and preferred for time efficiency and hygiene.

The only discomfort maybe a slight stinging feeling of the skin when cleaning the skin with the alcoholic swab which last a few seconds.

Possible embarrassment will be the patches of shaven area of hair on the participant's legs, which will be of concern to the male subjects due to the time taken for the hair to grow back.

E.4.2. If there are risks, please identify their probability and describe how they will be mitigated.

Please describe how these will be minimised or mitigated (e.g. participants do not need to answer a question that they find embarrassing or they may terminate an interview or there may be a qualified counsellor present in the interview or the findings will be reported in a way that ensures that participants cannot be individually identified, etc.) Possible risks and their mitigation should be fully described in the Information Sheets for participants.

No

E.4.3. If the participants are likely to experience any discomfort, embarrassment, or incapacity, what provision for counselling has been made, either with AUT Counselling (who also provide an online service) or with other counselling professionals (this is to be at no charge to the participants)?

Please refer to section 2.3 of AUTEC's Applying for Ethics Approval: Guidelines and Procedures *in the Ethics Knowledge Base. If the answer is No, please explain the arrangements which have been made to have qualified personnel available to deal with unexpected adverse physical or psychological consequences?*

Participants will be made aware of the skin preparation for the data collection of the muscle activity in the Information Sheet.

E.5. What risks are involved for the researcher(s) in the proposed project (such as physical, social, psychological, or safety risks)?

If this project will involve interviewing participants in private homes, undertaking research overseas, or going into similarly vulnerable situations, then a Researcher Safety protocol should be designed and appended to this application.

None

E.6. Will there be any other physical hazards introduced to AUT staff and/or students through the duration of this project?

If the answer is yes, please provide details of management controls which will be in place to either eliminate or minimise harm from these hazards (e.g. a hazardous substance management plan).

No

E.7. Is deception of participants involved at any stage of the research?

If the answer is yes, please provide full details of and rationale for the deception. Please refer to Section 2.4 of AUTEC's Applying for Ethics Approval: Guidelines and Procedures *when considering this question.*

No

E.8. How much time will participants have to give to the project?

15-20 minutes

E.9. Will any information on the participants be obtained from third parties?

If the answer is yes, please provide full details. This includes use of third parties, such as employers, in recruitment.

No

E.10. Will any identifiable information on the participants be given to third parties?

If the answer is Yes, please provide full details.

No

E.11. Provide details of any payment, gift or koha and, where applicable, level of payment to be made to participants.

Please refer to Section 2.1 of the AUTEC's Applying for Ethics Approval: Guidelines and Procedures *and Appendix A of that document for AUTEC's policy on Payment and Koha, especially in relation to recruitment.*

A small gift of snack bars will be offered to say thank you to the participant for volunteering their time in taking part in the research.

F. Data and Consent Forms

F.1. Who will have access to the data?

Yuting Zhu and Jeffrey Kilby

F.2. Are there plans for future use of the data beyond those already described?

The applicant's attention is drawn to the requirements of the Privacy Act 1993 (see Appendix I). If there are future plans for the use of the data, then this needs to be explained in the Information Sheets for participants.

No

F.3. Where will the data be stored once the analysis is complete?

Please provide the exact storage location. AUTEC normally requires that the data be stored securely on AUT premises in a location separate from the consent forms. If you are proposing an alternative arrangement, please explain why.

All written consent forms and the EMG data is to be stored on external data storage devices will be held in a secure location in the Yuting Zhu's office at AUT University for ten years at AUT North Shore Campus.

F.4. For how long will the data be stored after completion of analysis?

AUTEC normally requires that the data be stored securely for six years. If you are proposing an alternative arrangement, please explain why.

Yes, as the data is health related in terms of sport and recreation.

F.5. Will the data be destroyed?

If the answer is yes, please describe how the destruction will be effected. If the answer is no, please provide the reason for this.

Yes by erasing all the data collected and analysed from the computer data after ten years.

F.6. Who will have access to the Consent Forms?

Yuting Zhu and Jeffrey Kilby

F.7. Where will the completed Consent Forms be stored?

Please provide the exact storage location. AUTEC normally requires that the Consent Forms be stored securely on AUT premises in a location separate from the data. If you are proposing an alternative arrangement, please explain why.

All written consent forms and personal information on data storage devices will be held in a secure location at AUT University, North Shore for ten years in Yuting Zhu's office.

F.8. For how long will the completed Consent Forms be stored?

AUTEC normally requires that the Consent Forms be stored securely for six years. If you are proposing an alternative arrangement, please explain why.

Ten years.

F.9. Will the Consent Forms be destroyed?

If the answer is yes, please describe how the destruction will be effected. If the answer is no, please provide the reason for this.

Yes after ten years the consent forms will be shredded at the same time the data is erase from the data storage devices.

G. Material Resources

G.1. Has an application for financial support for this project been (or will be) made to a source external to AUT or is a source external to AUT providing (or will provide) financial support for this project?

No

G.1.1. If the answer to G.1 was 'yes', please provide the name of the source, the amount of financial support involved, and clearly explain how the funder/s are involved in the design and management of the research.

G.2. Has the application been (or will it be) submitted to an AUT Faculty Research Grants Committee or other AUT funding entity?

If the answer is yes, please provide details.

No

G.2.1. If the answer to G.2 was 'yes', please provide the name of the source, the amount of financial support involved, and clearly explain how the funder/s are involved in the design and management of the research.

G.3. Is funding already available, or is it awaiting decision?

Please provide full details.

No

G.4. Please provide full details about the financial interest, if any, in the outcome of the project of the researchers, investigators or research organisations mentioned in Part A of this application.

The outcome of the project may not create financial interest in the near future.

H. Other Information

H.1. Have you ever made any other related applications?

If the answer is yes, please provide the AUTEC application / approval number(s)

No

I. Checklist

Please ensure all applicable sections of this form have been completed and all appropriate documentation is attached as incomplete applications will not be considered by AUTEC.

Section A	General Information Completed	☐
	Signatures/Declaration Completed	☐
Section B	Project General Information Completed	☐
Section C	Project Details Completed	☐
Section D	Participant Details Completed	☐
Section E	Other Project Details Completed	☐
Section F	Data & Consent Forms Details Completed	☐
Section G	Material Resources Completed	☐
Section H	Other Information Completed	☐

Spelling and Grammar Check (please note that a high standard of spelling and grammar is required in documents that are issued with AUTEC approval) ☐

Attached Documents (where applicable)

Participant Information Sheet(s)	☐
Consent Form(s)	☐
Questionnaire(s)	☐
Indicative Questions for Interviews or Focus Groups	☐
Observation Protocols	☐
Recording Protocols for Tests	☐
Advertisement(s)	☐
Hazardous Substance Management Plan	☐
Any Confidentiality Agreement(s)	☐
Other Documentation	☐

Before submitting this application, please note the following:

- *Incomplete or incorrectly formatted applications will not be considered by AUTEC;*
- *Please check online for the most recent version of this form before submitting your application;*
- *Please do not alter the formatting of this form or delete any sections. If a particular question is not applicable to your research, please state that as your response to that question;*

This form needs to be submitted, along with all associated documents as follows:

- *In printed form;*
- *With the required signatures in sections A.8 and A.9;*
- *Single sided;*
- *Using clips rather than staples;*
- *By 4 pm on the agenda closing date at:*

The AUTEC Secretariat
Room WA505D, WA Building
55 Wellesley Street East, City Campus.

- *The Internal Mail Code is D-89. If sending applications by Internal Mail, please ensure that they are posted at least two days earlier to allow for any delay that may occur.*

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