NEXT-GENERATION WIRELESS ON-CHIP COMMUNICATION USING TERAHERTZ ANTENNAS

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By

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Abstract

The exponential growth of data-driven technologies, including artificial intelligence (AI), high-definition sensing, and wireless chip-to-chip interconnects, has intensified the demand for ultra-high-speed, energy-efficient communication systems. Conventional microwave and millimetre-wave solutions are reaching their physical and spectral limits, prompting a shift toward the terahertz (THz) band (0.1–10 THz) for next-generation wireless networks. The THz spectrum offers unprecedented bandwidth and spatial resolution but remains hindered by propagation loss, fabrication tolerances, and integration constraints within semiconductor environments. These challenges define a crucial research gap in realizing compact, low-loss, and CMOS-compatible THz antenna systems.

This thesis addresses that gap through the design and modelling of advanced on-chip and substrate-integrated THz architectures. First, a stacked substrate-integrated waveguide (SIW) pyramidal horn antenna is proposed to achieve beam symmetry, high gain, and planar compatibility. The design employs multilayer dielectric loading and Gaussian excitation to balance E- and H-plane radiation, demonstrating efficient operation around 210 GHz. Second, a broadband, probe-less rectangular-waveguide (RWG) to SIW mode converter is introduced, enabling low-reflection TE_{10} to TE_{20} transitions and compact interfacing between metallic and planar structures. Finally, the thesis models intra- and inter-chip THz communication channels using realistic on-chip antennas and packaging

materials, evaluating coupling efficiency, loss mechanisms, and spatial field behaviour for Wireless Network-on-Chip (WiNoC) applications.

Collectively, these works contribute new insights into THz front-end integration, demonstrating that multilayer SIW antennas and mode converters can deliver high performance and scalability within chip-scale systems. The research establishes a foundation for CMOS/BiCMOS-compatible THz transceivers, paving the way for future 6G and Integrated Sensing and Communication (ISAC) platforms. Future work should focus on fabrication, experimental validation, and reconfigurable metamaterial loading to further enhance bandwidth, tunability, and practical deployment of on-chip THz systems.

Contents

Attestation of Authorship

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for the qualification of any other degree or diploma of a university or other institution of higher learning.

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Signature of candidate

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Glossary and Notations

Glossary

3D	Three dimensional
3GGP	The 3rd Generation Partnership Project
5G	the fifth generation
AR	Axial ratio
AUT	Antenna under test
balun	Unbalance-to-balance
BW	Backward-wave
%BW	Percentage bandwidth
CCW	Counterclockwise
CEM	Computational electromagnetics
CNT	Carbon nanotube
Co-pol	Co-polarization
CP	Circularly polarized
CPS	Coplanar stripline
CPW	Coplanar waveguide
CSRR	Complimentary SRR
CVD	Chemical vapor deposition
CW	Clockwise

dB	Decibels
DGS	Defect ground structure
DMF	dimethyl formamide
DMSO	Dimethyl sulfoxide
DNG	Double Negative Material
DOD	Drop on demand
DWCNT	Double-wall carbon nanotube
EHF	Extremely High Frequency
ELC	Electric field coupled resonator
EM	Electromagnetic
ENZ	ε-near zero
FEM	Finite element methods
FIT	Finite integration technique
FNBW	First-Null Beamwidth
FR1	5G low-band (sub-6 GHz)
FR2	5G high-band (24-86 GHz)
FSS	Frequency Selective Surface
GDS	Grounded dielectric slab
GPS	Global positioning system
HFSS	High Frequency Structural Simulator
HPBW	Half Power Bandwidth
IC	Integrated circuit
IMI	Insulator-metal-insulator
IMT	International Mobile Telecommunications
IoT	Internet of Things
ISM	Industrial, scientific and medical

ITS	Intelligent transportation system
ITU	Internation Telecommunication Union
ITU	International Telecommunication Union
LHCP	Left-handed circular polarization
LHM	Left-handed Material
LMDS	Local multipoint distribution service
LMDS	Local multipoint distribution service
LOS	Line-of-Sight
LP	Linearly polarized
LPDA	Log-periodic dipole array
LTC	Linear-to-circular
MIMO	Multiple-input multiple output
mmWave	Millimeter Wave
MTC	Machine-type communication
NFC	Near-field communication
NIM	Negative-refractive Index Material
NPV	Negative phase velocity
PCB	Printed Circuit Board
PCR	Polarization conversion rate
PDMS	Polydimethylsiloxone
PE	Printed electronics
PET	Polyethlene terephthalate
PRS	Partially reflecting screen
PVP	Polyvinylpyrrolidone
RCS	Radar corss-section
RFID	Radio-frequency identification

RHCP	Right-handed circular polarization
RHM	Right-handed Material
RLBW	Return-loss bandwidth
SAR	Specific absorption rate
SEM	Scanning electron microscope
SHF	Super High Frequency
SIW	Substrate integrated waveguide
SMA	Sub-Miniature Version A
S-parameter	Scattering parameter
SPP	Surface plasmon polariton
sr	Steradian
SRR	Split ring resonator
SSR	Split Ring Resonator
SWCNT	Single-wall carbon nanotube
TE	Transverse electric
TM	Transverse magnetic
TPU	Thermoplastic polyurethane
UHF	Ultra-high frequency
UV	Ultraviolet
UWB	Ultra wideband
VNA	Vector network analyser
VSWR	Voltage standing wave ratio
WLAN	Wireless local area network
WPAN	Wireless personal area network
X-pol	Cross-polarization

Notation

A	area of a sphere
A_{bend}	amplitude of the bending sinusoidal curve
α	attenuation constant
α	bending angle
$\vec{B}$	magnetic flux density vector
β	phase constant
d	distance between transmit and receive antennas
D	largest dimension of an antenna
D	directivity of an antenna
$\vec{D}$	electric flux density vector
d	unit cell dimension
D_0	maximum directivity of an antenna
d_{ant}	distance between antenna and hand model
δ	surface depth of skin effect
$\Delta\phi$	phase difference
ΔL	extended microstrip patch length
d_l	director length coefficient
D_{max}	maximum directivity of an antenna
$\Delta\phi$	phase difference
d_{ref}	distance on the reference line
d_s	director space coefficient
$\mathbf{E}$	electric field
$\mathscr{E}$	instantaneous electric-field intensity
e	eccentricity
e_0	total antenna efficiency

$\bar{\varepsilon}$	dispersive permittivity
e_c	conduction efficiency
e_{cd}	conduction and dielectric efficiency
e_d	dielectric efficiency
E_{end}	voltage at the end of propagation
ε	electric permitivity
ε_0	free space electric permitivity
E_ϕ	far-zone electric-field ϕ component
ε_m	modified permittivity
ε_r	relative permitivity
ε_{reff}	effective dielectric constant
e_r	reflection efficiency
E_r	electric field of reflected wave
E_{start}	voltage at the end of propagation
η	intrinsic impedance of medium
η	wave impedance
η	conversion efficiency
E_θ	far-zone electric-field θ component
$\mathscr{E}_x$	x component of instantaneous electric-field
E_x	x component of electric field
e_x	unit direction vector on x-axis
E_{x0}	maximum magnitude of x component of electric-field
$\exp(jwt)$	time-harmonic convention
$\mathscr{E}_y$	y component of instantaneous electric-field
E_y	y component of electric field
e_y	unit direction vector on y-axis

E_{y0}	maximum magnitude of y component of electric-field
f	frequency
F	fitting parameter
f_0	resonant frequency
f_{0e}	electric resonant frequency
f_{0u}	magnetic resonant frequency
F_e	electric resonant intensity
f_{min}	minimum frequency
f_r	resonant frequency
F_u	magnetic resonant intensity
G_0	maximum gain
G_{0abs}	maximum absolute gain
$G_{0forward}$	maximum gain in forward direction
g_1	gap between "S" and "C" resonators
G_{abs}	absolute gain
Γ	reflection coefficient
G	antenna gain
γ	complex propagation constant
γ	damping factor
γ_e	electric damping factor
γ_u	magnetic damping factor
G_{dBi}	gain expressed in decibels
G_{max}	maximum gain
G_ϕ	ϕ component of gain
G_r	radiation conductance
$G_{r,dB}$	received gain in dB

G_θ	θ component of gain
$\mathbf{H}$	magnetic field
$\mathscr{H}$	instantaneous magnetic-field intensity
$\vec{J}_s$	surface current density
$\mathbf{k}$	wave vector
L	microstrip patch length
λ	wavelength of electromagnetic wave
λ_{eff}	effective wavelength
λ_g	guided wavelength of electromagnetic wave in waveguide
L_{eff}	effective length of microstrip patch
L_{joint1}	length of joint1
L_{joint2}	length of joint 2
L_{slit}	slit length
μ	magnetic permeability
μ_0	free space magnetic permeability
$\bar{\mu}$	dispersive permeability
μ_{eff}	effective permeability
μ_m	modified permeability
μ_r	relative permeability
n	refractive index
$\hat{\mathbf{n}}$	unit vector normal to a surface
∇	curl of a vector
Ω	solid angle
Ω_A	beam solid angle
ω	angular frequency
ω_{pl}	plasmon frequency

$\mathscr{P}$	instantaneous total power
P	perimeter of the cross-section area
p	periodicity
P_{avg}	average radiated power
P_{end}	power at the end of propagation
ϕ	azimuth angle
ϕ_x	x component phase
ϕ_{xy}	phase of y-to-x conversion
ϕ_y	y component phase
ϕ_{yy}	phase of y-to-y conversion
P_{in}	total input power
P_{lc}	conductor loss
$P_{L,dB}$	path loss in dB
P_{rad}	radiated power
P_r	received power level
P_{start}	power at the start of propagation
P_t	transmit power level
r	distance in spacial coordinates
R	field distance
r	reflection coefficient
R_{dc}	direct current resistance
ρ	resistivity
R_{rf}	effective radio frequency resistance
R_S	surface resistance
R_{xy}	reflection coefficient of y-to-x conversion
R_{yy}	reflection coefficient of y-to-y conversion

S_0	unit cell area
$S_{21,dB}$	S_{21} in dB
S	cross-section area of a conductor
σ	conductivity
σ	spacing factor of dipole array
τ	tilt angle of an ellipse
t or h	substrate thickness
τ	scale factor of dipole array
t	transmission coefficient
θ	elevation angle
U	radiation intensity
U_0	radiation intensity of an isotropic source
U_{max}	maximum radiation intensity
U_ϕ	ϕ component of radiation intensity
U_θ	θ component of radiation intensity
v_0	speed of light in free space
V	unit cell volume
$\mathscr{W}$	instantaneous Poynting vector
W	microstrip patch width
W_{avg}	average radiated power density
W_{rad}	radiated power density
W_{slit}	slit width
X_{joint2}	location of joint2 on x-axis
Y	admittance
Y_e	electric admittance
Y_{joint1}	location of joint1 on y-axis

Z_0	transmission line characteristic impedance
Z_0	characteristic impedance of microstrip line
Z	load impedance
Z_{in}	antenna input impedance
Z_m	magnetic impedance

Chapter 1

Introduction

1.1 THz Frequency Band

The exponential rise of data-driven technologies, especially artificial intelligence (AI), machine learning, and high-performance computing, has intensified the global demand for ultra-high-speed, energy-efficient, and low-latency communication systems. Modern AI accelerators require massive parallel data exchange among processing cores and memory units, yet existing CPU and GPU interconnects based on electrical wiring are reaching their physical and spectral limits. While the millimetre-wave (mmWave) band holds significant potential, its capacity may not be sufficient to meet the exponentially growing data demands of future wireless systems. Although mmWave frequencies are not yet fully exploited in commercial deployments due to practical implementation challenges, band congestion remains a plausible and widely anticipated scenario as data traffic continues to increase. This motivates the exploration of higher frequency bands, such as the terahertz (THz) band ($0.1 - 10$ THz), as a forward-looking solution to support next-generation computing and communication platforms [1–3].

The THz spectrum bridges the gap between microwave and infrared regions, combining

the strong penetration and low photon energy of microwaves with the high spatial resolution and directivity of infrared radiation as illustrated in Figure 1.1. Within this band, the lower-THz region (0.1-0.3 THz) allows partial reuse of existing semiconductor fabrication processes, while the core THz band (0.3-3 THz) represents the "THz gap," where neither conventional electronic nor optical technologies operate efficiently. The upper-THz range (3-10 THz) overlaps the far-infrared region, offering remarkable potential for imaging, spectroscopy, and sensing [1]. Standardization efforts such as IEEE 802.15.3d for 252–325 GHz links have already demonstrated feasibility for short-range, high-capacity communications [3].

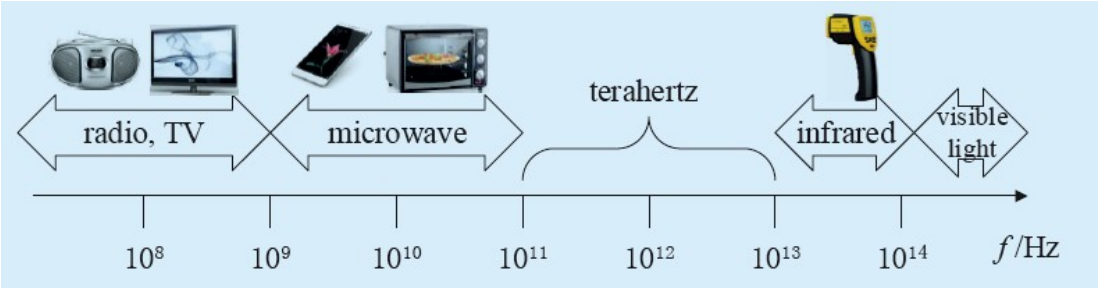


Figure 1.1: Illustration of the terahertz (THz) range within the electromagnetic spectrum, positioned between the microwave and infrared regions (adapted from [1])

THz electromagnetic waves provide extremely wide bandwidths that can theoretically support terabit-per-second data rates [4]. Their short wavelengths enable compact, highly directive antennas ideal for dense spatial reuse, while their non-ionizing nature allows safe integration for chip-scale applications. Nevertheless, high free-space path loss, molecular absorption, and dielectric losses at these frequencies remain major challenges, prompting research into low-loss guiding and radiation mechanisms such as Substrate Integrated Waveguides (SIWs), dielectric resonators, leaky-wave antennas, and metasurface-based solutions [5, 6].

1.2 THz On-Chip Antennas

The explosive growth of AI and high-performance computing has shifted the performance bottleneck from computation to communication. As transistor counts rise and chiplet-based architectures become common, the demand for ultra-fast inter-core and inter-chip data exchange has outpaced the capabilities of metallic interconnects. These wired links suffer from parasitic capacitance, resistive losses, crosstalk, and excessive power consumption, which collectively restrict system scalability and efficiency [7, 8]. To overcome these limitations, researchers are exploring wireless on-chip communication using the terahertz (THz) spectrum as a promising alternative for short-range, high-bandwidth data transfer.

Wireless Network-on-Chip (WiNoC) architectures [9–11] replace many conventional signal traces with compact wireless links embedded within the chip package, enabling single-hop or broadcast connectivity between cores, caches, and accelerators. Operating in the THz band provides access to massive bandwidths while maintaining sub-millimetre antenna dimensions compatible with standard CMOS or BiCMOS processes. Studies done by [12, 13] have shown that THz wireless interconnects can significantly alleviate communication bottlenecks in large AI accelerators.

At the core of this paradigm are on-chip antennas, which serve as the primary interface for THz signal transmission and reception within the chip environment. These antennas must deliver wide bandwidth, high radiation efficiency, and strong coupling while remaining compatible with silicon substrates and multilayer packaging. Various geometries, dipole, zigzag, slot, and Yagi types, have been investigated to optimize impedance matching and field confinement in silicon and polymer dielectrics. Through continued advancements in antenna miniaturization and material engineering, on-chip THz antennas have become essential enablers for next-generation computing architectures, supporting the data-transfer demands of AI, high-speed processors, and future 6G

systems.

Antenna design in the terahertz (THz) regime has evolved considerably, transitioning from bulky metallic horns to compact, integrable dielectric and metamaterial-based structures. Broadly, THz antennas can be classified into three categories: metallic, dielectric, and new-material types [1, 2]. Metallic antennas, such as conical and corrugated horns, remain the most established THz radiators due to their high gain and broadband characteristics, though their miniaturization and integration with planar circuits become increasingly challenging at sub-millimetre dimensions [14, 15]. Dielectric antennas offer improved planar compatibility and reduced conductor loss but often suffer from surface-wave propagation that limits radiation efficiency; this can be mitigated through lens loading, substrate thinning, or electromagnetic-band-gap (EBG) structures [16, 17]. Meanwhile, emerging carbon-based and graphene-plasmonic antennas exhibit tunable and reconfigurable radiation properties with promising efficiency improvements [18, 19].

Despite these advances, many THz antenna designs still exhibit narrow bandwidth, high insertion loss, and limited compatibility with standard semiconductor technologies. These limitations reinforce the importance of developing compact, low-loss, and CMOS-compatible on-chip THz antennas capable of supporting the rapidly increasing data-transfer demands of AI, high-speed processors, and 6G systems [20].

1.3 Research Challenges and Gaps

Despite major progress in THz antenna and system research, many challenges remain before commercialization. The current THz antennas are often scaled adaptations of mmWave designs rather than genuinely new architectures, limiting their efficiency at THz frequencies [1]. Key challenges include:

- **Propagation Loss**: THz waves suffer extremely high atmospheric absorption and

scattering, particularly by water vapour and molecular resonances, which limit effective link distances even in controlled environments. For example, recent studies show that free-space path loss at THz frequencies can increase by tens of dB relative to mm-wave links, demanding antennas with both high gain and very narrow beamwidths for viable performance [20–22].

- **Fabrication Tolerances**: At THz wavelengths (sub-millimetre to micron-scale), even tiny dimensional deviations or alignment errors in metallic or dielectric features significantly degrade antenna impedance matching, radiation efficiency, and predictable beam patterns. Manufacturing precision must reach micrometre levels, and surface roughness control becomes critical for reproducible THz antenna performance [23, 24].

- **Substrate Loss and Mismatch**: High-permittivity silicon and packaging materials often introduce substantial dielectric and surface-wave losses in THz antennas, coupling into substrate modes and the grounding/layer stack can distort beams and reduce radiated efficiency. THz antenna designs must carefully manage substrate thickness, grounding, and dielectric loss tangent to preserve performance at THz [25, 26].

- **Integration Complexity**: Embedding antennas on-chip or in flip-chip packages requires coexistence with active circuits, power delivery networks, heat-dissipation paths and shielding structures, which collectively impose constraints on antenna placement, electromagnetic interference, and packaging parasitics. Studies of on-chip THz antenna systems show that packaging parasitics and integration-induced losses often dominate over free-space radiation loss for very short links [20].

Moreover, many THz prototypes rely on off-chip lenses or horn configurations, which

are impractical for a compact transceiver [6, 27]. The need to bridge high-performance free-space antenna architectures and fully integrated on-chip designs remains a significant open frontier.

1.4 Motivation

The rapid expansion of data-intensive applications, including real-time analytics, virtual reality, and high-speed computing, demands communication systems capable of operating beyond the mm-Wave spectrum. Despite extensive research on mm-Wave antennas, achieving high gain, beam symmetry, and low loss at THz frequencies remains a significant challenge. Conventional horn antennas offer excellent gain but suffer from large size and poor compatibility with planar fabrication. In contrast, microstrip or slot-based THz antennas often face high losses and narrow bandwidths.

To overcome these challenges, advanced electromagnetic structures such as substrate-integrated waveguides (SIWs), mode converters, and on-chip antennas have been developed. SIW technology provides a planar equivalent to conventional rectangular waveguides, offering low loss, high quality factor, and excellent compatibility with standard PCB or CMOS processes [28, 29]. Similarly, broadband mode converters enable smooth transitions between different waveguide modes (e.g., TE_{10}-to-TE_{10}), facilitating compact and efficient integration of front-end components. At the chip level, wireless intra- and inter-chip communication using THz antennas has been investigated to address the limitations of traditional metallic interconnects [30, 31]. Collectively, these technologies form the foundation for compact, efficient, and integrable THz systems.

Specifically, this research is motivated by the need to bridge this performance gap through innovative SIW-based architectures and on-chip integration strategies. The work aims to:

1. Develop a compact, multilayer SIW pyramidal horn antenna with beam symmetry suitable for THz front-end modules;

2. Design an efficient RWG–SIW mode converter for broadband and low-reflection transition;

3. Investigate THz intra-/inter-chip communication channels to establish design guidelines for future wireless network-on-chip (WiNoC) systems.

1.5 Research Questions

To guide the investigation, the following primary research questions are posed:

- **RQ1**: How can a multilayer SIW-based pyramidal horn antenna be designed to achieve equal half-power beamwidths in both E- and H-planes at THz frequencies, while maintaining high gain and integrability with CMOS/BiCMOS processes?

- **RQ2**: What design methodology and geometrical parameters enable a broadband, low-reflection RWG–SIW mode converter transitioning from TE_{10} to TE_{20} at THz frequencies, and how does this converter impact antenna feed performance?

- **RQ3**: What are the propagation characteristics, coupling efficiency, and substrate effects of THz intra- and inter-chip wireless links using on-chip antennas, and how can these insights inform design guidelines for future WiNoC systems?

1.6 Objectives

The overarching goal of this thesis is to design, model, and validate compact, efficient, and integrable terahertz (THz) antenna systems suitable for short-range communication and sensing. To achieve this goal, the specific objectives are defined as follows:

- **Objective 1 – SIW Horn Antenna Design:** To design and optimize a multilayer Substrate Integrated Waveguide (SIW) pyramidal horn antenna that achieves equal half-power beamwidths in both E- and H-planes. The antenna will employ Gaussian aperture excitation and stacked dielectric layers to enhance gain, beam symmetry, and integration compatibility with CMOS and BiCMOS technologies.

- **Objective 2 – Mode Converter Development:** To develop a broadband, probeless Rectangular Waveguide (RWG)–to–SIW mode converter that enables efficient TE_{10}–to–TE_{20} transition. The design will minimize reflection ($S_{11} < -10$ dB) and achieve high transmission efficiency ($S_{21} > -5$ dB) across a wide impedance bandwidth to facilitate low-loss coupling between waveguide and on-chip structures.

- **Objective 3 – On-Chip THz Channel Modeling:** To model and analyze intra- and inter-chip THz communication channels using integrated on-chip antennas. This includes evaluating coupling efficiency, propagation loss, field confinement, and substrate effects within flip-chip and silicon packages to establish design guidelines for future Wireless Network-on-Chip (WiNoC) architectures.

1.7 Original Contribution

The main contributions of this thesis include:

- **A Stacked Substrate Integrated Waveguide-based Pyramidal Horn Antenna for Terahertz Communications**

  In this research, a stacked substrate integrated waveguide (SIW) pyramidal horn antenna is proposed as a novel contribution to terahertz (THz) front-end design. The work introduces a five-layer dielectric-loaded SIW horn architecture with an

optimized slot-coupled feeding network that ensures efficient TE_{10}-mode power transfer and equal half-power beamwidths in both E- and H-planes, achieving beam symmetry rarely demonstrated in conventional THz horn antennas. By employing a Gaussian excitation profile with uniform phase, the design attains high gain (10 dBi), low sidelobe levels (≈ -3.2 dB), and broadside radiation stability across the 210 GHz band. The proposed stacked configuration transforms the traditional bulky horn into a planar and integrable structure, compatible with CMOS/BiCMOS and MMIC technologies. This work represents one of the first demonstrations of a multilayer SIW-based pyramidal horn optimized for THz communication systems, providing a compact, efficient, and fabrication-friendly solution for next-generation wireless, imaging, and sensing applications.

- **A Broadband Mode Converter Antenna for Terahertz Communications.**

  The proposed mode converter enables an efficient transition from a rectangular waveguide (WR-0.43) in TE_{10} mode to a substrate-integrated waveguide (SIW) in TE_{20} mode using a compact structure composed of a tapered waveguide, widened waveguide, zigzag antenna, and aperture slot. The zigzag antenna couples energy into the slot, generating a quasi-slotline mode with odd symmetry to excite the TE_{20} mode in the SIW. Full-wave simulations confirm the mode transition, and back-to-back TE_{10}-to-TE_{10} configuration demonstrates the ~ 5 dB insertion loss and > 10 dB return loss over $2.15 - 2.36$ THz. An on-chip antenna fed by the TE_{20} mode achieves 4.49 dB gain, and a balun design further verifies the excitation of higher-order modes.

- **Design and modeling of a terahertz transceiver for intra-and inter-chip communications in wireless network-on-chip architectures**

  This study presents a wireless intra-chip and inter-chip communication approach using THz-band antennas integrated into a System-on-Chip (SoC) architecture.

By employing dipole and zigzag antennas within a flip-chip package, the design enables high-frequency communication at 446 GHz and 462.5 GHz. Electromagnetic simulation using Ansys HFSS analyzes transmission coefficient, path-loss, and electric field distributions, revealing that the zigzag antenna offers superior field strength. The communication link is shown to be feasible with energy consumption under 1 pJ/bit. Results indicate that signal transmission is primarily supported by ground plane reflections within the chip structure.

1.8 Publications

Publications of the author are listed as below [32–39]:

Journal Publications

J1. B. Paudel, X. J. Li, and B. C. Seet, "A Broadband Mode Converter Antenna for Terahertz Communications," *Electronics*, vol. 14, pp. 1–12, 2025. (MDPI Electronics, Special Issue on Broadband Antennas and Antenna Arrays)

J2. B. Paudel, X. J. Li, and B. C. Seet, "Design and Modeling of a Terahertz Transceiver for Intra- and Inter-Chip Communications in Wireless Network-on-Chip Architectures," *Sensors*, vol. 24, p. 3220, 2024.

J3. B. Paudel, X. J. Li, and B. C. Seet, "A Stacked Substrate Integrated Waveguide-based Pyramidal Horn Antenna for Terahertz Communications", Electronics, under review, November 2025.

Conference Publications

C1. B. Paudel, X. J. Li, and B. C. Seet, "A THz Perpendicular Mode Converter for Interconnections Between Rectangular Waveguides to Substrate Integrated Waveguides,"

2025 IEEE 13th Asia-Pacific Conference on Antennas and Propagation (APCAP), Christchurch, New Zealand, 2025, pp. 188–189.

C2. B. Paudel, X. J. Li, B. C. Seet, and X. Lin, "Rectangular Waveguide TE_{10} to Substrate Integrated Waveguide TE_{20} Probe-less Mode Converter for Planar Terahertz Applications," *2025 6th Australian Microwave Symposium (AMS)*, 2025, pp. 1–2.

C3. B. Paudel, X. J. Li, and B. C. Seet, "Using Terahertz On-Chip Antennas for Intra-Chip Wireless Communications within a Multi-Core Processor," *49th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, 2024, pp. 1–2.

C4. B. Paudel, X. J. Li, and B. C. Seet, "A 254–276 GHz On-Chip THz Antenna Using Substrate Integrated Waveguide and Metamaterials for Short-Range Wireless Communications," *IEEE Region 10 Symposium (TENSYMP)*, 2023, pp. 1–6.

C5. B. Paudel and X. J. Li, "A Terahertz On-Chip Antenna for Intra-Chip Wireless Communications," *IEEE Conference on Antenna Measurements and Applications (CAMA)*, 2022, pp. 1–3.

C6. B. Paudel and X. J. Li, "Dual-Band On-Chip Terahertz Antenna for Short-Range Wireless Communications," *IEEE Microwave, Antennas, and Propagation Conference (MAPCON)*, 2022, pp. 1–5.

1.9 Thesis Outline

The rest of this thesis is organised as follows:

Chapter 2 provides a comprehensive overview of terahertz (THz) technology and its relevance to next-generation on-chip wireless communication systems. It begins by defining the THz spectrum and outlining its advantages, such as large bandwidth, high spectral resolution, and material penetration, while noting challenges like propagation

loss and fabrication limitations. The discussion then focuses on on-chip antennas (OCAs), emphasizing the importance of integration with CMOS and BiCMOS platforms to enable compact, high-speed transceivers. Various OCA types are reviewed, including patch, slot, dipole, monopole, loop, and Yagi configurations, highlighting their design principles, performance trade-offs, and efficiency-enhancement strategies using artificial magnetic conductors (AMCs), metamaterials (MTMs), and metasurfaces (MTSs).
The chapter further examines Substrate Integrated Waveguide (SIW) technology as a bridge between traditional rectangular waveguides and planar circuits, explaining its mode propagation characteristics, loss mechanisms, and suitability for THz systems. It details how SIW-MTM/MTS hybrid structures improve field confinement, bandwidth, and gain, leading to compact, high-efficiency on-chip designs. Dielectric resonator antennas (DRAs) are also reviewed for their ability to minimize conductor losses and achieve high radiation efficiency using higher-order modes and SIW-fed configurations. Collectively, the chapter identifies key research gaps in developing efficient mode converters, broadband SIW-based horns, and integrated THz channels, establishing the foundation and motivation for the novel antenna and mode-converter designs explored in subsequent chapters.

Chapter 3 presents the design and analysis of a stacked substrate integrated waveguide (SIW) pyramidal horn antenna for terahertz (THz) communications. The chapter introduces the motivation for using multilayer SIW structures to achieve compactness, low loss, and beam symmetry. It describes the antenna geometry, design methodology, and full-wave optimization process leading to equal half-power beamwidths in both E- and H-planes. Simulation results demonstrate a gain of 10 dBi, sidelobe levels around -3.2 dB, and efficient radiation at 210 GHz. A five-way SIW power-splitter network is developed to provide Gaussian amplitude excitation and uniform phase across stacked layers. The chapter concludes with validation of the complete antenna

system and discussion of its suitability for short-range THz links and integrated sensing applications.

Chapter 4 focuses on the design and development of a broadband rectangular waveguide (RWG) to substrate integrated waveguide (SIW) mode converter antenna for terahertz (THz) applications. The chapter introduces a probe-less transition structure that efficiently converts the TE_{10} mode in RWG to the TE_{20} mode in SIW, ensuring low reflection and wideband operation. The design methodology, field analysis, and parametric optimization are presented using full-wave simulations. Results demonstrate improved impedance matching, high coupling efficiency, and stable radiation characteristics across the operating band. The chapter also discusses the mode converter's integration capability with planar THz systems and its potential as a feed structure for high-gain on-chip antennas.

Chapter 5 investigates the modeling and design of terahertz (THz) intra- and inter-chip wireless communication channels using integrated on-chip antennas. It begins by discussing the challenges of signal propagation, loss mechanisms, and coupling efficiency within chip-scale environments. The chapter presents full-wave electromagnetic simulations to analyze path loss, antenna coupling, and channel characteristics across different substrate materials and configurations. The results highlight the influence of chip packaging, interconnect spacing, and antenna placement on communication performance. The study provides design guidelines for optimizing link efficiency and minimizing interference in dense chip networks. Finally, the chapter demonstrates the feasibility of using on-chip THz antennas for high-speed, short-range interconnects in future wireless network-on-chip systems.

Chapter 6 concludes this thesis and provides recommendations for future work.

Chapter 2

Literature Review

This chapter presents a review of the relevant literature and theoretical background necessary to support the research covered in this thesis. It begins with a Section 2.1 providing an overview of terahertz (THz) technology. including its applications and associated challenges. It then shifts the discussion to on-chip antennas in Section 2.2 at THz frequencies, with a focus on the need for integration, associated limitations, and a brief survey of existing on-chip antenna types. Following this in Section 2.3, substrate integrated waveguide (SIW) technology is examined as a promising platform for THz on-chip antenna design, highlighting its fundamental concepts, advantages, and current limitations. The chapter concludes by identifying key research gaps in the existing literature, which serve as the motivation for the contributions developed in subsequent chapters.

2.1 Overview of THz Technology

The rapid growth of wireless devices and the shift from wired to mobile platforms have driven an unprecedented surge in data traffic, often referred to as the data traffic explosion. Current wireless systems are increasingly constrained by spectrum scarcity,

as conventional frequency bands are unable to accommodate the escalating demand for high-speed connectivity. To address this limitation, the terahertz (THz) band has emerged as a promising candidate for next-generation ultra-broadband communication systems.

2.1.1 THz Band

THz waves occupy the spectral region between microwaves and infrared light. Depending on the definition, the THz band spans frequencies from $0.1 - 10$ THz, with wavelengths in the range of $0.03 - 3$ mm [40]. According to IEEE standards, THz waves are more specifically defined as being between 0.3 and 10 THz [41, 42]. This frequency window is often referred to as the "THz gap", a vast unexplored region compared to its microwave and optical counterparts.

THz waves possess unique physical properties that make them highly attractive for both communication and sensing applications:

- **Low photon energy**: unlike X-rays, THz radiation has extremely low photon energy, minimizing biological hazards and enabling biomedical applications such as cancer detection and non-invasive imaging [43].
- **High spectral resolution**: Large molecules exhibit characteristic spectral signatures in the THz band, facilitating applications in chemical analysis, security screening, and the detection of explosives or hazardous materials [44].
- **Material penetration and imaging**: Due to its short wavelength, THz waves can penetrate non-metallic and non-polar materials, enabling high-resolution imaging, particularly in security scanners and non-destructive evaluation [45].
- **Large available bandwidth**: As one of the highest frequency bands accessible to electronic systems, the THz band can support extremely high data rates,

potentially scaling to terabits per second (Tbps) [46].

In addition to communication, THz technology bridges the advantages of mm-Wave and optical systems. Compared to mm-Waves, THz frequencies offer greater available bandwidth, narrower beam directivity, and improved resistance to interference. Relative to optical frequencies, THz signals achieve higher energy efficiency and better penetration capability, which is advantageous for compact wireless systems.

2.1.2 Why is THz Communications Important?

The exponential rise in wireless data demand, which is driven by data-intensive applications, cloud services, and ubiquitous mobile connectivity, has pushed existing technologies toward their physical and spectral limits. Over the past three decades, wireless data rates have approximately doubled every 18 months [47] and are now approaching the performance of wired communication systems. To meet future needs, wireless networks must evolve to deliver multi-gigabit to terabit-per-second data rates reliably and efficiently.

- Conventional bands below 0.1 THz face two fundamental limitations: spectrum scarcity and insufficient bandwidth to support Tbps-scale communication. Even with advanced schemes such as OFDM or large-scale MIMO, systems operating below 5 GHz are capped at around 1 Gbps (e.g., LTE-A networks), while mm-Wave technologies at 60 GHz can achieve 10 Gbps over short ranges. These figures remain two or three orders of magnitude below the Tbps targets.

- On the opposite end of the spectrum, optical and free-space optical (FSO) systems operating above 10 THz offer very high bandwidth but are hindered by several practical limitations. Eye-safety power restrictions, sensitivity to atmospheric attenuation (e.g., fog, rain, dust), diffuse scattering losses, and misalignment

issues make them less suitable for short-range, mobile, or personal communication systems.

The THz band ($0.1 - 10$ THz) strikes an optimal balance between these two extremes. It provides bandwidths more than an order of magnitude greater than state-of-the-art mm-Wave systems, while operating at frequencies significantly lower than optical systems, thereby reducing susceptibility to atmospheric impairments. Advances in THz transceiver architecture, novel antenna designs, and emerging materials with unique electromagnetic properties are gradually overcoming the so-called "THz gap".

Nevertheless, significant challenges remain, including high propagation losses, the need for compact high-power transceivers, efficient ultra-broadband antennas, and the development of modulation and communication protocols tailored to the peculiarities of THz channels. Moreover, regulatory frameworks for THz spectrum allocation are still under development. Recognizing its importance, standardization efforts such as the IEEE 802.15 Study Group 100 Gbits/s Wireless (SG100G) have been initiated to define protocols and enable multi-Gbps to Tbps THz links.

2.2 THz On-Chip Antennas

Antennas lie at the heart of any wireless communication system, acting as the critical interface between electronic circuits and free-space propagation. Without an efficient antenna, even the most advanced transceiver architectures cannot launch, steer or receive electromagnetic waves with the required fidelity and throughput. As noted by [48], antennas are the “linchpins” that enable high-performance connectivity in wireless systems. Furthermore, [49] that in miniature wireless devices, antenna design becomes one of the most significant constraints due to the need for compactness, multi-band operation and reliable radiation performance.

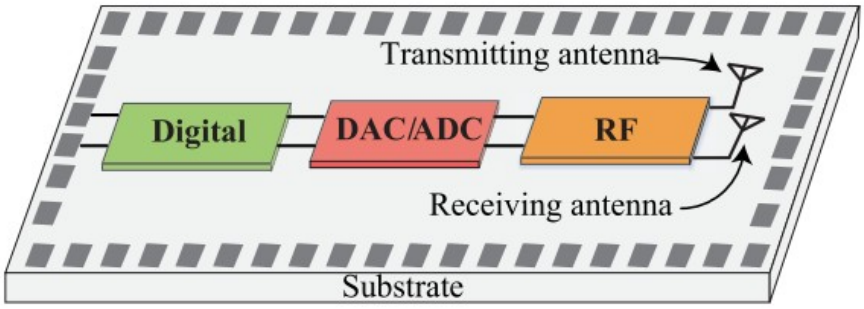


Figure 2.1: SoC-based integration: all transceiver blocks, including antennas, are implemented on a single substrate, removing lossy interconnects and enabling compact, low-loss, and power-efficient THz modules [50]

In the context of terahertz (THz) on-chip systems, this means that antenna design is not simply another component but a core enabler: it must deliver high gain, efficient radiation, precise beam control and minimal loss, all while being integrated within a silicon-based platform and co-existing with other RF and digital circuits as shown in Figure 2.1.

2.2.1 On-Chip Integration

The rapid growth of THz communication systems, targeting data rates from tens to hundreds of gigabits per second, has driven the development of antennas that can be seamlessly integrated within semiconductor technologies. At the same time, the exploding computational power required by artificial-intelligence (AI) workloads is pushing multi-core CPU/GPU and multi-chiplet architectures toward data-movement bottlenecks; communication, not computation, is increasingly the limiting factor in many-core systems [7, 51]. Traditional off-chip solutions, such as metallic waveguides and horn antennas, though offering excellent gain and low transmission loss, are inherently bulky and incompatible with the miniaturized architecture of modern integrated circuits (ICs) [50, 52]. Their fabrication typically relies on mechanical machining or complex multi-layer assembly, which is unsuitable for standard CMOS or MEMS

processes and leads to increased cost and poor scalability for mass production [53, 54].

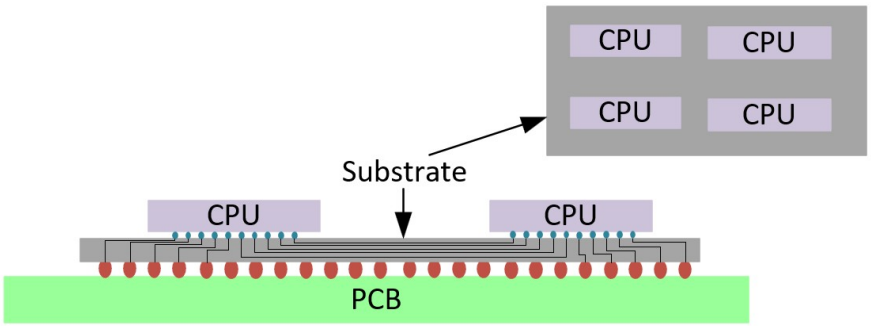


Figure 2.2: Multi-chip module with wired interconnects on a shared substrate, illustrating bottlenecks that motivate wireless on-chip THz links

Figure 2.2 illustrates a typical multi-chip module where dense metal interconnects link several CPU cores on a common substrate, highlighting the physical and bandwidth limitations that motivate wireless on-chip THz solutions. To overcome these limitations and to meet the urgent need for high-throughput intra- and inter-chip wireless links in AI/HPC platforms, on-chip antennas (OCAs) have emerged as a key enabling technology for compact and fully integrated THz front-ends. By integrating the radiating element directly onto the semiconductor substrate, OCAs eliminate the need for external interconnects and packaging transitions, significantly reducing parasitic losses and improving overall signal integrity [55, 56]. This monolithic approach enables the antenna, transceiver and base-band circuitry to coexist within a single silicon die, thereby realizing true system-on-chip (SoC) architectures that are compact, lightweight, power-efficient and better aligned with the scaling demands of AI-centric compute platforms.

From a system perspective, on-chip integration enables precise phase and amplitude control across multiple radiating elements, facilitating beamforming networks, phased arrays and massive multiple-input multiple-output (MIMO) architectures at THz frequencies [29, 57]. Furthermore, since the antennas can be fabricated using the top metal layers of standard CMOS or SiGe BiCMOS processes, the integration is fully

compatible with existing back-end-of-line steps [57, 58]. This compatibility simplifies co-design with amplifiers, mixers, and oscillators, allowing high-level integration without additional fabrication steps.

However, embedding antennas within semiconductor substrates introduces significant electromagnetic challenges. The high relative permittivity and loss tangent of typical substrates such as silicon ($\epsilon_r \approx 11.9$) or gallium arsenide ($\epsilon_r \approx 12.9$) confine the electromagnetic fields near the surface, resulting in substrate-guided modes, surface-wave propagation, and reduced radiation efficiency [59]. Consequently, the design of on-chip antennas involves a critical trade-off between miniaturization, radiation efficiency, and fabrication compatibility.

Despite these challenges, on-chip antennas provide numerous advantages for emerging THz applications. They enable cost-effective wafer-level batch fabrication, reduce packaging complexity, and support large-scale integration of transceivers for high-data-rate short-range communication, imaging, and sensing systems [60, 61]. As such, on-chip integration represents a fundamental step toward realizing compact, reconfigurable and fully monolithic THz transceivers, especially in the context of AI-driven multi-core and multi-chip platforms where high-speed wireless interconnects become mission-critical.

2.2.2 Key Challenges: Substrate Loss, Efficiency, Miniaturization

Despite their potential, on-chip antennas exhibit several fundamental challenges that limit their practical radiation performance at THz frequencies.

- **Substrate Loss:** At THz frequencies, the combined effect of finite metal conductivity and dielectric loss in the substrate leads to substantial attenuation of surface currents and radiated power. Silicon, the most common platform for THz circuits, exhibits a relatively high dielectric loss tangent ($\tan\delta \approx 0.005 - 0.02$)

and high relative permittivity ($\epsilon_r \approx 11.9$) [58, 62]. These properties confine electromagnetic energy within the substrate rather than allowing efficient radiation into free space, resulting in surface-wave excitation, substrate-mode coupling, and significant ohmic dissipation [59, 63]. Consequently, a large portion of the radiated energy becomes trapped in substrate-guided modes, which distort the radiation pattern and degrade overall efficiency.

To mitigate these effects, several approaches have been proposed. The use of high-resistivity silicon (HRS) substrates reduces conduction loss by minimizing free-carrier absorption [64]. Alternatively, micro-machined cavities or suspended membranes can physically separate the radiator from the lossy bulk [65]. Low-loss dielectric layers such as benzocyclobutene (BCB) or polyimide are also employed as superstrates to confine fields within low-loss regions [66]. More advanced configurations exploit substrate-integrated waveguide (SIW) and metamaterial (MTM) concepts, where quasi-metallic sidewalls or electromagnetic band-gap (EBG) structures suppress surface-wave propagation and enhance radiation into free space [67].

- **Radiation Efficiency:** The radiation efficiency of on-chip antennas generally remains within 20%–40% over the $0.1-1$ THz range, significantly lower than that of off-chip counterparts [68, 69]. This inefficiency arises from both material losses and impedance mismatch between the antenna and the surrounding circuitry (typically 50Ω). Achieving good matching requires careful co-design of the antenna geometry, feeding structure, and ground configuration [70].

  Moreover, as operating frequency increases, the skin depth of metals becomes comparable to the surface roughness and the thin back-end metallization layers used in CMOS or BiCMOS processes. This amplifies ohmic losses and disrupts uniform current flow across the radiating surface [29, 71]. Advanced solutions

employ dielectric resonators, artificial magnetic conductors (AMCs), or metasurface (MTS) superstrates to redirect radiated fields and achieve constructive interference between direct and reflected waves [61, 72]. These techniques can improve radiation efficiency beyond $70-80\%$, although they introduce additional design and fabrication complexity.

- **Miniaturization and Bandwidth:** While the sub-millimetre wavelength at THz frequencies naturally allows compact antenna layouts, excessive miniaturization severely limits the effective radiation aperture, resulting in reduced gain and narrow bandwidth [73, 74]. Most planar geometries, such as patches, dipoles, and slots, are inherently resonant and thus exhibit limited impedance bandwidths (often below 10%). Miniaturization through the use of high-ϵ_r substrates further exacerbates the problem by increasing stored reactive energy and reducing radiation resistance [75]. To overcome these limitations, broadband structures such as stacked patches, log-periodic arrays, or slot-coupled configurations have been investigated [76, 77]. In addition, multilayer stacking, metamaterial inclusions, and aperture-coupled feeds can extend the operational bandwidth while maintaining compactness [78]. The key design challenge, therefore, lies in achieving an optimal balance between physical miniaturization, radiation efficiency, and bandwidth, while ensuring compatibility with standard semiconductor fabrication processes.

2.2.3 Types of OCAs

2.2.3.1 Patch-Type and Slot-Based OCA

Patch and slot-based antennas are the most common on-chip implementations due to their planar geometry and direct compatibility with CMOS metal layers. Single or stacked patch antennas provide easy integration and impedance matching but often

suffer from narrow bandwidth and low radiation efficiency on silicon substrates. To enhance bandwidth and radiation, variations such as aperture-fed and slot-coupled patches are employed, where coupling slots or buried feeds excite the radiating surface while isolating it from the lossy substrate. Tapered-slot (Vivaldi) and bow-tie geometries further extend bandwidth and gain, whereas fractalized versions achieve miniaturization without significantly degrading performance. These structures remain the foundation for compact, broadband OCAs in the mm-Wave and low-terahertz regions.

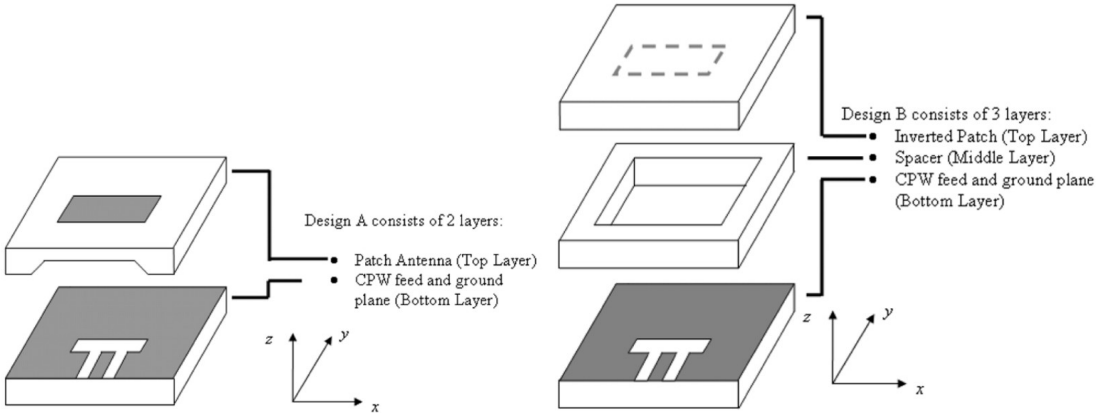


Figure 2.3: Three-dimensional schematic of the proposed CPW-fed microstrip patch antenna. (**a**) Configuration A: The radiating patch is positioned on the top surface of the upper substrate. (**b**) Configuration B: the patch is embedded on the lower surface of the upper substrate, functioning as a superstrate-loaded structure [79]

[79] study presents two high-gain 24 GHz microstrip patch antenna designs using high-permittivity substrates (Taconic CER-10 and high-resistivity silicon $\epsilon_r = 11.9$). Both antennas employ a CPW-fed slot-coupled multilayer structure with an air gap to suppress surface waves and enhance efficiency. Two configurations are analyzed: one with the patch on the top surface (Figure 2.3**(a)**) and another with the patch beneath the upper substrate acting as a superstrate (Figure 2.3**(b)**). The measured results show gains above 6 dBi and $|S_{11}| < -10$ dB, confirming strong impedance matching and stable radiation performance. The proposed CPW-fed air-gap approach demonstrates

an effective means for achieving compact, high-gain mm-wave antennas on silicon substrates.

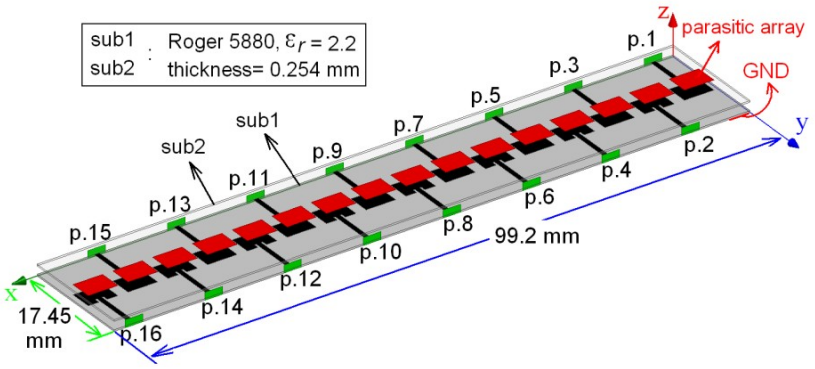
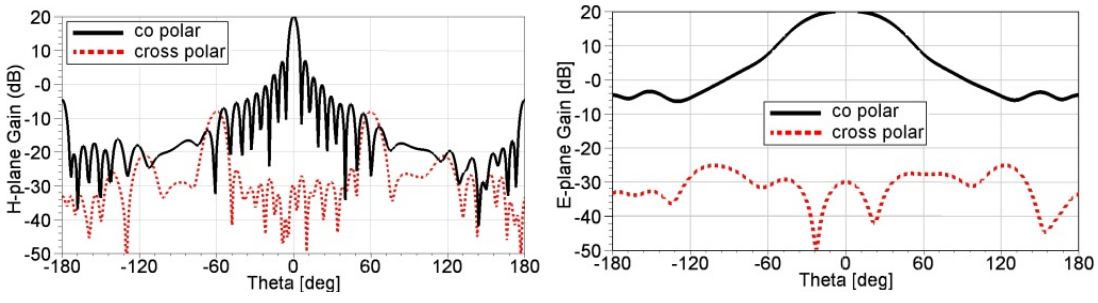


Figure 2.4: Layout of the $16-$Element $180°$ alternate parasitic-patch inset-fed patch array antenna [80]

A Ka-band 16-element inset-fed microstrip array antenna for 5G applications across $26-31$ GHz is presented in [80]. The overall antenna layout is illustrated in Figure 2.4, where parasitic patches are stacked above the main radiating elements and rotated by $180°$ to enhance radiation symmetry and reduce mutual coupling. The design achieves a 24.4% bandwidth, -15 dB reflection loss, and a broadside gain of 19.9 dBi. As desired, the main beam is centred at $\theta_0 = 0°$, with over 50 dB co-cross polarization isolation and an FTBR above 25 dB, as shown in Figures 2.5**(b-c)**.



(a) **(b)**

Figure 2.5: Simulated gains of the 16-element patch antenna array. **(a)** H-plane and **(b)** E-plane at 28 GHz [80]

Vivaldi and tapered slot antennas (TSAs) are widely employed in mm-wave and THz

systems for their broadband impedance and stable end-fire radiation. A 60 GHz OCA Vivaldi antenna demonstrates improved matching and radiation stability through optimized taper geometry and substrate configuration, enabling compact broadband integration [81]. Figure 2.6**(a)** demonstrates the structural evolution of the antenna, showing the introduction of corrugations and a reflector to optimize end-fire radiation. The S-parameter result in Figure 2.6**(b)** reveals that all configurations achieve reflection coefficients below -10 dB across $50-70$ GHz, with the final design exhibiting improved matching and gain. Similarly, a distributed stacked on-chip Vivaldi array at 180 GHz achieves $\approx 45\%$ bandwidth and high efficiency through multilayer integration suitable for high-speed THz interconnects [82]. Extending these principles, a compact four-port balanced antipodal Vivaldi antenna (BAVA) was proposed for $76-77$ GHz MIMO radar in autonomous vehicles [83]. The antenna, shown in Figure 2.7**(a)**, employs a symmetric flare geometry with strip-line feed transitions on an LTCC substrate to achieve wide bandwidth and compact integration. Figure 2.7**(b)** illustrates the distinct radiation patterns of each port, confirming effective pattern diversity with beam gains of $6-7$ dBi and high isolation. This configuration provides 90° beam coverage per module, supporting full 360° sensing when deployed at vehicle corners. Together, these works highlight the scalability of Vivaldi-based topologies for broadband and directional THz and mm-wave systems.

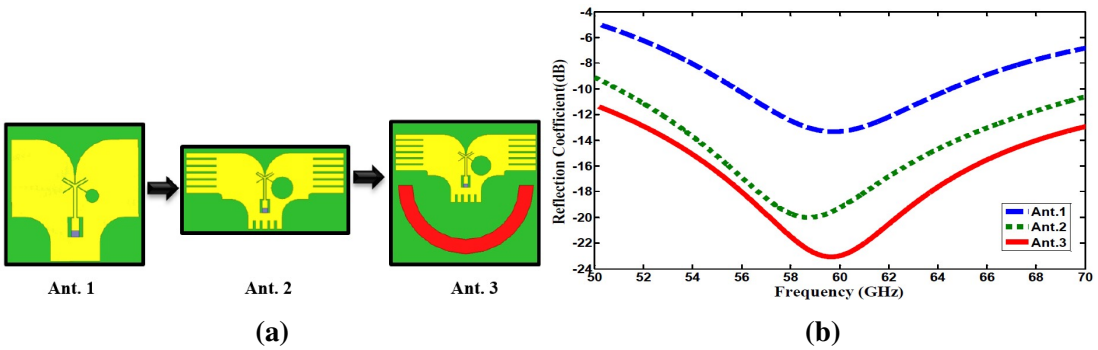
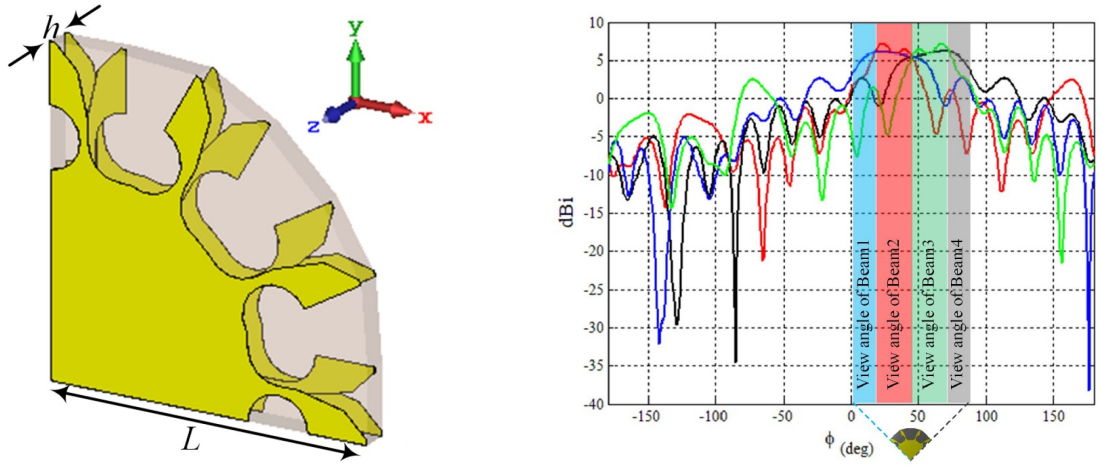
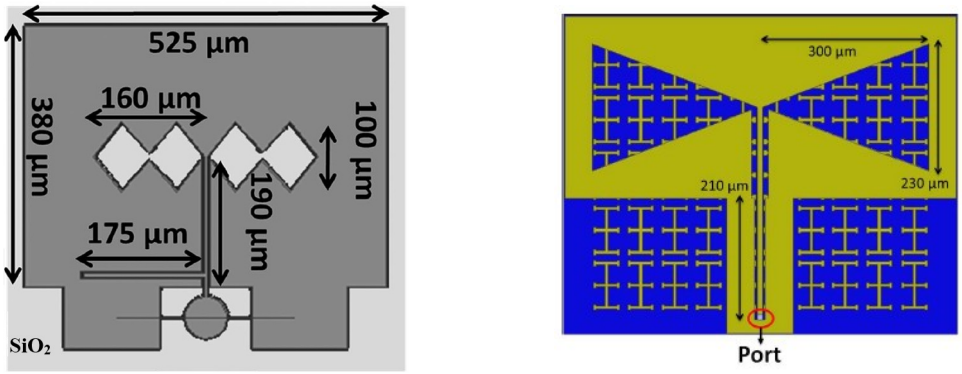


Figure 2.6: Tapered slot Vivaldi Antenna **(a)** Modification of designed antenna and **(b)** Simulated $|S_{11}|$ of the three design antenna [81]



(a) **(b)**

Figure 2.7: MIMO BAVA Antenna **(a)** Perspective view and **(b)** Radiation pattern in xy-plane [83]

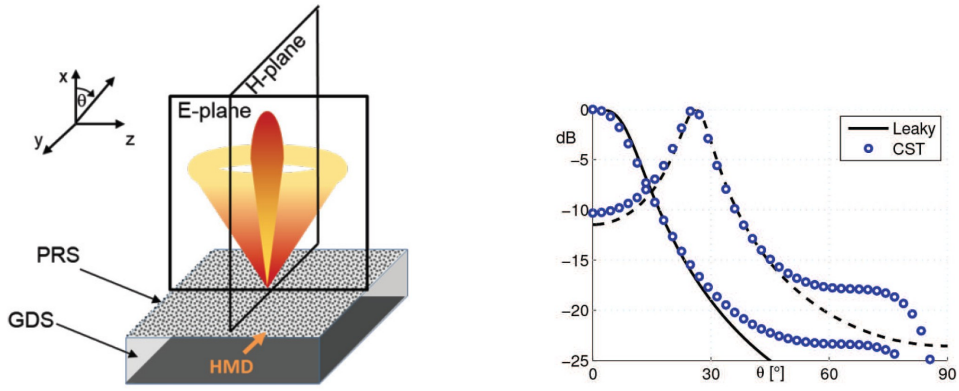


(a) **(b)**

Figure 2.8: Bowtie-slot OCA **(a)** Double-rhomboid [84] and **(b)** Back-to-back E-shaped FSS [59] Bowtie antenna

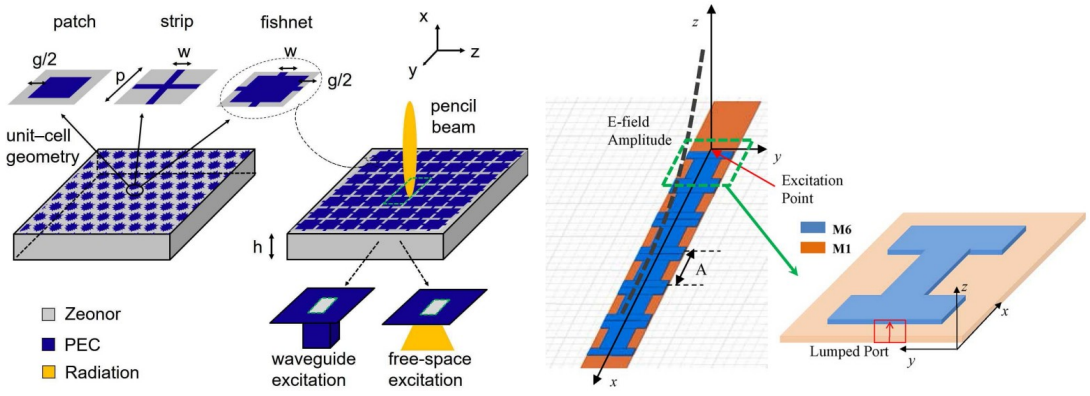
Bowtie-based OCA has emerged as a promising candidate for high-gain, wideband THz and mm-wave integration due to its planar structure and strong current concentration at the feed. In Figure 2.8**(a)** of the W-band double-rhomboid bowtie-slot design [84], an EBG-backed silicon substrate is used to suppress surface waves, improving radiation efficiency and FTBR. The optimized configuration achieves ≈ 10 dBi gain and $> 85\%$ radiation efficiency across the $85 - 105$ GHz band. Similarly, Figure 2.8**(b)** from the 94 GHz bowtie-slot antenna study demonstrates an E-shaped FSS backing, enhancing

impedance bandwidth ($\approx 14\%$) and providing effective isolation from the lossy silicon substrate [59]. Both approaches confirm that introducing EBG or FSS layers beneath the bowtie significantly improves radiation performance while maintaining CMOS compatibility and compactness.



(a) **(b)**

Figure 2.9: **(a)** The FPC-based leaky-wave antenna is energized by a horizontal magnetic dipole positioned parallel to the y-axis, serving as the primary excitation source and **(b)** Comparison of radiation pattern by analytical leaky-wave theory and CST simulation [85]



(a) **(b)**

Figure 2.10: **(a)** Model of the FPC-LWA with a homogenized metasurface. The upper inset shows unit-cell geometries with key dimensions, where the fishnet design yields a directive pencil beam. The lower inset illustrates two excitation schemes: waveguide-fed and back-illuminated slot [86] and **(b)** Six dogbone elements aligned along x with period p form a high-impedance surface under y-periodic boundaries. The dashed line shows the leaky wave's exponential decay from the feed edge [87].

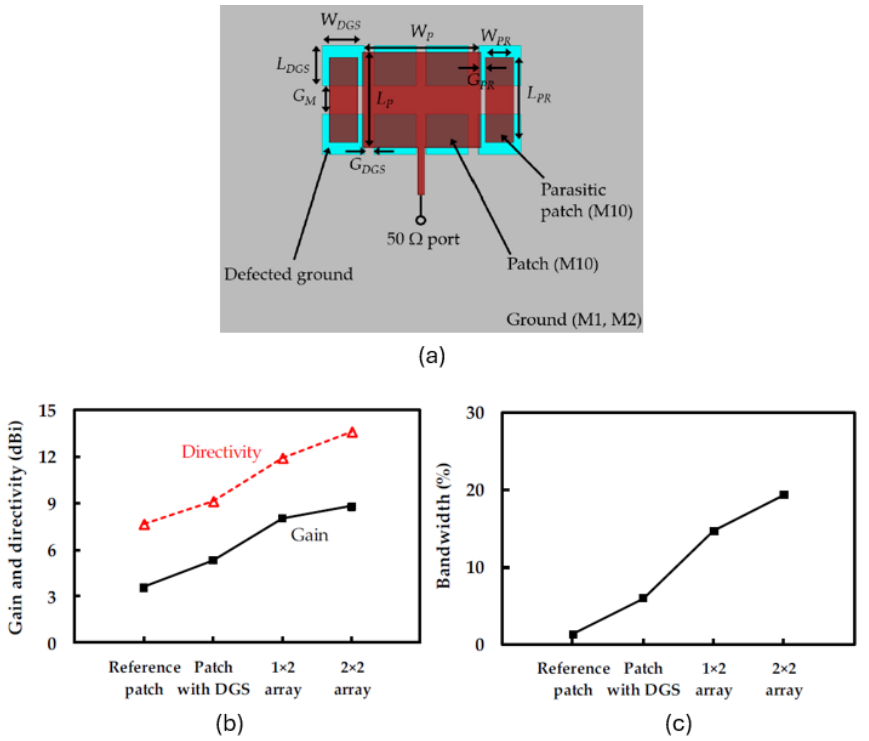


Figure 2.11: **(a)** Proposed CMOS on-chip patch antenna with DGS and **(b-c)** Gain and bandwidth of OCA array as a function of element spacing [88]

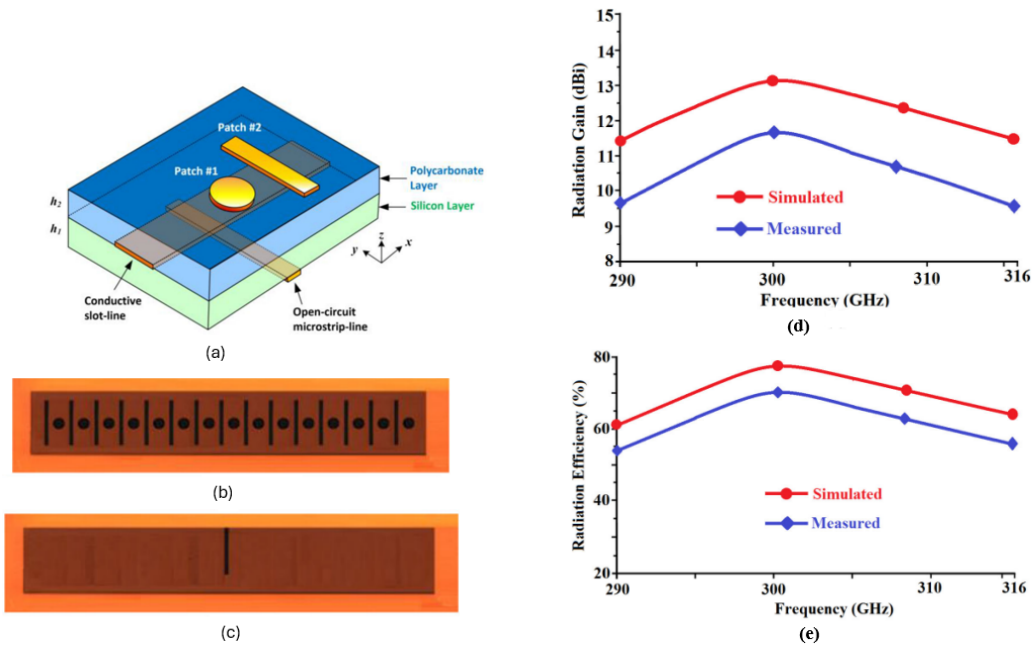


Figure 2.12: Silicon-based integrated OCA: **(a)** Side view with partial magnification; **(b)** top view of the 15-element array; **(c)** bottom view; **(d)** gain versus frequency; and **(e)** radiation efficiency [89]

Leaky-wave antennas (LWAs) at THz frequencies have gained attention for their ability to provide frequency-controlled beam steering and high directivity in compact platforms. Fuscaldo et al. [85] introduced a Fabry–Perot cavity (FPC) LWA as illustrated in Figure 2.9**(a)** based on a homogenized fishnet metasurface, where the tunable surface reactance enables beam scanning with minimal dispersion. Figure 2.9**(c)** illustrates the beam steering characteristics across different operating frequencies, validating the leaky-wave theory (black lines) predictions through full-wave simulations (blue circles). In related research, [86] presented a systematic methodology for designing terahertz leaky-wave antennas (LWAs) utilizing homogenized metasurface-based partially reflective surfaces (PRSs). The proposed FPC-LWA homogenized metasurface antenna model (Figure 2.10**(a)**) effectively demonstrates the integration of periodic PRS elements to control the phase distribution and leakage constant, thereby enabling high-gain radiation with tunable beam directivity. The simulated and theoretical results exhibit strong correlation, validating the accuracy of the homogenization approach and the efficiency of the metasurface configuration in beam-steering applications at THz frequencies. Additionally, Pan et al. [87] proposed an ultra-thin metasurface-backed BiCMOS on-chip LWA antenna having aligned six dog-bone elements as illustrated in Figure 2.10**(b)** operating at 94 GHz, achieving high gain and bandwidth in a compact form. Collectively, these studies highlight metasurface-assisted LWAs as compact, tunable, and fabrication-friendly options for THz communication systems. These metasurface-based LWAs provide reconfigurability, compactness, and fabrication compatibility, making them promising candidates for THz communication and sensing systems.

A THz CMOS on-chip patch antenna presented by [88] using a defected ground structure (DGS) to enhance gain, bandwidth, and radiation efficiency. The proposed antenna configuration, illustrated in Figure 2.11**(a)**, incorporates a DGS beneath the radiating patch to improve radiation resistance and reduce mutual coupling between antenna elements. The variation of gain and directivity with element spacing is shown in Figure

2.11**(b-c)**, demonstrating improved radiation performance and array behavior. A 1×2 and 2×2 antenna array is implemented, achieving gains up to 8.2 dBi with bandwidth up to 28% at 300 GHz. The proposed design demonstrates a low-cost, high-performance solution fully compatible with standard CMOS processes.

A high-gain sub-THz OCA using an aperture-fed mechanism on a silicon-polycarbonate substrate is presented by [89]. A 15-element array of circular and rectangular patches is excited via a slot-line coupled to an orthogonal open-ended microstrip as illustrated in Figure 2.12**(a-c)**. The antenna achieves a measured gain of 11.7 dBi and radiation efficiency of 70% at 0.3 THz, with a wide operating bandwidth from 0.29 to 0.316 THz as shown in Figure 2.12**(d-e)**. Its compact size ($20 \times 3.5 \times 0.126$ mm^3) makes it suitable for integrated sub-THz systems.

Table 2.1 consolidates recent patch- and slot-based on-chip antenna designs, spanning from early CPW-fed microstrip structures to hybrid metasurface-backed and tapered-slot geometries.

Table 2.1: Comparison of patch and slot-based OCA used in literature review designs.

Reference	Type	Design	Performance	Remarks
[87]	Patch /MTS	Ultra-thin MTS radiator (10μm SiO_2) using BiCMOS M1 ground	2.5 dBi gain; > 10 GHz BW	Fully on-chip patch, compact, wideband design
[84]	Slot/EBG	Double-rhomboid bowtie-slot with E-shaped EBG reflector	-0.58 dBi gain; $75-100$ GHz BW	EBG enhances efficiency; 1×1 mm^2 die
[59]	Slot/FSS	Bowtie-slot OCA with E-shaped FSS backing in BiCMOS	Gain ↑ from -2.7 to -1.9 dBi; $S_{11}< -10$ dB ($90-105$ GHz)	Gain enhancement without extra processing
[86]	Slot/ MTS hybrid	Homogenized fishnet MTS radiator with Fabry-Perot cavity	$15-30$ directivity	Foundational method for MTS slot antenna design
[85]	Slot/ Tunable MTS	Fabry-Perot slot antenna with graphene & liquid crystal PRS	Beam steering > 30°; reconfigurable pattern	Demonstrates tunable MTS slot antenna concept
[81]	Tapered-Slot (Vivaldi)	CPW-fed vivaldi with corrugated edges and arc reflector	-0.4 dBi gain; $\eta = 32\%$	End-fire on-chip design with improved gain & back lobe control
[80]	Patch Array	16-element parasitic patch array with phase-rotated feeds	19.9 dBi gain; 24% BW ($24-31$ GHz)	High-gain array with low SLL for Ka-band front-ends
[79]	Patch Slot-Coupled	Dual-substrate patch feb by CPW with air gap for wave suppression	> 6 dBi gain at 24 GHz	Early patch/slot hybrid reducing surface wave loss
[88]	Patch with DGS	CMOS patch antenna with DGS extended to an array	Gain: 8.2 dBi bandwidth: 28% at 300 GHz	DGS improves bandwidth, gain, and isolation; compact and CMOS-compatible
[89]	Cavity/aperture-coupled array	Aperture feed via slotline to $15-$ element patch array	$0.29-0.316$ THz; $\eta = 70.8\%$; Gain: 11.71 dBi	Wideband sub-THz on silicon with high efficiency

2.2.3.2 Dipole, Monopole, and Loop OCA

Dipole and monopole AoCs are simple, balanced or unbalanced radiators that are easy to co-design with differential transceivers. Their symmetry allows direct integration with on-chip differential ports, minimizing matching networks. Monopoles offer compactness and reduced substrate-cavity losses, while loops or inductive coils rely on

magnetic coupling, making them suitable for near-field or power-harvesting applications such as RFID and biomedical implants. Enhanced variants, such as artificial-magnetic-conductor (AMC)-backed monopoles, improve radiation efficiency and circular polarization by reflecting fields in-phase. Yagi and quasi-Yagi configurations extend this family toward directional radiation, yielding higher gain and enabling phased-array integration for 5G and THz beamforming links.

Dipole OCAs have been extensively investigated across CMOS and SiGe technologies to enhance radiation efficiency and mitigate substrate losses in mm- and THz-wave applications.

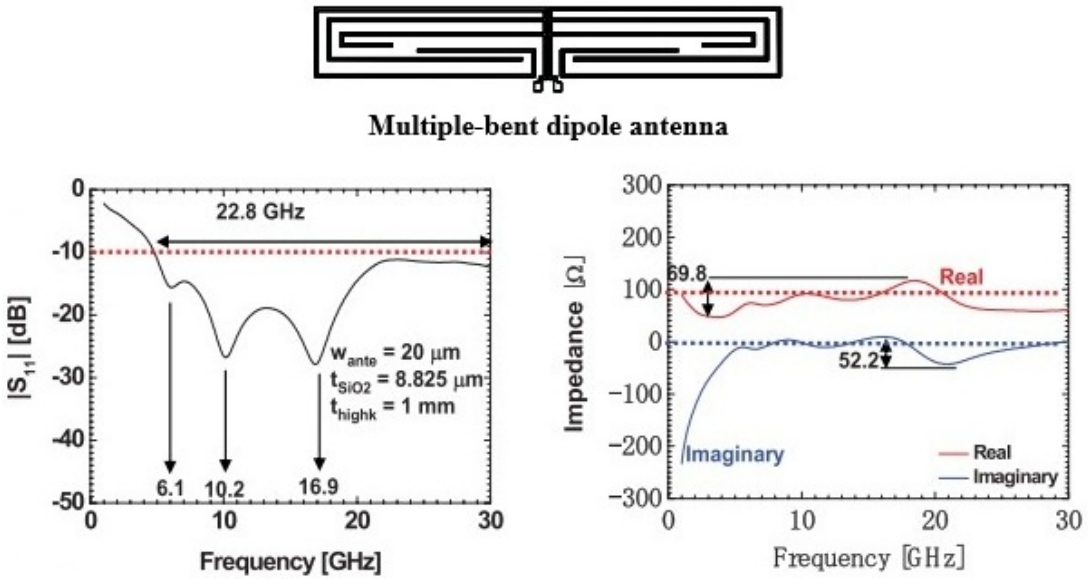


Figure 2.13: Plain view and EM response of the multiple-bent antenna, illustrating its structural layout, simulated return loss S_{11}, and corresponding complex impedance characteristics [90].

At lower frequencies, Kubota et al. [90] demonstrated a 10 GHz multiple-bent dipole antenna fabricated in 65 nm CMOS, integrated with a higher$-\kappa$ interposer ($\epsilon_r = 38$) that guided EM laterally, achieving 22.8 GHz bandwidth and reliable 2 Gb/s inter-chip communication over 10 mm. The Figure 2.13 shows the S_{11} and impedance of multiple-bent dipoles, effectively illustrating the impedance-matching optimization enabling

wideband impulse transmission. Building upon this, Hirano et al. [91] introduced a 60 GHz CMOS dipole antenna employing helium-3 ion irradiation to locally reduce silicon conductivity to 0.01 S/m, which increased radiation efficiency from 5% to 48% and yielded 2.7 dBi gain at 62 GHz, a pioneering demonstration of substrate modification for mm-Wave OCAs.

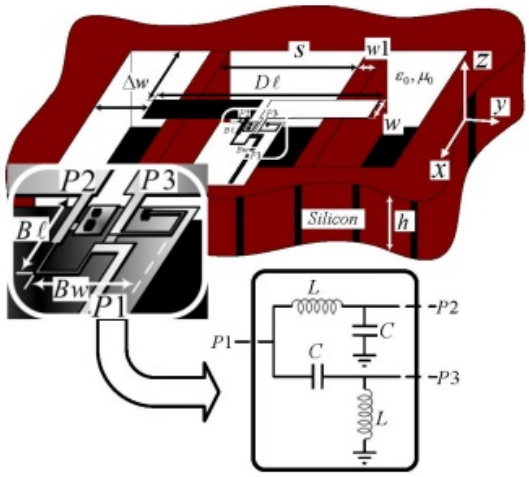


Figure 2.14: 3D schematic of the designed 77 GHz flat dipole antenna, accompanied by its equivalent lumped-element circuit model representing the feeding LC balun for impedance transformation and balanced excitation [92].

At 77 GHz, Seyyed-Esfahlan et al. [92] developed a SiGe strip dipole integrated with a lumped balun circuit and a finite-size ground plane fabricated using the IHP LBE module, achieving 4 dBi measured gain and $7 - 12$ GHz impedance bandwidth. Figure 2.14 depicts the integrated dipole-balun schematic on an etched substrate, clearly demonstrating the use of balanced feeding and localized etching to reduce dielectric losses and enhance directivity. Advancing toward the D-band, Ng and Kissinger [93] designed a 120 GHz two-channel SiGe BiCMOS radar sensor employing folded on-chip dipoles fabricated with a selective localized backside etching (LBE) technique. The structure achieved 6 dBi gain, 54% efficiency, and +6 dB EIRP improvement, making it one of the earliest MIMO-capable on-chip radar front-ends.

At higher frequencies, Sato et al. [94] introduced a 140 GHz CMOS folded dipole

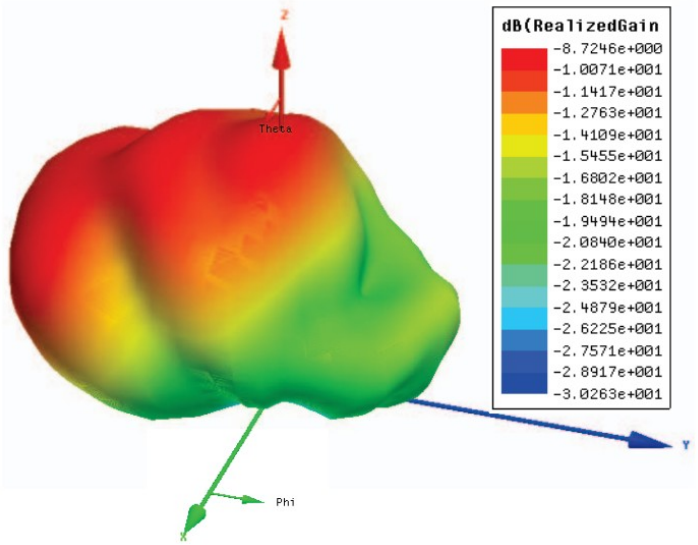


Figure 2.15: Simulated radiation pattern with vertical reflecting structure (VRS) [94].

antenna featuring a vertical reflector structure (VRS) and ion-irradiated high-resistivity silicon, achieving a 5 dB gain enhancement and -2.7 dBi measured gain. Figure 2.15 shows the simulated radiation pattern with the vertical reflecting structure, effectively visualizing how unidirectional emission and substrate optimization boost efficiency in deep-sub-micron CMOS. Pushing into the sub-THz regime, Guo et al. [95] realized a dual-polarized 300 GHz on-chip antenna enabling full-duplex operation by orthogonally coupling two dipoles, achieving -1.6 dBi gain with cross-polar isolation better than 20 dB, suitable for compact 300 GHz transceivers. Similarly, Zhang et al. [96] presented three antenna-array designs operating from 37 GHz up to 140 GHz using broadband dipole-array architectures for mm-Wave and terahertz systems. The 140 GHz implementation, fabricated in LTCC, achieves $\approx$ 20.5 dBi peak gain and 59% radiation efficiency, confirming broadband and high-gain performance. Finally, El Masri et al. [9] investigated Ka-band ($30 - 40$ GHz) integrated dipoles on high-resistivity silicon, achieving $\sim$ 1.7 dB gain and 21% bandwidth, and identified cavity-mode and surface-wave resonances as key loss mechanisms in intra-chip WiNoC channels.

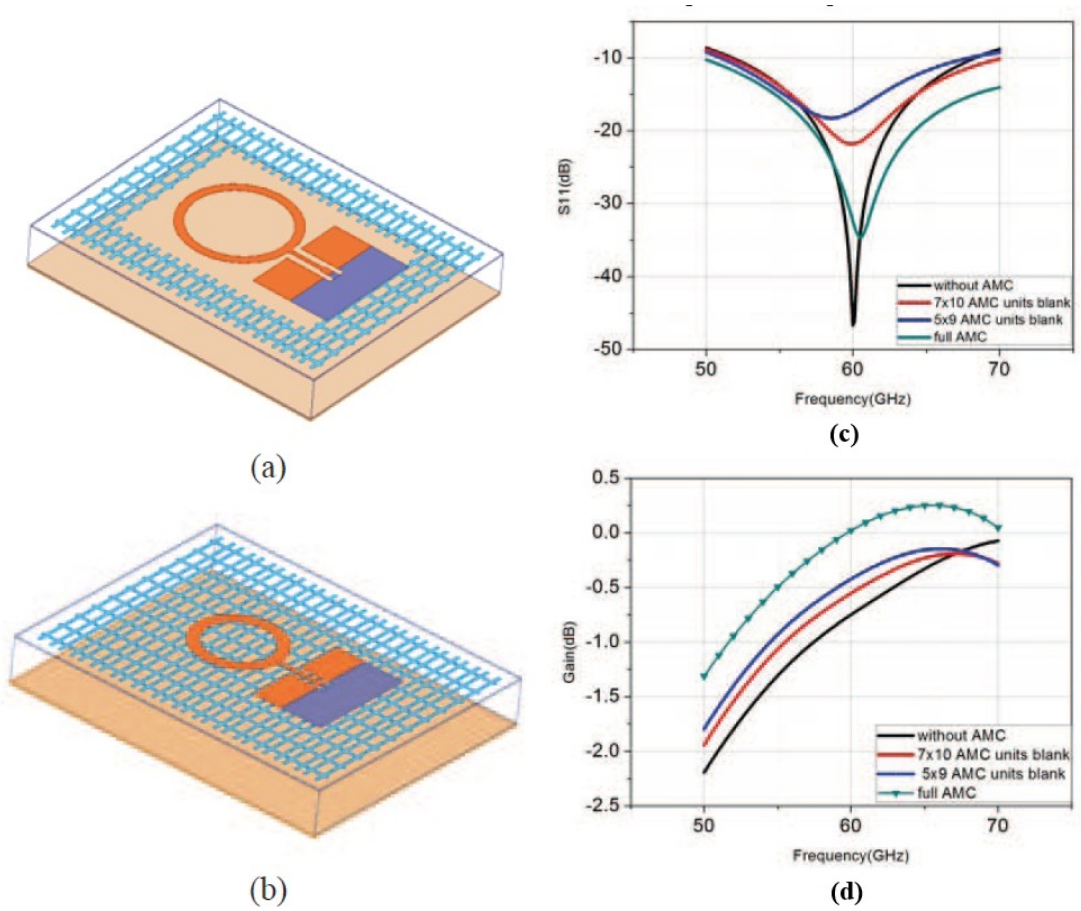
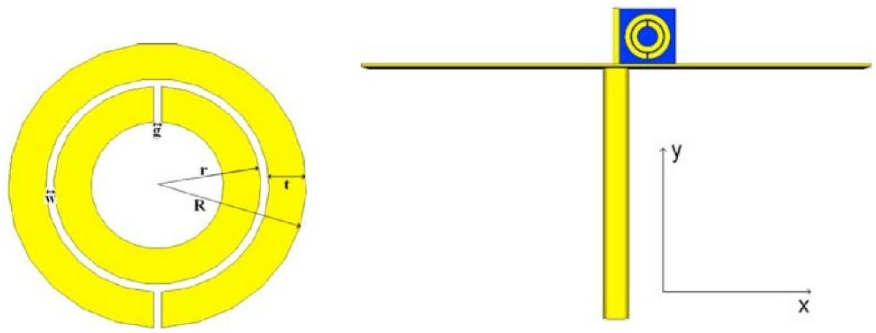


Figure 2.16: OCA configuration with **(a)** partially 7×9 AMC units and **(b)** a fully implemented AMC surface; Simulated result with different AMC planes **(c)** $|S_{11}|$ and **(d)** gain [97].



(a) Split-ring-resonator (SRR) **(b) SRR inserted monopole antenna**

Figure 2.17: Structural illustration of the **(a)** split-ring resonator (SRR) and **(b)** its integration within the monopole antenna configuration [98].

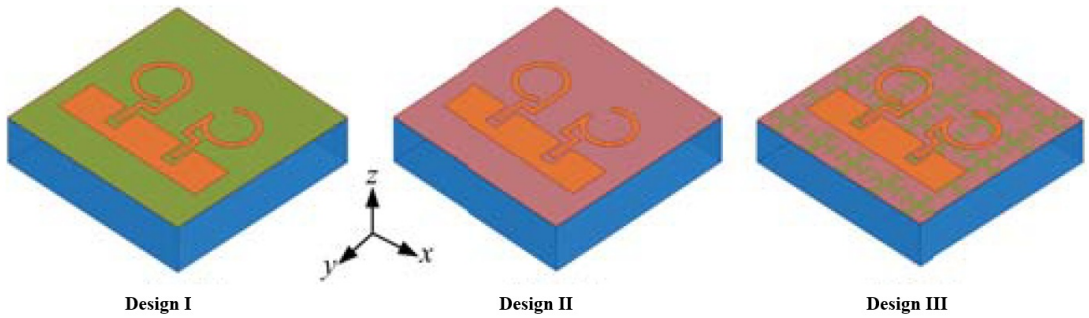
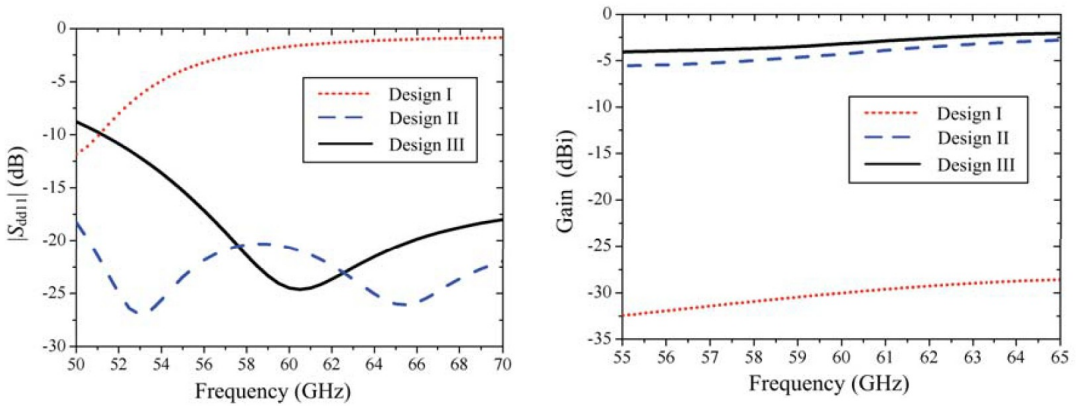


Figure 2.18: Geometrical comparison of three on-chip antennas fabricated on the M1 layer: Design I with a PEC surface, Design II without any underlying surface, and Design III incorporating an AMC structure [73].



(a) (b)

Figure 2.19: Comparison of simulated OCA of three designs **(a)** $|S_{dd11}|$ and **(b)** gain [73].

Upadhyay et al. [99] designed a circular disk monopole on a CMOS substrate, achieving a wide impedance bandwidth ($40 - 70$ GHZ) with $|S_{11}| = -31.5$ dB at 58.5 GHz and -4.9 dB gain at 60 GHz. To mitigate silicon losses, [97] introduced a circular ring monopole integrated with an AMC reflector as illustrated in Figure 2.16, which improved gain from -0.75 dB to 0.02 dB and radiation efficiency from 29% to 35%. Figure 2.16**(b)** shows the S_{11} and gain comparison of antennas with and without AMC, demonstrating enhanced bandwidth. At lower microwave frequencies, Alici and Özbay [98] proposed a split-ring-resonator (SRR)-loaded monopole (Figure 2.17), achieving -32 dB return loss, 6.5 dBi directivity, and 42.9% efficiency.

Artificial magnetic conductors (AMCs) have been employed to counter silicon substrate losses and enhance gain in OCA. [100] designed a 60-GHz circularly polarized loop antenna integrated with a modified AMC reflector in 0.18μm CMOS, achieving 4.4 dBi gain and a $57-67$ GHz circular-polarization bandwidth within a compact $1.8 \times 1.8 \times 0.3$ mm^3 chip. Similarly, Wang and Sun [73] developed a differential-red circularly polarized antenna using a Jerusalem-cross AMC, yielding 9.1 % axial-ratio bandwidth and -3.2 dBi gain with stable radiation. Figure 2.18 - 2.19 illustrate the design evolution and simulated performance of the AMC-backed on-chip antennas. Figure 2.18 presents the geometrical configurations of the three designs, Figure2.19**(a)** depicts the corresponding impedance bandwidth characteristics, and Figure 2.19**(b)** compares the simulated gains, revealing an enhancement from -3.2 dBi to 1.1 dBi. Alibakhshikenari et al. [101] proposed a high-gain on-chip antenna employing a metasurface-based artificial magnetic conductor (AMC) structure using a 2D composite right/left-handed (CRLH) transmission line on a polyimide substrate for sub-terahertz integrated circuits. The AMC, formed by concentric metallic and dielectric rings, effectively suppressed surface waves and substrate losses, resulting in 8.15 dBi gain and 65.7% efficiency across $0.35-0.385$ THz. Together, these designs confirm that AMC integration significantly improves gain and polarization while remaining CMOS-compatible.

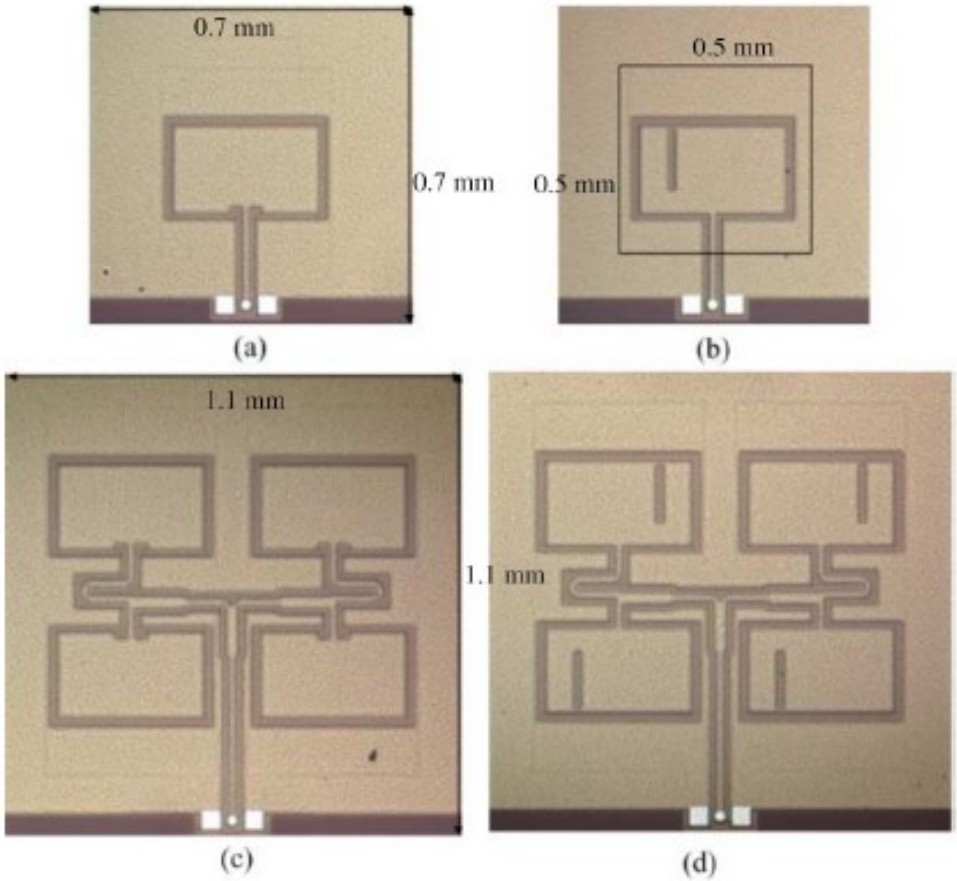


Figure 2.20: Micrograph of the fabricated on-chip antenna prototypes and their corresponding arrays: **(a)** Antenna 1, **(b)** Antenna 2, **(c)** Array 1, and **(d)** Array 2 [102].

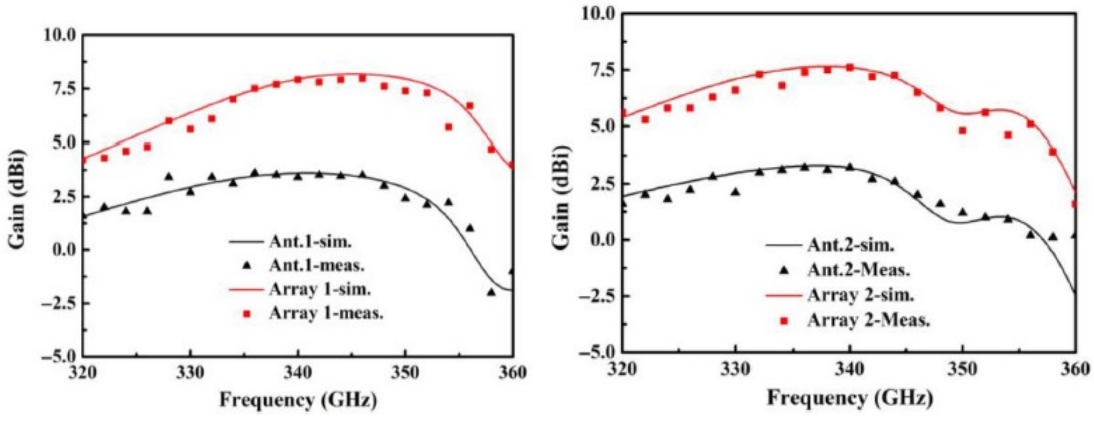


Figure 2.21: Simulated and measured gain performance of antennas and their corresponding arrays **(a)** Ant.1 with Array 1, and **(b)** Ant.2 with Array 2) [102].

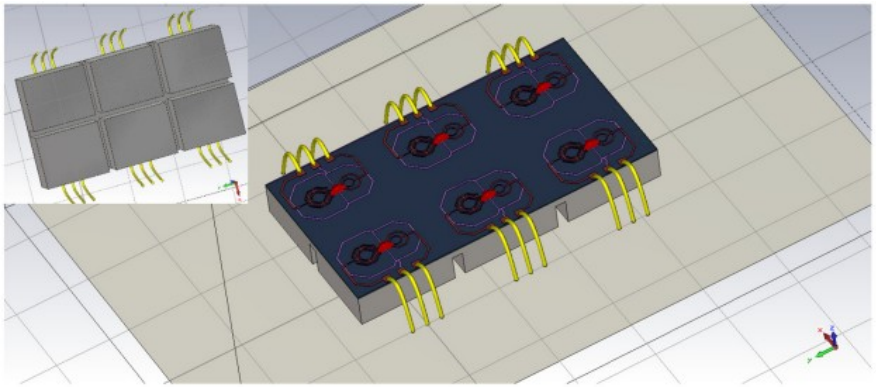
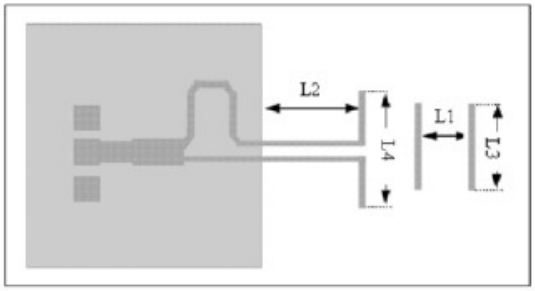
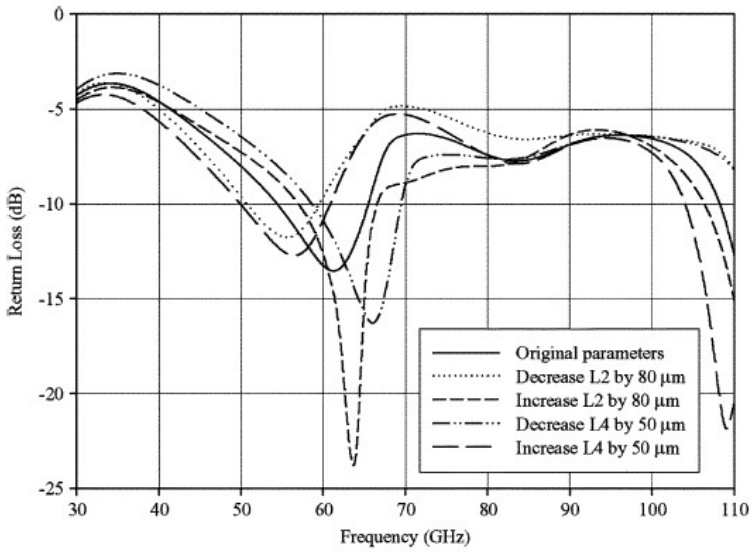


Figure 2.22: Structural model of the 2×3 loop-antenna array illustrating the element arrangement and mutual-coupling configuration [103].

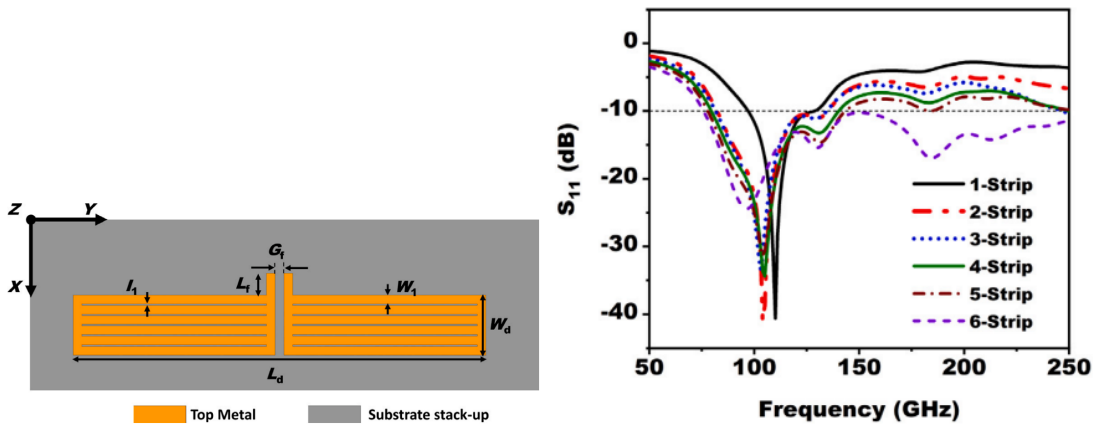


(a)



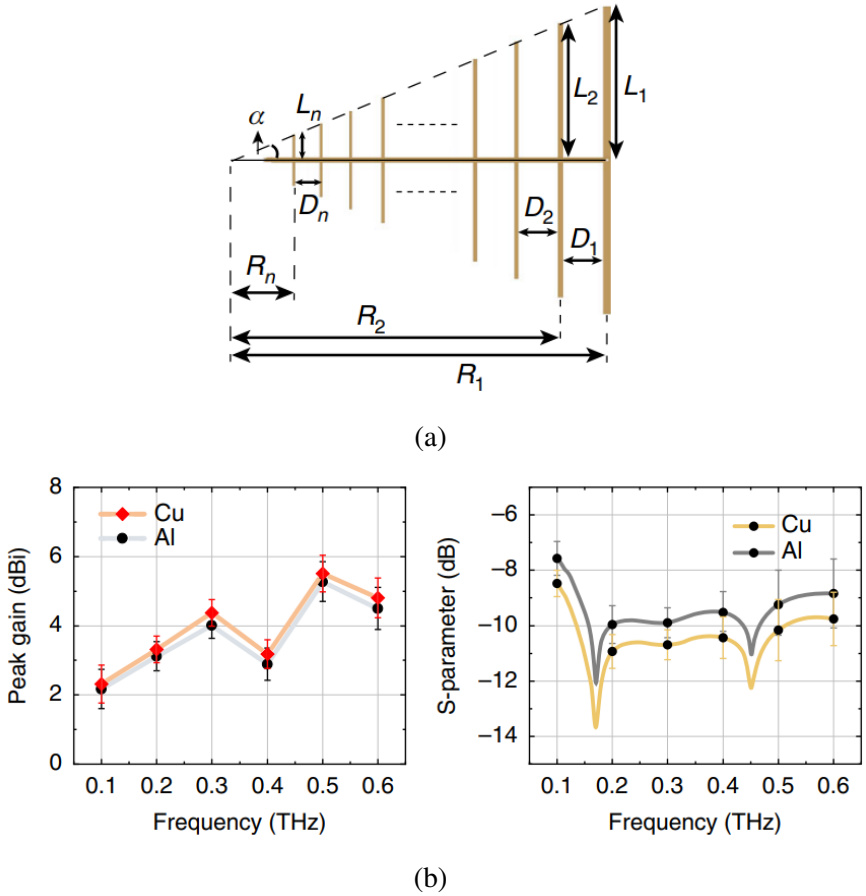
(b)

Figure 2.23: **(a)** layout of the quasi-Yagi OCA and **(b)** return loss with variation of the parameters [57]



(a) (b)

Figure 2.24: **(a)** Configuration of the proposed 6-strip straight-slotted on-chip antenna; **(b)** simulated S_{11} responses for on-chip dipole antennas with 1 to 6 strips [104]



(a)

(b)

Figure 2.25: **(a)** Linear log-periodic antenna schematic **(b)** MCLPA gain and S_{11} over $0.1 - 0.6$ THz [105]

Loop-type OCA have gained attention for compact, high-efficiency THz and mm-wave integration. Song et al. proposed a V-band dielectric resonator antenna excited by a CMOS loop, achieving 8 dBi gain and 96.7% efficiency using a high-resistivity substrate and off-chip ground [106]. Deng et al. developed a 340 GHz SIW cavity-backed magnetic slot loop antenna, reaching 7.9 dBi gain and 48% efficiency through field confinement in the SIW cavity [102]. Figure 2.20 illustrates the micrograph of the rectangular loop antenna and array configuration. Figure 2.21**(a-b)** illustrates the gain enhancement achieved through array synchronization, demonstrating how the loop structure forms a magnetic current radiator that improves overall performance. At higher frequencies, [103] demonstrated a 300 GHz wirelessly locked 2×3 loop array (Figure 2.22), achieving $+5.4$ dBm power and 5.1% DC-to-RF efficiency in 65 nm CMOS.

Yagi-type on-chip antennas offer high directivity and gain for silicon-based mm-wave systems. Zhang et al. [57] designed a 60 GHz quasi-Yagi antenna using a post-BEOL CMOS process, achieving 12.5 dBi gain and -6.75 dB return loss, demonstrating compact end-fire radiation on silicon. Figure 2.23**(a)** shows the layout of the quasi-Yagi antenna, and Figure 2.23**(b)** shows the measured return loss of this antenna, demonstrating good agreement and wide bandwidth performance from $55-65$ GHz. At higher frequencies, [64] realized a 340 GHz 3D Yagi-like on-chip antenna combining an SIW cavity-backed driver with a dielectric resonator director, attaining 10 dBi gain and 80% efficiency in 0.13 µm SiGe BiCMOS. [104] investigates on-chip dipole antennas in the sub-THz range, introducing slotted topologies to enhance impedance bandwidth while complying with foundry design rules. The straight-slotted dipole is chosen for its simplicity and flexibility. A $6-$strip design, shown in Figure 2.24**(a)**, achieves an ultra-wide $76-262$ GHz bandwidth (110% fractional) with -0.6 dBi gain, as illustrated in Figure 2.24**(b)**, while occupying minimal silicon area. A novel micro circular log-periodic antenna (MCLPA) is proposed by [105], optimized using an evolutionary neural

network (ENN) for THz applications, as shown in Figure 2.25**(a)**. The ENN-driven design enables efficient optimization, achieving ultra-wide bandwidth ($0.135 - 0.507$ THz) and a peak gain of 5.51 dBi, as illustrated in Figure 2.25**(b)**, with high radiation efficiency ($\sim 82\%$). The compact circular architecture enhances integration capability while maintaining broadband performance and high sensitivity for THz detection.

Table 2.2: Comparison of dipole-, monopole-, loop-type OCA used in literature review designs.

Reference	Type	Key Features	Performance	Remarks
[103]	Dipole Array	2×3 on-chip dipoles wireless injection locking	EIRP 5.4 dBM; η =5.1%; at ∼300 GHz	Coherent THz on-chip dipole array with integrated source
[95]	Dipole & Monopole	Orthogonal dipole-monopole pair on InP/BCB	4.9 dBi; BW ≈36 GHz; Isolation > 90 dB	Full-duplex operation via cross-polarized isolation
[100]	Loop/AMC	Dual open-loop with integrated AMC reflector	4.4 dBi; axial ratio BW 57-67 GHz	AMC surface improves gain and circular polarization
[99]	Monopole	CPW-fed circular disk monopole on Si	-4.8 dBi; 45-70 GHz BW	Simple wideband monopole; low-efficiency
[9]	Dipole	$\lambda/2$ dipole on high-resistivity Si	1.7 dB at 30 GHz; BW 6.7 GHz	Validated on-silicon; low-loss Ka-band link
[96]	Dipole Array	8×8 SIW-fed magneto-electric dipoles	26.7 dBi; BW≈17%	High-gain scalable array; packaging reference
[107]	Dipole/Loop hybrid	Polyimide CRLH-TL MTS radiator	8.1 dBi; BW 350-385 GHz; η =66%	MTS enhances bandwidth & efficiency
[98]	SRR & Monopole	SRR coupled with a quarter-wave monopole	3.52 GHz; Gain 2.35 dBi; η =42.9%	Electrically small; steerable by multi-SRR arrangement
[97]	Monopole/AMC	Circular CPW-fed ring monopole on 0.18 μm CMOS AMC plane	0.02 dBi at 60 GHz; η ≈35%; BW 57-66 GHz;	AMC raises efficiency and gain without additional loss
[104]	square slotted dipole	$1 - 6$ strips straight-slotted on-chip dipole antenna	$76 - 262$ GHz 110% fractional bandwidth	Small silicon area 567μm $\times 112\mu$m
[105]	MCLPA (micro Circular Log-Periodic Antenna)	Circular log-periodic structure ENN-based optimization compact & broadband design	$0.135 - 0.507$ THz; Gain $= 5.51$ dBi; $\eta \sim 82\%$; $S_{11} \approx -13.7$ dB	High bandwidth & η with compact size; Suitable for THz detection

2.2.3.3 SIW and MTM/MTS-Based OCA

Advanced electromagnetic structures such as metamaterials (MTMs), metasurfaces (MTSs), and substrate-integrated waveguide (SIW) platforms have emerged as key enablers of high-performance system-on-chip (SoC) antennas [60]. These engineered media enhance impedance bandwidth and radiation efficiency by suppressing surface-wave modes and tailoring phase propagation. Their compatibility with high-permittivity substrates like silicon, GaAs, and polyimide allows compact integration with microwave integrated circuits (MICs). MTMs and MTSs exhibit engineered dispersion and negative refractive index properties, enabling miniaturized, broadband, and efficient THz components [52].

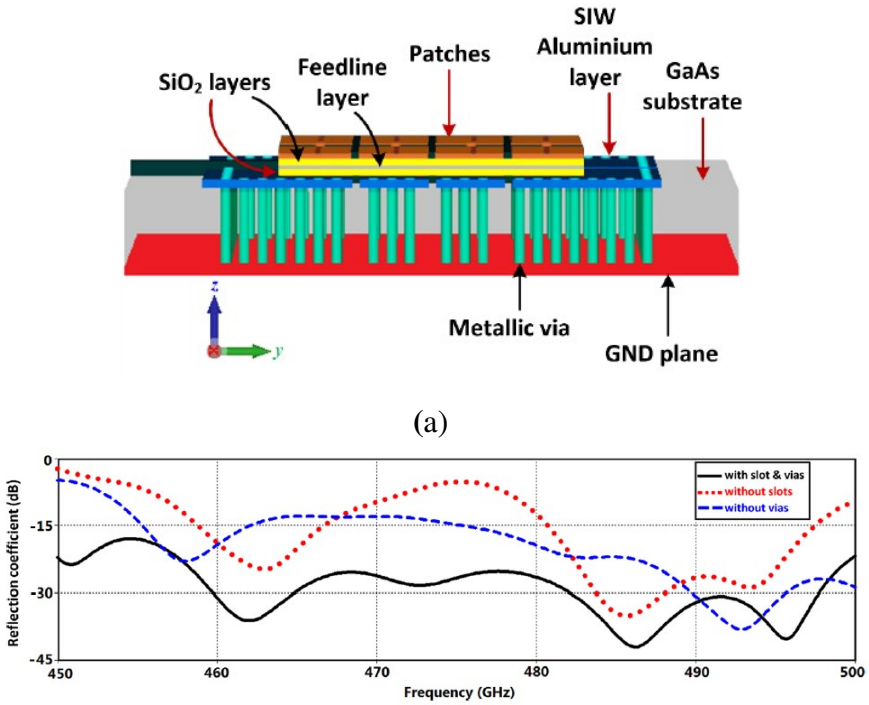


Figure 2.26: Metamaterial and SIW technology incorporated OCA [61]

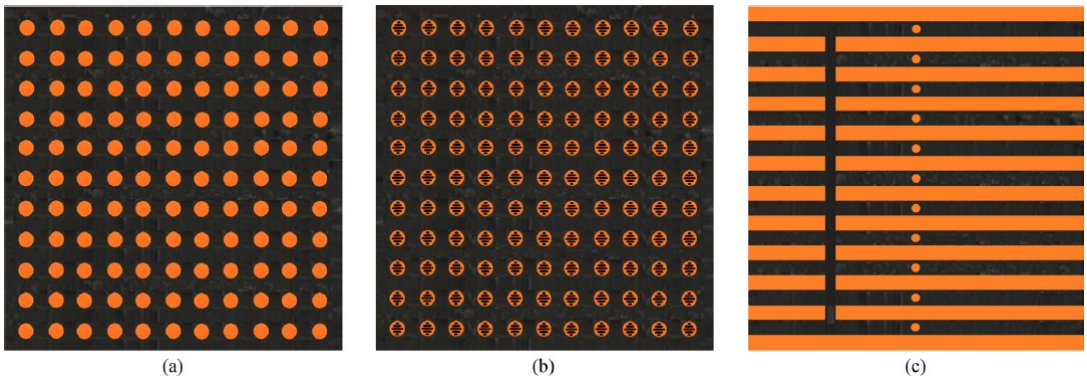


Figure 2.27: Fabricated on-chip antenna prototypes comparing the reference design (without metasurface slots) and the proposed design (with metasurface slots). **(a)** Top view of the reference antenna, **(b)** top view of the metasurface-integrated antenna, and **(c)** back view of both designs. [71]

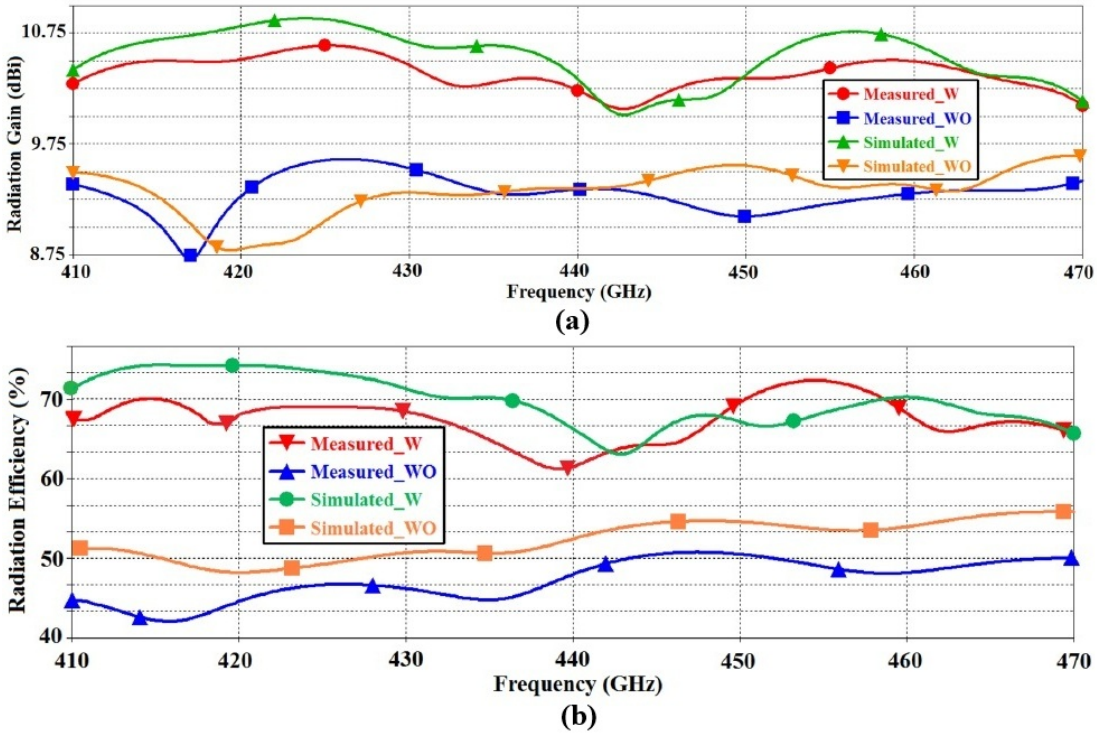
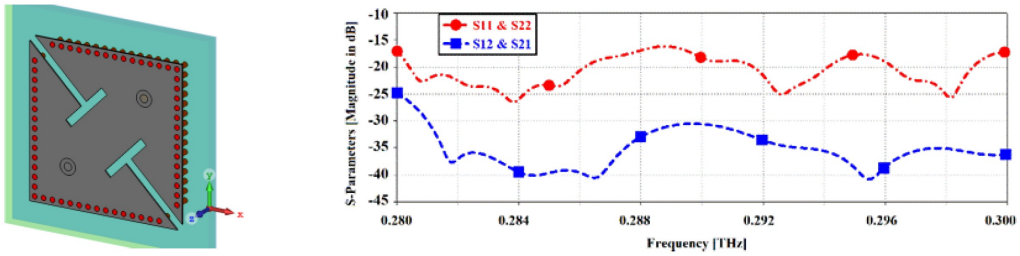


Figure 2.28: Simulated and measured **(a)** radiation gain and **(b)** efficiency plots for the on-chip antennas without (WO) and with (W) metasurface slot-lines. [71]



(a) (b)

Figure 2.29: **(a)** MTM–SIW on-chip antenna layout and **(b)** Simulated reflection and transmission coefficients [67]

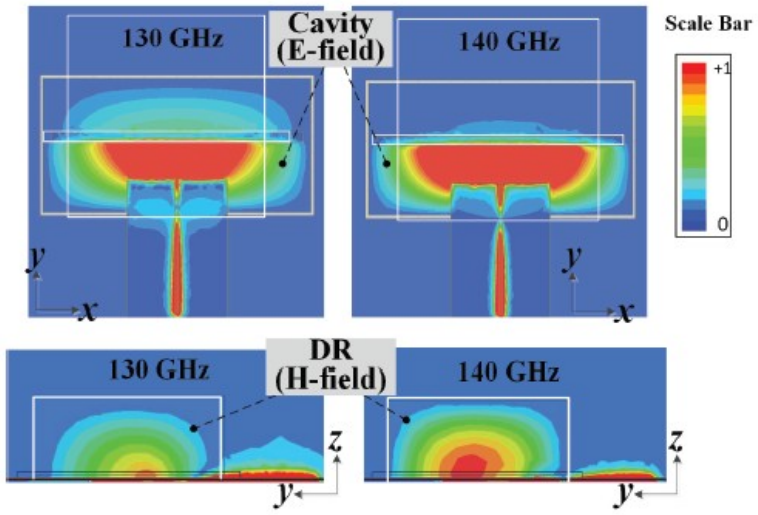
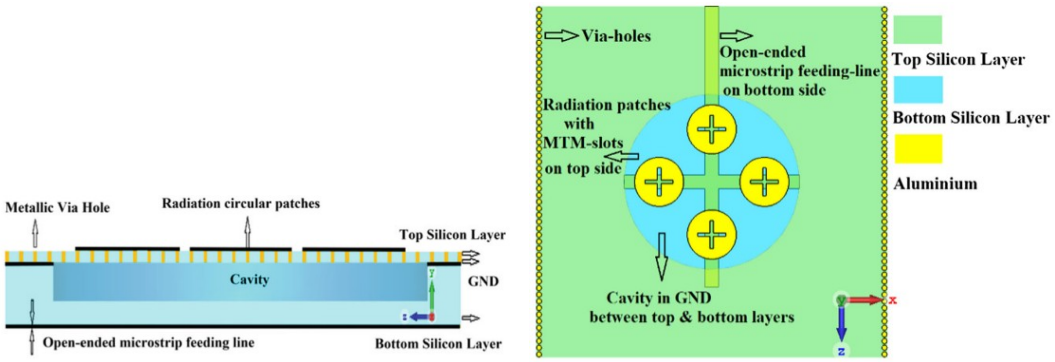


Figure 2.30: Electric (cavity) and magnetic (resonator) fields at 130 and 140 GHz [108].



(a) **(b)**

Figure 2.31: MTM-inspired cross-slot OCA: **(a)** Side-view, **(b)** Top-view [29]

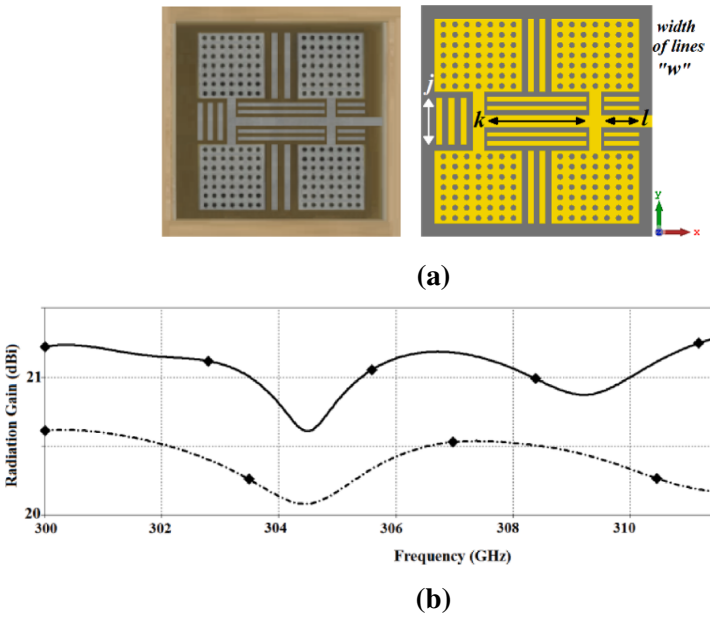


Figure 2.32: **(a)** MTS and AMC-based OCA array with decoupling elements ($j = 92\mu$m, $k = 200\mu$m, and $l = 67\mu$m) and **(b)** 2×2 OCA array gain [109]

SIW combined with MTM/MTS loading has emerged as a unifying strategy to confine fields, suppress surface waves, and raise gain/efficiency in on-chip THz/mm-wave antennas. On GaAs, stacked SIW–MTS radiators using 2×4 patch arrays with subwavelength circular slots enlarge effective aperture and deliver maximum gain and efficiency of 7.4 dBi and 70% respectively [61]. Figure 2.26**(a)** shows the multilayer geometry and excitation (CPW-in-oxide) that frames the radiating MTS with via fences, illustrating how SIW confinement reduces substrate loss and how the slot-row transforms the array into a metasurface, and Figure 2.26**(b)** shows the significant improvement over the antenna's impedance performance with the use of MTS and SIW. Building on this, [71] proposed a $0.41 - 0.47$ THz GaAs MTS OCA with 11×11 circular patches and leaky-slot feeding, demonstrating > 10 dBi and > 60% over a wide band. Figure 2.28**(a-b)** presents the measured gain and efficiency curves, highlighting the benefit of slot-coupled aperture extension. On silicon, [67] designed a thin (50 μm) SIW–MTM two-port patch with T-shaped slots as shown in Figure 2.29**(a)** that forms quarter/eighth-mode SIW cavities

that radiate from both cavity edges and the resonant slots. Figure 2.29**(b)** shows its S-parameters with > 30 dB inter-port isolation across $0.28 - 0.30$ THz, evidencing inherent self-isolation without extra decouplers.

At D-band, half-mode SIW cavity-fed DRAs excite higher-order modes to boost gain to $6.2 - 7.5$ dBi with $\sim 42 - 46\%$ simulated efficiency [108]. Figure 2.30 displays E/H-plane patterns that verify stable main lobe and higher-order-mode shaping from the half-mode SIW feed. SIW–MTS concepts [110] also integrate cleanly with front-ends, a $0.3 - 0.31$ THz GaAs transceiver conjugate-matches a slotted SIW-MTM radiator so the antenna filters harmonics while radiating with $\sim 55\%$ efficiency. Beyond single radiators, metasurface-fed arrays push directivity by patterning the feed and slot topology, while polyimide CRLH-MTS on standard CMOS reaches ~ 8.15 dBi gain and efficiency of 65.7% from $0.35 - 0.385$ THz [107], confirming material/process portability of MTS aperture synthesis. In parallel, reviewed SIW beam-forming networks (couplers, magic-tees, six-ports) [111] show that SIW distribution remains compact and low-cost, supporting on-chip/antenna-in-package arrays. This system-level perspective motivates SIW feeds beneath MTS layers. Alibakhshikenari et al. [29] introduced a five-layer silicon on-chip antenna (Figure 2.31**(a)**) combining metamaterial (MTM)-inspired crossed-slot patches (Figure 2.31**(b)**) with substrate-integrated waveguide (SIW) confinement to suppress surface waves and minimize substrate loss. The antenna achieved 6.9 dBi gain, 53% efficiency, and 13% bandwidth across $0.285 - 0.325$ THz, validating MTM-SIW synergy for compact, CMOS-compatible THz systems. Finally, μ-negative MTM rings used around patches (at lower GHz) [112] demonstrate surface-wave insulation and directivity gain, a mechanism analogous to SIW–MTS apertures at THz, narrowing the beam and increasing the gain achievable by MTM loading.

Likewise, [109] presents a THz OCA array based on MTS and AMC technologies to enhance radiation performance. The design employs sub-wavelength structures to improve impedance bandwidth, gain, and radiation efficiency, as shown in Figure

2.32**(a)**. A large-scale array (2×24 elements) achieves a high measured gain of 20.36 dBi at $0.3 - 0.314$ THz, as demonstrated in Figure 2.32**(b)**.

Collectively, the silicon and GaAs studies, including the hybrid SIW–MTM and high-performance MTS single and array designs, demonstrate a consistent trend where via-walled SIW cavities combined with slot-based metasurfaces or CRLH lattices yield compact, broadband, and efficient on-chip antennas (AoCs) compatible with CMOS, BiCMOS, and GaAs integration technologies [29, 67, 78, 110]. Table 2.3 compares SIW and cavity-based OCA reported in the literature. These works collectively demonstrate that combining SIW confinement with MTS or cavity enhancement yields significant improvements in radiation efficiency, port isolation, and gain across sub-THz bands.

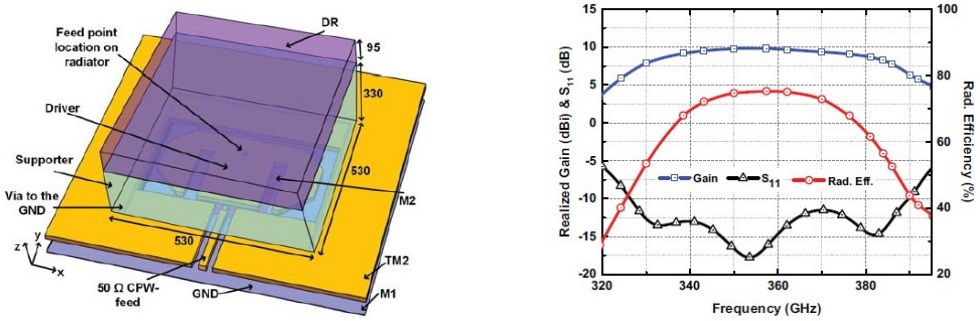
Table 2.3: Comparison of SIW and cavity-based OCA used in literature review designs.

Reference	Antenna Type	Design Overview	Performance	Remarks
[61]	SIW MTS cavity	7 layer GaAs; 2×4 patches with sub-λ slots; CPW feed	$0.45 - 0.50$ THz; Gain:~ 6.5 dBi; $\eta \sim 65\%$	SIW vias & MTS enlarge aperture, suppress surface waves
[29]	Hybrid SIW cavity	5 alternating metal/Si layers; SIW via fence; cavity coupling	$0.285 - 0.325$ THz; Gain:~ 6.9 dBi; $\eta \sim 53\%$	simple open-ended microstrip excitation; on-chip CMOS compatible
[108]	HM-SIW/ cavity-fed DRA	Half-mode cavity feed; higher-order TE modes	135 GHz; $6.2/7.5$ dBi ($TE_{x13\delta}$ / $TE_{x15\delta}$); 7% BW	compact high-gain on-chip DRA via cavity feeding
[109]	MTS and AMC based OCA array	OCA array using MTS and AMC technique	Gain: up to 20.36 dBi; $\eta \sim 37.5\%$ at $0.3 - 0.314$ THz	MTS and AMC enhance gain, BW and η
[67]	SIW dual-port cavity	patch with T-slots; vias-shorted (SIW); 2 ports	$0.28 - 0.3$ THz; Gain~ 4.5 dBi $\eta \sim 65\%$; > 30 dB isolation	self-isolation dual-port on-chip SIW radiator
[71]	MTS cavity (SIW-like)	11×11 circular patches; slot-lines; vias; thin GaAs	$0.41 - 0.47$ THz; Gain> 10 dBi; $\eta > 60\%$	thin substrate avoids substrate modes; high directivity
[110]	slotted SIW MTM	SIW high-pass radiator integrated with tripler, VCO, PA	$0.3 - 0.31$ THz; Gain> 1 dBi; $\eta \sim 55\%$ Tx-15 dBm	fully-integrated GaAs TRX with on-chip SIW antenna
[112]	MTM (cavity-like)	dual-layer D-SSRR rings around patch	$5.2/6.75$ GHz; gain $+ \geq 2.2$ dB HPBW$\sim 20°$vs. plain patch	non-SIW MTM example showing cavity-like confinement benefits

2.2.3.4 Dielectric-Resonator and Resonant-Element OCA

Dielectric-resonator antennas (DRAs) utilize high-permittivity materials such as silicon, GaN, or MgO as the main radiator, excited through slots or microstrip feeds. By confining energy within the dielectric body instead of the lossy substrate, they achieve higher efficiency ($70 - 80$ %) and substantial gain at THz frequencies. Variants include shorted-ring or annular structures that broaden bandwidth and suppress surface waves, as well as GaN-on-Si microstrip arrays designed for monolithic THz integration. These resonant designs provide strong radiation confinement and high power-handling capability, making them ideal for imaging, sensing, and high-frequency communication circuits.

Dielectric-resonator antennas (DRAs) have become one of the most effective on-chip radiator types for terahertz and mm-wave systems because they eliminate conduction losses from metal patches and provide strong field confinement in low-loss dielectrics.



(a) **(b)**

Figure 2.33: **(a)** Geometry of the on-chip antenna with inverted E-shaped feed, support structure, and dielectric resonator (DRA); **(b)** simulated $|S_{11}|$, gain, and radiation efficiency results [113]

A sub-terahertz wideband dielectric resonator antenna (DRA) operating around 350 GHz employs an inverted-E half-mode SIW driver beneath a hemispherical resonator to excite multiple hybrid modes, achieving approximately 10 dBi gain, 75% efficiency, and 18.5% fractional bandwidth [113]. The corresponding results are illustrated in

Figure 2.33, where **(a)** shows the stacked SIW–DRA configuration and **(b)** presents the simulated $|S_{11}|$, gain, and efficiency curves, confirming smooth impedance matching across the operating band.

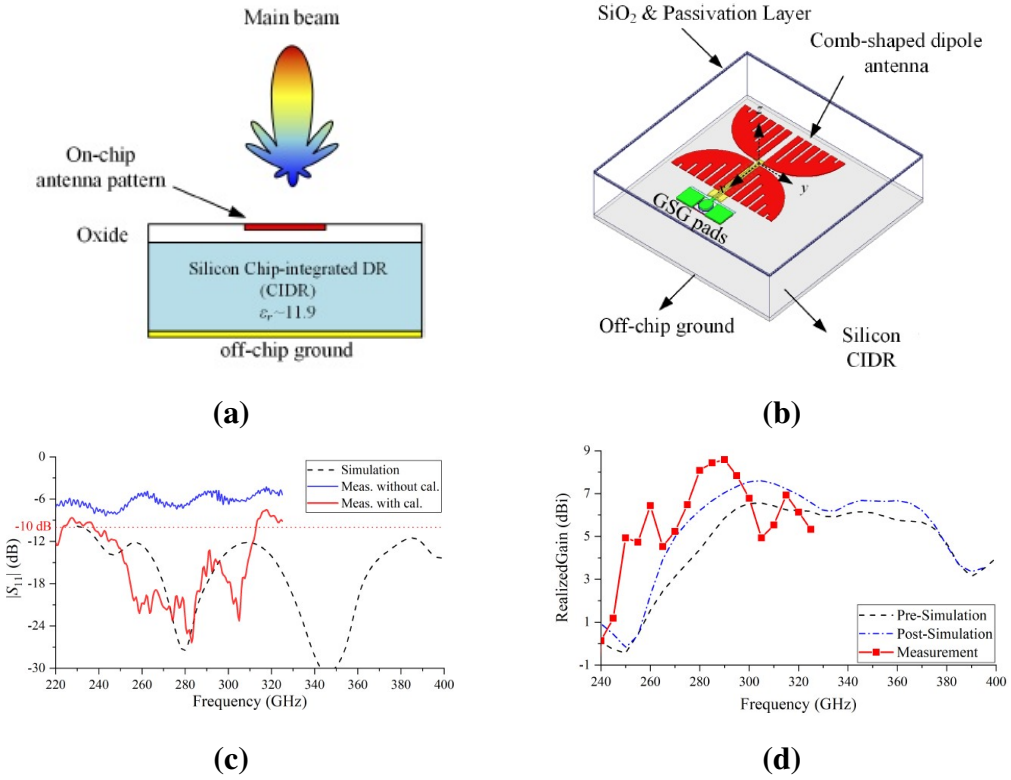


Figure 2.34: **(a)** On-chip antenna with a silicon-based CIDR; **(b)** layout of the comb-type antenna; **(c)** simulated and measured S-parameters; **(d)** measured and simulated gain (measurements above 325 GHz unavailable) [114]

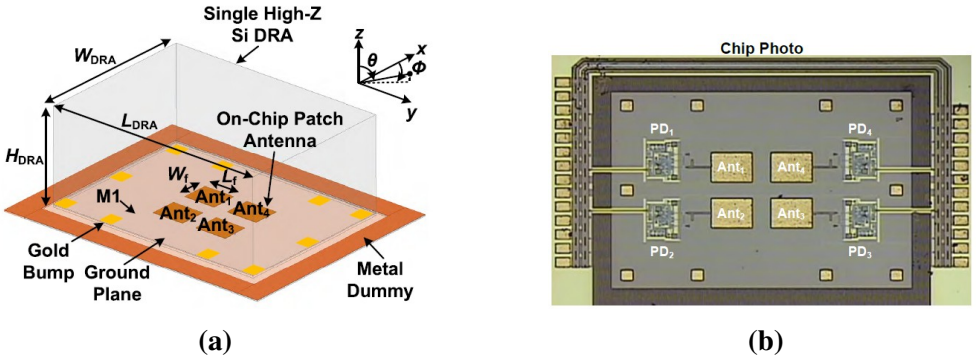


Figure 2.35: Layout of DRA 2×2 antenna array **(a)** isometric view and **(b)** chip photo in high-Z Si [115].

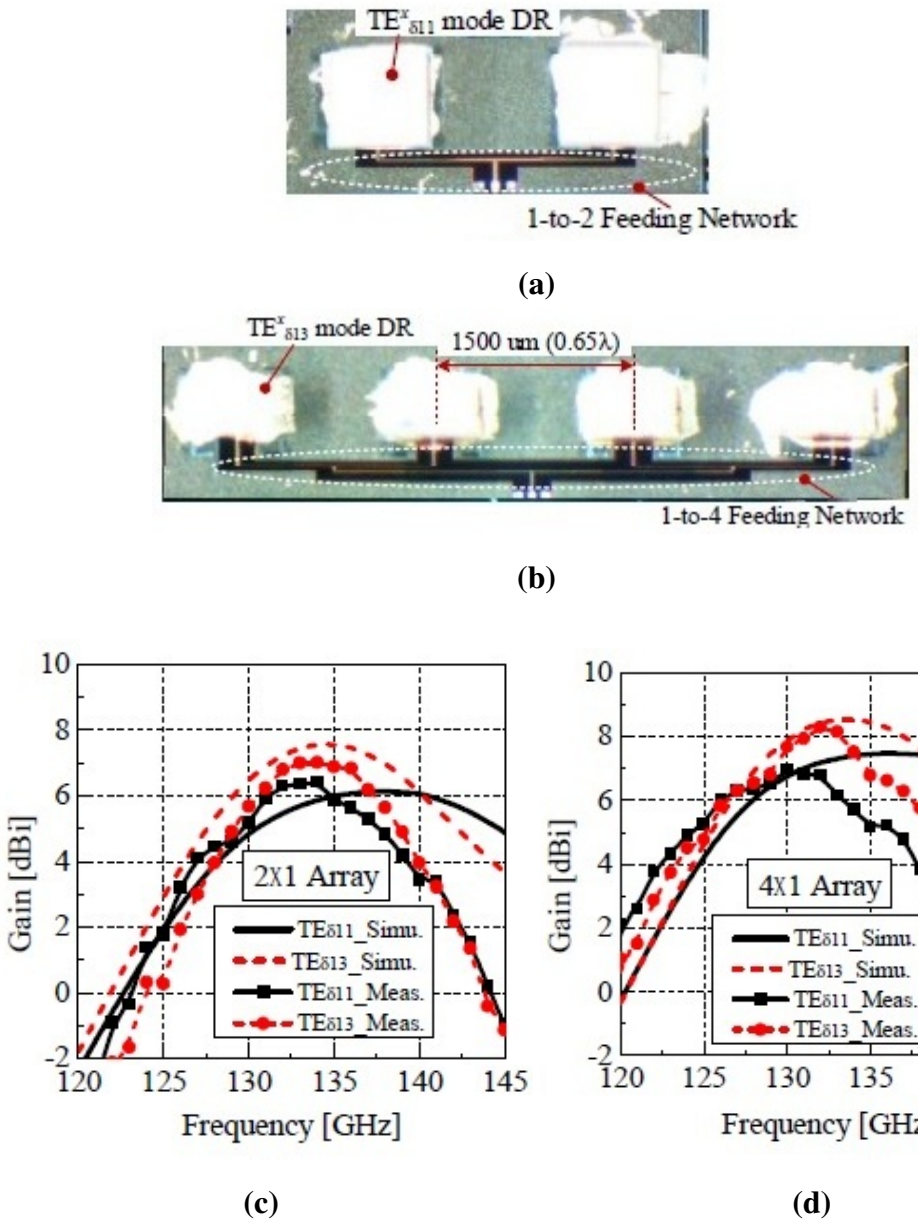


Figure 2.36: Microphotographs of the fabricated antenna arrays are shown in **(a)** for the 2×1 configuration employing TE^x_{11} mode dielectric resonators and **(b)** for the 4×1 configuration utilizing TE^x_{13} mode resonators. The corresponding simulated and measured gain responses **(c)** 2×1 and **(d)** 4×1 arrays [116]

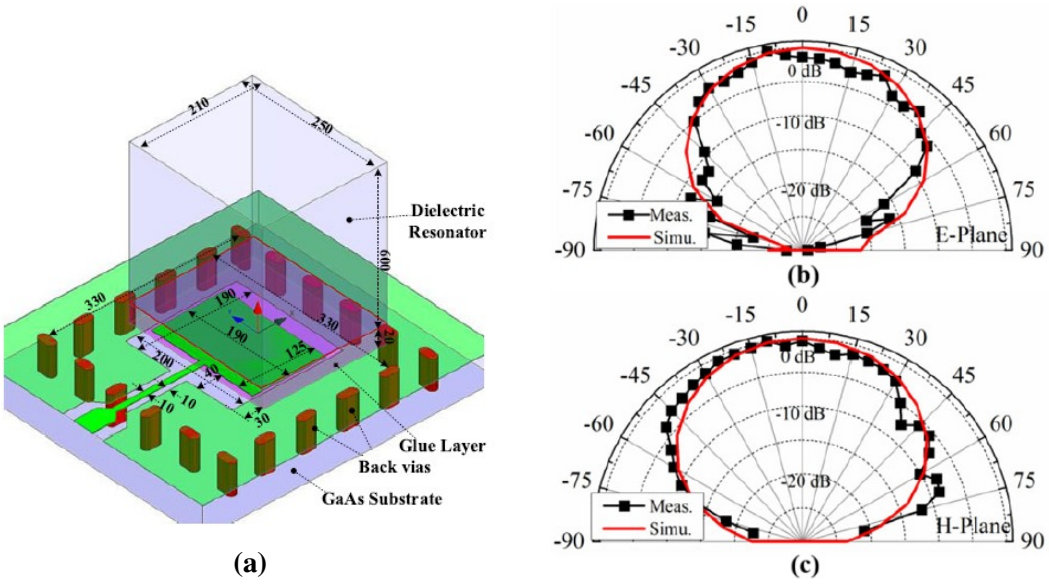


Figure 2.37: **(a)** On-chip antenna configuration incorporating a higher-order-mode dielectric resonator, and **(b–c)** simulated and measured radiation patterns of the on-chip DRA in the E-plane and H-plane at 270 GHz, respectively [117]

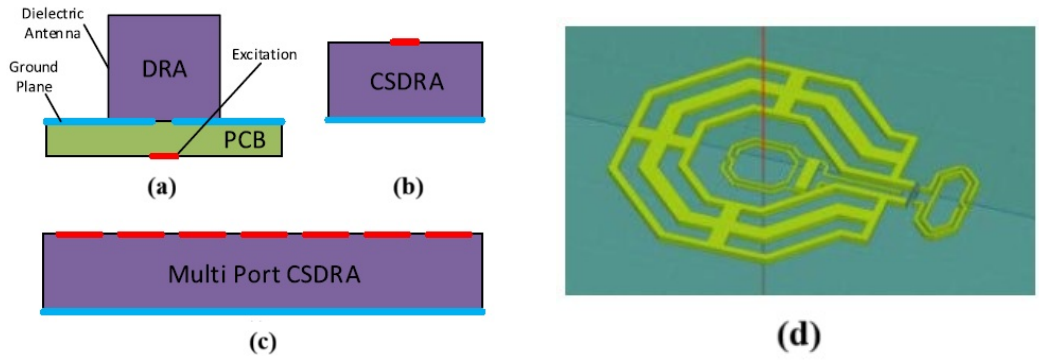


Figure 2.38: Development stages of the multiport CSDRA: **(a)** conventional bottom-excited DRA, **(b)** top-fed silicon-based CSDRA, **(c)** multi-excitation configuration, and **(d)** compact VCO layout with integrated source and gate inductors. [118]

Extending this idea, a chip-integrated dielectric resonator (CIDR) as shown in Figure 2.34**(a)** embedded in the passivation of a CMOS wafer couples electric and magnetic fields through a comb-shaped dipole, achieving 8.6 dBi gain and $44 - 50\%$ impedance/gain bandwidths [114]. Figure 2.34**(b)** illustrates the CIDR geometry, and Figures 2.34**(c-d)** the measured $|S_{11}|$ and gain versus-frequency expansion resulting from hybrid cavity–DRA modes.

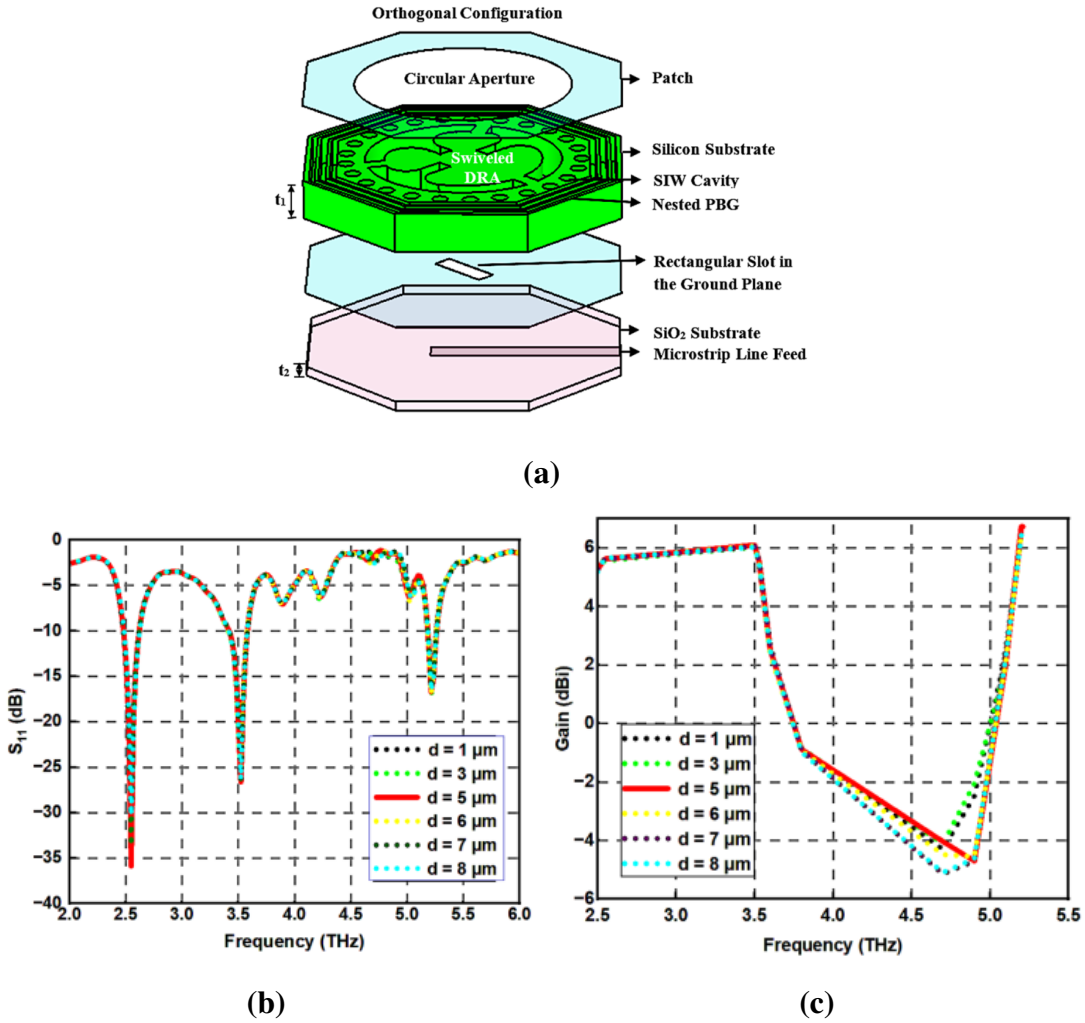


Figure 2.39: **(a)** Geometry of the proposed encapsulated tri-band THz swiveled DRA with SIW and nested PBG crystal; **(b-c)** Simulated return loss and gain of the proposed antenna for PBG-1, PBG-2, and PBG-3 [119]

For array integration, [115] proposed a flip-chip-mounted DRA above a 2×2 CMOS array (at ~ 340 GHz) that transforms the on-chip dipole field into a radiating dielectric aperture as shown in Figure 2.35, increasing per-element gain from 0.1 dBi to 8.6 dBi. Similarly, 130 GHz HM-SIW-fed DRA arrays with 2×1 and 4×1 configurations excite $\mathrm{TE}^{x}_{\delta 11}$ and $\mathrm{TE}^{x}_{\delta 13}$ modes [116], providing $6 - 8.2$ dBi gain and 10% HPBW gain. Figure 2.36**(a–b)** illustrates the layout of the 2×1 and 4×1 antenna arrays, while Figure 2.36**(c–d)** compares the simulated and measured gain responses, showing close

agreement with minor deviations attributed to gain reduction and a slight frequency shift. On the GaAs side, a 270 GHz $\times 9$ multiplier chain MMIC integrates a high-order-mode ($TE_{\delta 13}$) DRA (Figure 2.37**(a)**) directly at the output stage [117], yielding $+2$ dBm EIRP over $33 - 40$ GHz bandwidth. Figure 2.37**(b-c)** illustrates that the measured E- and H-plane radiation patterns closely align with the simulated results, confirming the accuracy of the proposed antenna model. A complementary multi-port chip-scale DRA (CSDRA) (shown in Figure 2.38**(a-c)**) concept treats the silicon die itself as the resonator, driven by distributed harmonic VCO ports (Figure 2.38**(d)**) to deliver $+9$ dBm TRP and $+24$ dBm EIRP at 0.28 THz [118].

A tri-band THz antenna that embeds a "Mickey Mouse"-shaped DRA inside a SIW, surrounded by a nested octagonal PBG crystal on a silicon substrate, is proposed by [119], and is illustrated in Figure 2.39**(a)**. The antenna resonates at $2.5, 3.5,$ and 5.2 THz, achieving gains of $6.75, 6.86,$ and 6.82 dBi respectively through surface wave suppression and optimized swiveling/chamfering, as demonstrated in the return loss and gain plots of Figure 2.39**(b-c)**. The compact $80 \times 80 \times 12.5 \mu m^3$ design is proposed for 6G communications, THz imaging, and IoT sensing applications.

Fundamentally, these advances stem from DRA design theory, the optimization of permittivity, aspect ratio, and excitation type to control TE_{δ} and $HEM_{mn\delta}$ modes [120]. More recent work introduces metamaterial-assisted double-DRA arrays on GaAs operating at $0.45 - 0.475$ THz, achieving 4.5 dBi gain and 45.7% efficiency, in which the MTM loading increases the effective aperture without enlarging the chip [121]. Likewise, a high-efficiency H-slot-excited DRA around 35 GHz reports 48% efficiency while preserving compactness [122]. Collectively, these silicon and GaAs implementations demonstrate that half-mode SIW feeds, higher-order dielectric modes, metamaterial coupling, and packaging-aware DR placement enable compact, broadband, and high-efficiency on-chip antennas that are scalable to sub-THz integration.

Table 2.4: Comparison of Dielectric-Resonator and Resonant-Element based OCA used in literature review designs.

Reference	Antenna Type	Key Features	Performance	Remarks
[118]	Multi-port CSDRA	65μm CMOS; $1.45 \times 1.45\text{mm}^2$ chip, 5×6 ports	$+9$ dBm TRP & $+24$ dBm EIRP at 0.28 THz	uses Si as resonator; high integration and power density
[115]	Flip-chip DRA	Si DRA on 0.18μm CMOS array; $\text{TE}_{3\delta 9}$ mode	Gain: $0.1 \rightarrow 8.6$ dBi at 339 GHz	simple assembly; effective aperture coupling
[116]	on-chip DRA array	130 GHz CMOS; HM-SIW feed; $2 \times 1/4 \times 1$ array	Gain: $6. - 8.2$ dBi BW: $\sim 10\%$	higher-order mode control improves pattern
[123]	on-chip mounted DRA	1 mm Al_2O_3 cylinder $\lambda/4$ microstrip feed	BW: 3% & $\eta = 65\%$ at 80 GHz	easy mount; stable wide beam
[117]	GaAs DRA multiplier	0.1μm GaAs pHEMT; $\text{TE}_{\delta 13}$ mode output stage	EIRP $+2$ dBm; BW: 33 GHz	compact J-band chain; low spurious output
[114]	chip-integrated DRA	Si substrate; comb-dipole hybrid feed	Gain:8.6 dBi; BW: $44 - 50\%$	dual-mode operation; broadband compact design
[121]	series-fed double DRA	$0.45 - 0.475$ THz Si array; MTM coupling	Gain: 4.5 dBi $\eta = 45.7\%$	MTM loading enhances BW and gain
[113]	HM-SIW fed DRA	350 GHz GaAs; stacked resonator	Gain: 10 dBi; BW: 18.5% $\eta = 75\%$	combines cavity and DRA modes for high η
[122]	H-slot fed DRA	Si CMOS; compact rectangular DR	Gain: 2.3 dBi & $\eta = 48\%$ at 35 GHz	low-loss feed; mm-wave integration
[119]	Tri-band THz swiveled DRA with SIW	mickey mouse-shaped DRA, circular SIW, octagonal PBG	$2.5, 3.5, 5.2$ THz; Gain: $6.75, 6.86, 6.82$ dBi	compact high-gain tri-band; narrow bandwidth at 5.2 THz

2.2.4 Review of THz On-Chip Antennas

Terahertz on-chip antennas (OCAs) have emerged as a key enabling technology for next-generation wireless systems due to their unique integration and performance capabilities. One of the primary advantages is their ability to support monolithic integration with CMOS and BiCMOS technologies, allowing antennas to be fabricated directly on the same substrate as active circuits. This significantly reduces interconnect losses and eliminates the need for external packaging transitions [124].

Another major benefit is the compact size enabled by short wavelengths at THz frequencies, which enables the realization of highly miniaturized antennas suitable for dense integration in multi-core and many-core processors [40]. Additionally, on-chip antennas enable high-data-rate communication by leveraging the extremely wide bandwidth of the THz spectrum, potentially supporting terabit-per-second transmission [125]. From a system perspective, OCAs facilitate wireless network-on-chip (WiNoC) architectures, reducing reliance on conventional wired interconnects that suffer from parasitic effects, latency, and power consumption [126]. Furthermore, their compatibility with batch fabrication processes makes them cost-effective and scalable for mass production.

Despite these advantages, currently reported THz on-chip antennas suffer from several critical limitations. One of the most significant issues is low radiation efficiency, typically in the range of $20\% - 40\%$, primarily due to high substrate losses and surface-wave excitation in silicon-based platforms [127]. The high dielectric constant and loss tangent of semiconductor substrates confine electromagnetic energy within the substrate, leading to significant power dissipation and degraded radiation performance. This also results in distorted radiation patterns and reduced gain [128].

Another key limitation is narrow bandwidth and impedance matching challenges, as many designs struggle to maintain stable performance over wide frequency ranges. Additionally, fabrication tolerances at THz frequencies become extremely critical, where even micrometre-level deviations can significantly affect antenna characteristics such as resonance, gain, and beam direction [57]. Integration also introduces complex electromagnetic interactions, including coupling with nearby circuits, packaging parasitics, and thermal constraints. In many cases, the performance of on-chip antennas is further limited by the need for off-chip components such as silicon lenses or dielectric superstrates, which contradicts the goal of full integration [129].

Overall, while THz on-chip antennas offer significant advantages in terms of integration, scalability, and high-speed communication, their practical implementation is still constrained by low efficiency, high losses, and integration complexity. These limitations highlight the need for advanced structures, such as substrate integrated waveguide (SIW)-based antennas and novel feeding mechanisms, to achieve improved performance while maintaining compatibility with planar fabrication technologies.

2.3 Substrate Integrated Waveguide (SIW)

2.3.1 Why is SIW Important?

Conventional metallic waveguides remain the benchmark for high-performance mm-Wave systems owing to their excellent quality factor and low-loss characteristics. However, their suitability for modern applications is limited. Classical waveguide technology is costly and cumbersome, requiring complex assembly and post-fabrication tuning, which hinders low-cost mass production. Furthermore, the inherently bulky and heavy nature of metallic waveguides restricts their use in compact and lightweight systems.
On the other hand, while planar integrated circuits provide advantages of low cost and ease of fabrication, they suffer from intrinsic limitations when implementing low-loss, high-Q components such as band-pass filters and diplexers. As a result, hybrid approaches combining planar and non-planar structures have been pursued. Yet, existing hybrid designs based on planar circuits integrated with rectangular waveguides present challenges in terms of manufacturability, impedance matching, and packaging, which restrict their practical deployment in high-volume production.
Alternative solutions, such as dielectric waveguides, have also been investigated but have not gained widespread adoption due to two fundamental issues: radiation losses at discontinuities and difficulties in achieving efficient transitions to planar circuits.

The development of non-radiating dielectric (NRD) waveguides partially addressed these shortcomings, enabling better hybrid integration. However, the complexity of combining NRD structures with planar technologies still limits scalability.

To overcome these challenges, the concept of substrate integrated circuits (SICs) was proposed [130], with the substrate integrated waveguide (SIW) as a key building block. SIW technology effectively unifies planar and non-planar integration within a single substrate or multilayer platform. It allows waveguide-like structures to be synthesized using arrays of metallized via-holes in standard printed circuit board (PCB) or low-temperature co-fired ceramic (LTCC) processes. This approach retains the low-loss and high-Q characteristics of conventional waveguides while offering the low-cost, lightweight, and compact benefits of planar fabrication. Moreover, SIW enables the straightforward integration of passive components such as resonators [116], filters [131], couplers [111], dividers [132, 132–135], circulators, and antennas [61, 67, 71, 107, 108, 110], thereby providing a scalable and versatile platform for high-frequency systems.

2.3.2 Fundamental of SIW

2.3.2.1 Basic Structure & Concept

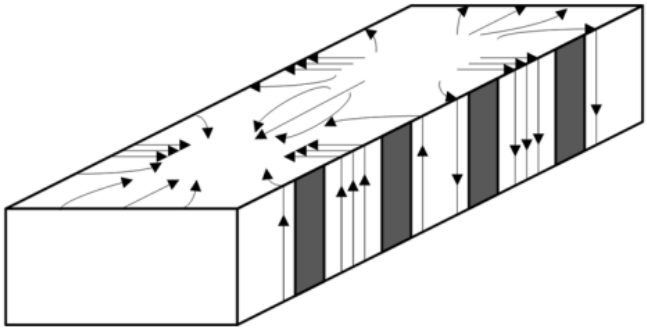


Figure 2.40: Surface current distribution of the TE_{10} mode in a RWG with slots along the narrow sidewalls [136]

Although SIW share many similarities with conventional RWG, important distinctions exist due to their periodic nature. An SIW is essentially a quasi-RWG synthesized by rows of metallic vias embedded in a dielectric substrate and enclosed by metallic planes. Because of this periodic arrangement, SIW behave as a discrete guided-wave structure, which introduces unique characteristics not observed in continuous RWG.
First, the periodic via lattice can give rise to electromagnetic band-stop effects, which are absent in uniform waveguides. Second, due to the inherent gaps between adjacent vias, leakage losses may occur if the design constraints are not carefully maintained. These features influence the modal behavior of SIW, resulting in differences compared to standard RWG. In particular, leakage waves may appear if the operating conditions are not satisfied [130, 137].

Importantly, only TE modes can be supported in SIW, while TM modes cannot be effectively sustained. This is a direct consequence of the surface current distribution (Figure 2.40). An SIW can be regarded as an RWG with periodic slots along its narrow walls. When TE modes are excited, the corresponding surface currents flow longitudinally along the sidewalls. Since the slots are oriented parallel to the surface currents, they do not significantly disturb current continuity, and radiation losses remain minimal. As a result, TE modes are preserved and can propagate effectively within the SIW [138].
In contrast, if TM modes were excited, their associated magnetic fields would induce longitudinal surface currents that are intersected by the via "slots". Such interruptions lead to substantial radiation leakage, preventing the stable propagation of TM modes. Similarly, higher-order hybrid modes involving transverse currents would also be radiated away due to slot coupling [136, 139]. This behavior is consistent with the well-established principle of slot-antenna design, where currents flowing through slots result in radiation.

Therefore, the SIW inherently supports TE modes as its dominant field distribution, with TE_{10} being the fundamental propagation mode. The preservation of these modes is attributed to the alignment of the via slots with the current flow, ensuring minimal disturbance to the guided fields. This feature, which distinguishes SIWs, enables them to operate as low-loss planar analogues of traditional rectangular waveguides. Properties of the TE_{m0} modes are listed in the Table 2.5.

Table 2.5: Properties of TE modes in SIW

Property	**TE_{m0} modes**
Generating function	$\psi_{m0} = \cos\frac{m\pi x}{a}$
Cutoff wavenumber	$k_{c,m0} = \frac{m\pi}{a}$
Propagation constant	$\Gamma_{m0}^2 = k_{c,m0}^2 - k^2$, $k = \omega\sqrt{\mu\epsilon}$
Magnetic field	$\overrightarrow{H_t} = \pm\Gamma_{m0}\nabla_t\psi_{m0}e^{\pm\Gamma_{m0}z}$, $H_{zm0} = k_{cm0}^2\psi_{m0}e^{\pm\Gamma_{m0}z}$
Electric field	$\overrightarrow{E_t} \pm Z_h\hat{a}_z \times \overrightarrow{H}$, $Z_h = \frac{j\omega\mu_0}{\Gamma} = \frac{jk_0\eta}{\Gamma}$
Power flow	$ab\eta k\beta_{m0}\frac{k_{cm0}^2}{4}$

2.3.3 Design of SIW

2.3.3.1 Design Parameters

By using the BI-RME [140] method combined with Floquet's theorem, dispersion properties of SIW are obtained, which shows that the SIW and RWG have similar guided wave character. The design equations are derived using the dispersion curves as follows [141]:

$$w_{eff} = w - \frac{d^2}{0.95p} \tag{2.1}$$

where d is the diameter of metallic vias, p is the spacing between two vias, and w is the width of the SIW.

Equation 2.1 provides a first-order approximation for the equivalent width of SIW; however, it proves insufficient as it neglects the contribution of the via spacing (p) to the width (w) ratio. As a result, discrepancies arose when predicting propagation constants, particularly when the via spacing was not negligibly small. To address this limitation, Xu et al. [136] introduced an empirically refined expression that incorporates both dimensional and spacing effects, thereby achieving much closer agreement with experimental and numerical results (i.e., numerical multimode calibration integrated with full-wave finite-element simulations using HFSS and finite-difference frequency-domain (FDTD) analysis).

$$w_{eff} = w - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{w} \tag{2.2}$$

Another refined formulation has been introduced based on the mode-matching technique (MMT) for accurately determining the actual SIW width (a_{SIW}) as a function of the equivalent rectangular waveguide width (w_{equi}), which governs both the frequency range and the operational bandwidth of the structure [142]. The relation is expressed as

$$a_{SIW} = w_{equi} + p\left(0.766e^{0.4482\frac{d}{p}} - 1.176e^{-1.214\frac{d}{p}}\right) \tag{2.3}$$

This expression is derived from minimizing the reflection at the transition between an all-dielectric waveguide of width w_{equi} and an SIW of width a_{SIW}. By ensuring that the reflection coefficient is minimized, the effective SIW width can be optimally adjusted to match the equivalent waveguide width, thereby yielding an accurate design rule that enhances bandwidth prediction and overall performance.

2.3.3.2 Loss Mechanisms and Optimization

SIW is a type of planar transmission line that can be used to fabricate printed circuit boards (PCBs) and mimic the guiding properties of traditional rectangular waveguides. Although SIWs are small, inexpensive, and well-suited for THz-wave integration, their performance in high-frequency applications is limited by propagation losses. Three main mechanisms account for these losses: dielectric loss, ohmic (conductor) loss, and radiation leakage. Optimizing SIW designs requires an understanding of the physical causes of these losses as well as how they vary with material and structural characteristics.

- **Conductor loss** in a SIW arises from the finite conductivity of the metallic layers forming the top, bottom, and the metallic vias. As we already established that the field distribution in SIW closely resembles that of conventional RWG, the empirical expression originally derived for RWG can be adopted to estimate the attenuation constant due to conductor loss (α_c) in SIW. In this adaptation, the physical width of the RWG is replaced by the equivalent width (w_{eqv}) of the SIW [143].

$$\alpha_c(f) = \frac{\sqrt{\pi f \epsilon_0 \epsilon_r}}{h\sqrt{\sigma_c}} \frac{1 + 2\left(f_0/f\right)^2 h/w_{eqv}}{\sqrt{1 - \left(f_0/f\right)^2}} \tag{2.4}$$

  where h is thickness of the substrate, ϵ_0 is the permittivity of the free space, ϵ_r is the dielectric constant of the substrate, σ_c is the conductivity of the metal, f is the operating frequency (Hz), and f_0 is the cutoff frequency for the given SIW.

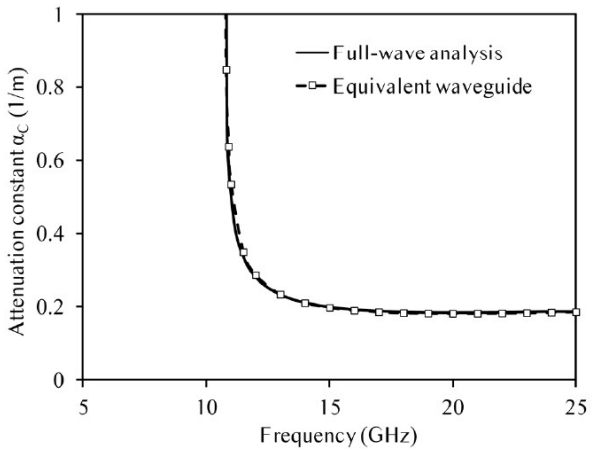


Figure 2.41: Comparison of analytically computed α_c (using Equation 2.4) and full-wave result for an SIW ($w_{eqv} = 10$ mm, $D = 1$ mm, $P = 2$ mm, $h = 1$ mm, $\epsilon_r = 2.2$, $\sigma_c = 5.8 \times 10^7$ S/m) [143].

Figure 2.41 compares the computed attenuation constant (α_c) as a function of frequency for an SIW with a cutoff frequency (f_0) of approximately 10 GHz. The results obtained from full-wave simulations in Ansys HFSS are shown alongside those calculated using the analytical formula 2.4. From this equation, it is evident that conductor loss decreases with increasing substrate thickness. However, in practice, the substrate thickness of SIW structures is typically much smaller than that of conventional hollow waveguides; therefore, conductor loss in SIWs is generally higher than in standard metallic waveguides.

- **Dielectric loss** in SIW originates from the intrinsic losses of the dielectric substrate, quantified by the loss tangent ($\tan\delta$). Similar to conductor loss, the analytical expression developed for conventional RWG can be adapted to SIW for evaluating the attenuation constant due to dielectric loss (α_d). In this case, the formulation directly incorporates the dielectric properties of the substrate:

$$\alpha_d = \frac{\pi f \sqrt{\epsilon_r}}{c\sqrt{1-(f_0/f)^2}} \tan\delta \tag{2.5}$$

where c represents the speed of light in vacuum and $\tan\delta$ represents the dielectric loss tangent.

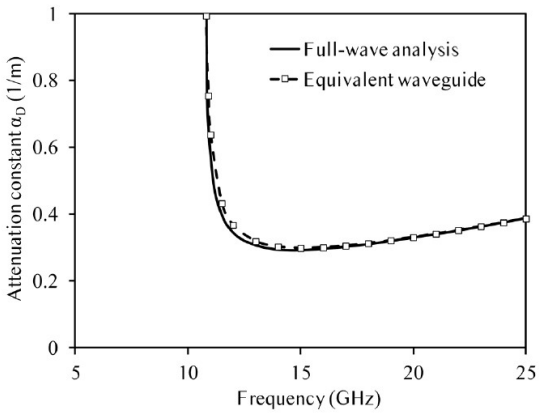


Figure 2.42: Comparison of analytically computed α_c (using Equation 2.5) and full-wave result for an SIW ($w_{eqv} = 10$ mm, $D = 1$ mm, $P = 2$ mm, $h = 1$ mm, $\epsilon_r = 2.2$, $\tan\delta = 0.0009$) [143].

Figure 2.42 illustrates the variation of α_d with frequency for the same SIW configuration in the conductor section. The analytical results based on Equation 2.5 are compared with full-wave simulations carried out using the Ansys HFSS. A strong correlation between the two methods is observed, validating the applicability of the adapted analytical model. It is also evident from the expression that dielectric loss is independent of the substrate thickness (h). This distinguishes it from conductor loss, which scales inversely with h. Furthermore, dielectric loss in SIWs is significantly higher than in traditional hollow metallic waveguides. This is because hollow waveguides generally use air as the filling medium, whose dielectric loss tangent is essentially negligible. By contrast, SUW utilizes practical substrates (e.g., polyimide, silicon dioxide, or Rogers laminates), which exhibit finite $\tan\delta$ values, thereby introducing measurable attenuation.

- **Radiation loss** is one of the most directly tied to the geometry of the via lattice. Unlike conventional RWG, periodic vias perforate the SIW sidewalls, and the

finite spacing (or pitch p) between them forms "gaps" through which energy leaks. Although experimental guidelines that limit leakage, such as maintaining the via spacing to diameter ratio (p/D) below ~ 2, do not offer a numerical approximation of the attenuation constant. While simple geometric rules provide qualitative guidance, the semi-analytical formula derived by Pasian et al. [144] offers a quantitative prediction of attenuation constant α_r as a function of via diameter (D), via pitch (p), and equivalent width (w_{eqv}) as:

$$\alpha_R\,[\text{dB/m}] = \frac{\frac{\xi^2}{2}\frac{1}{w_{eqv}}\left(\frac{d}{w_{eqv}}\right)^{2\gamma}\left(\frac{p}{d}-1\right)^{2\tau}}{\sqrt{\left(\frac{2w_{eqv}}{\lambda}-1\right)}} \tag{2.6}$$

where ξ, γ, and τ are the scalar coefficients obtained from least-squares fitting of full-wave simulation, and λ is the wavelength in the dielectric medium at the operation frequency.

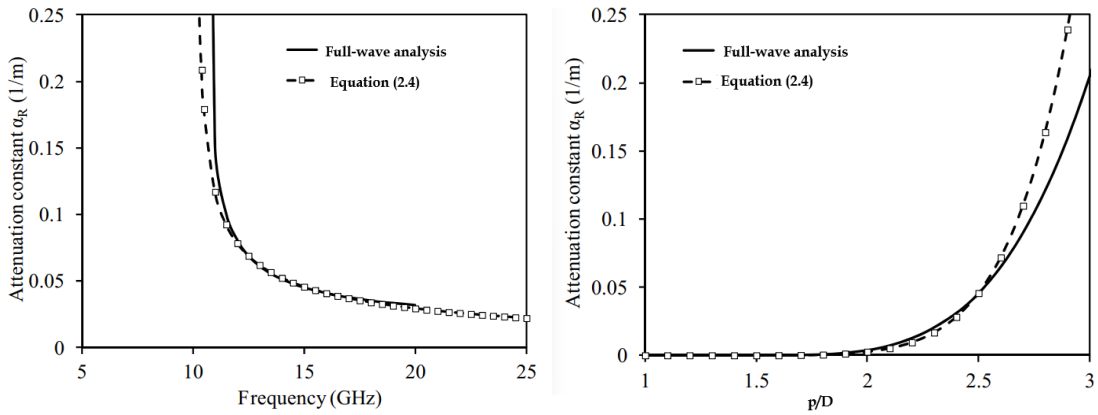


Figure 2.43: Variation of radiation attenuation (α_R) in an SIW ($w_{eqv} = 10$ mm, $d =$ 1mm, $h = 1$ mm, $\epsilon_r = 2.2$) at 15 GHz: **(a)** fixed via pitch $p = 2.5$ mm; **(b)** p varying from $1.5 - 3.5$mm [143]

Using Equation 2.6, the attenuation constant as a function of frequency is depicted in Figure 2.43**(a)** for an SIW with a pitch-to-diameter ratio of ($P/D = 2.5$). The

results indicate that attenuation is higher in the vicinity of the cutoff frequency and gradually decreases with increasing frequency. This behavior can be attributed to the improved confinement of the guided mode at higher frequencies, where the effective wavelength becomes smaller compared to the periodic gaps, thereby reducing radiation leakage.

- **Surface roughness**: At mm-Wave and THz frequencies, conductor loss becomes one of the dominant attenuation mechanisms in substrate-integrated waveguide (SIW) structures. Beyond the intrinsic resistivity of the copper metallization, the microscopic roughness at the metal–dielectric interface substantially increases the effective surface resistance. In printed-circuit fabrication, this roughness is deliberately introduced to enhance mechanical adhesion between copper foils and dielectric laminates; however, as the operating frequency extends to tens of gigahertz, even moderate roughness levels markedly amplify conductor attenuation and therefore must be incorporated into accurate SIW loss modeling [145].

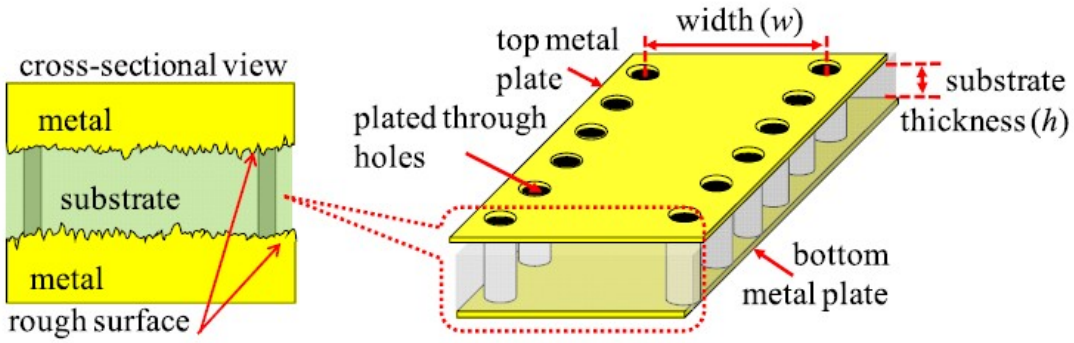


Figure 2.44: An SIW illustration depicting the roughness at the metal-to-dielectric junction, adapted from [145]

The skin effect and current crowding phenomena primarily govern the attenuation in an ideal, smooth conductor. When surface roughness is present, the effective surface area and current path length increase, resulting in a higher equivalent resistance and excess loss. Experimental and full-wave studies have

shown that standard-profile copper foils can exhibit up to twice the loss of low-profile (smooth) foils [145]. This excess attenuation is generally captured by introducing a frequency-dependent roughness coefficient K_H, which scales the smooth-conductor attenuation as [145, 146]:

$$\alpha_{c,\text{rough}} = K_H, \alpha_{c,\text{smooth}} \tag{2.7}$$

where K_H is a dimensionless coefficient that approaches unity when the skin depth δ is much larger than the average rms roughness height R_q, and increases with frequency as δ becomes comparable to R_q, eventually reaching a saturation level that depends on the surface morphology and fabrication process.

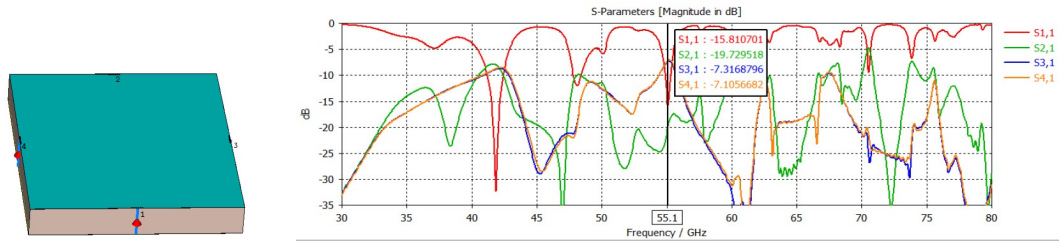
The most widely adopted formulation for K_H was proposed by Hammerstad and Jensen through an empirical model that predicts $K_H \approx 1$ for $\delta >> R_q$ and a saturation near 2 for $\delta << R_q$ [146]. Later, Huray's "snowball" model [147] represented the rough surface using an array of hemispherical particles, providing improved accuracy at higher frequencies and for complex metal textures. These formulations have since been applied and validated in modern SIW structures, confirming that surface roughness significantly influences conductor attenuation within the W-band [145].

2.4 Recent Development of SIW

2.4.1 On-Chip THz Communication

Wireless Networks-on-Chip (WiNoC) architectures have emerged as a promising alternative to conventional wired interconnects, addressing critical bottlenecks in latency, scalability, and energy efficiency that hamper modern chip-multiprocessor

design [148, 149]. As transistor counts soar and core-count per chip reaches into the hundreds or thousands, traditional metal interconnects become increasingly constrained by parasitic capacitance, propagation delay, signal-integrity issues, and power dissipation. In this context, the adoption of millimetre-wave and THz frequency bands offers a paradigm shift: ultra-broadband, short-wavelength propagation enables highly compact antennas and wireless links embedded directly within the chip package, enabling intra-chip and inter-chip communication pathways that bypass the overhead of long metal traces [150]. By utilizing the THz spectrum, such wireless links can reduce the physical routing burden, shorten signal paths, and dramatically lower latency and power per bit, thereby aligning with the needs of next-generation AI accelerators, high-performance compute systems, and 6G-era architectures.



(a) **(b)**

Figure 2.45: **(a)** Edge-placed rectangular meander OCA and **(b)** simulated S-parameters [151]

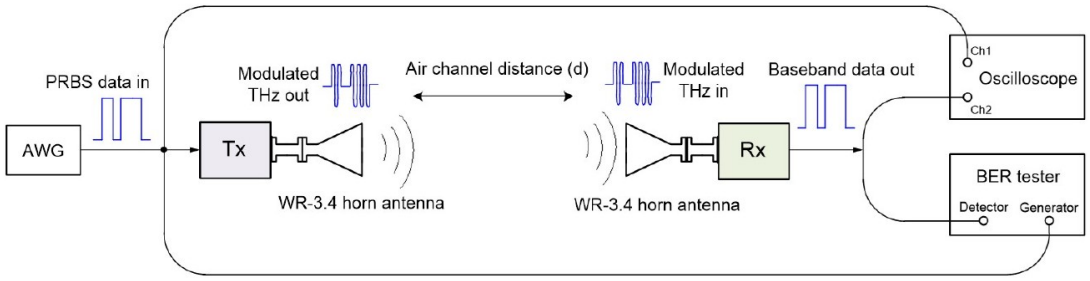
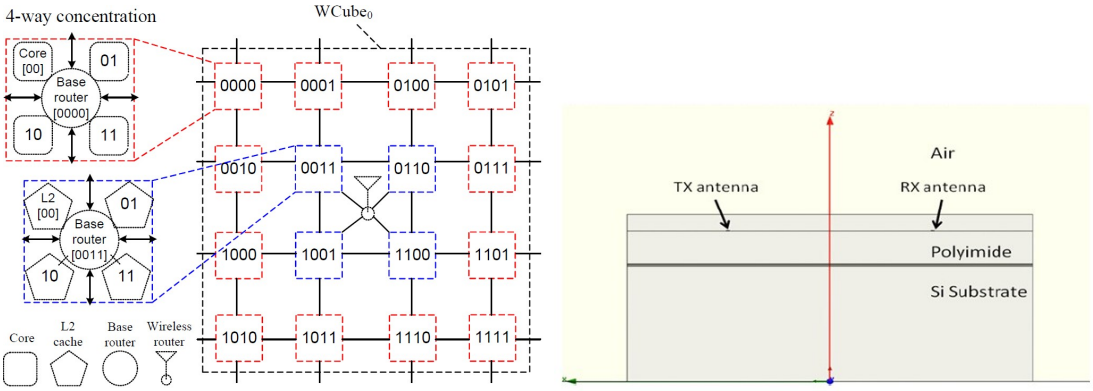


Figure 2.46: Configuration of the experimental setup employed for wireless data transmission utilizing THz OOK transceiver modules [152]



(a) **(b)**

Figure 2.47: **(a)** Layout of the $WCube_0$ architecture, consisting of a cluster of 16 base routers accommodating a total of 64 nodes. The numerical labels within the nodes and base routers denote the corresponding node IDs and base IDs, respectively and **(b)** sectional view of THz antenna placement in a chip [11]

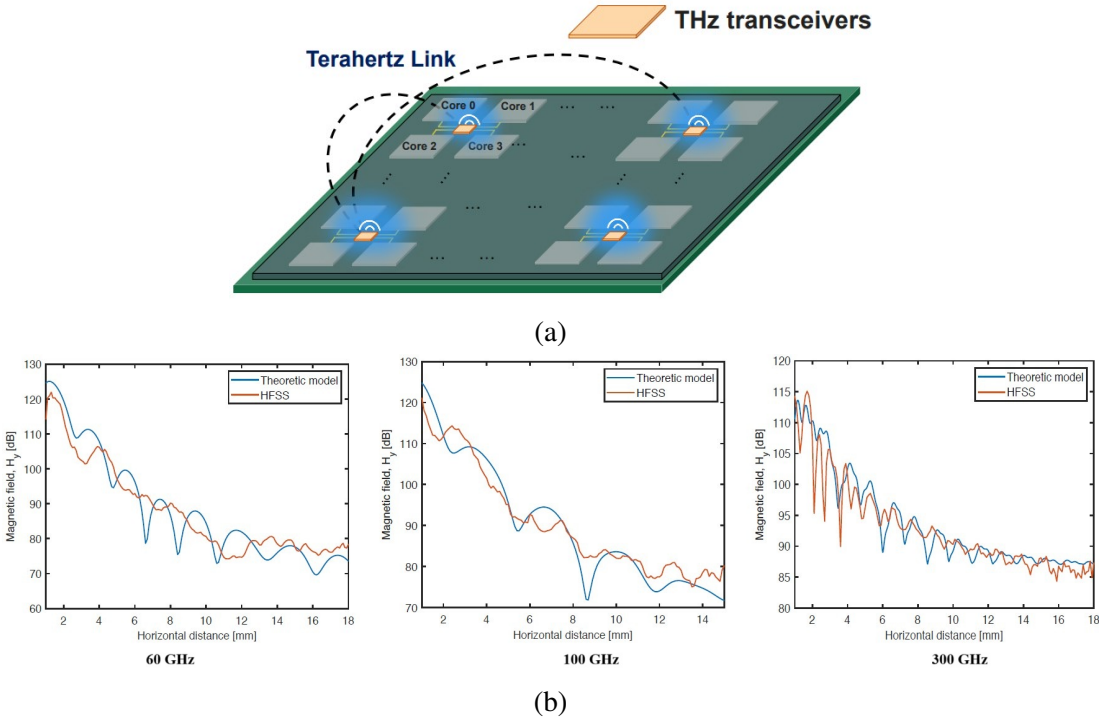
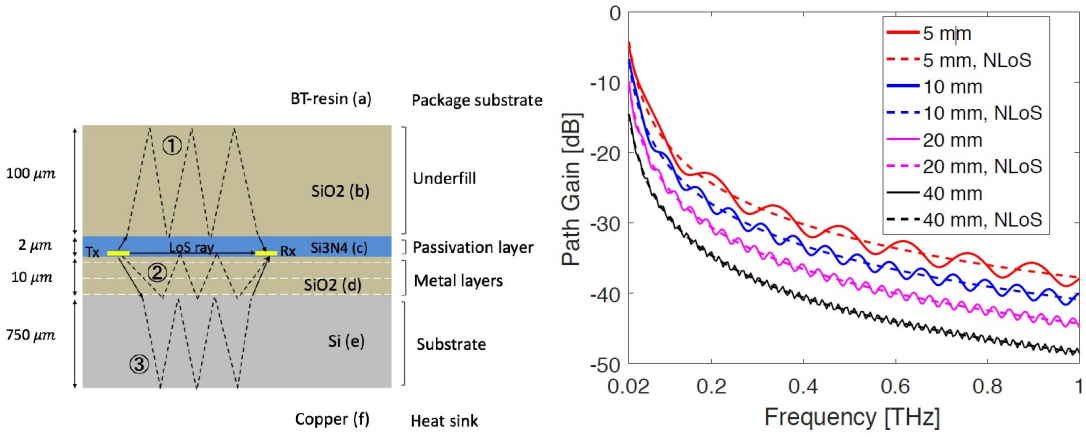


Figure 2.48: **(a)** Wireless network-on-chips THz transceiver and **(b)** variation of electric field magnitude with propagation distance across multiple operating frequencies [153]



(a) **(b)**

Figure 2.49: **(a)** WiNoC architecture with ray-trajectory between TX and RX **(b)** Gain and frequency relationship [154]

Recent work by Deepa and Sudha [151] investigated intra-chip communication using four antenna geometries (zig-zag, triangular monopole, bow-tie, and meander) operating in the $10-75$ GHz range. Simulation results revealed that the meander antenna achieved superior matching with $|S_{11}| = -15$ dB and VSWR ≈ 12, offering high radiation efficiency and minimal edge coupling interference. Figure 2.45**(a-c)** illustrates the transceiver configuration using the rectangular meander antenna in a single substrate and the corresponding reflection characteristics.

Building upon this, [152] proposed a THz wireless interconnect system for chip-to-chip communication employing On–Off Keying (OOK) modulation and WR-3.4 standard horn antennas as transceivers. Operating within the $220 - 330$ GHz band, the system achieved multi-gigabit data transfer with bit-error rates (BER) below 10^{-9} for short-range interconnects. The study demonstrated that THz frequencies provide sufficient bandwidth for high-speed chip-scale data transfer when coupled with low-loss substrates. Figure 2.46 may illustrate the experimental setup for chip-to-chip THz link configuration, showing the horn pair using an OOK modulation scheme.

At the architectural level, Lee et al. [11] introduced the WCube structure, a scalable

two-tier hybrid wired/wireless interconnect for thousands of cores in CMPs. The design integrates a single transmit antenna and multiple receive antennas embedded in a low-loss polyimide layer to minimize substrate absorption at sub-THz frequencies ($100-500$ GHz). Full-wave electromagnetic simulations indicated a $20-30$ dB improvement in channel loss compared to conventional silicon implementations, and $20-45\%$ latency reduction compared with traditional 2-D mesh topologies. Figure 2.47**(a)** presents the WCube topology, and Figure 2.47**(b)** provides the cross-sectional view of THz antenna placement in the polyimide substrate layer.

For in-depth channel characterization, Chen et al. [153] developed a six-layer stratified medium model that includes the passivation, metal, silicon, under-fill, package substrate, and heat sink layers. By modeling electromagnetic propagation from a Hertzian dipole embedded above the top metal layer, they demonstrated a channel capacity up to 0.95 Tb/s with strong agreement between analytical predictions and HFSS full-wave results. The study revealed that optimizing the silicon thickness ($\approx 200-300\mu$m) and reducing under-fill thickness significantly improve path gain and minimize inter-layer reflection. Figure 2.48**(a)** shows the isometric view of the WiNoC architecture, and Figure 2.48**(b)** depicts the e-field intensity versus the distance with different frequencies of operation. Complementary to this work, [154] presented a ray-tracing multipath propagation model for flip-chip packaged WiNoC systems. The model predicts that intra-chip channel capacity can exceed 1 Tb/s at 5 mm, but gradually declines to approximately 0.38 Tb/s at 40 mm, primarily due to dielectric loss and multi-path fading. Figure 2.49**(a)** depicts the ray-based tracing trajectories, and Figure 2.49**(b)** the corresponding gain and frequency relationship.

To consolidate the key developments in on-chip communication, Table 2.6 summarizes representative studies across architectural, modeling, and design perspectives.

Table 2.6: Summary of on-chip communication studies

Reference	Design Focus	Key Results	remarks
[11]	WCube hybrid wired/wireless CMP interconnect ($100-500$ GHz); antenna in polyimide layer	$20-45\%$ latency reduction; ~ 100 μm antenna; operation 300 GHz	Demonstrated scalable, low-loss sub-THz WiNoC architecture
[154]	Six-layer WiNoC channel model (Si, metal, under-fill, package)	Analytical & HFSS validation; path gain $\uparrow$ with thinner under-fill	First physics-based THz WiNoC model including package effects
[153]	Hybrid analytical/statistical WiNoC channel model	Path loss < 90 dB at 1 THz (20 mm); capacity ≈ 1 Tb/s	Showed THz intra-chip viability; analyzed substrate losses
[151]	Four on-chip antennas (zigzag, bow-tie, meander, etc.) for $10-75$ GHz	Meander: $\lvert S_{11}\rvert = -17$ dB, VSWR ≈ 1.2	Validated multi-antenna edge placement for short-range WiNoC
[152]	System-level THz wireless link ($0.3-1$ THz, OOK)	$10-15$ Gb/s at 10 mm, BER < 10^{-9} at 24 dB SNR	Provided benchmark for chip-to-chip THz link design

2.4.2 SIW Horn Antennas

Conventional rectangular waveguide (RWG) horns are well known for their high gain and low loss, but remain bulky and unsuitable for monolithic integration in mm-Wave and THz-scale systems. Substrate Integrated Waveguide (SIW) horn antennas have thus

emerged as a planar and compact alternative, offering comparable performance with greater ease of fabrication. Their ability to confine electromagnetic energy between metallized via walls while maintaining compatibility with standard PCB or LTCC processes makes them particularly promising for terahertz front-ends and SoC-based applications.

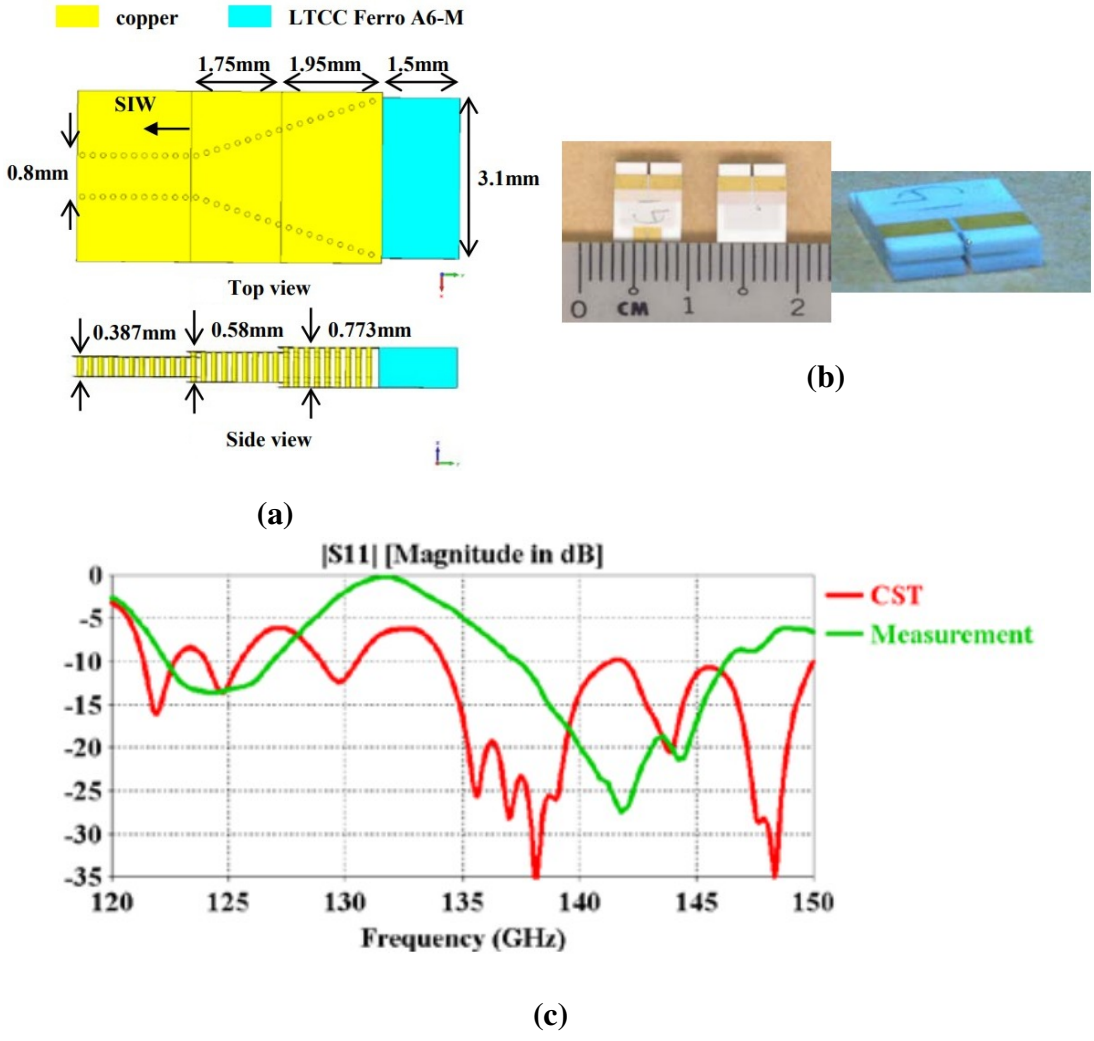
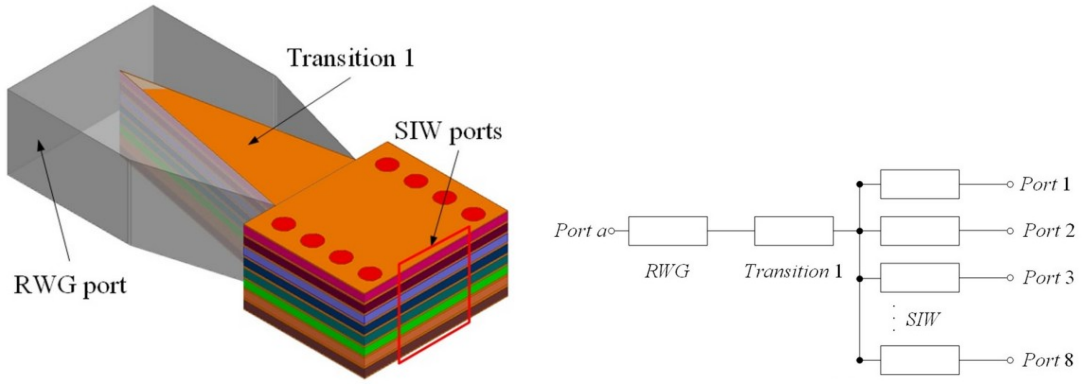
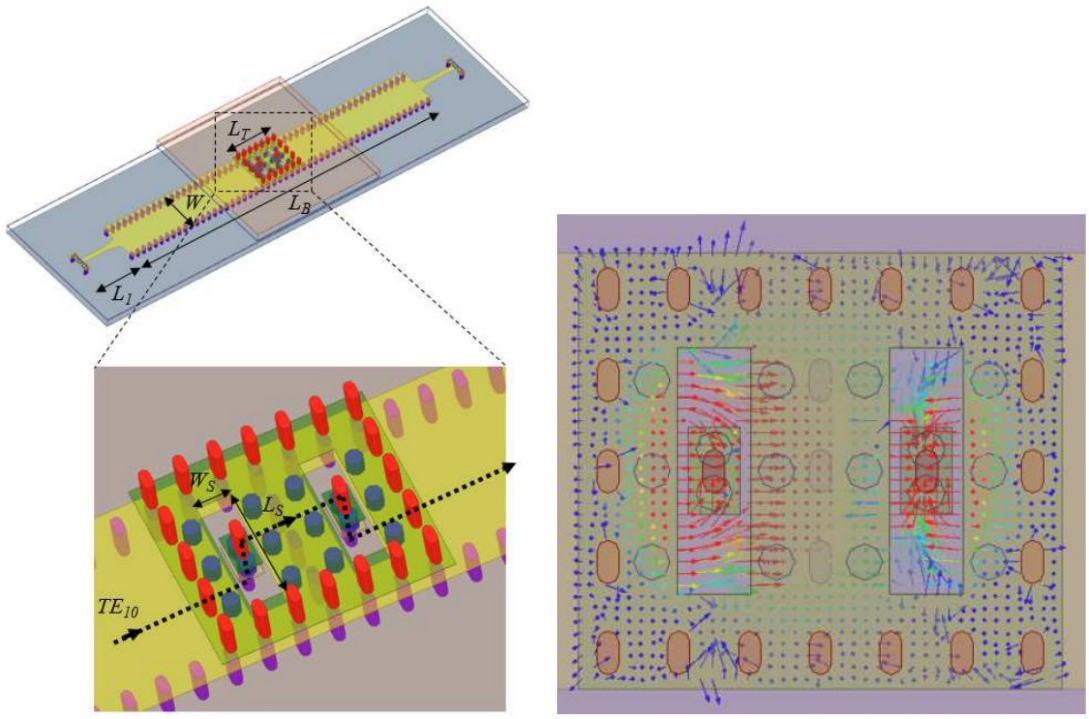


Figure 2.50: SIW horn antenna element implemented on an LTCC substrate **(a)** structural layout, **(b)** fabricated prototype, and **(c)** simulated and measured $|S_{11}|$ [133]



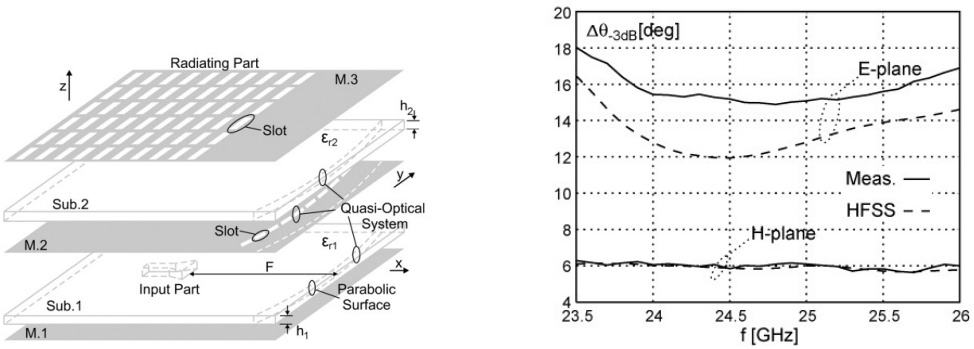
(a) **(b)**

Figure 2.51: Eight-way stacked power divider: **(a)** schematic configuration of the proposed structure, and **(b)** its corresponding equivalent circuit model [132]



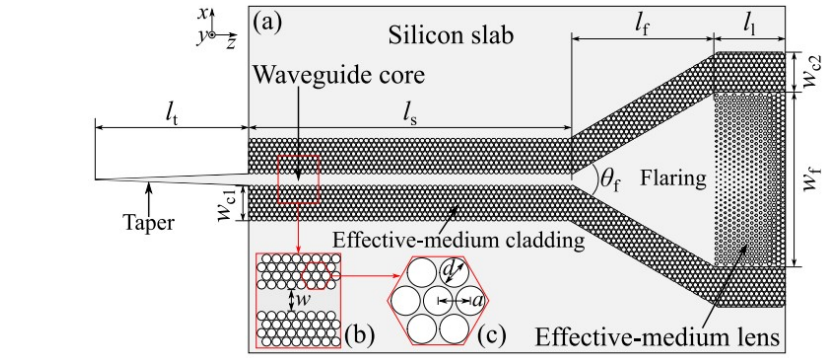
(a) **(b)**

Figure 2.52: Stacked SIW-to-SIW transition: **(a)** three-dimensional isometric view of the proposed structure, and **(b)** electric field distribution around the rectangular coupling slots at 150 GHz [155]

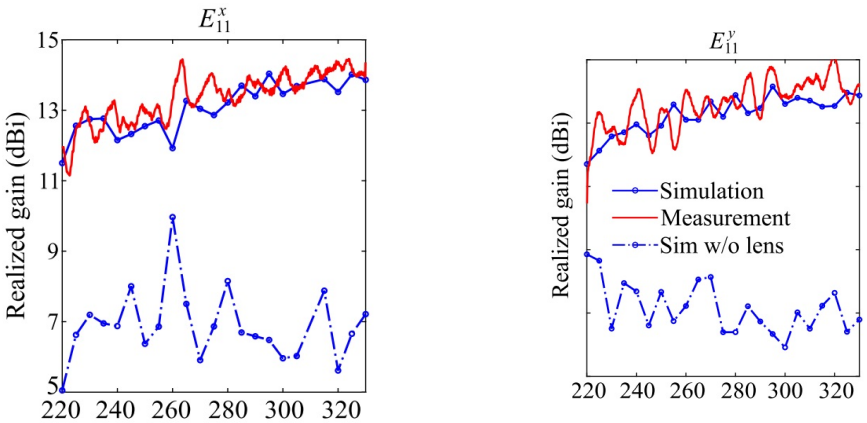


(a) **(b)**

Figure 2.53: **(a)** Three-dimensional view of the proposed pillbox transition horn structure and **(b)** comparison of measured and simulated HPBW in the E- and H-planes for feed port #4 [156]



(a)



(b) **(c)**

Figure 2.54: **(a)** Schematic representation of the all-silicon 2D horn antenna. Simulated and measured realized gains corresponding to the **(b)** E_{11}^{x} and **(c)** E_{11}^{y} modes [157]

Early SIW horn efforts demonstrated fundamental array feasibility using multilayer low-temperature co-fired ceramic (LTCC) processes. A 2×2 SIW horn array operating at 140 GHz integrated both vertical and horizontal power-dividing networks within stacked ceramic layers to achieve approximately 13 dBi simulated gain and -10 dB impedance bandwidth of 9 GHz [133]. However, asymmetric E/H-plane beamwidths and elevated sidelobes indicated that LTCC thickness and flare geometry strongly affect beam symmetry and aperture efficiency. Figure 2.50**(a-b)** shows the layout and the fabricated prototype of the antenna array on an LTCC Ferro A6-M ($\epsilon_r = 5.9$ and $\tan\delta = 0.001$) and the comparison results is depicted in Figure 2.50**(c)** highlighting a slight discrepancy between the simulated and measurement, primarily due to fabrication tolerance.

Subsequent works focused on refining multilayer SIW power-divider networks to support broader bandwidth and improved amplitude balance for feeding such horns. [134] proposed compact Ka-band 1×4 and 1×8 multilayer SIW power dividers using coupling-slot transitions between layers, achieving nearly half the footprint of conventional designs while maintaining -15 dB reflection from $33.5 - 35.5$ GHz. Zhou et al. [132] extended this concept to the sub-THz regime ($90 - 110$ GHz) using an eight-layer stacked-SIW power divider as displayed in Figure 2.51 with a wedge transition between a WR-10 rectangular waveguide and the SIW stack, attaining < 1.35 dB insertion loss and > 19 dB isolation.

To enable vertical electromagnetic coupling between layers, [155] introduced a broadband stacked SIW-to-SIW transition for $110 - 160$ GHz. This flip-chip integrated passive device (IPD) implementation uses through-silicon vias (TSVs) as shown in the Figure 2.52**(a)** and gold-bump quasi-coaxial structures to support TE_{10} coupling with only 0.28 dB insertion loss at 133 GHz. Figure 2.52**(b)** depicts the vector E-field distribution through the stacked transition, establishing the efficient vertical transitions essential for multilayer SIW horn feeding networks. On the antenna-front side, Ettorre

et al. [156] proposed a multilayer SIW leaky-wave "pillbox" horn structure integrating a quasi-optical parabolic coupling system between stacked substrates as shown in Figure 2.53**(a)**. Figure 2.53**(b)** presents the HPBW, showing nearly constant values of about 15° in the E-plane and 6° in the H-plane. Minor deviations arise from conductor losses and unmodeled metal thickness. The metallic-pin parabola and multi-slot transitions improve phase uniformity, bandwidth, and reflection performance in PCB-compatible SIW horn designs.

At higher frequencies, [157] demonstrated an all-silicon planar horn operating from 220–330 GHz using a sub-wavelength hole-lattice effective medium to form a 2-D dielectric lens for wavefront flattening as shown in Figure 2.54**(a)**. Fabricated by deep reactive ion etching, the antenna achieved $11 - 15$ dBi realized gain for both in-plane and out-of-plane polarizations 2.54**(b-c)**, showcasing full CMOS-compatible integration potential without metallic loss. To summarize major SIW horn antenna designs reported in literature, Table 2.7 compares key configurations, performance metrics, and implementation remarks.

Overall, the evolution from LTCC-based multilayer SIW horns to all-silicon planar designs reveals a clear research trajectory toward broadband, fabrication-friendly, and highly integrated terahertz horn antennas. The proposed work in this thesis (chapter 3) builds on these advances by developing a stacked SIW horn structure at 210 GHz employing a slot-coupled multilayer SIW power splitter engineered for Gaussian amplitude and near-uniform phase ($\Delta\phi \approx 0^\circ$) across five layers. This approach explicitly targets balanced HPBWs in both E- and H-planes using PCB/LTCC-compatible SIW processes.

Table 2.7: Comparison of SIW Horn Antenna

Reference	**Design Focus**	**Key Results**	**remarks**
[133]	2×2 SIW horn array on 20-layer LTCC with vertical/horizontal dividers	13.3 dBi gain; -10 dB BW ≈ 10	Compact but asymmetrical E/H beams; high sidelobes
[134]	$1 \times 44/1 \times 8$ multilayer SIW dividers using slot coupling	-15 dB return loss ($33.5 - 35.5$ GHz)	50% size reduction; simple feed network
[155]	Flip-chip stacked SIW–SIW transition (TSVs + gold bumps)	$108 - 158$ GHz BW; 0.28 dB IL at 133 GHz	Broadband vertical feed; 3D integration compatible
[132]	8-layer stacked SIW divider with wedge RWG–SIW transition	IL < 1.35 dB; Isolation > 19 dB	High isolation; compact sub-THz feed design
[156]	Multi-beam SIW pillbox horn with parabolic slot transition	Wideband; improved phase uniformity	Validated PCB-compatible multi-beam horn concept
[157]	All-silicon planar horn with sub-λ hole-lattice lens	$11 - 15$ dBi gain; $220 - 330$ GHz BW (40%)	CMOS-compatible; improved matching and flat wavefront

2.4.3 Mode Converters (RWG $TE_{10} \leftrightarrow$ SIW TE_{20})

Early studies on waveguide-to-SIW transitions primarily focused on converting the fundamental TE_{10} mode of RWG into the same mode in SIW. Methods such as stepped

transformers [158], aperture coupling [159], and ridged structures [160] were commonly employed to realize broadband transitions in the microwave and mm-Wave frequency bands.

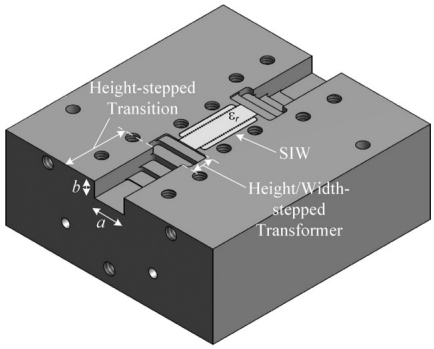


Figure 2.55: Isometric view of the back-to-back air-filled waveguide to SIW transition [161].

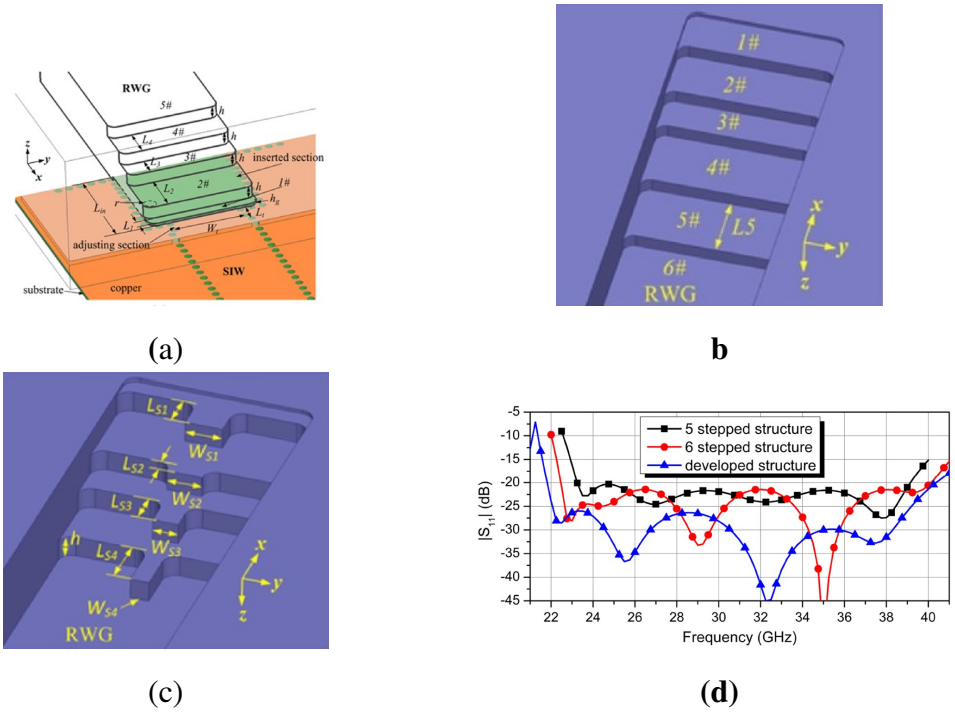


Figure 2.56: Layout of the waveguide transition to SIW using rigid steps **(a)** 5-stepped transition and **(b)** 6-stepped, **(c)** 5-rigid stepped structures, and **(d)** simulated results of all three structures [160]

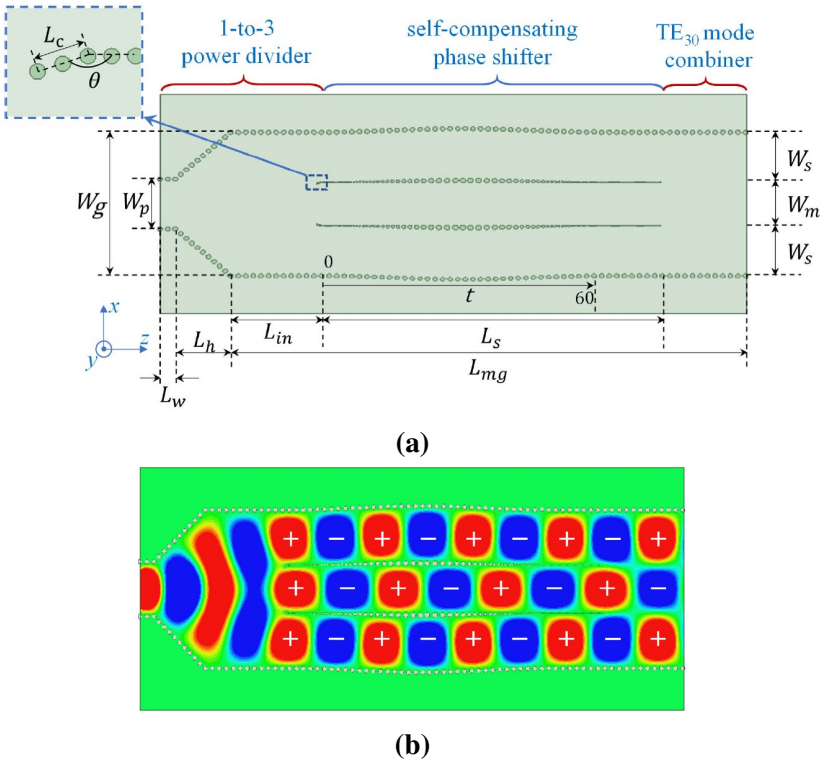


Figure 2.57: SIW TE_{10}-TE_{30} mode converter showing **(a)** structural configuration and **(b)** simulated E-field distribution at 13 GHz [162]

Cano et al. [161] designed an air-filled RWG with stepped waveguides to achieve efficient coupling, as shown in Figure 2.55, while Li et al. [160] developed a compact broadband transition between a rectangular waveguide (RWG) and a substrate integrated waveguide (SIW) using a five-step ridged structure to enhance impedance matching and minimize reflections. As shown in Figures 2.56**(a-c)**, the ridged steps within the RWG concentrate the electric field near the center, improving coupling efficiency and extending the bandwidth compared with conventional multi-step designs as shown in the simulated result Figure 2.56**(d)**. This ridged-step approach effectively concentrates the electric field in the central region, minimizing reflection and enabling compact, low-loss transitions suitable for mm-Wave and THz systems. Similar work using aperture coupling and perpendicular placements of RWG and SIW structures also demonstrated

successful mode conversion with compact geometries [158, 159, 163].

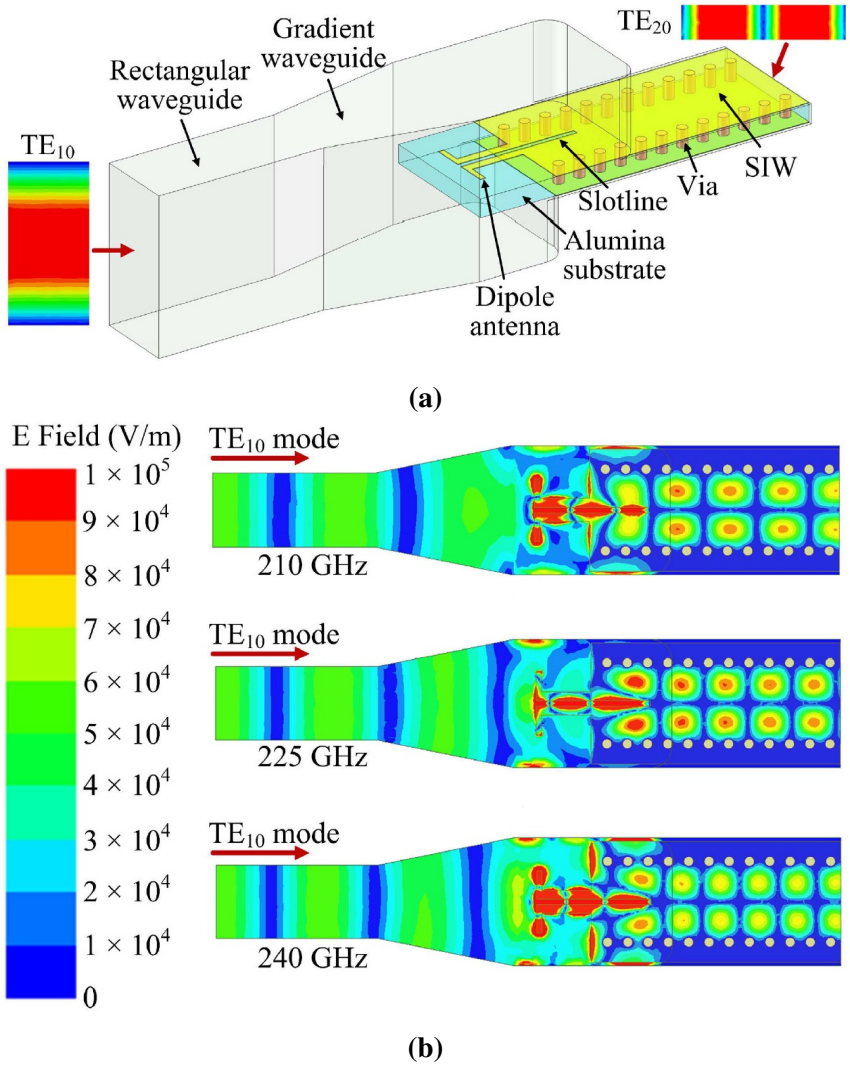


Figure 2.58: RWG TE_{10}–to–SIW TE_{20} mode converter: **(a)** three-dimensional schematic illustrating the dipole and slotline-based transition structure, and **(b)** simulated electric-field distributions at 210, 240, and 255 GHz [164]

Although effective, these approaches were limited to relatively low-frequency ranges and primarily targeted TE_{10} - TE_{10} operation, restricting their potential for advanced THz systems.

Building on this foundation, researchers explored converters capable of exciting higher-order modes to exploit additional bandwidth and radiation characteristics. Several

designs attempted TE_{10} - TE_{20} conversion using techniques such as dipole antennas and slot-line excitation, as shown in Figure2.58**(a)** along with its E-field 2.58**(b)** [164]. Wu et al. [165] and Shu et al. [166] demonstrated wideband converters with improved field distribution control, while other works employed multi-step or layered substrates to achieve efficient transitions [167, 168]. Zhang et al. [162] extended this concept by proposing a TE_{10}-TE_{30} converter that utilizes phase-shifting and power-dividing techniques (antenna geometry is shown in Figure 2.57**(a)**), achieving high conversion efficiency at microwave frequencies. Figure 2.57**(b)** shows the TE_{30} E-field distribution achieved at 13 GHz. Despite these advancements, most higher-order mode converters were designed for microwave-to-mm-wave applications, with limited research addressing their feasibility and performance at THz frequencies.

At THz frequencies, achieving reliable higher-order mode conversion becomes considerably more complex. Precise control over geometrical dimensions is required to maintain impedance matching and avoid excessive propagation loss, which increases sensitivity to fabrication imperfections and substrate variability. Furthermore, while modes such as TE_{30} or TE_{40} have been successfully demonstrated in certain antenna arrays and leaky-wave structures, these implementations often rely on combining multiple TE_{20} modes, limiting their applicability for integrated THz circuits [162, 169, 170]. As a result, despite notable progress in lower-frequency designs, the development of compact and broadband converters capable of efficiently exciting and isolating higher-order SIW modes in the THz band remains an open research problem. Addressing this gap is essential for enabling scalable, low-loss, and high-gain THz front-end circuits. Table 2.8 summarizes efficient transitions between rectangular waveguides (RWG) and substrate integrated waveguides (SIW), as well as to excite higher-order SIW modes for planar THz systems. The listed works demonstrate techniques such as aperture coupling, stepped or ridged transitions, and wideband TE_{10}-TE_{20}/TE_{30} excitations.

Table 2.8: Comparison of reported mode converter designs for RWG $\leftrightarrow$ SIW and higher-order SIW excitations

Reference	**Design Focus**	**Key Results**	**remarks**
[167]	Direct TE_{30} excitation in SIW via CPW-slot; Yagi-Uda demo	46% BW($7.8 - 12.4$ GHz); Gain: 8.5 dBi	Higher-mode feed simplifies network vs TE_{10}
[166]	H-plane T-junction with septum & irises	$228.8 - 293.1$ GHz; $S_{21} \approx -1$ dB; $S_{11} \approx -15$ dB	Compact, aligned ports; nano-CNC prototype
[167]	Two wideband TE_{20} exciters: midline slot & aperture-coupled slotline	Balun demonstration: ≈50% FBW with good RL/imbalance	Simple, compact transitions for even TE_{n0} modes
[163]	H-plane slot-to-slot RWG↔SIW transition	At 30 GHz: IL≈0.11 dB, RL < -10 dB (26.3-30.7 GHz)	Low-profile H-plane variant, suitable for arrays
[164]	RWG dipole → grounded slotline → SIW TE20	198-238 GHz (18.3%); back-to-back 2.1-5.0 dB IL	First 220 GHz RWG TE_{10} to SIW TE_{20} converter; shows filter/balun apps
[162]	1→3 divider & self-compensating 3-way phase shifter with combiner	11.28-14.8 GHz (27%); >95% efficiency & mode purity	Single-layer PCB; clean TE30 single-mode propagation
[171]	Height-stepped WG & single-step widening transformer	32-50 GHz; back-to-back IL 0.68 dB, RL 15 dB	Full-band, no dielectric probe; low loss
[160]	RWG 5 ridged steps & multi-section SIW	23.83-40 GHz; RL > 15 dB, IL<2.45 dB (B2B)	Broadband ridge-assisted transformer
[158]	Stepped dielectric transformers; no machining in RWG	180-240 GHz; single IL<0.9 dB, RL>10 dB	THz-friendly, easy assembly; wideband

2.5 Research Gaps

2.5.1 SIW Horn Antenna

The rapid increase in global data traffic driven by applications such as IoT, autonomous systems, and real-time multimedia services continues to push wireless communication into the terahertz (THz) spectrum [155]. While THz technology promises ultra–high-speed transmission, antenna design at these frequencies remains constrained by fabrication limits, propagation loss, and the need for compact, high-gain, and beam-symmetric configurations [157].

Rectangular horn antennas provide high gain and wide bandwidth but suffer from bulky structures that hinder planar integration with MMICs [133, 172–174]. Substrate Integrated Waveguide (SIW) technology offers an effective alternative, combining low loss, compactness, and planar compatibility while preserving the key properties of traditional rectangular waveguides [175].

SIW horn antennas further enable efficient excitation via mode transitions or aperture coupling [33, 34]. Their performance can be enhanced using dielectric loading [174], sub-wavelength hole arrays for impedance matching [157], or extended parallel-plate structures for improved beam symmetry [176]. Despite progress in SIW horn antenna designs, several limitations remain unresolved. Many antennas exhibit imbalanced radiation with unequal E- and H-plane beamwidths, limiting performance. Existing designs often use complex or bulky feeding structures, reducing suitability for compact or on-chip integration. Although techniques like dielectric loading and multilayer designs are explored, achieving both high gain and beam symmetry in a compact form is still challenging. Additionally, most designs are not optimized for THz on-chip environments due to fabrication constraints and substrate losses. Building on these research gaps, chapter 3 proposes a compact stacked SIW horn antenna with optimized

slot transitions and aperture field control, achieving high gain, equal HBPWs in both planes, and efficient multi-layer excitation for next-generation THz systems.

2.5.2 Mode Converters (RWG $TE_{10} \leftrightarrow$ SIW TE_{20})

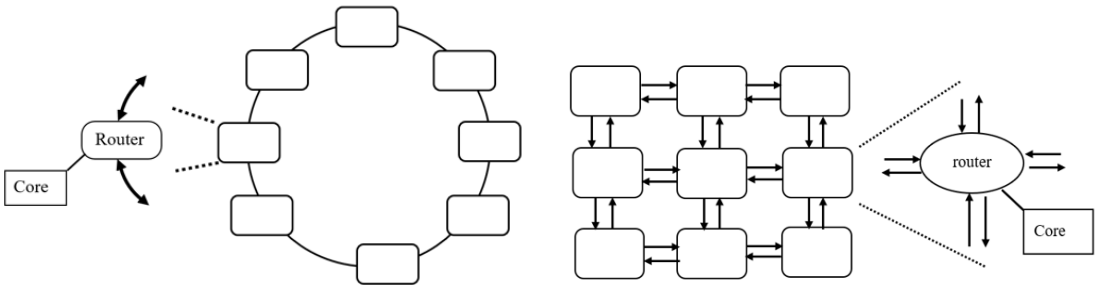
The rapid growth of artificial intelligence has intensified the demand for ultra–high-speed computing, driving the need for advanced on-chip communication technologies. Terahertz (THz) wireless interconnects have emerged as a promising solution to support high-density interconnects, multi-core and many-core architectures, and three-dimensional (3D) circuit integration for future AI-driven systems [35, 36, 38]. Within such systems, mode converter antennas play a crucial role in enabling transitions between different waveguide modes. However, most existing converters are confined to microwave and millimeter-wave frequencies [160, 164–166], leaving a gap in efficient mode conversion techniques at THz frequencies.

Most reported converters focus on TE_{10} - TE_{10} transition in the microwave and mm-Wave ranges, typically using stepped transformers, aperture coupling, or probe-based matching structures. While these approaches are effective at lower frequencies, they are not optimized for the THz band, where higher-order modes such as TE_{20} and beyond provide advantages in bandwidth, radiation performance, and power handling. Early attempts at higher-order mode excitation often suffered from limited bandwidth, bulky geometries, or reliance on multilayer substrates that hinder parallel integration. Furthermore, existing designs exhibit challenges with impedance mismatch, fabrication tolerances, and suppression of dominant modes that coexist in dual-mode regions. As a result, despite incremental progress, compact, wideband, and probe-less TE_{10} - TE_{20} converters specifically designed for planar THz integration remain scarce.

This gap motivates the exploration of novel converter designs that can efficiently excite single higher-order modes, suppress unwanted fundamental modes, and support

scalable integration with on-chip antennas [64, 177], filters [131], baluns [164], and power dividers [135]. Recent works, including perpendicular interconnects employing dipole-slot excitation and probe-less designs leveraging stepped metallic layers, have demonstrated the feasibility of compact and fabrication-friendly converters at THz frequencies. However, these efforts remain early steps toward fully optimized, broadband, and system-ready solutions. Developing such converters is therefore crucial for realizing low-loss, high-gain, and easily integrable THz front-end circuits, enabling next-generation applications in WiNoC, sensing, and high-speed communications.

2.5.3 On-Chip THz Communication



(a) (b)

Figure 2.59: Comparison of network topologies: **(a)** Ring and **(b)** Mesh [36].

In conventional wired interconnections of multi-core processors, communication among cores is established through metallic wires arranged in various network-on-chip (NoC) topologies, such as ring and mesh [178], illustrated in Figure 2.59, Sipergon STNoC [179], star, binary tree, butterfly, and torus topologies [180], have been proposed to optimize performance. However, a fundamental limitation arises from network diameter. For example, in an $N \times N$ mesh configuration, the diameter scales as $(2N - 1)$. Consequently, a 3×3 mesh requires four hops for communication between edge cores, which introduces higher latency. To address this, approaches such as the flattened

butterfly topology [181, 182] have been suggested, reducing hop counts by employing concentrated links. Nonetheless, these solutions rely on long global wires, which at high speeds suffer from resistive-capacitive (RC) delays and signal attenuation [183]. The rapid advancement of multi-core and many-core processors has further intensified the demand for high-speed and energy-efficient communication between integrated circuits. Conventional wired interconnects not only suffer from increased latency due to multi-hop communication, but also experience significant power consumption and signal integrity issues caused by parasitic resistance and capacitance. As data rates continue to scale, these limitations become a critical bottleneck in overall system performance.

In this context, wireless interconnects (WNoCs) have emerged as a promising alternative. Unlike wired systems, where signals propagate through metallic conductors and are constrained by RC parasitics, wireless communication performance is influenced by attenuation, path loss, interference, and noise. Despite these challenges, the terahertz (THz) band offers orders-of-magnitude larger bandwidth, enabling multi-gigabit and even terabit-per-second data rates. By exploiting this wide bandwidth, THz inter-chip communication enables high data-rate wireless links over short distances, making it particularly suitable for chip-to-chip communication, wireless network-on-chip (WiNoC) architectures, and heterogeneous system integration.

Furthermore, the compact size of THz antennas allows for dense on-chip integration, facilitating parallel transmissions without physical interconnect constraints [184]. In inter-chip communication, antennas play a crucial role in enabling efficient wireless links between closely spaced chips or modules. However, achieving this requires antennas that are compact, highly efficient, and compatible with planar fabrication technologies. These requirements make on-chip and substrate-integrated antennas strong candidates for THz interconnect applications.

In addition, THz inter-chip communication can significantly reduce routing complexity

and improve system scalability by replacing traditional wired links with wireless connections. This is particularly beneficial in high-performance computing systems, data centers, and advanced packaging technologies such as system-in-package (SiP) and three-dimensional integrated circuits (3D-ICs). Furthermore, omnidirectional broadcasting inherent to wireless communication reduces synchronization time between cores and minimizes energy consumption, as intermediate routers and multiple hops are avoided. A comparative study on 64-core processors indicates that wireless interconnects improve bandwidth per core by 15% and enhance energy efficiency per packet by 39% compared to their wired counterparts [185]. The incorporation of multiplexing schemes further amplifies these advantages, supporting higher data throughput and flexible resource sharing.

Overall, the transition from wired to THz wireless interconnects addresses key bottlenecks in NoC designs such as latency, scalability, and energy efficiency, positioning WiNoCs as a compelling paradigm for next-generation multi-core processors.

2.6 Chapter Summary

This chapter presented an extensive review of terahertz (THz) technology and on-chip antenna developments that underpin next-generation wireless communication systems. It began with an overview of the THz spectrum, emphasizing its wide bandwidth and high data-rate potential, along with major challenges such as propagation loss, fabrication complexity, and integration constraints at sub-millimeter wavelengths.

The discussion then focused on various on-chip antenna (OCA) structures, highlighting their design evolution, advantages, and limitations. Patch and slot antennas were recognized for their planar simplicity and CMOS compatibility, but constrained by narrow bandwidth and low efficiency. Bow-tie and Vivaldi antennas demonstrated broadband impedance and end-fire radiation suited for high-frequency integration,

while leaky-wave antennas (LWAs) enabled frequency-controlled beam steering and high directivity using metasurface and Fabry–Perot concepts.

Further, dipole, monopole, and loop antennas were analyzed for compactness, symmetry, and ease of differential integration. Enhanced variants such as AMC-backed, Yagi, and quasi-Yagi configurations provided improved gain and polarization purity. The review also explored substrate integrated waveguide (SIW) and metamaterial/metasurface (MTM/MTS) platforms, which suppress surface-wave losses and enhance impedance bandwidth through engineered dispersion and field confinement. Finally, dielectric-resonator antennas (DRAs) were identified as highly efficient radiators offering strong field confinement, high gain, and compatibility with hybrid SIW and MTS excitations. Collectively, the literature reveals a clear progression from conventional planar OCAs to advanced hybrid SIW–MTS–DRA architectures, which achieve an optimal balance among compactness, bandwidth, and radiation efficiency. These insights establish the theoretical foundation and motivate the novel antenna and mode-converter designs developed in the following chapters.

Chapter 3

Stacked SIW-Based Pyramidal Horn Antenna for THz Communications

As discussed earlier in Chapter 2, antennas play an indispensable role in wireless communication systems. They function as interfaces that radiate or capture electromagnetic waves, typically realized using metallic structures of diverse geometries such as wires, rods, lenses, or patches. Essentially, an antenna serves as a transition element between a guided medium and free space, enabling the transfer of electromagnetic energy to and from an electronic circuit. With the continuous advancement of semiconductor-based integrated circuits (ICs) and wireless communication technologies, antenna design methodologies have evolved dramatically, particularly in terms of miniaturization and integration. As modern electronic systems become increasingly compact, antennas too must scale down accordingly while maintaining optimal performance.

Horn antennas are well known for their high gain, broadband, and strong power-handling capabilities. However, conventional metallic horns are bulky and incompatible with planar fabrication techniques, particularly at THz frequencies. To overcome these limitations, SIW technology provides a compact and fabrication-friendly alternative that

retains the desirable properties of waveguides while enabling integration with planar circuitry.

This chapter presents the design and performance evaluation of a stacked SIW-based pyramidal horn antenna that achieves equal HPBWs in both E- and H-planes while maintaining compactness and fabrication feasibility. The remainder of this chapter details the design rationale, geometry, simulation results, feeding network, and integrated system performance.

3.1 Design Rationale

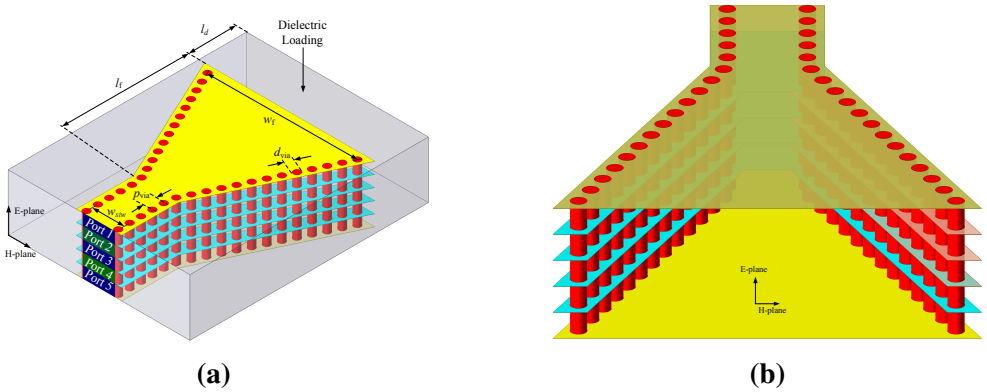
The aperture field distribution of a horn antenna plays a pivotal role in determining its HPBW, directivity, SLLs, and front-to-back ratio (FTBR). For high-frequency applications such as THz communications, achieving beam symmetry in both the E- and H-planes is particularly critical to ensure uniform coverage and stable radiation gain. However, both conventional designs often yield unequal HPBWs across the two planes, primarily due to the inherent differences in their flare geometries. This asymmetry leads to beam distortion and compromises the overall radiation performance, thereby limiting their suitability for compact, high-frequency systems. Thus, ensuring identical beamwidths in both planes remains a fundamental design objective.

To overcome these limitations and enable compact yet high-performance THz components, multilayer antenna technologies have garnered increasing attention. While a single-layer SIW-based horn antenna provides simplicity, its feeding network typically occupies a substantial footprint, which restricts miniaturization and integration flexibility. By contrast, vertically stacked multilayer SIW configurations transform the antenna into a quasi-3D architecture, improving integration density and offering greater design flexibility at THz frequencies [156, 157, 186, 187].

In the proposed design, multiple SIW horn antenna layers are vertically stacked, with

the common metallic layers between adjacent horns removed to form a continuous E-plane aperture. The number of layers directly governs the aperture size and hence the beamwidth. Nevertheless, excessive stacking can introduce aperture phase errors, which in turn degrade gain and overall radiation performance despite the physically larger aperture [188]. To address this trade-off, careful optimization of both the flare geometry and the number of stacked layers was carried out using Ansys HFSS full-wave simulations. This approach ensures uniform beam symmetry across the E- and H-planes, minimizes phase distortion, and achieves a compact form factor well-suited for integrated THz front-end systems.

3.2 Antenna Geometry



(a) **(b)**

Figure 3.1: Structural configuration of the proposed SIW horn antenna, highlighting the metal layers and via hole arrangement **(a)** isometric view and **(b)** sectional view

The proposed antenna features a five-layer stacked SIW horn configuration, each layer incorporating a dielectric loading to enhance confinement and radiation efficiency. The structure is excited through a five-port TE_{10} mode feeding network and is designed to operate at a center frequency of 210 GHz. The overall geometry of the antenna is illustrated in Figure 3.1, while the optimized structural dimensions are derived following standard SIW design methodologies [130] and are presented in Table 3.1.

These dimensions were meticulously optimized to suppress radiation leakage and to ensure impedance continuity and broadband performance across the operational band.

Parameter	**Value** (in mm)
w_{siw}	0.65
w_{f}	5.65
l_{f}	3.9
l_{d}	1.25
p_{via}	0.25
d_{via}	0.15

Table 3.1: Parameter of the Proposed SIW Horn Antenna

Each layer is fabricated on a polyimide substrate characterized by a relative permittivity (ϵ_r) of 3.5, a loss tangent ($\tan\delta$) of 0.008, and a total layer thickness of 1.25 mm. The horn's H-plane flare angle is maintained at $60°$, providing an optimal compromise between compactness, impedance matching, and directivity. At THZ frequencies, realizing a conventional E-plane flare presents substantial fabrication challenges due to limited substrate thickness and strict alignment tolerances. To circumvent these constraints, the proposed architecture employs a vertically stacked multilayer configuration that emulates an E-plane flare through sequential SIW stacking. This arrangement produces a continuous E-plane aperture while maintaining mechanical simplicity and planar manufacturability.

The resulting multilayer SIW horn achieves near-symmetric radiation characteristics in both E- and H-plane, overcoming the beam asymmetry commonly observed in single-layer SIW horn designs. This configuration not only enables high gain and wideband radiation at 210 GHz but also ensures scalability and compatibility with

standard micro-fabrication processes, making it highly suitable for integrated THz front-end systems.

3.2.1 Design Steps

The design steps for the proposed stacked SIW pyramidal horn antenna are summarized as follows:

1. Initial determination of the SIW waveguide dimensions based on the target operating frequency of 210 GHz.

2. Optimization of the horn flare section, including the flare width and length, which define the fundamental dimensions of the H-plane horn antenna.

3. Introduction of the multilayer stacked structure, incorporating the removal of shared layers to realize the required pyramidal horn configuration.

4. Assignment of individual ports to each layer and evaluation of the required magnitude and phase distribution to achieve optimum performance, particularly symmetric half-power beamwidths (HPBWs) in both the E- and H-planes.

5. Design of the initial feeding mechanism for the multilayer H-plane antenna structure.

6. Placement of coupling slots to enable efficient vertical energy coupling between multiple layers from a single feeding layer.

7. Optimization of the slot dimensions to achieve the desired phase and magnitude responses while maintaining a reflection coefficient below -10 dB at the target frequency.

8. Final full-wave simulation of the complete antenna with a single feeding port to evaluate the overall radiation characteristics, including gain, sidelobe levels, and radiation pattern.

3.3 Simulation and Performance Analysis

3.3.1 Radiation Characteristics

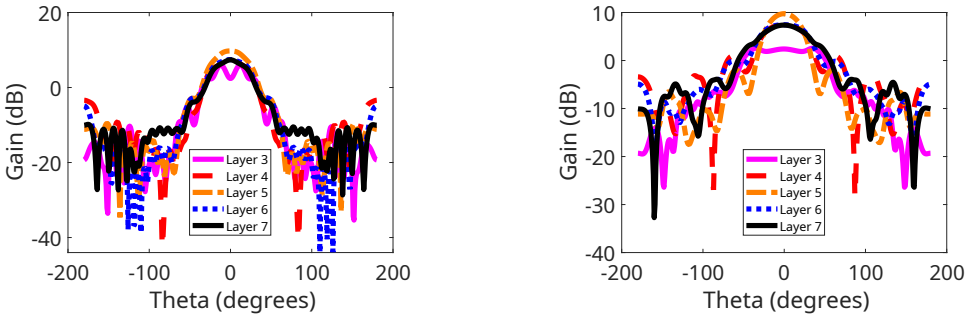


Figure 3.2: Simulated radiation gain at 210 GHz for varying number of stacked SIW layers with uniform port excitation (magnitude and phase): **(a)** E-plane and **(b)** H-plane

The full-wave simulations were carried out using a lossy dielectric substrate (polyimide) and copper metallization to account for realistic material properties at THz frequencies. The simulated radiation gains in both the E- and H-planes, obtained under uniform excitation conditions (equal amplitude and phase at each feeding port), are presented in Figure 3.2. To examine the scalability of the antenna's radiative performance, the number of vertically stacked SIW horn layers was systematically varied from three to seven. As anticipated, the overall gain increased with aperture height, reaching its maximum for the five-layer configuration. Beyond this point, however, a performance decline was observed, especially a noticeable gain reduction in the six-layer structure, with the seven-layer case exhibiting a comparable level. This trend indicates that the radiation performance saturates once the stack exceeds five layers.

The observed behavior originates from inter-layer phase non-uniformity rather than numerical inaccuracies. Under identical excitation conditions, the additional layers perturb the phase coherence between the stacked apertures, leading to partial field cancellation and a reduction in the effective aperture efficiency. Moreover, at the operating frequency of 210 GHz, the increased stack thickness introduces higher dielectric and conductor losses, which further limit the achievable gain enhancement. These combined effects explain the gain saturation and slight degradation observed in configurations beyond the optimized five-layer design.

3.3.2 Dielectric Loading Effects

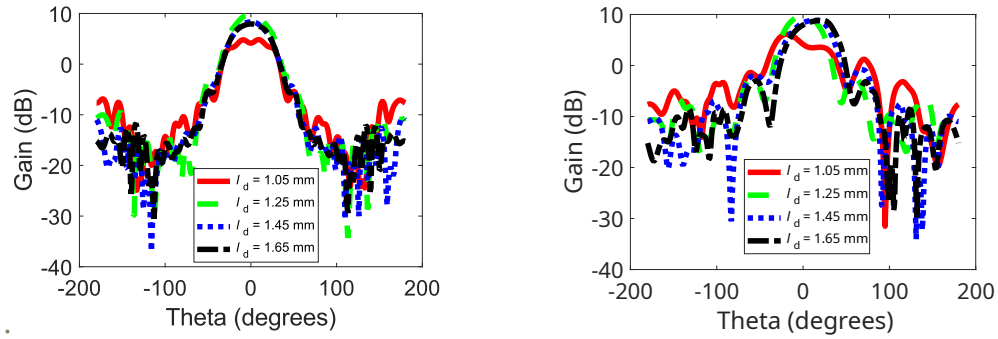


Figure 3.3: Radiation gain at 210 GHz for a five-layer SIW horn with varying dielectric lengths under uniform excitation: **(a)** E-plane, **(b)** H-plane

The simulated E- and H-plane gains, shown in Figure 3.3, exhibit a performance increase with dielectric leading length (l_{d}) up to an optimal point near $l_{\mathrm{d}} = 1.25$ mm, beyond which the gain begins to deteriorate. The length l_{d} was initially chosen to be on the order of the guided wavelength (λg) within the dielectric loaded region and subsequently fine-tuned at 210 GHz to achieve $l_{\mathrm{d}} \approx 1.2\lambda_{\mathrm{g}}$. Physically, a shorter dielectric section leads to insufficient phase compensation across the aperture, resulting in a broader H-plane beam and reduced directivity. Conversely, an excessively long dielectric section

introduces over-lensing effects, leading to additional dielectric loss and phase non-uniformity across the aperture. This produces beam broadening and a corresponding reduction in gain. The observed trend aligns well with previously reported behaviour for dielectric-loaded SIW H-plane horn [189].

3.3.3 Magnitude Excitation Profiles

The proposed SIW horn antenna incorporates five input ports, labeled Port 1 through Port 5, as illustrated in Figure 3.1**(a)**. Each port is excited in the TE_{10} mode under either uniform (equal amplitude and phase) or non-uniform (varying amplitude and/or phase) excitation conditions. To enhance the overall radiation characteristics of the stacked SIW horn, a Gaussian amplitude excitation profile is employed across the feeding ports [190]. This excitation scheme generates a tapered field distribution that closely approximates ideal aperture illumination, a principle commonly used in high-frequency antenna design to suppress side lobes, improve beam symmetry, and enhance directivity. Such an approach is particularly advantageous for THz antennas, where the physical aperture size is inherently constrained by fabrication limits.

The excitation amplitude for each input port is defined by a Gaussian distribution, mathematically expressed as

$$A(n) = A_0 e^{-\frac{(n-c)^2}{2\sigma^2}}, n = 1, 2, 3, ..., N \tag{3.1}$$

where $A(n)$ represents the amplitude applied to the n^{th} port $A_0 = 1$ denotes the peak amplitude at the center port, $c = 3$ is the central index corresponding to the middle layer in the five-layer stacked SIW horn configuration, σ is the standard deviation that governs the taper sharpness of Gaussian profile, and $N = 5$ is the total number of layers or ports.

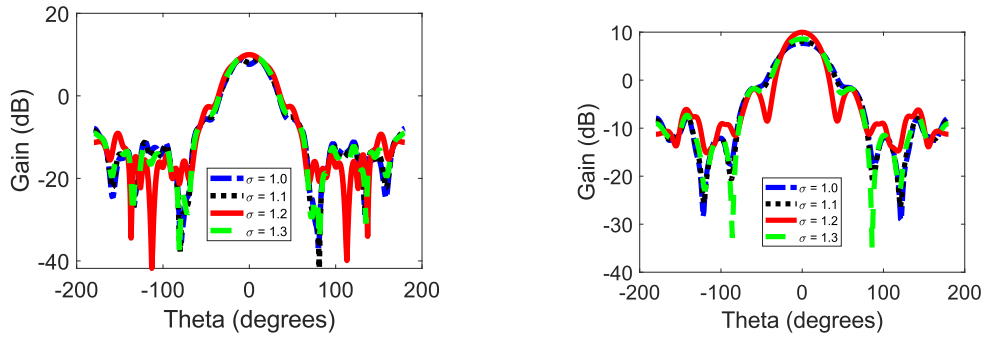


Figure 3.4: Simulated radiation gain at 210 GHz for varying excitation magnitudes under uniform phase excitation: **(a)** E-plane and **(b)** H-plane

To evaluate the influence of amplitude tapering on the antenna's radiation behavior, the standard deviation σ was varied between 1.0 and 1.3. This range was chosen to control the tapering effect without excessively reducing excitation at the other outer ports. The optimal configuration was achieved for $\sigma = 1.2$, which yielded enhanced beam symmetry and significantly reduced SLLs in the H-plane as shown in Figure 3.4**(b)**. In contrast, the E-plane radiation characteristics, presented in Figure 3.4**(a)**, remained largely unaffected across the tested σ values. This observation aligns with previous findings that horizontally distributed field components in compact, multilayer SIW horn structures are less sensitive to excitation tapering effects [172].

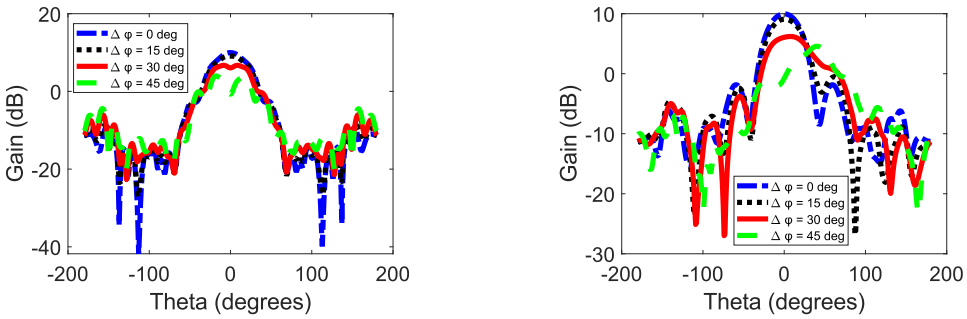
3.3.4 Phase Excitation Variations

Furthermore, to investigate the effect of phase imbalance across the feeding network, four symmetric phase excitation sets were applied:

- **Set A:** Uniform phase excitation (0° at all ports)
- **Set B:** $+30^\circ, +15^\circ, 0^\circ, -15^\circ, -30^\circ$
- **Set C:** $+60^\circ, +30^\circ, 0^\circ, -30^\circ, -90^\circ$

- **Set D:** $+90°, +45°, 0°, -45°, -90°$

These phase distributions are symmetric with respect to the central port (Port 3), ensuring that the main beam remains aligned along the boresight under ideal conditions. The progressive increase in phase gradient from Set A to Set D allows a systematic evaluation of the antenna's sensitivity to phase imbalance, particularly its impact on beam symmetry, HPBW, and SLL suppression, without introducing undesired beam steering.

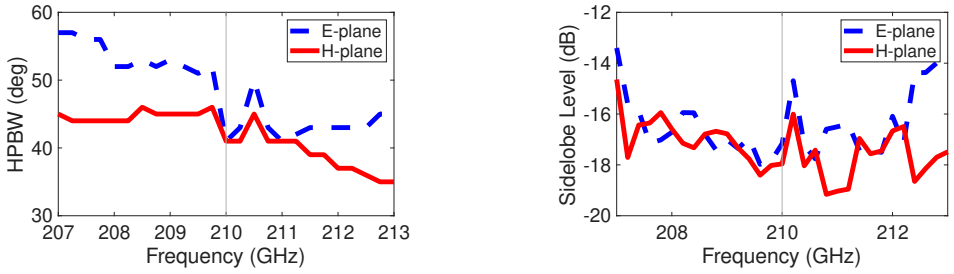


(a) **(b)**

Figure 3.5: Simulated radiation gain at 210 GHz for varying phase differences while maintaining a constant excitation magnitude ratio of $\sigma = 1.2$: **(a)** E-plane and **(b)** H-plane

The simulation results presented in Figure 3.5 demonstrate that uniform phase excitation across all feeding ports produces constructive interference of the radiated fields in the end-fire direction. This leads to enhanced directivity and improved beam symmetry in both the E- and H-planes. Such behavior is consistent with classical antenna array theory [191], wherein uniform phase excitation ensures coherent field superposition at the desired pointing direction, maximizing the resultant radiation intensity. In contrast, introducing phase variations among the ports disturbs the aperture field uniformity, thereby causing phase misalignment and partial destructive interference. This manifests as main-lobe distortion and elevated SLL, ultimately deteriorating the overall radiation efficiency and beam uniformity of the antenna.

3.3.5 HPBW and SLL



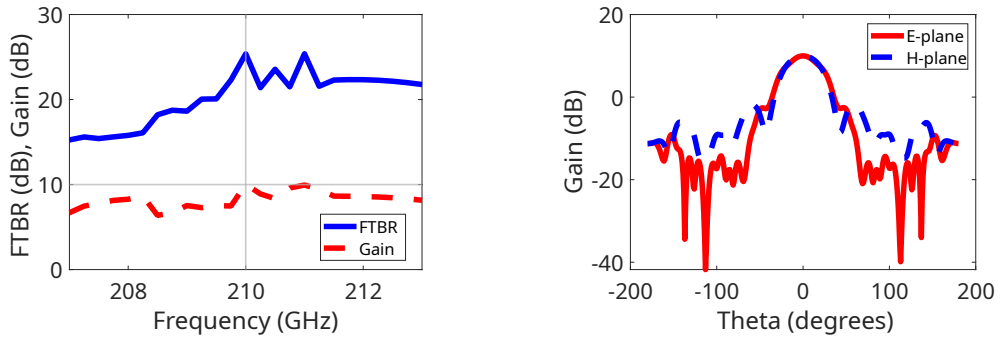
(a) **(b)**

Figure 3.6: Performance summary of the simulated stacked SIW horn antenna at 210 GHz for σ = 1.2 and $\Delta\phi = 0°$: (a) Half-Power Beamwidth (HPBW), (b) Side Lobe Level (SLL)

The simulated results for the half-power beamwidth (HPBW) as a function of frequency are presented in Figure 3.6**(a)**. The observed variation between the E- and H-planes primarily originates from the inherent aperture geometry of the stacked SIW horn. Owing to the smaller effective aperture dimensions in the E-plane, the resulting HPBW is generally broader compared to that of the H-plane [191]. At the operating frequency of 210 GHz, the implementation of a Gaussian amplitude excitation combined with uniform phase distribution ensures balanced aperture illumination, producing nearly identical HPBWs of approximately $41°$ in both principal planes.

Similarly, the side-lobe levels (SLLs), shown in Figure 3.6**(b)**, exhibit consistent behavior across the two planes. The proposed stacked SIW pyramidal horn achieves an SLL of around -17 dB, indicating a deliberate design compromise that favors planar compactness and beamwidth symmetry over aggressive SLL suppression. This optimization ensures a balanced trade-off between radiation uniformity, gain, and manufacturability, which is essential for practical THz front-end integration.

3.3.6 FTBR and Gain



(a) **(b)**

Figure 3.7: Simulated performance of SIW stacked antenna for $\sigma = 1.2$ and $\Delta\phi = 0°$ **(a)** FTBR and **(b)** Gain in E- and H-plane at 210 GHz

As illustrated in Figure 3.7**(a)**, simultaneous tuning of both excitation magnitude and phase across the operating frequency band results in front-to-back ratio (FTBR) variations of approximately 10 dB, while maintaining a peak gain of about 10 dB. The optimal radiation performance is observed at the design frequency of 210 GHz, as shown in Figure 3.7**(b)**. In practical implementations, achieving a constant input phase and amplitude across a broad frequency range is inherently challenging due to fabrication tolerances and frequency-dependent dispersion. Nevertheless, independent adjustment of these parameters at discrete frequency points enables precise optimization of the radiation characteristics, ensuring balanced gain and pattern stability across the operational bandwidth.

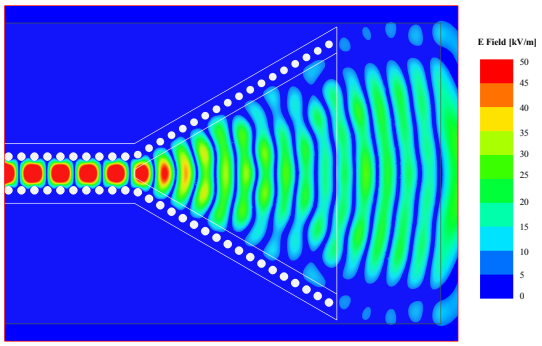
The aperture efficiency of the proposed stacked SIW pyramidal horn antenna was estimated using the standard gain-aperture relationship [192]:

$$\eta_{ap} = \frac{Gc^2}{4\pi A_{phy} f^2} \tag{3.2}$$

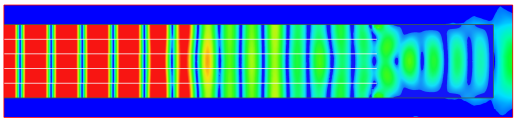
where G is the simulated peak gain in linear scale, c is the speed of light in vacuum, A_{phy} is the physical aperture area, and f is the operating frequency. With a simulated

peak gain of 10 dBi, the resulting aperture efficiency at 210 GHz is approximately 23%. This relatively modest value is consistent with several well-established loss mechanisms in SIW-based horn antennas. First, the TE_{10} mode field distribution in the H-plane follows a cosine amplitude taper across the aperture, resulting in non-uniform illumination and reduced effective aperture utilization compared to an ideal uniform distribution [193]. Second, the multilayer stacked configuration introduces inter-layer phase non-uniformity, leading to partial field cancellation at the aperture [194].

3.3.7 E-field plots



(a)



(b)

Figure 3.8: Simulated R-field at 210 GHz for a stacked SIW horn ($\sigma = 1.2$, $\Delta\phi = 0°$): **(a)** H-plane, **(b)** E-plane along the central axis

Using the optimized excitation configuration, defined by a Gaussian amplitude taper with $\sigma = 1.2$ and uniform phase excitation across all ports, the electric field (E-field) distribution is examined along two principal planes. The H-plane distribution, shown in Figure 3.8**(a)**, corresponds to the conventional H-plane behavior of an SIW horn antenna, whereas the E-plane field distribution is presented in Figure 3.8**(b)**.

In the E-plane, the uniform phase excitation of the five input TE_{10} ports initiates field coupling at the point where the adjacent metallic layer is removed, allowing energy to propagate into the flared aperture. As the wave travels towards the aperture, the field intensity gradually diminishes due to spatial energy spreading within the expanding region of the horn. Near the aperture, the dielectric loading functions as an integrated lens that effectively focuses the radiated energy in the end-fire direction. A complete focusing effect is observed in the H-plane, demonstrating consistent behavior across both principal planes [172].

3.4 Stacked-Layer SIW Feeding Network

3.4.1 Feeding Network Architecture

The proposed SIW horn antenna employs five vertically stacked input ports, each operating in the fundamental TE_{10} mode. The excitation across the ports follows a Gaussian amplitude distribution with a standard deviation of $\sigma = 1.2$ and a uniform phase at the design frequency of 210 GHz. Any deviation from these excitation parameters leads to noticeable degradation in the antenna's performance, including increased SLL, reduced gain, and distortion in beam symmetry.

To enable efficient EM coupling across the stacked layers, a rectangular slot ($l_{\text{slot}} \times w_{\text{slot}}$) is etched into the metallic layer of the feeding SIW. This slot acts as the coupling interface between the feeding network and the radiating horn aperture, ensuring effective power transfer between layers. Furthermore, a metallic short-circuit block is strategically positioned to suppress undesired EM leakage and confine the field propagation along the intended path, thereby maintaining energy efficiency within the multilayer structure [186, 187].

The characteristic impedance of a single SIW feeding port, denoted as Z_{sp} is defined by:

$$Z_{sp} = \frac{\pi h_{sub}}{2w_{eqv}} \cdot \frac{120\pi}{\sqrt{\epsilon_r}\sqrt{1-\left(\frac{\lambda_g}{2w_{eqv}}\right)^2}} \tag{3.3}$$

where h_{sub} represents the substrate thickness of a single port, w_{eqv} is the equivalent SIW width [142], λ_g is the guided wavelength, and ϵ_r denotes the substrate's relative permittivity. For an N-layer stacked structure, the total combined impedance Z_c can be expressed as:

$$Z_c = \frac{Z_{sp}}{N} \tag{3.4}$$

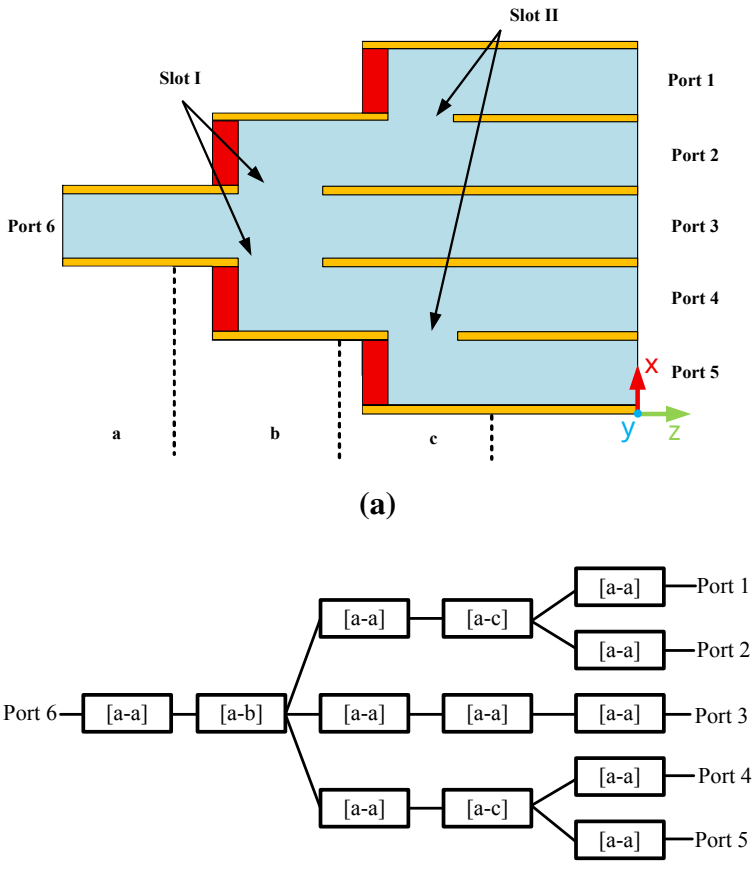


Figure 3.9: Layout of the proposed five-way SIW power divider: **(a)** lateral view of the complete structure and **(b)** simplified recurring section for uniform power distribution.

This relationship ensures impedance matching between the feeding network and the stacked horn structure, thereby minimizing reflection losses and maintaining high transmission efficiency across all ports.

To excite the five-layer stacked SIW horn antenna, a multilayer substrate integrated waveguide (SIW) power splitter was designed. Figure 3.9 illustrates the overall geometry and the corresponding topological model, along with the adopted coordinate convention: the x-axis represents the stacking (thickness) direction, the y-axis defines the SIW width, and the z-axis denotes the longitudinal propagation direction. The input Port 6 excites the SIW in its dominant TE_{10} mode, which propagates along the z-direction through the power-division sections. The first stage, [a–b], performs a $1 \rightarrow 3$ division across the stacked layers, while the second stage, [a–c], realizes an additional $1 \rightarrow 2$ split.

Two coupling apertures, Slot I and Slot II (each of size $l_{\text{slot}} \times w_{\text{slot}}$), are etched into the common metallic planes between adjacent layers. These slots are aligned with one edge along the y-axis transverse to the direction of propagation to intersect the TE_{10} electric field maxima (E_y). This configuration enables efficient vertical coupling of electromagnetic energy between layers while maintaining high mode purity and minimal cross-polarization.

Full-wave electromagnetic simulations were employed to optimize the slot dimensions and placement, ensuring effective power distribution with reflection coefficients below -10 dB at 210 GHz. The optimized configuration achieved good impedance matching, with the inter-port phase deviation among the outputs confined within a few degrees, thereby preserving phase coherence and modal integrity across all layers.

In this architecture, section [a–a] serves as a through-line for single-layer propagation, while sections [a–b] and [a–c] form the core power-splitting stages. The detailed geometrical layouts and corresponding electric field distributions of these sections are presented and analyzed in the subsequent subsections.

3.4.2 [a-b] Section (1-to-3 Splitter)

The [a–b] section represents the first power-division stage of the feeding network and serves as a critical element in the overall SIW power splitter design. Its primary function is to transition electromagnetic (EM) energy from a single-layer SIW input to a three-layer configuration, thereby initiating the vertical power distribution across the stacked structure.

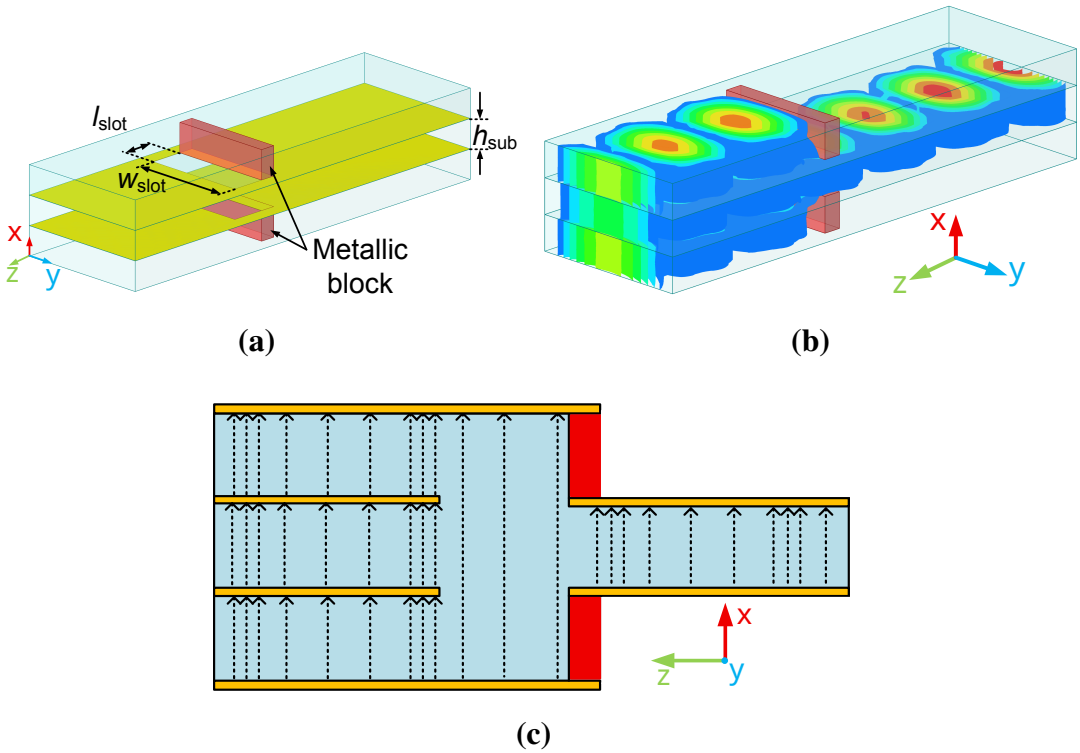


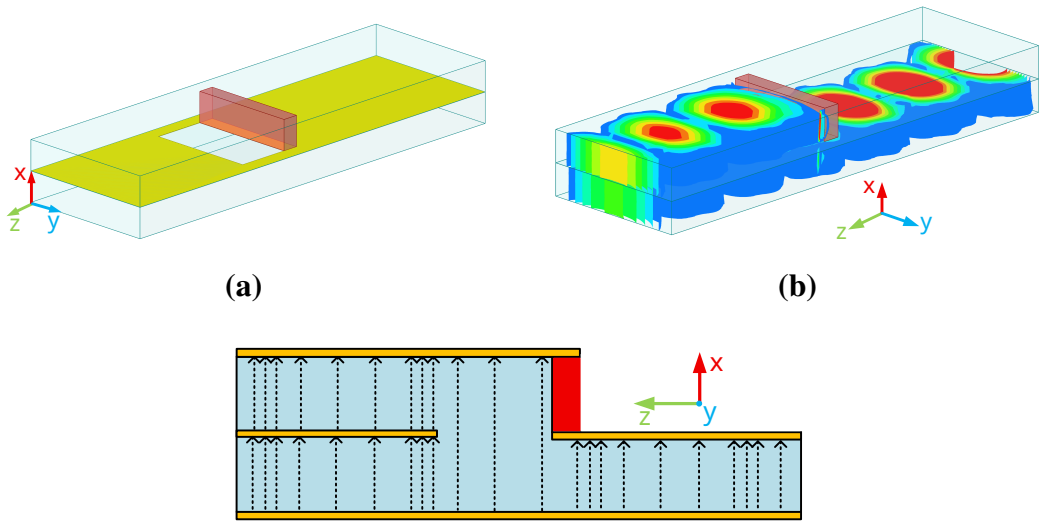
Figure 3.10: Internal structure of the [a–b] region of the proposed SIW power splitter (excluding conductors and vias): **(a)** perspective view, **(b)** electric-field distribution during 1-to-3 TE_{10} transition, and **(c)** conceptual field-line illustration

Figure 3.10**(a)** illustrates the isometric view of the [a–b] splitter, with the external conductors removed to emphasize the internal coupling mechanism. A rectangular slot is etched into the intermediate metallic layers to facilitate controlled coupling of the incident field into the three output layers. A central metallic block is incorporated beneath the slot to confine energy propagation along the intended path and minimize

undesired leakage, effectively serving as an electromagnetic shield.

The slot dimensions: $l_{\text{slot}} \times w_{\text{slot}} = 422, \mu\text{m} \times 422, \mu\text{m}$ in this design, were precisely optimized through full-wave simulation to ensure equal power division and phase balance among the three output ports. The input port, positioned at the right-hand side of Figure 3.10, is excited in the TE_{10} mode. As the wave interacts with the coupling slot, it is efficiently divided into three vertically aligned SIW layers, each supporting a TE_{10} mode with minimal phase deviation. The simulated electric field distribution at 210 GHz, shown in Figure 3.10**(b)**, clearly demonstrates the uniform power transfer and field confinement achieved within the [a–b] section.

3.4.3 [a-c] Section (1-to-2 Splitter)



(a) **(b)**

(c)

Figure 3.11: Internal view of region [a–c] of the SIW splitter (no conductors/vias): **(a)** perspective, **(b)** E-field for 1–2 TE_{10} transition, and **(c)** conceptual field lines

The [a–c] section constitutes the second power-division stage within the multilayer SIW power splitter, where the electromagnetic energy is evenly distributed into two output layers. As shown in Figure 3.11**(a)**, this section follows the three-way division achieved in the [a–b] section and interfaces directly with the stacked SIW horn antenna.

The simulated electric field distribution at 210 GHz, presented in Figure 3.11**(b)**, confirms efficient power transfer with reflection levels maintained below -10 dB throughout the region of interest. The design employs the same slot dimensions used in the [a–b] section ($l_{\text{slot}} \times w_{\text{slot}} = 422, \mu\text{m} \times 422, \mu\text{m}$), ensuring consistent coupling characteristics and maintaining a Gaussian excitation profile with $\sigma = 1.2$ across the output ports. This configuration achieves a uniform phase distribution and balanced amplitude, providing the required excitation conditions for the stacked SIW horn antenna to operate optimally.

3.4.4 Complete Power Splitter

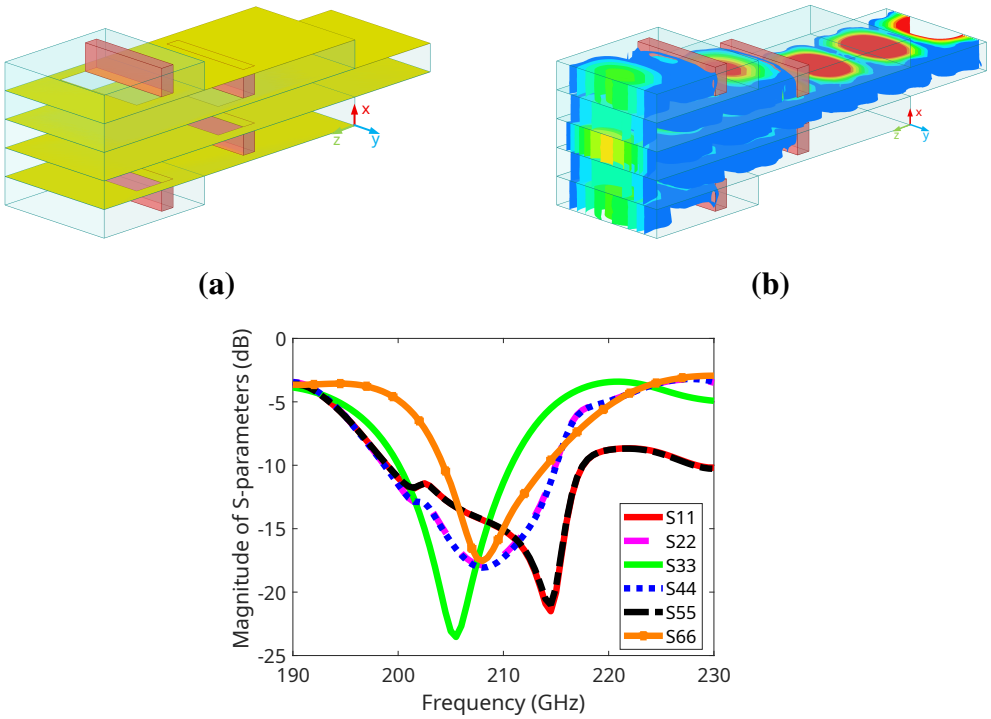


Figure 3.12: Proposed five-way SIW power divider (no conductors/vias): **(a)** perspective, **(b)** E-field (TE_{10} transition), and **(c)** S-parameters

The complete configuration of the multilayer SIW power splitter, along with its simulated electric field distribution and corresponding S-parameters, is shown in Figure 3.12.

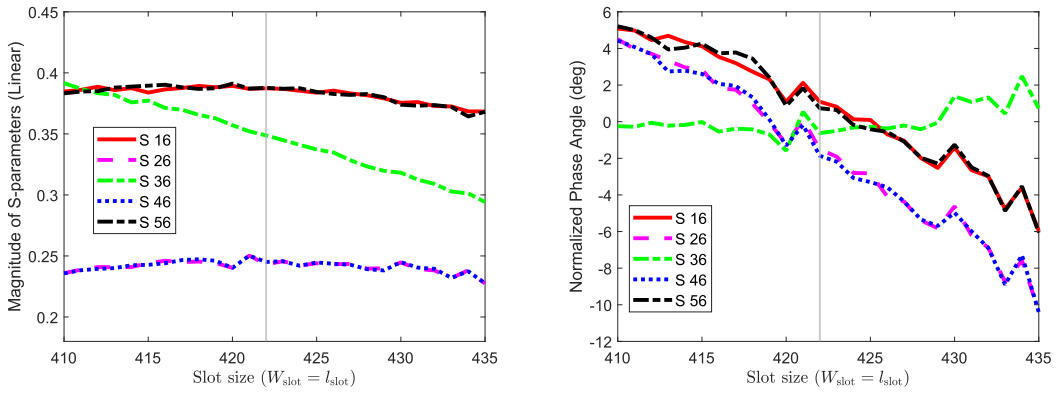
This structure serves as the feeding network for the stacked SIW-based horn antenna. Ideally, the proposed divider suppresses higher-order modes while achieving equal power division and phase balance across all output ports. In practice, minor amplitude deviations may arise due to unequal electrical path lengths or slight impedance mismatches within the internal transitions.

To ensure balanced power distribution, the dimensions of Slot I and Slot II, located in the [a–b] and [a–c] sections, were symmetrically optimized, maintaining identical geometry to preserve phase uniformity. The resulting excitation magnitudes closely follow a Gaussian-like distribution. At the target frequency of 210 GHz, the input port (Port 6) achieves a reflection coefficient below -10 dB, confirming good impedance matching.

The transmitted power levels demonstrate the designed symmetry: Ports 1 and 5 exhibit equal output magnitudes, as do Ports 2 and 4, while Port 3 achieves a power level approximately 3 dB higher than Ports 2 and 4 and about 1 dB lower than Ports 1 and 5. This behavior aligns well with the intended Gaussian amplitude taper ($\sigma = 1.2$), validating the design approach. A quantitative comparison between the simulated and ideal Gaussian excitation values is provided in Table 3.2.

Table 3.2: Comparison of theoretical Gaussian and simulated normalized magnitudes at 210 GHz ($\sigma = 1.2$, normalized to Port $3 = 1.0$, slot dimension $= 422\mu$m $\times$ 422μm)

Port	**Theoretical Gaussian**	**Simulated normalized magnitude**
1	0.25	1.13
2	0.80	0.70
3	1.0	1.0
4	0.80	0.72
5	0.25	1.13



(a) **(b)**

Figure 3.13: Simulated characteristics of the SIW-based feeding network operating at 210 GHz, illustrating **(a)** the variation of transmission magnitude $|S_{n6}|$ with slot dimension and **(b)** the corresponding phase response as a function of slot size.

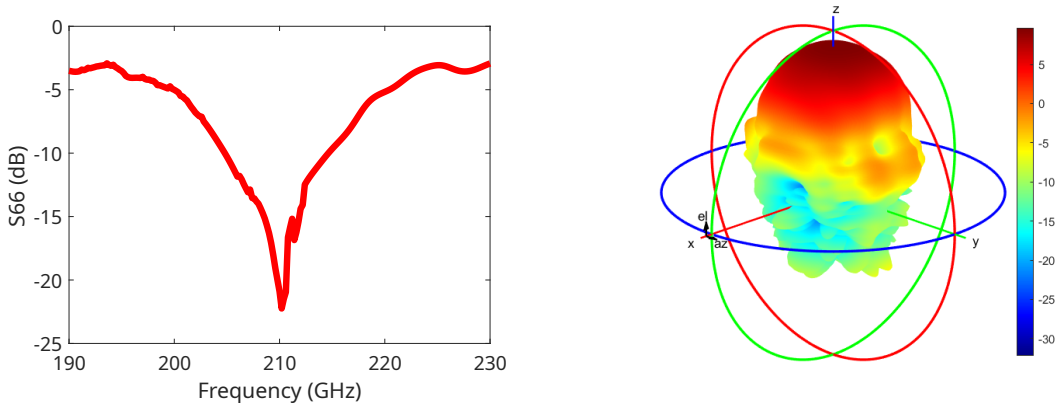
Figure 3.13**(a)** illustrates the simulated S-parameter magnitudes as a function of slot dimensions at 210 GHz. For the optimized slot size of 422 μm $\times$ 422 μm, the excitation magnitudes across the output ports closely follow the target Gaussian profile ($\sigma = 1.2$), with only minor deviations observed at Ports 1 and 5. The corresponding phase distribution, shown in Figure 3.13**(b)**, exhibits a maximum phase deviation of less than 4° across all ports, confirming high phase uniformity.

To assess fabrication tolerance, the slot dimensions were varied by ± 20 μm around the nominal value. The resulting data, presented in Figures 3.13**(a)**–**(b)**, indicate that moderate geometric deviations (≈5%) introduce less than 0.15 dB variation in coupling magnitude and below 5° phase imbalance, both of which fall within standard LTCC and PCB process tolerances.

At the nominal slot dimension, the simulated amplitudes were normalized with respect to the central port (Port 3 = 1.0) and compared with the theoretical Gaussian excitation distribution for $\sigma = 1.2$, as summarized in Table 3.2. Slight amplitude discrepancies at Ports 1 and 5 arise from edge truncation and discontinuities at the boundary ports. Nonetheless, the overall agreement between simulation and theory remains strong, with

deviations within $\pm 10\%$, validating that the slot-coupled feeding network accurately reproduces the intended Gaussian taper across the five stacked ports. These results confirm that the proposed feeding structure is robust against typical fabrication variations and maintains stable excitation performance for practical THz implementations.

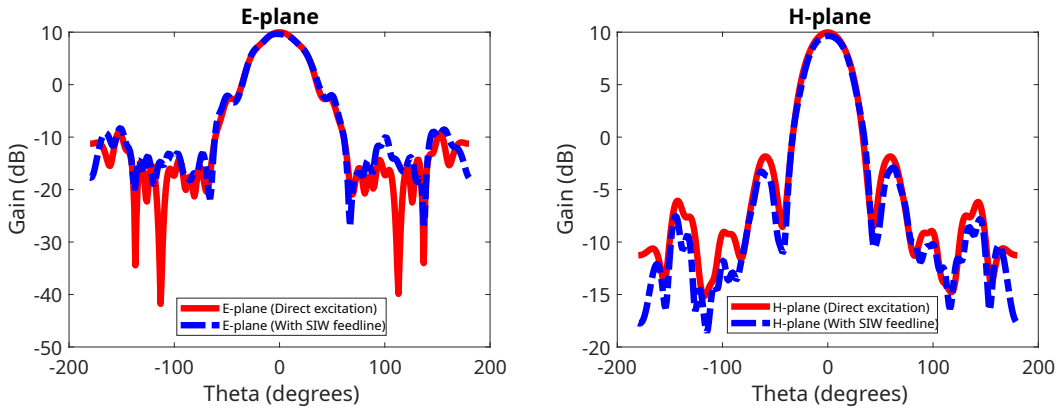
3.5 Integrated Antenna Feeding Network



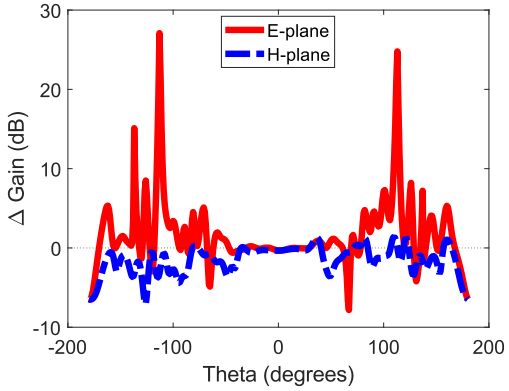
(a) (b)

Figure 3.14: Simulated performance of the integrated SIW horn antenna excited through the designed feeding network: **(a)** S-parameter $|S_{66}|$ and **(b)** 3D radiation pattern illustrating gain distribution at 210 GHz.

The simulated S-parameter response of the complete antenna fed through a single input port is shown in Figure 3.14**(a)**. A clear resonance is observed at 210 GHz, where the reflection coefficient $|S_{66}|$ falls below -10 dB, confirming excellent impedance matching at the intended operating frequency. The corresponding three-dimensional radiation pattern, depicted in Figure 3.14**(b)**, exhibits a well-defined main lobe directed along the end-fire axis, achieving a peak gain of approximately 10 dB. This result validates the effectiveness of the proposed stacked SIW horn antenna and its feeding network in maintaining coherent excitation and efficient radiation at terahertz frequencies.



(a) (b)



(c)

Figure 3.15: Comparison of radiation characteristics between direct excitation and excitation through the SIW feeding network: **(a)** E-Plane, **(b)** H-plane, and **(c)** Differential gain distribution, defined as $\Delta G(\theta) = G_{\text{feedline}}(\theta) - G_{\text{direct}}(\theta)$

The simulated E- and H-plane radiation gain patterns obtained from both direct excitation and excitation through the SIW feed network are depicted in Figure 3.15**(a)**–**(b)**. The corresponding differential gain (ΔG) between these two cases is illustrated in Figure 3.15**(c)**. At an observation angle of approximately $\theta = 41°$, corresponding to the main beam direction in both planes, the gain difference approaches 0 dB, indicating that the SIW feed line effectively preserves the antenna's primary radiation characteristics, including gain and half-power beamwidth (HPBW). Beyond this angular region, slight deviations in ΔG are observed, with the E-plane exhibiting more pronounced

fluctuations than the H-plane. This minor imbalance is primarily attributed to marginal amplitude variations at the outer ports (Ports 1 and 5) of the feeding network, which predominantly influence the E-plane side-lobe levels. All simulations were conducted at an operating frequency of 210 GHz.

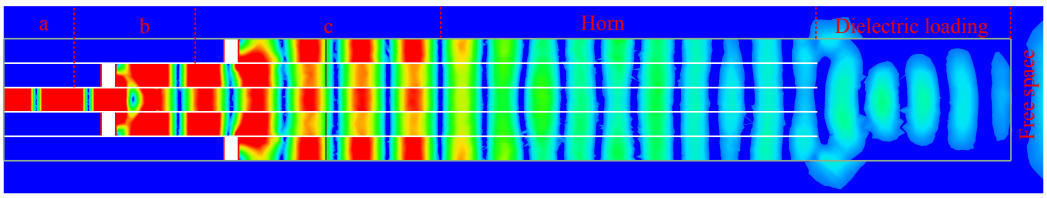


Figure 3.16: E-plane distribution of the electric field for the complete SIW horn antenna integrated with the SIW feeding network, evaluated at 210 GHz.

The electric field distribution of the complete SIW horn antenna excited through the integrated multilayer feeding network is depicted in Figure 3.16. The antenna is energized via a single input port, where the guided wave is progressively divided into five stacked layers through sequential slot-coupling transitions. Each coupling aperture is carefully engineered to achieve the desired excitation magnitude and phase balance across the five outputs. The first slot (Slot I) facilitates a 1-to-3 power division, while the subsequent slot (Slot II) further bifurcates one of these branches, resulting in a total of five ports. The phase and amplitude at each output are finely controlled by adjusting the slot geometry, ensuring high field uniformity and minimal inter-layer phase deviation. As the electromagnetic wave propagates through the multilayer SIW structure, energy is gradually distributed among the layers, producing a controlled reduction in field intensity with depth. The upper horn sections, together with the dielectric loading, act as an electromagnetic lens that collimates the radiated field toward the end-fire direction. This integrated configuration enhances the aperture efficiency and directivity of the antenna while maintaining compactness and compatibility with planar THz front-end architectures.

3.6 Discussion

The proposed stacked SIW-based pyramidal horn antenna operating at 210 GHz demonstrates strong potential for emerging terahertz (THz) applications, including non-invasive imaging systems, high-resolution sensing, and short-range, high-capacity wireless communication links. The vast available bandwidth at THz frequencies makes this antenna particularly suitable for sixth-generation (6G) front-haul and backhaul networks, as well as ultra-high-speed wireless backhaul systems, where highly directive beams can effectively mitigate atmospheric attenuation [195].

Moreover, the antenna's compact and multilayer architecture allows integration into radar-type integrated sensing and communication (ISAC) platforms [196]. Minor modifications to the feeding network, such as achieving tighter inter-port phase control, incorporating compact phase shifters for beam steering and shaping [197], integrating duplexing mechanisms with radome protection, and introducing stronger amplitude tapering for improved side-lobe suppression, can enable its deployment in multifunctional THz transceiver systems.

At 210 GHz, several fabrication-related challenges become significant. The foremost among these are inter-layer alignment accuracy, which is essential for maintaining phase coherence across the stacked E-plane apertures; slot etching precision, as the coupling slots primarily govern both the amplitude taper and phase balance among layers; and via-fence integrity, since deviations in via diameter, pitch, or metallization quality directly influence SIW wall continuity and confinement. To mitigate these issues, the proposed geometry adheres strictly to standard PCB and LTCC design constraints. Specifically, the slot dimensions (422μm × 422μm) and via diameter-to-pitch ratio ($d_{\text{via}}/p_{\text{via}} = 150/250\mu$m) were chosen to fall well within conventional fabrication limits.

As shown in Figure 3.13, both the reflection and phase characteristics exhibit strong

stability around the nominal slot dimension, confirming that the design is tolerant to minor fabrication variations. The slot size, being the most sensitive parameter, was centred within the process tolerance range to ensure amplitude and phase symmetry. Alignment precision is maintained using full-panel fiducials and balanced lamination during stack-up, while via fences follow standard drilling and metallization protocols to preserve the effective SIW width (S_{siw}) and suppress leakage.

Although this work primarily reports simulated results, all geometric and material parameters were deliberately selected to comply with existing SIW/LTCC manufacturing capabilities. Looking ahead, a potential fabrication pathway for the proposed structures involves established micro-fabrication techniques such as multilayer micro-machining or advanced lithography-based processes. In particular, the stacked SIW structure could be fabricated by forming individual substrate layers using standard photolithography and metallization processes, followed by precise layer alignment and bonding techniques such as wafer bonding or adhesive bonding. The via structures, which are critical to the SIW formation, could be realized through deep reactive ion etching (DRIE) or laser micro-machining, followed by metal filling or plating. These fabrication approaches are compatible with modern semiconductor and MEMS manufacturing processes and provide a feasible pathway for realizing the proposed THz antenna structure, and will be considered as part of future work.

3.7 Chapter Summary

This chapter presented the design and simulation of a stacked Substrate Integrated Waveguide (SIW) pyramidal horn antenna optimized for 210 GHz operation. The proposed multi-layer configuration transforms a conventional planar SIW into a compact three-dimensional structure that achieves symmetric radiation in both principal planes while maintaining compatibility with standard LTCC and PCB fabrication processes.

Through parametric optimization of the number of layers, dielectric loading, and Gaussian amplitude excitation, the antenna achieved a peak gain of approximately 10 dB with nearly equal HPBWs of 41° in the E- and H-planes.

A five-layer SIW power-divider network was developed to realize Gaussian-tapered amplitude excitation with uniform phase distribution. The integrated structure exhibited low reflection ($|S| < -10$ dB), stable phase alignment, and strong tolerance to fabrication variations. Overall, the proposed antenna demonstrates a compact, manufacturable, and high-performance solution for THz front-end systems, offering promising potential for high-speed communications, sensing, and imaging applications.

Chapter 4

Mode Converter Designs for Planar Terahertz Applications

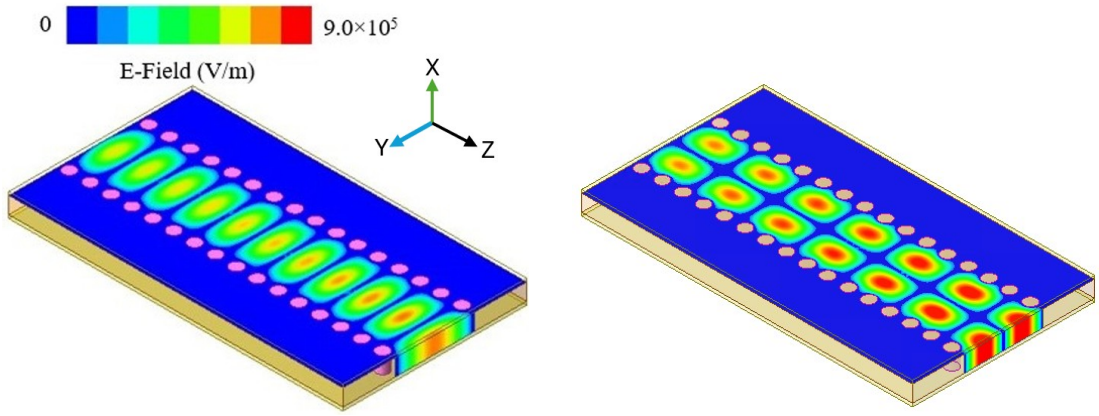
The development of the pyramidal SIW horn antenna presented in Chapter 3 demonstrated the potential of SIW structure for achieving high gain and compact THz radiation. However, the performance of such an antenna is strongly dependent on the excitation mechanism and the supported waveguide modes. In particular, the excitation of higher-order SIW modes can enable improved field distribution, bandwidth enhancement, and radiation characteristics. To address this, the Chapter 4 focuses on the design of an efficient RWG TE_{10} to SIW TE_{20} mode converter, which serves as a critical structure for exciting the desired SIW modes and further advancing the performance of SIW-based THz antennas.

4.1 Background

The RWG-to-SIW converter plays a key role in enhancing the RF circuit integration by enabling circuit miniaturization, ensuring compatibility with measurement equipment,

simplifying fabrication, and allowing smooth mode conversion across different technologies. Although SIWs and RWGs differ in structure, the SIWs preserve essential RWG features such as high-Q factor, internal field distribution, and cutoff frequency, while also providing advantages like compact size, low cost, and ease of integration. These attributes make the converter effective for both planar designs [160, 163, 171] and right-angle configurations [158, 160].

4.2 Modes of Propagation in SIW



(a) (b)

Figure 4.1: Electric field distributions of SIW modes

The SIW is a planar transmission line technology specifically developed for high-density millimeter and THz circuits and antenna systems. It can be regarded as a dielectric-based modification of the conventional RWG, where rows of metallized via holes embedded in a dielectric substrate, bounded by metallization on the top and bottom surfaces, emulate the conducting walls of an RWG. While employing a substrate with a higher relative permittivity (ϵ_r) enhances EM field confinement, it also introduces increased transmission losses [130, 143].

The SIW design methodology generally relies on iterative full-wave EM simulations

combined with parameter optimization to achieve performance targets. Closed-form equations for the effective width of SIWs, provided in [142], can be used to generate initial dimensions and accelerate the optimization process. Since the guided propagation modes in an SIW are analogous to those in an RWG, the same cutoff frequency formulation is applicable [198].

The associated electric field distribution for SIW in TE_{10} and TE_{20} modes is shown in Figure 4.1. According to classical waveguide theory, the field components for a TE_{mn} mode in an SIW can be expressed as:

$$E_x = \frac{j\omega\mu n\pi}{k_c^2 b} A\cos\frac{m\pi x}{a}\sin\frac{n\pi y}{b}e^{-j\beta z} \tag{4.1}$$

$$E_y = \frac{-j\omega\mu m\pi}{k_c^2 a} A\sin\frac{m\pi x}{a}\cos\frac{n\pi y}{b}e^{-j\beta z} \tag{4.2}$$

where a and b denote the waveguide width and height, respectively. For a transverse electric (TE) mode, the electric field has no longitudinal components along the propagation axis, i.e., the z-axis. Consequently, the field is entirely transverse in nature, and the longitudinal electric field component vanishes ($E_z = 0$);

$$H_x = \frac{j\beta m\pi}{k_c^2 a} A\sin\frac{m\pi x}{a}\cos\frac{n\pi y}{b}e^{-j\beta z} \tag{4.3}$$

$$H_y = \frac{j\beta n\pi}{k_c^2 b} A\cos\frac{m\pi x}{a}\sin\frac{n\pi y}{b}e^{-\beta z} \tag{4.4}$$

$$H_z = A\cos\frac{m\pi x}{a}\cos\frac{n\pi y}{b}e^{-j\beta z} \tag{4.5}$$

$$\beta = \sqrt{k^2 - k_c^2}\ ,\ k = \omega\sqrt{\mu\epsilon_o\epsilon_r}\ ,\ k_c = \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{4.6}$$

For a SIW operating in the TE_{20} mode (with mode indices $m = 2$, $n = 0$), the solution

of Equations (4.1) – (4.5) yields the following expression:

$$E_y = -A_{20}\frac{j\omega\mu w_{\text{siw}}}{2\pi}\sin\left(\frac{2\pi}{w_{\text{siw}}}x\right)e^{-j\beta z} \tag{4.7}$$

$$H_x = A_{20}\frac{j\beta w_{\text{siw}}}{2\pi}\sin\left(\frac{2\pi}{w_{SIW}}x\right)e^{-j\beta z} \tag{4.8}$$

$$H_z = A_{20}\cos\left(\frac{2\pi}{w_{\text{siw}}}x\right)e^{-j\beta z} \tag{4.9}$$

$$E_x = E_z = H_y = 0 \tag{4.10}$$

where ω, A_{20}, and w_{siw} represent the angular frequency, the amplitude coefficient for the TE_{20} mode, and the width of the SIW, respectively. Under this condition, the electric field exhibits no components along the x- and z-axes, while the magnetic field has no component along the y-axis.

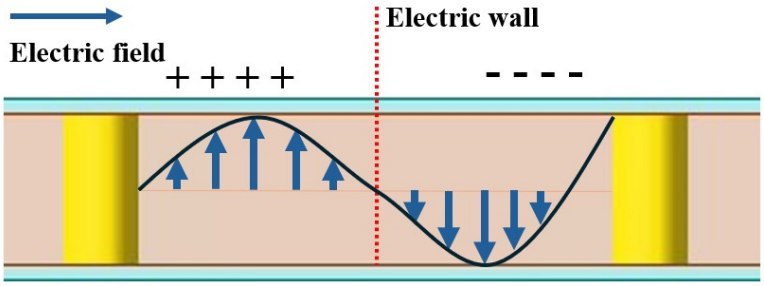


Figure 4.2: E-field lines in TE_{20} SIW mode

From Equation (4.7), it follows that when $x = w_{\text{siw}}/2$, the y-directed electric field component becomes zero. This indicates that, in the TE_{20} mode, the electric field distribution is symmetric about the line $x = w_{\text{siw}}/2$, with equal magnitudes but opposite polarities on either side. Consequently, this symmetry plane can be interpreted as an electric wall or a virtual ground [164]. Leveraging this property, electromagnetic energy in the TE_{20} mode can be efficiently coupled into the SIW, while simultaneously suppressing the dominant TE_{10} mode through appropriate excitation techniques.

4.3 Zigzag Antenna Based RWG TE_{10} to SIW TE_{20} Mode Converter

The zigzag antenna is adopted as the coupling element because its alternating arm geometry introduces controlled current phase reversals. Compared with straight dipole/slot couplers, the segmented zigzag path provides an effectively longer electrical length in a compact footprint and multiple in-phase radiating segments, which together enhance bandwidth and coupling efficiency to the aperture slot [199, 200]. This choice is planar-process-friendly and aligns with monolithic THz integration. The detailed geometry and parametric optimization of the zigzag antenna are presented in Sections 4.3.1.2 and 4.3.3.

4.3.1 Designing the Mode Converter

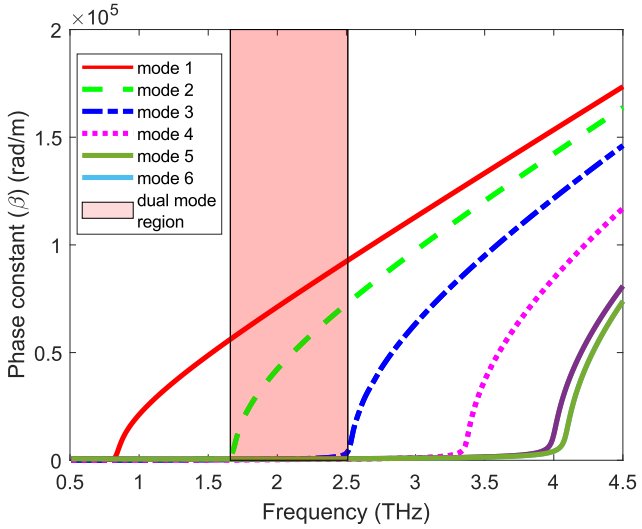


Figure 4.3: Simulated dispersion curve of SIW

For the optimized geometry considered, the SIW width (w_{siw}) was determined as 95μm, with via dimeter (d_{via}) as 25μm, via pitch (p_{via}) as 25μm, and substrate thickness (h_{sub}) as 20μm. The substrate material was polyimide, characterized by a relative dielectric

constant (ϵ_r) of 3.5 and a dielectric loss tangent ($\tan\delta$) of 0.008. Additional design constraints governing the via diameter-to-pitch ratio are provided in [130].

Figure 4.3 illustrates the supported SIW modes, where the frequency range of $1.66 - 2.5$ THz corresponds to the dual-mode regime, permitting the simultaneous excitation and propagation of both TE_{10} and TE_{20} modes.

4.3.1.1 Geometry Overview

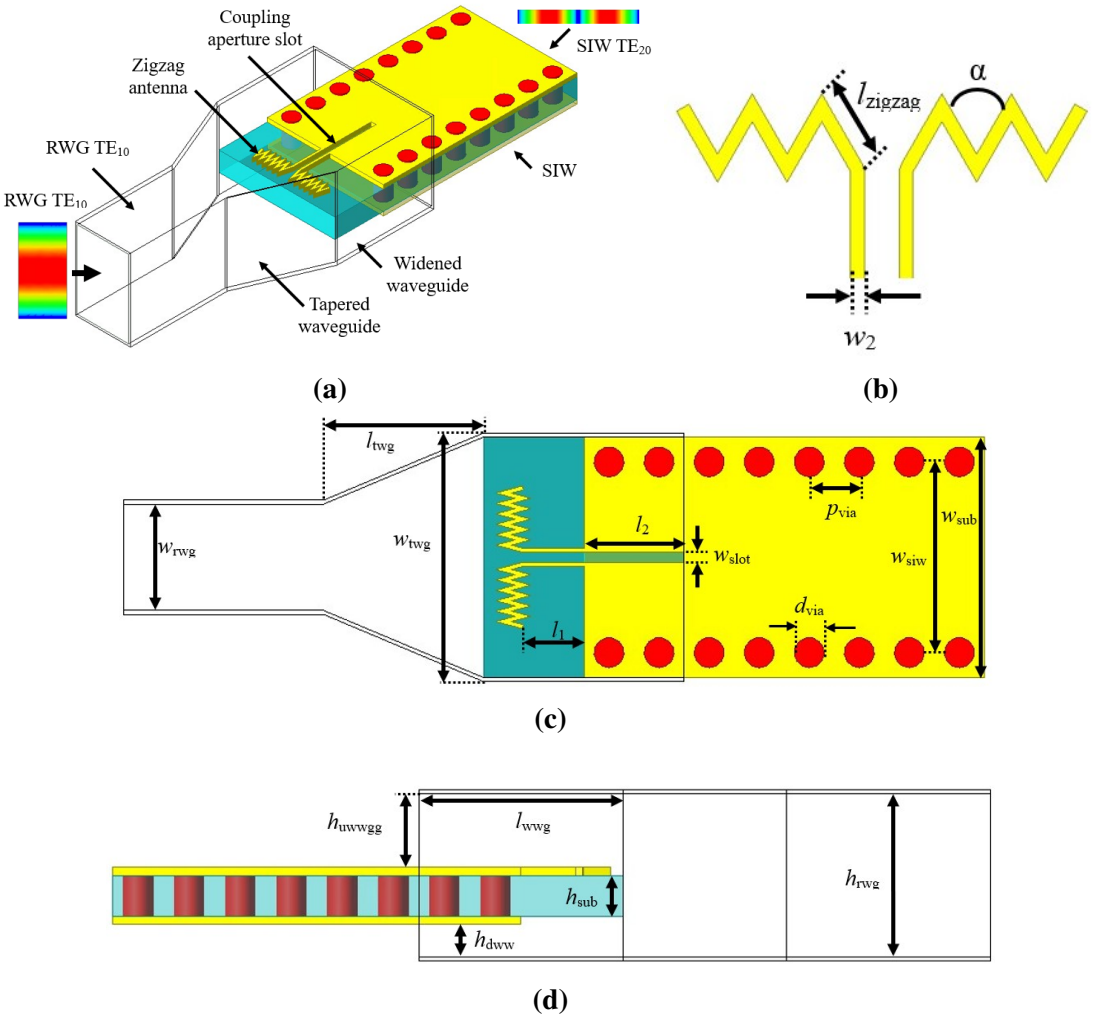


Figure 4.4: Proposed RWG TE_{10} to SIW TE_{20} mode converter **(a)** isometric view, **(b)** zigzag antenna, **(c)** top view, and **(d)** side view.

The complete configuration of the proposed mode converter is illustrated in Figure 4.4. It comprises a standard RWG (WR-0.43), a tapered RWG section, a broadened waveguide, a zigzag antenna, an aperture-coupling slot, and a single polyimide substrate sandwiched between metallized top and bottom layers, with via fences along the sidewalls. The top metallization incorporates both the centre-fed zigzag antenna and the aperture slot, which extend into the tapered RWG. Within this region, the incident y-polarized TE_{10} mode of the RWG is transformed into a z-polarized TE_{20} mode [135].

4.3.1.2 Zigzag Antenna Design

The first stage of mode conversion occurs at the junction of the extended RWG and the centre-fed zigzag antenna. Unlike a conventional dipole antenna with equal arm lengths, the zigzag antenna is employed due to its greater design flexibility, enabling independent adjustment of arm lengths as well as the inter-arm angle. This flexibility facilitates the excitation of standing waves along the antenna arms, where alternating current flows through the angled segments. These alternating currents act as multiple radiating sources, producing constructive interference that enhances radiation efficiency, energy coupling, and directivity [199]. Additionally, the zigzag geometry effectively extends the electrical length of the antenna without increasing its physical footprint, making it highly suitable for compact, high-frequency mode conversion structures.

4.3.1.3 Mode Conversion Process

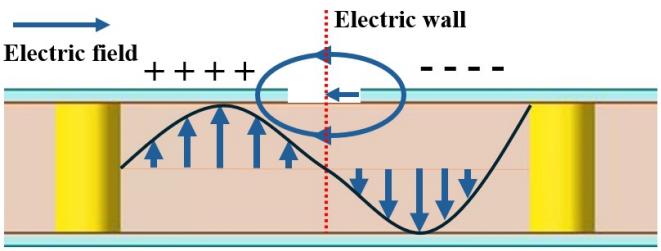


Figure 4.5: E-field lines in the quasi-slotline mode

Under the conditions of impedance matching, the incident EM waves couple into the zigzag antenna at its resonance frequency, which is primarily governed by the arm length (l_{zigzag}) and the inter-arm angle (α). Once coupled, the zigzag antenna extracts energy from the incoming TE_{10} mode of the RWG and transfers it transversely to the aperture-coupling slot. The slot excites a quasi-slotline (odd) mode, characterized by an e-field distribution of the SIW TE_{20} mode, as illustrated in Figure 4.5. Both Figures 4.2 and 4.5 exhibit a symmetric field pattern across the x-y plane, equivalent to an electric wall boundary.

As a result, efficient EM coupling is achieved between the quasi-slotline mode and the SIW TE_{20} mode [158, 164, 165]. Therefore, the zigzag antenna plays a pivotal role in receiving the incident RWG energy, converting it into the odd-mode excitation of the slotline, and subsequently enabling strong coupling into the TE_{20} modes of the SIW, thereby realizing the desired mode conversion.

4.3.2 Simulated E-field Results

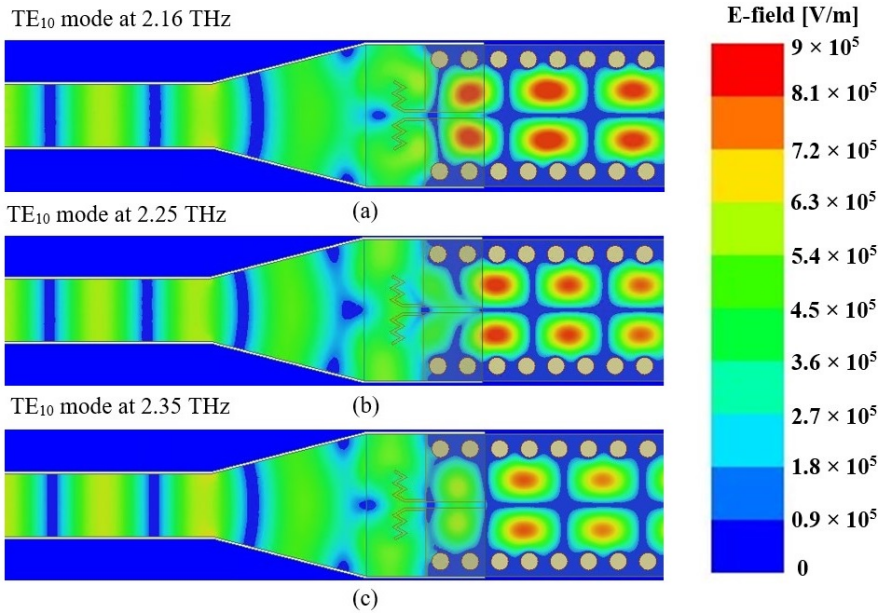


Figure 4.6: Simulated E-field distribution of the RWG-to-SIW mode converter, showing TE_{10} - TE_{20} mode transformation at: **(a)** 2.16 THz, **(b)** 2.25 THz, and **(c)** 2.35 THz.

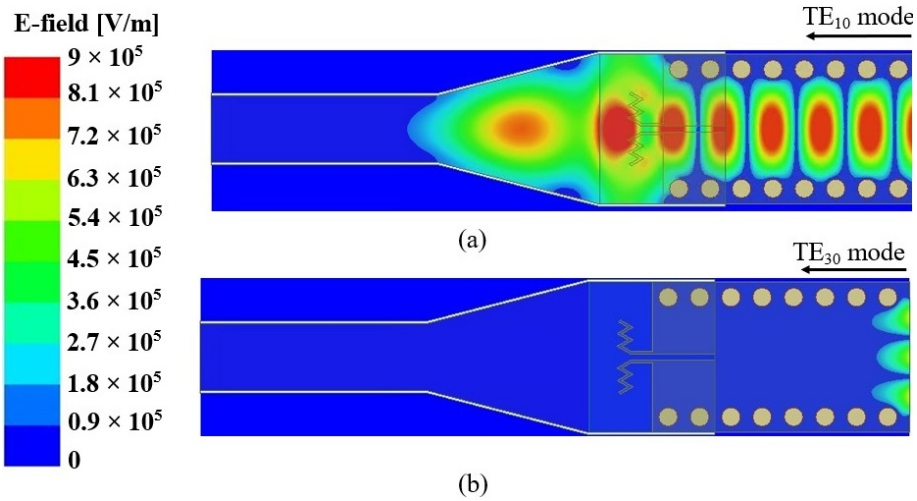


Figure 4.7: Simulated E-field distribution of the proposed converter at 2.25 THz, showing the SIW operating in: **(a)** TE_{10} mode and **(b)** TE_{30} mode.

The performance of the proposed RWG-to-SIW mode converter was evaluated through full-wave simulations, with the e-field distributions shown in Figures 4.6 and 4.7. Figure 4.6 illustrates the conversion of the RWG TE_{10} mode to the SIW TE_{20} mode over a wide frequency range from 2.16 to 2.35 THz. Although the SIW supports a dual-mode region between 1.6 and 2.5 THz (Figure 4.3), the converter selectively excites only the TE_{20} mode, effectively suppressing the dominant TE_{10} mode of the SIW.

Figure 4.7 further demonstrates the mode-selective behavior of the converter at 2.25 THz. when the SIW operates in the TE_{10} mode, no coupling occurs with the RWG. For the TE_{30} mode, propagation is prohibited, as the operating frequency lies below the mode's cutoff. These results confirm the converter's ability to isolate the TE_{20} mode while attenuating unwanted modes.

The field distributions reveal that the TE_{10} mode of the RWG is transformed into a quasi-slotline mode with an odd-mode e-field across the aperture, enabled by the resonance of the zigzag antenna. The discontinuity in the tangential e-field suppresses the excitation of even modes, in accordance with Maxwell's boundary conditions [201]. Consequently, the TE_{20} mode of the SIW exhibits an electric field profile (Figure 4.2)

closely matching that of the odd-mode slotline (Figure 4.5). In configurations such as the conductor-backed slotline (CBSL), even modes can be generated [202]; however, these correspond to the TE_{20} mode of the SIW [164], thereby preserving the suppression of the TE_{10} mode in the dual-mode frequency region.

This analysis confirms that the proposed converter not only facilitates efficient TE_{10} to TE_{20} mode conversion but also ensures mode selectivity, enabling robust operation within the SIW's dual-mode regime.

4.3.3 Back-to-Back RWG TE_{10} to RWG TE_{10} Converter

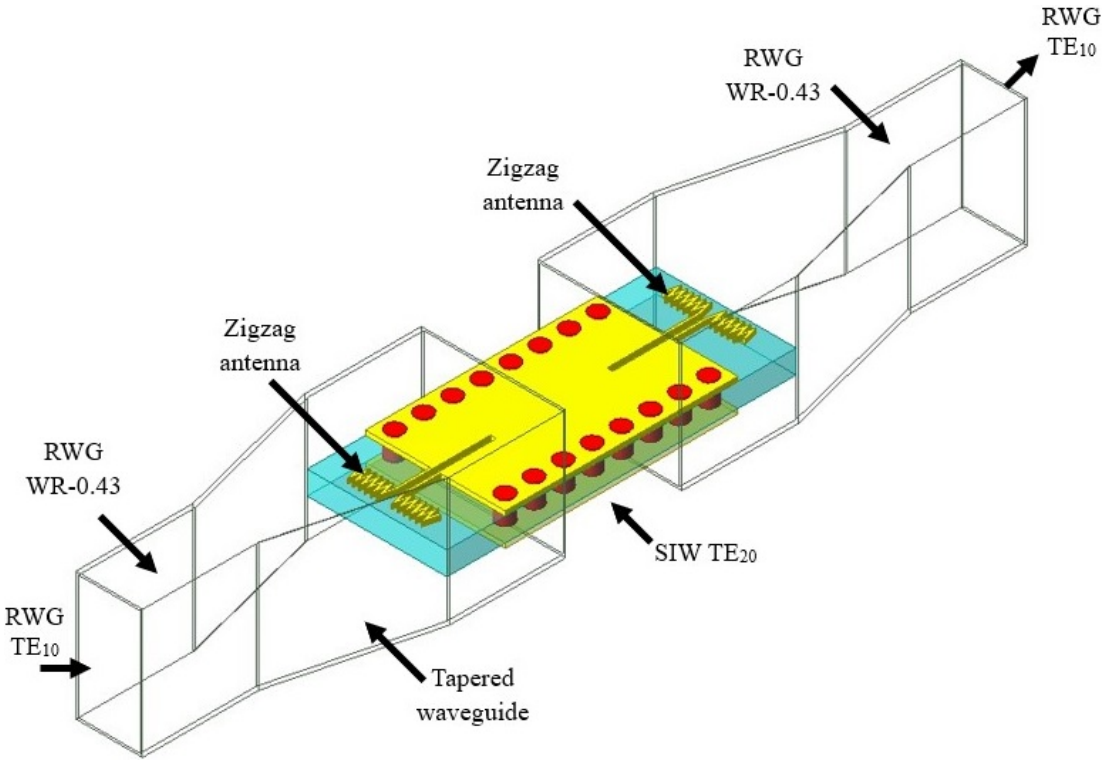
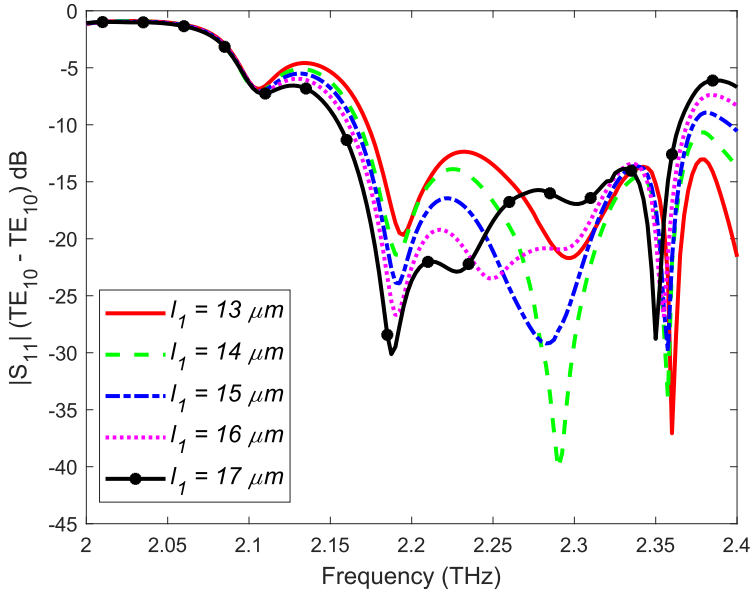


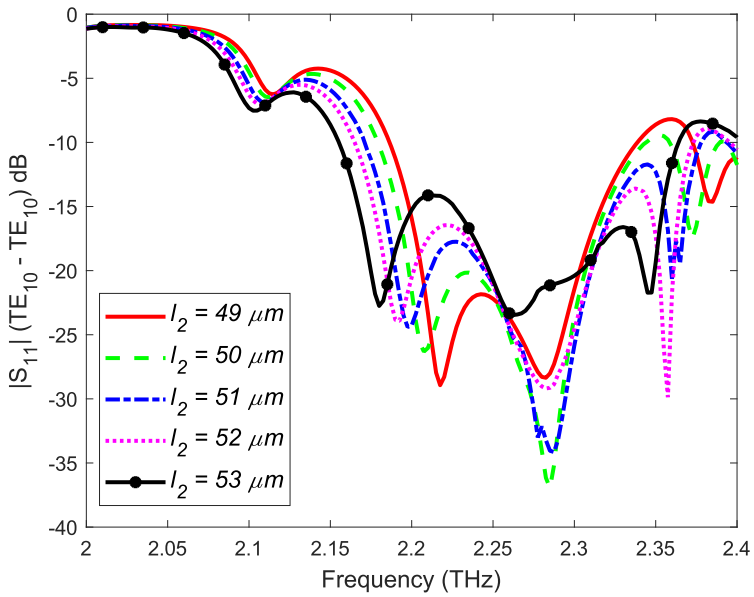
Figure 4.8: Isometric view of the proposed back-to-back TE_{10}–TE_{10} mode converter

As illustrated in Figure 4.8, a complete back-to-back mode converter was developed. In this structure, the TE_{10} mode guided within the RWG is first transformed into the TE_{20} mode of the SIW and then reconverted back into the TE_{10} mode of the RWG. This

back-to-back configuration not only demonstrates the feasibility of the proposed mode conversion mechanism but also serves as a setup for extracting the S-parameters.

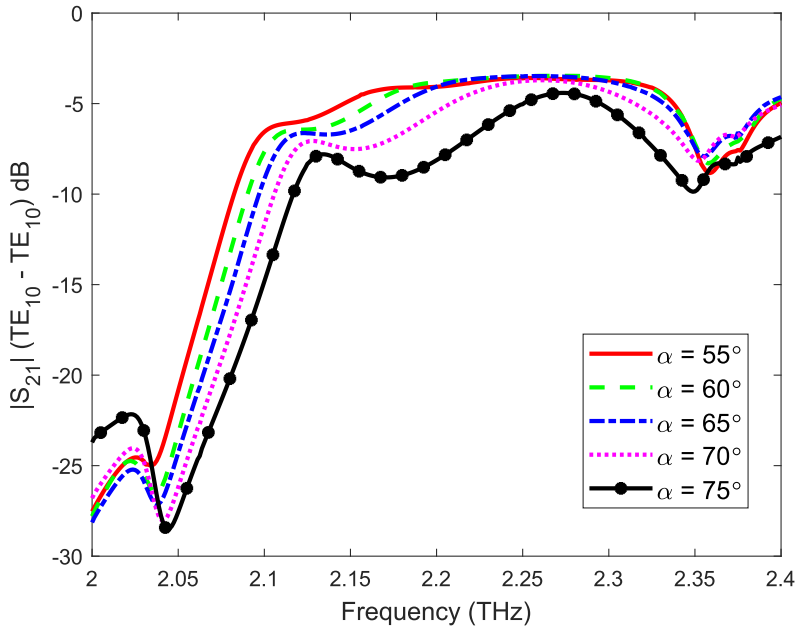


(a)

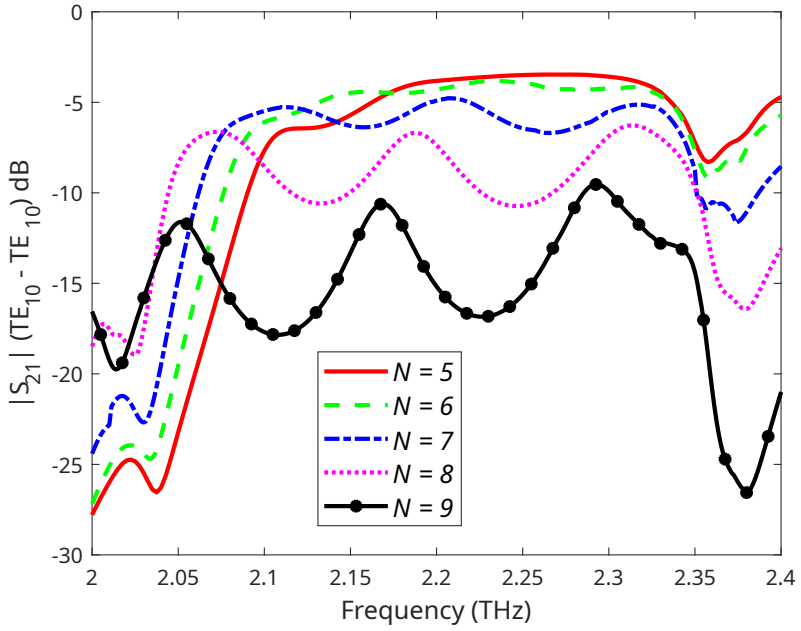


(b)

Figure 4.9: Simulated $|S_{11}|$ (TE_{10} - TE_{10}) of the back-to-back converter at different parameter values: **(a)** l_1 and **(b)** l_2.



(a)



(b)

Figure 4.10: Simulated $|S_{21}|$ (TE_{10} - TE_{10}) of the back-to-back converter at different parameter values: **(a)** l_1 and **(b)** l_2.

The simulated performance of the proposed back-to-back mode converter is presented

in Figures 4.9 and 4.10, highlighting the impact of four key design parameters: l_1, l_2, the zigzag antenna angle (α), and the number of zigzag arms (N). The overall structure has a physical length of $380\mu m$ and employs a polyimide substrate with a dielectric constant (ϵ_r) of 3.5 and a loss tangent ($\tan\delta$) of 0.008. As shown in Figure 4.9, the reflection coefficient ($|S_{11}|$) was evaluated for varying values of l_1 and l_2. These parameters were tuned to achieve proper impedance matching across the operating bandwidth. ensuring stable performance around the center frequency.

Similarly, the zigzag antenna configuration (Figure 4.4**(b)**) was analyzed in terms of its number of arms (N) and arm angle (α). From Figure 4.10, it is evident that the number of arms has a more significant influence on the transmission coefficient $|S_{21}|$ of TE_{10} - TE_{10} converter than the arm angle. Consequently, minimizing insertion loss was primarily achieved by reducing the number of zigzag arms. Following design, simulation, and subsequent optimization, the finalized dimensional parameters of the proposed mode converter are summarized in Table 4.1

Table 4.1: Geometrical design parameters of the proposed mode converter

Parameters	w_{rwg}	h_{rwg}	l_{twg}	l_{wwg}	h_{uwwg}	h_{dwrwg}
Values (μm)	53	106	130	100	57.5	29
Parameters	h_{sub}	p_{via}	d_{via}	w_{slot}	w_{siw}	w_{sub}
Values (μm)	20	25	14	5	95	120
Parameters	l_1	l_2	w_2	l_{zigzag}	α	w_{twg}
Values (μm)	17	53	2	10	55°	57

4.3.4 Equivalent Circuit model

For an RWG operating in the fundamental TE_{10} mode, the characteristic impedance can be expressed as the product of the intrinsic wave impedance and the aspect ratio of the wave-guide's short to long side [203], as formulated as:

$$\mathrm{Z}_{\mathrm{rwg}} = \frac{w_{\mathrm{rwg}}}{h_{\mathrm{rwg}}} Z_{rwg}^{\mathrm{TE10}} \tag{4.11}$$

where w_{rwg}, h_{rwg}, and $Z_{\mathrm{rwg}}^{\mathrm{TE10}}$ denote the waveguide width, height, and wave impedance, respectively. By analogy, the characteristic impedance of the widened waveguide and the SIW can be expressed as:

$$\mathrm{Z}_{\mathrm{wwg}} = \frac{w_{\mathrm{wwg}}}{h_{\mathrm{rwg}}} \mathrm{Z}_{\mathrm{rwg}}^{\mathrm{TE10}} \tag{4.12}$$

$$\mathrm{Z}_{\mathrm{siw}} = \frac{h_{\mathrm{sub}}}{w_{\mathrm{eqv}}} \mathrm{Z}_{\mathrm{siw}}^{\mathrm{TE10}} \tag{4.13}$$

where w_{wwg}, h_{wwg}, and $Z_{\mathrm{rwg}}^{\mathrm{TE10}}$ correspond to the width, height, and wave impedance of the widened waveguide, while h_{sub}, w_{eqv}, and $Z_{\mathrm{siw}}^{\mathrm{TE10}}$ represent the substrate thickness, equivalent width, and wave impedance of the SIW, respectively. Further details on the derivation of wave impedance for both RWG and SIW can be found in [204].

It should be noted that the widened waveguide exhibits a higher characteristic impedance than the conventional RWG (Equation 4.12). The inclusion of a tapered transition section between these structures ensures smooth impedance matching and minimizes reflections by gradually redistributing the wave impedance and electric field between the RWG and widened waveguide [205–207].

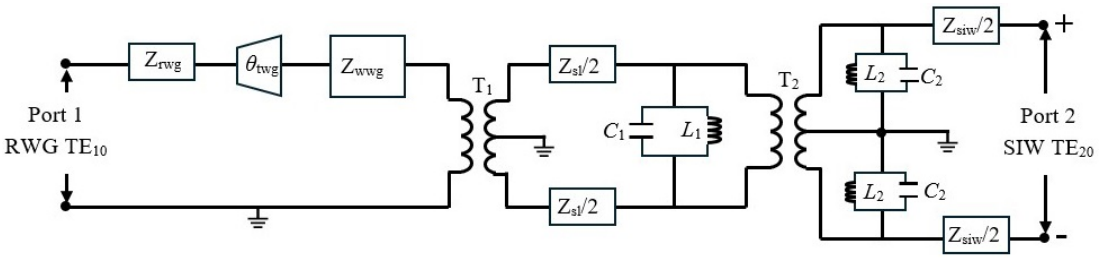


Figure 4.11: Equivalent lumped-element model for the RWG–SIW mode converter operating from TE_{10} to TE_{20}

The equivalent circuit model of the proposed converter, shown in Figure 4.11, incorporates lumped reactive elements, characteristic impedance, and coupling transformers to represent the transition. Equivalent circuit representations of similar transitions have been reported previously, including microstrip-to-waveguide converters [208], slot-line to double-sided parallel-strip line transition in magic-T structures [209], slot-line to SIW transitions [165], and RWG-to-SIW transitions [164].

In the present design, transformer T_1 models the coupling between the RWG and the aperture slotline, while transformer T_2 accounts for the coupling between the slotline and the SIW operating in TE_{20} mode. In this mode, the electric field vanishes along the central symmetry plane (x-y plane), which behaves as a virtual ground. The field distribution exhibits equal magnitudes but opposite directions on either side of this plane (Figure 4.2), analogous to a differential pair in circuit terms. Thus, the slotline and the TE_{20} mode of the SIW can be regarded as differential ports.

The lumped elements in the equivalent circuit capture the reactive energy storage in the transition. Specifically, C_1 and L_1 correspond to the capacitive and inductive contributions arising from the slotline geometry, primarily governed by its width (w_{slot}) and length (L_2) [165]. Similarly, C_2 and L_2 account for capacitive discontinuities and magnetic energy storage within the SIW, influenced by the metallic via array during the conversion from slotline excitation to the TE_{20} mode [164].

Table 4.2: Equivalent circuit elements and their physical interpretations in the proposed RWG–SIW mode converter.

Circuit Element	**Physical Interpretation**
T_1	Coupling transformer representing the energy transfer between the RWG and the aperture slotline.
T_2	Coupling transformer modeling the transition between the slotline and the SIW operating in TE_{20} mode.
C_1	Capacitive effect due to the discontinuity across the slotline, primarily dependent on slot width (w_{slot}) and length (l_2).
L_1	Inductive effect associated with current flow along the slotline, also governed by slot geometry.
C_2	Capacitive energy storage within the SIW, originating from discontinuities during the slotline-to-SIW TE_{20} transition.
L_2	Inductive effect corresponding to magnetic energy storage due to the metallic via array in the SIW.

4.3.5 Design Guidelines for Mode Converter

The fundamental operating principle of the proposed RWG-SIW mode converter is based on impedance matching between the two waveguide structures and the transformation of the unbalanced RWG TE_{10} port into a balanced differential SIW TE_{20} port. This dual requirement increases the complexity of the circuit design, as accurately relating the structural dimensions to the equivalent electrical components is non-trivial. Consequently, a combined approach of theoretical analysis and numerical optimization was adopted to realize effective mode conversion.

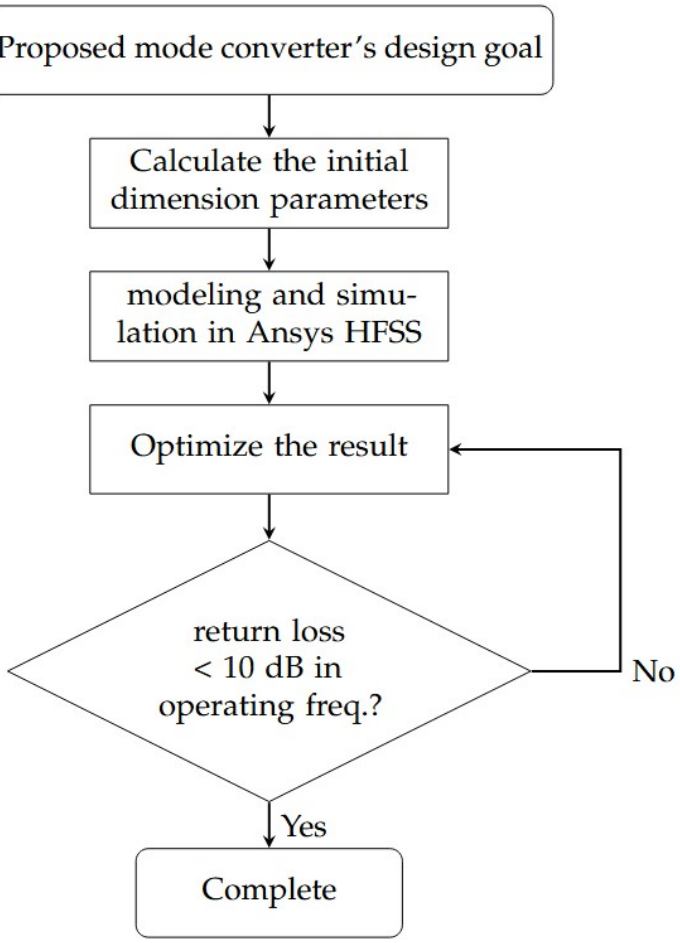


Figure 4.12: Flowchart for the design process of the proposed RWG TE_{10} to SIW TE_{20} mode converter.

Consequently, a combined approach of theoretical analysis and numerical optimization was adopted to realize effective mode conversion. The overall design methodology is summarized in the flow chart presented in Figure 4.12.

The primary design objective was to enable reliable conversion from the TE_{10} mode of the RWG to the TE_{20} mode of the SIW. The dimensions of the RWG were selected in accordance with the IEEE WR-0.43 standard [210]. The determination of the tapered waveguides electrical length θ_{twg} follows the approach detailed in [207], which ensures a smooth impedance transition between sections. For the initial SIW parameters, the theoretical analysis provided in Section 2.3 was used, where the formulas are directly

dependent on the targeted frequency band.

The zigzag antenna dimensions were chosen to guarantee resonance within the operational frequency range, thereby maximizing energy transfer into the aperture slot. The slot length, l_2, was initially set to half of the guided wavelength, while its width, w_{slot}, was selected to be sufficiently narrow to allow the electric field to penetrate across the symmetry plane.

The complete model was then implemented in the Ansys High-Frequency Structure Simulator (HFSS) environment for full-wave electromagnetic analysis. To achieve the desired design specifications, namely a return loss below 10 dB and effective impedance matching across the bandwidth, the dimensional parameters were refined using the built-in sequential nonlinear optimization algorithm.

4.4 Extension of Mode Converter

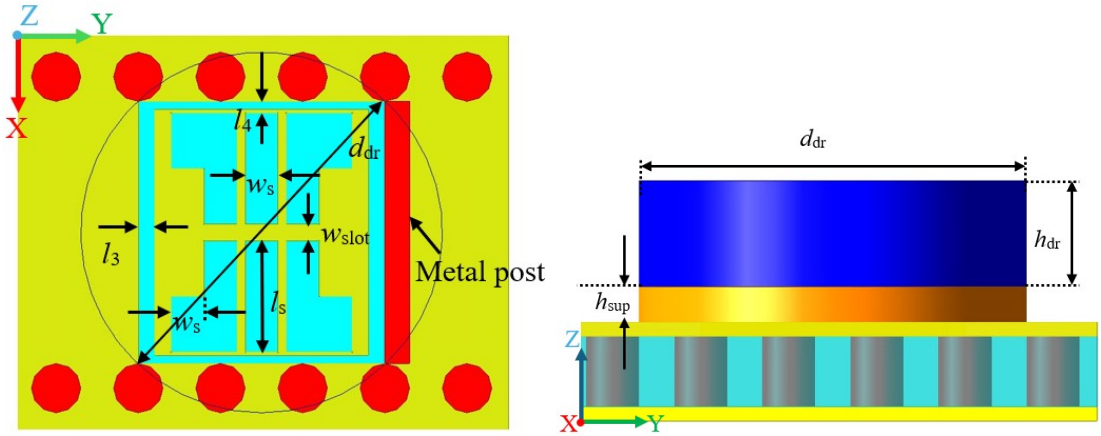
The mode converter developed in the preceding section can be extended to feed on-chip antennas, enabling seamless energy transfer between rectangular waveguides and substrate-integrated radiating elements. This extension leverages the TE_{20} mode generated within the SIW to excite planar antennas directly, thereby eliminating bulky interconnects and minimizing mismatch losses between off-chip and on-chip domains. Such integration is particularly valuable for THz front-end modules where compactness, low-loss transitions, and high field confinement are essential for realizing fully monolithic transceivers.

4.4.1 On-Chip antenna Fed by SIW TE_{20} Mode

Numerous strategies have been explored to improve the performance of on-chip antennas, such as employing dielectric superstrates [211] and artificial magnetic conductors (AMCs) [61]. However, these methods are often limited by issues such as undesired

back radiation and surface wave excitation. To mitigate these effects, the proposed design adopts TE_{20}-mode excitation within the SIW. The higher-order field symmetry of this mode effectively reduces surface-wave coupling while enhancing radiation directivity.

4.4.1.1 Antenna Geometry and Feeding Mechanism



(a) **(b)**

Figure 4.13: Proposed antenna layout, illustrating **(a)** the top view and **(b)** the side view.

The proposed on-chip antenna (OCA) is realized using an L-shaped radiating patch integrated on the top metallization of the SIW, as shown in Figure 4.13. This configuration enlarges the effective radiating aperture, thereby enhancing both radiation efficiency and gain [37, 38, 177]. Unlike conventional TE_{10}-fed designs, the antenna is excited using the TE_{20} mode of the SIW. The higher-order TE_{20} mode offers a more uniform electric field distribution across the radiating aperture, resulting in an improved impedance bandwidth and enhanced radiation characteristics [212]. Furthermore, since the cutoff frequency of the TE_{20} mode is greater than that of the TE_{10} mode, this approach supports higher operational frequencies and contributes to increased channel capacity [213].

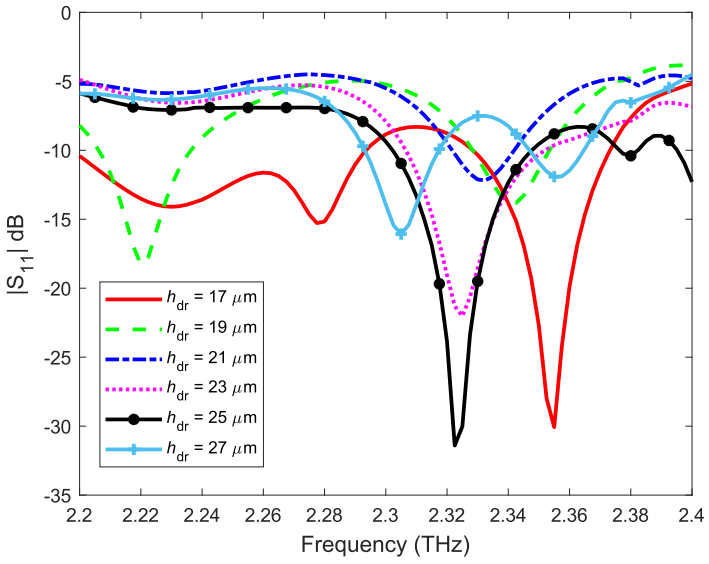
4.4.1.2 Dielectric resonator loading

To further improve impedance matching and extend the operational bandwidth, a dielectric resonator (DR) was integrated above the radiating patch, supported by a low-permittivity substrate layer [64, 177]. The DR and its support structure share a common diameter (d_{dr}). The DR, fabricated from silicon with a relative permittivity $\epsilon_{\text{dr}} = 11.9$, provides strong field confinement, while the support layer, realized in Rogers RT/duroid 5880 with $\epsilon_{\text{sup}} = 2.2$, ensures mechanical stability and impedance matching. Loading the radiating element with a DR presents several advantages: it introduces a high-Q resonant structure that concentrates the electromagnetic energy into a confined volume, thereby reducing conductor and substrate losses and boosting radiation efficiency, an effect widely reported in dielectric resonator antenna (DRA) research [214, 215]. The use of the DR as a parasitic resonant element not only enhances bandwidth but also enables fine-tuning of polarization characteristics [120].

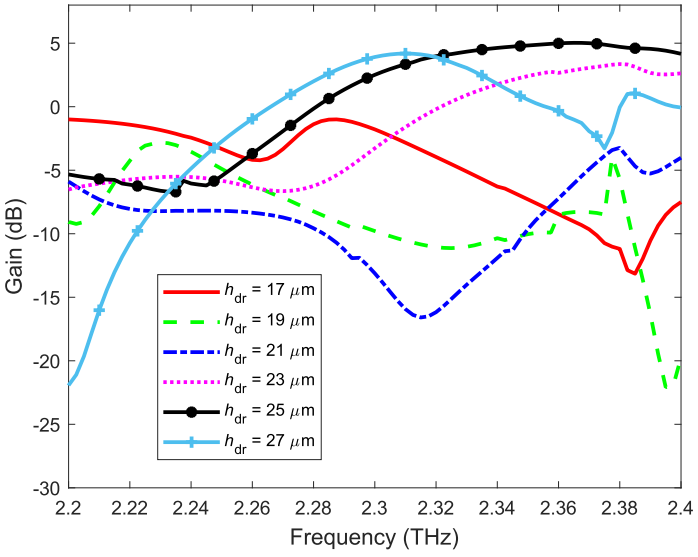
4.4.1.3 Radiation Leakage Suppression

A major challenge in OCA designs is unwanted radiation leakage into the surrounding circuit environment. In this work, the issue is mitigated by incorporating a metallic wall adjacent to the radiating patch [158, 177]. This structure resembles a Yagi-inspired configuration, in which the radiating slot acts as the driven element and the dielectric resonator functions as a director, thereby enhancing forward radiation without the need for a separate reflector [64]. The metallic wall acts as a lateral confinement boundary, suppressing lateral surface-wave energy and forcing more radiated power into the main lobe. In doing so, it helps maintain a compact footprint compatible with monolithic integration, while preserving radiation efficiency and reducing coupling to neighboring components.

4.4.1.4 Parametric Analysis and Optimization

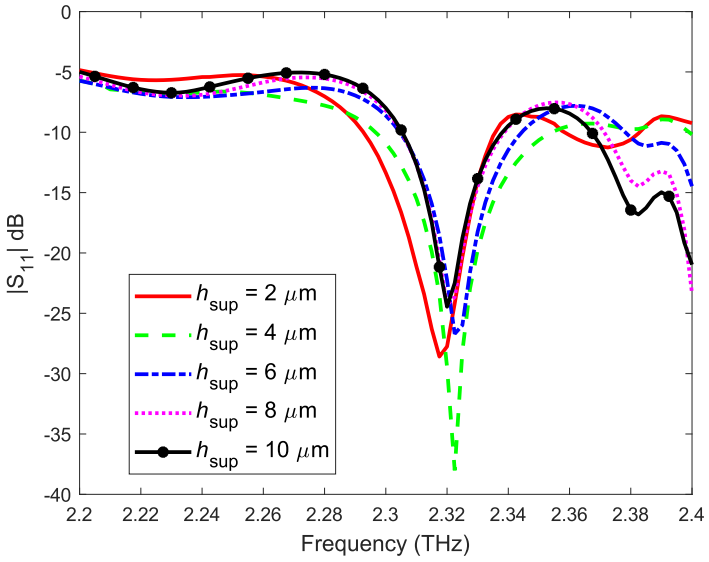


(a)

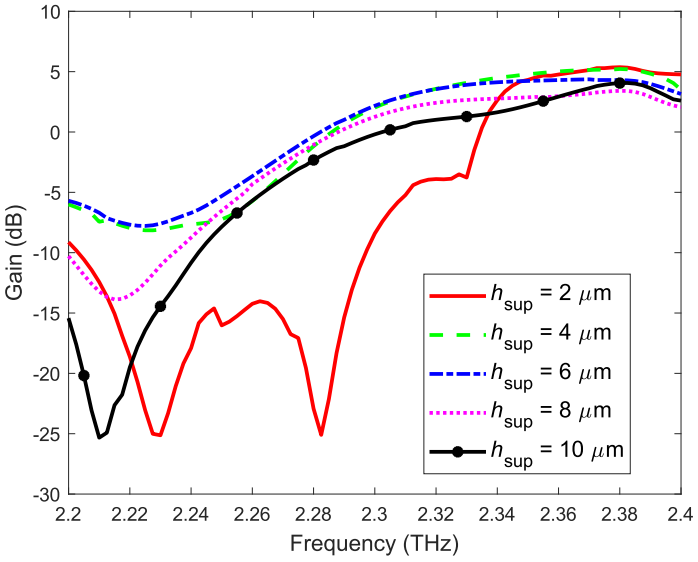


(b)

Figure 4.14: Simulated results of antenna performance at different thicknesses of the dielectric resonator substrate (h_{dr}):**(a)** reflection coefficient $|S_{11}|$ and **(b)** gain.



(a)



(b)

Figure 4.15: Simulated results of antenna performance at different thicknesses of the dielectric supporter (h_{sup}): **(a)** reflection coefficient and **(b)** gain.

The effect of the DR and supporting-layer thicknesses on antenna performance was systematically investigated. As shown in Figure 4.14, variations in the DR thickness significantly influence both the reflection coefficient ($|S_{11}|$) and gain, whereas changes

in the dielectric supporter have only a minor impact, as illustrated in Figure 4.15. Consequently, the DR thickness was identified as a key design variable for bandwidth and gain optimization [216]. The final optimized parameters are: $l_3 = 5$ μm, $l_4 = 2.5$ μm, $w_s = 10$ μm, $l_s = 34$ μm, $h_{\mathrm{dr}} = 25$ μm, $h_{\mathrm{sup}} = 5$ μm, and $d_{\mathrm{dr}} = 110$ μm. With these values, the antenna achieved a maximum gain of 4.49 dB at 2.32 THz.

4.4.1.5 Mode Excitation and Radiation Pattern

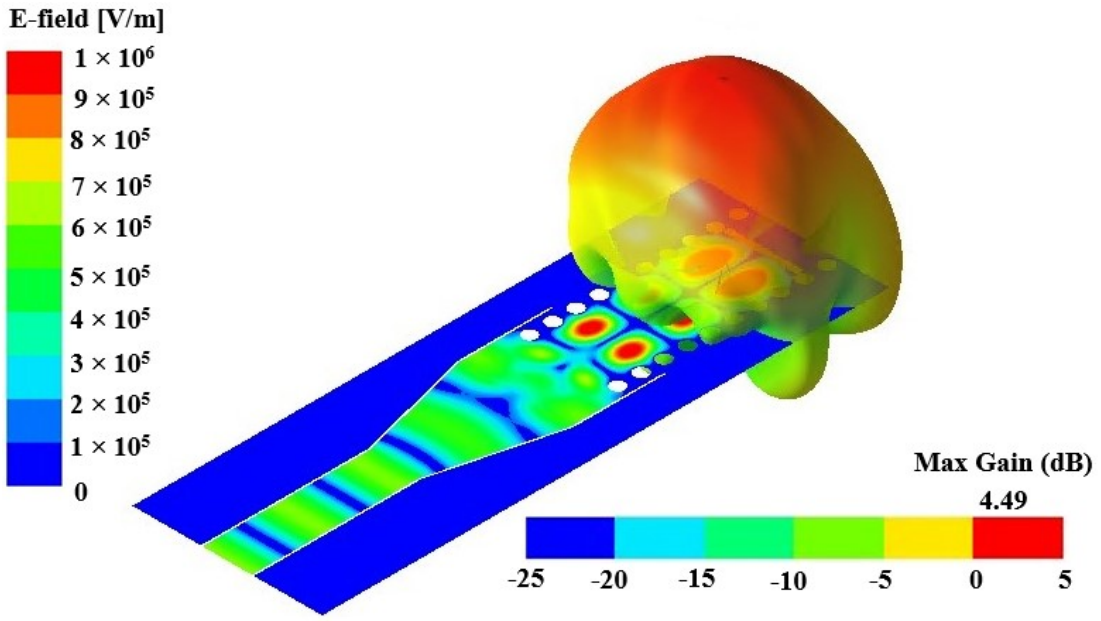


Figure 4.16: Isometric visualization of the TE_{20} mode SIW electric field distribution overlaid with its corresponding 3D radiation pattern.

The simulated field distributions and 3D radiation patterns, shown in Figure 4.16, confirm that although the TE_{20} mode exhibits two field lobes within the SIW, the patch antenna radiates a broadside pattern with a dominant main lobe and occasional side lobes. This behavior is consistent with higher-order SIW-fed patch antennas reported in literature [169, 177, 217].

4.4.2 Balun Based on SIW

The use of a SIW platform for balun implementation offers a highly attractive solution for THz systems requiring compactness, low loss, and planar compatibility. Traditional baluns, such as coaxial, Marchand, or microstrip branch-line types, often suffer from high radiation loss, phase imbalance, and fabrication complexity at sub-millimeter wavelengths [218, 219]. In contrast, SIW structures emulate the behavior of conventional rectangular waveguides while retaining the ease of integration associated with planar circuits [220]. And their quasi-TEM propagation, low conductor loss, and inherent shielding make them suitable for balanced-to-unbalanced transformations at THz frequencies. Moreover, the SIW platform supports multiple higher-order modes such as TE_{20}, which naturally exhibit differential electric-field distributions, ideal for realizing balun functionality without additional phase-shifting networks [218]. Consequently, the SIW-based balun not only minimizes fabrication complexity but also ensures strong mode confinement, reduced coupling, and excellent compatibility with on-chip antenna and transceiver integration.

4.4.2.1 Balun Fundamentals

A balun (balanced–unbalanced transformer) is a widely used RF component that provides an interface between single-ended (unbalanced) and differential (balanced) transmission lines. It effectively acts as a power divider, producing two output signals of equal magnitude but opposite phase (180°). In an unbalanced port, the signal propagates along one conductor with respect to ground, whereas in a balanced configuration, both conductors carry equal and opposite signals. Since a balun is reciprocal in nature, its operation can be described by the following S-parameter relations [203]:

$$S_{31} = S_{13} = -S_{21} = -S_{12} \tag{4.14}$$

4.4.2.2 SIW TE_{20} Mode as a Balun

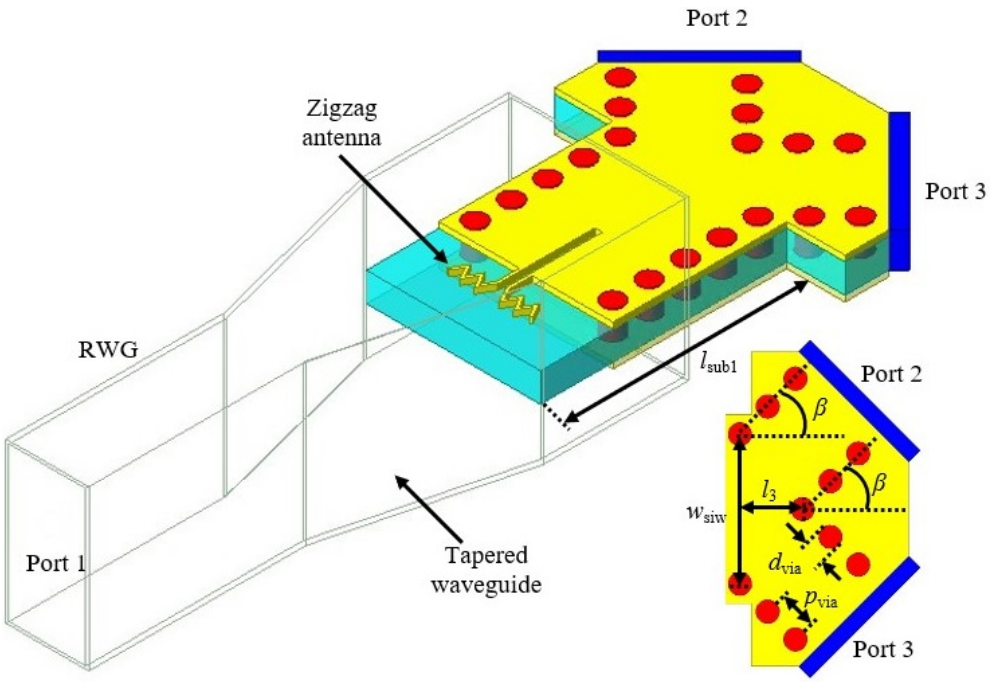


Figure 4.17: Isometric representation of the proposed SIW balun operating in the TE20 mode. The principal structural parameters are $l_3 = 41.25$ μmm and $\beta = 45°$, while the remaining geometrical specifications are summarized in Table 4.1

The electric field distribution of the SIW in TE_{20} mode inherently exhibits symmetry about the x–y plane, with equal magnitudes but opposite polarities on either side. This distribution is analogous to the behavior of a differential pair, where the two balanced ports of a balun carry signals with a $180°$ phase difference. Leveraging this property, a balun can be realized directly within the SIW by exploiting its TE20 mode. The proposed balun, derived from the mode converter architecture, is shown in Figure 4.17.

In the proposed design, the two half-modes of the TE_{20} SIW are extracted symmetrically into two ports (port 2 and port 3) with respect to the x-axis, separated by an angle $\beta = 45°$. Metallic vias ensure confinement and guidance of the modes toward the output ports. The key structural dimensions are $l_3 = 41.25$ μm and $\beta = 45°$, with the remaining values summarized in Table 4.1.

4.4.3 Field Distribution and Performance Metrics

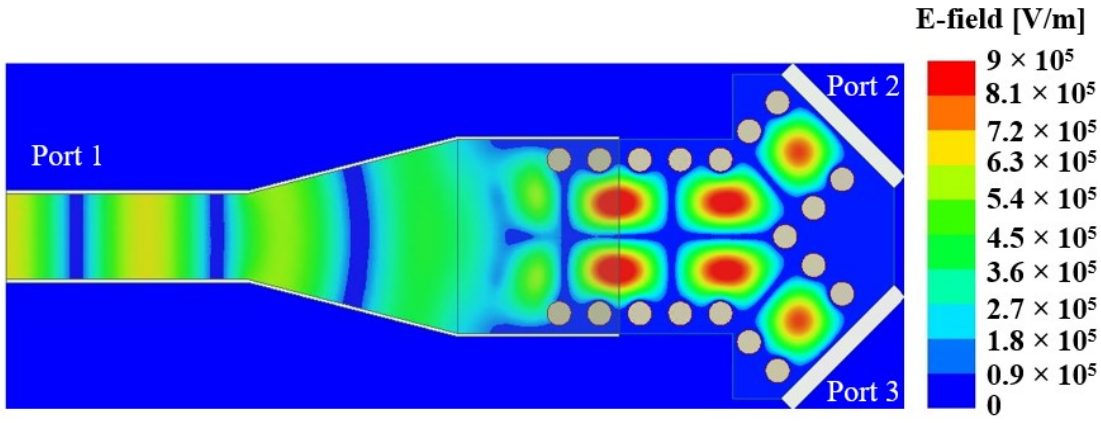
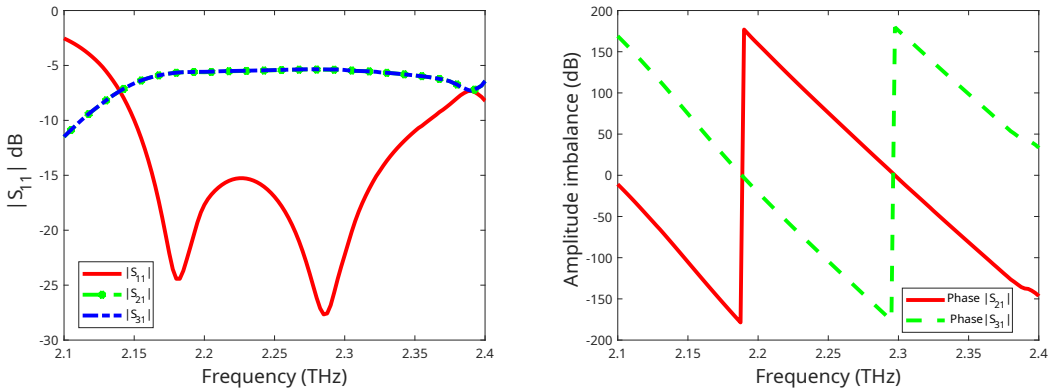


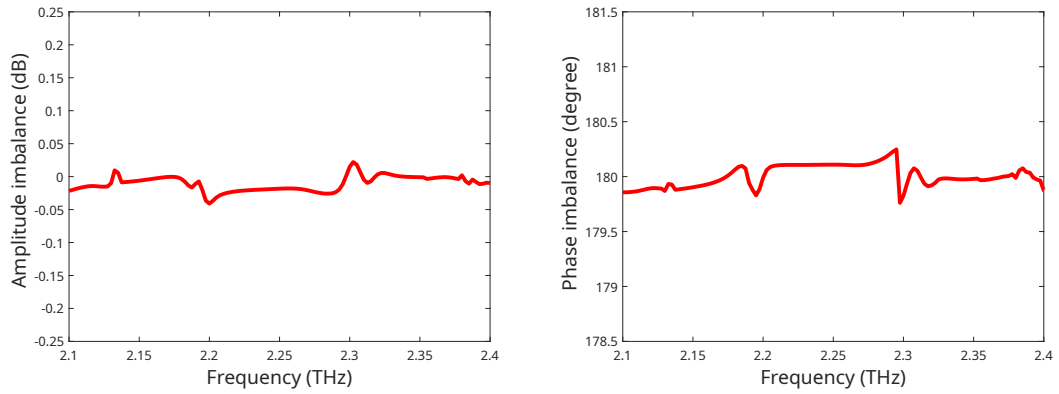
Figure 4.18: Computed electric field distribution of the THz SIW balun configured to operate in the TE_{20} mode.

Figure 4.18 illustrates the simulated electric field distribution at 2.25 THz. The TE20 mode field inside the SIW divides into two TE10 half-modes at the output ports. These TE_{10} modes can subsequently be transformed into quasi-TEM modes of microstrip lines through tapered transitions without vias [164]. This transformation is essential for integration with planar RF circuits.



(a) **(b)**

Figure 4.19: Computed results for the THz SIW balun based on the TE_{20} mode: **(a)** S-parameter response and **(b)** phase variation between ports 2 and 3



(a) **(b)**

Figure 4.20: Computed results for the THz SIW balun based on TE_{20} excitation: **(a)** amplitude mismatch and **(b)** phase mismatch between the balanced output ports.

The simulated performance of the balun is shown in Figure 4.19. The reflection coefficient $|S_{11}|$ remains below -10 dB over the frequency range $2.15 - 2.35$ THz, indicating good impedance matching. The intrinsic insertion loss is approximately $5.3 - 6.5$ dB within this band. For the differential output ports, the amplitude imbalance was limited to ± 0.037 dB as shown in Figure 4.20**(a)**, while the phase imbalance remained below 1° across the operating frequency range as depicted in Figure 4.20**(b)**. These results confirm the effectiveness of the TE_{20}-mode SIW balun in achieving high-fidelity balanced outputs at terahertz frequencies.

4.4.3.1 Application

The proposed balun is particularly useful in feeding structures that require balanced excitation. For example, in dipole antennas, the differential outputs (ports 2 and 3) provide the necessary 180° out-of-phase signals derived from a single-ended excitation (port 1), typically driven by a coaxial input [221]. Similarly, in antenna arrays, the balun ensures equal-amplitude and opposite-phase feeding to adjacent elements, enabling controlled radiation patterns and beamforming capabilities [222].

4.5 Probe-less RWG TE_{10} to SIW TE_{20} Mode Converter

The probe-less rectangular-to-SIW mode converter is introduced to overcome the fabrication and alignment challenges associated with conventional probe- or slot-fed transitions. Traditional probe-fed converters often suffer from impedance mismatch, parasitic inductance, and mechanical fragility at sub-THz frequencies, where even μm-scale misalignment can significantly degrade performance [223, 224]. The proposed probe-less design eliminates the need for metallic feed probes by employing a stepped transformer and aperture-coupled excitation, which ensures smoother field continuity between the RWG and SIW. This approach not only simplifies fabrication and integration with planar substrates but also enhances broadband operation and reduces ohmic and contact losses, making it particularly suitable for compact THz front-end systems and on-chip interconnect architectures [158, 218].

4.5.1 Structure and Design Principle

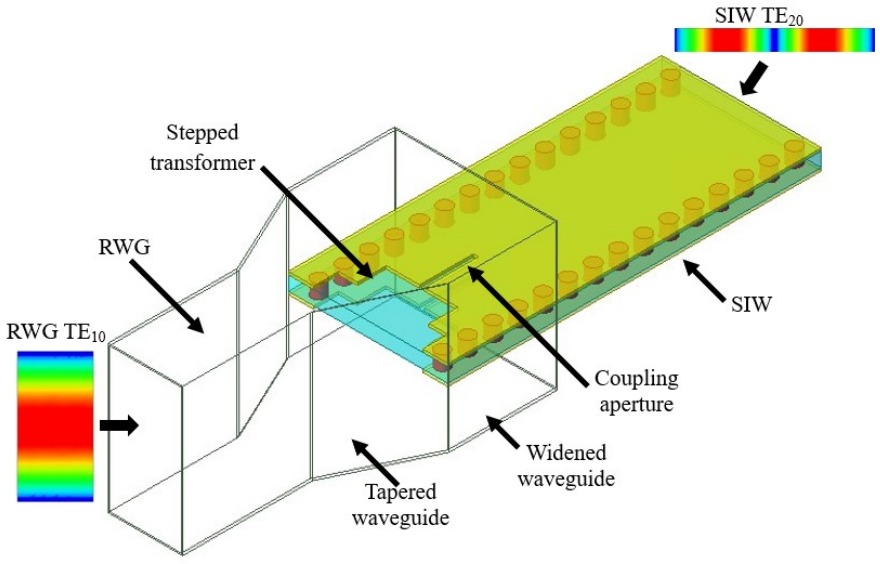


Figure 4.21: Isometric view of the probe-less RWG TE_{10} mode to SIW TE_{20} mode converter

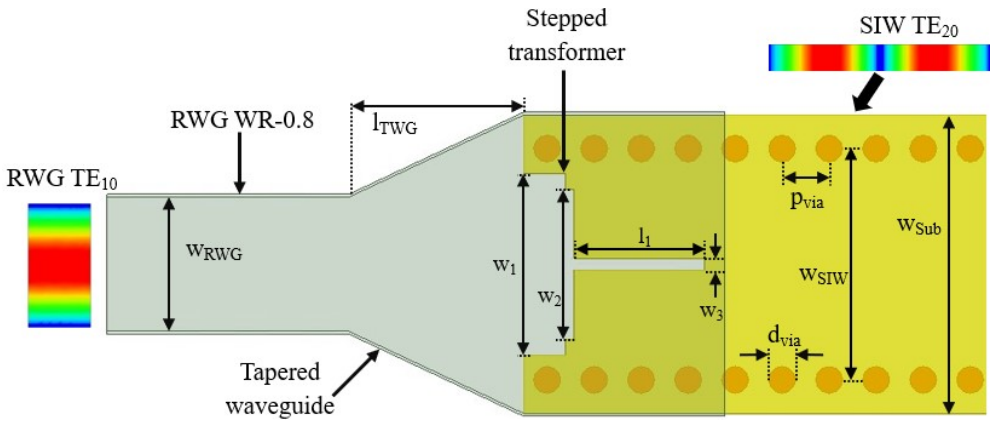


Figure 4.22: Top view of the probe-less RWG TE_{10} mode to SIW TE_{20} mode converter

Figure 4.22 illustrates the top view of the proposed converter structure. The design begins with a standard WR-0.8 rectangular waveguide (RWG), which is extended into a tapered and subsequently widened waveguide section. The configuration incorporates a stepped-width top metallization of the SIW, along with an aperture-coupling slot that facilitates energy transfer. The tapered waveguide serves as a transition region, gradually transforming the incident y-polarized electric field of the RWG into a z-polarized field distribution [135].

The first stage of conversion occurs at the stepped metallic layer of the SIW, which behaves as a dipole antenna. Its resonant frequency is determined by the stepped width; it excites and radiates transversely. The second stage involves quasi-slot excitation from the aperture slot in the top metallization [164]. This quasi-slotline mode is analogous to the TE_{20} mode of the SIW, as both represent odd modes characterized by equal magnitudes but opposite electric field directions on either side of the symmetry plane. Through this field symmetry, the quasi-slotline couples effectively with the SIW TE_{20} mode, thereby completing the mode conversion. A comprehensive theoretical explanation of the mode conversion process is provided above in Section 4.3.1.3.

4.5.2 Performance Metrics

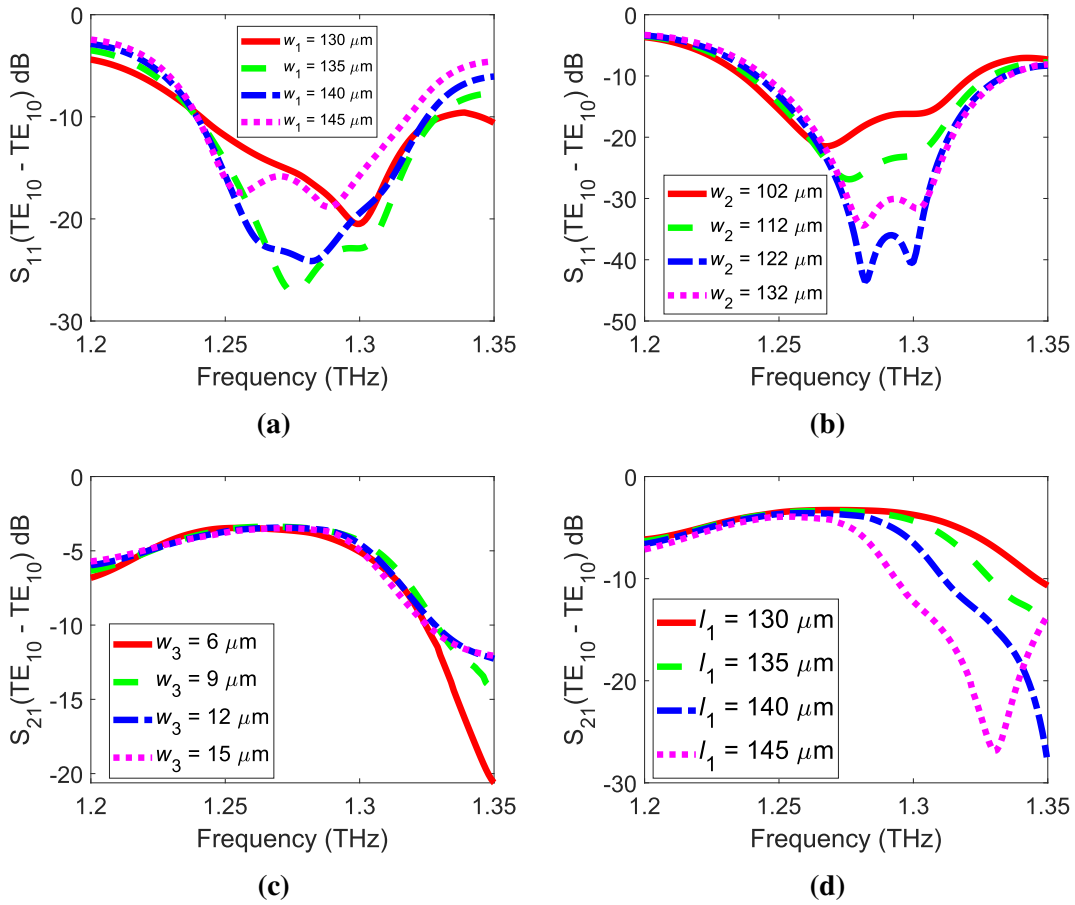


Figure 4.23: Simulated reflection (|S11|) for variations in **(a)** w_1 and **(b)** w_2, and transmission (|S21|) for variations in **(c)** w_3 and **(d)** l_1 of the back-to-back mode converter

Figure 4.23**(a-b)** presents the simulated reflection ($S|_{11}|$) coefficients of the back-to-back probe-less converter. The dimensional parameters w_1 and w_2 were optimized to achieve impedance matching across the operational frequency range, resulting in a reflection coefficient below –10 dB over the desired bandwidth. As shown in Figure 4.23**(c-d)**, variations in w_3 and l_1 primarily influence the transmission behavior, where a broader pass-band and reduced insertion loss are obtained at the optimized dimensions. These results confirm that the stepped transformer configuration enables efficient power transfer and low reflection between the RWG and SIW sections, ensuring stable operation

within the sub-THz range.

4.5.3 Field Distribution

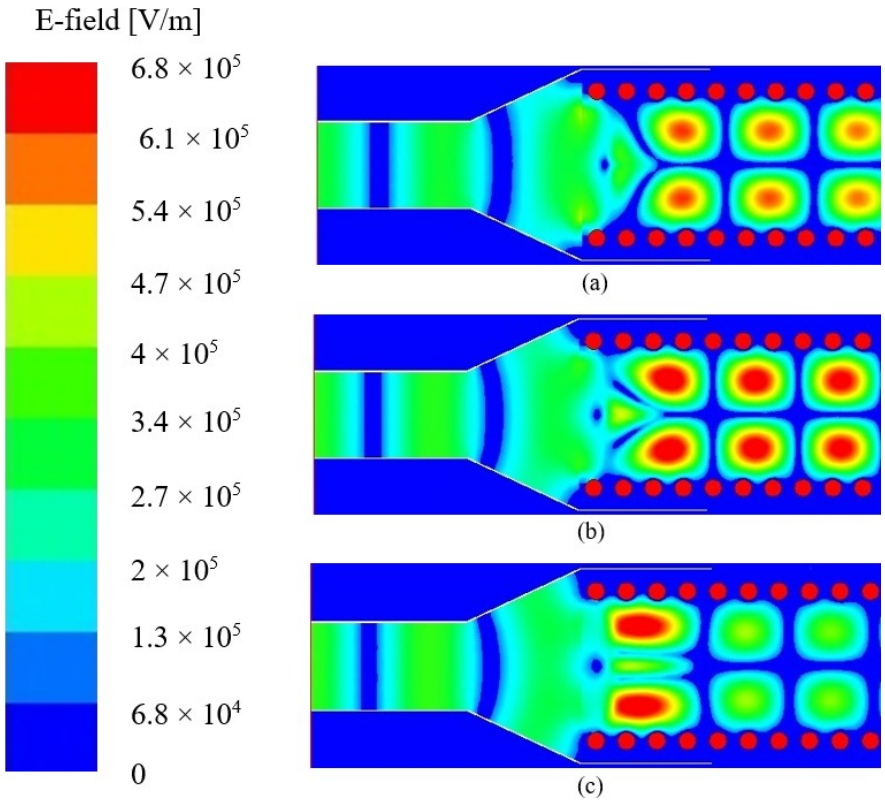


Figure 4.24: E-field distribution of the probe-less mode converter at: **(a)** 1.27, **(b)** 1.29, and **(c)** 1.31 THz

The simulated electric-field distribution presented in Figure 4.24 illustrates the gradual evolution of the field across the stepped region of the converter. The field maintains strong confinement along the propagation path, with the intensity symmetrically divided as the energy couples into the SIW section over the frequency range of $1.27 - 1.31$ THz. Distinct dual-lobe field patterns are clearly visible, confirming the excitation of the TE_{20} mode within the SIW. The results validate that the proposed structure achieves stable field transition and well-balanced power distribution across the operating band.

4.6 Perpendicular RWG TE_{10} to SIW TE_{20} Mode Converter

While planar transition techniques, such as zigzag antennas (Section 4.3) and stepped metallic layers (Section 4.5), effectively facilitate horizontal coupling between RWG and SIW, they are inherently confined to in-plane integration [158]. This limitation restricts their suitability for multilayer or 3D circuit topologies, where EM signals must traverse between stacked modules or different substrate layers. In contrast, vertical transitions enable out-of-plane interconnections, reduce routing complexity, and support compact multilayer integration for advanced THz systems. Such structures are particularly essential for multilayer packaging, antenna characterization, and high-density 3D interconnects [225].

4.6.1 Geometry Overview

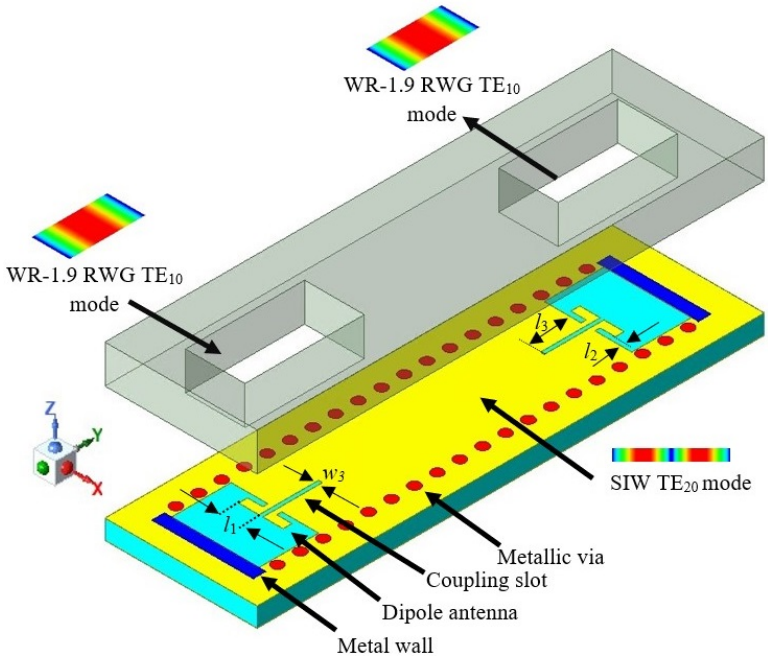


Figure 4.25: Geometry of the perpendicular RWG-SIW TE_{10}-TE_{20} mode converter showing vertical coupling layout

The geometric configuration of the proposed perpendicular RWG TE_{10} to SIW TE_{20} mode converter is illustrated in Figure 4.25. The design employs a WR-1.9 rectangular waveguide (RWG) supporting the TE_{10} mode, mounted vertically on the SIW layer to enable out-of-plane EM coupling. Within the groove region of the SIW, a dipole-like coupling structure and an aperture slot are integrated to facilitate energy transfer from the incident TE_{10} field of the RWG into the TE_{20} mode of the SIW. The perpendicular arrangement allows compact 3D interconnection while preserving the field symmetry required for efficient mode conversion. A metallic enclosure surrounding the junction region serves to suppress parasitic radiation and minimize field leakage, thereby ensuring stable propagation and improved mode purity at terahertz frequencies [158].

4.6.2 Performance

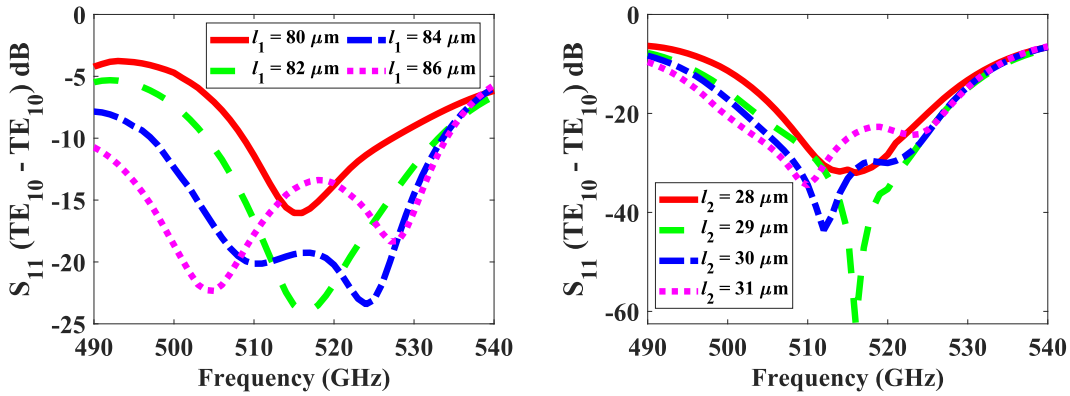


Figure 4.26: Simulated $|S_{11}|$ (TE_{10} - TE_{10} for the perpendicular mode transfer at different values of: **(a)** l_1 and **(b)** l_2

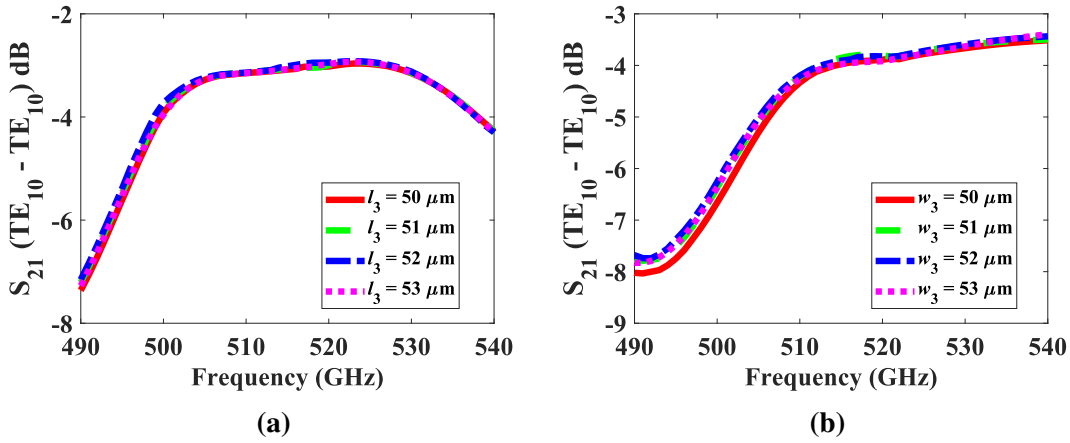


Figure 4.27: Simulated $|S_{21}|$ (TE_{11} - TE_{11} for the perpendicular mode transfer at different values of: **(a)** l_3 and **(b)** w_3

Figure 4.26 presents the simulated reflection ($|S_{11}|$) of the proposed perpendicular back-to-back mode converter. The dipole arm lengths (l_1 and l_2) were optimized to ensure impedance matching, while variations in the aperture slot dimensions (l_3 and w_3) were used to fine-tune the bandwidth and transmission characteristics as illustrated in Figure 4.27. The reflection coefficient remains below -10 dB across the intended operating band, confirming good impedance matching and stable mode conversion between the RWG and SIW structures.

The corresponding electric field distribution, shown in Figure 4.28, demonstrates the smooth mode transition from the RWG TE_{10} mode to the SIW TE_{20} mode and back to RWG TE_{10}. The observed field symmetry and continuity across the vertical interface indicate strong coupling efficiency and minimal radiation leakage. These results validate the robustness of the perpendicular configuration for compact multilayer and three-dimensional terahertz interconnect implementations.

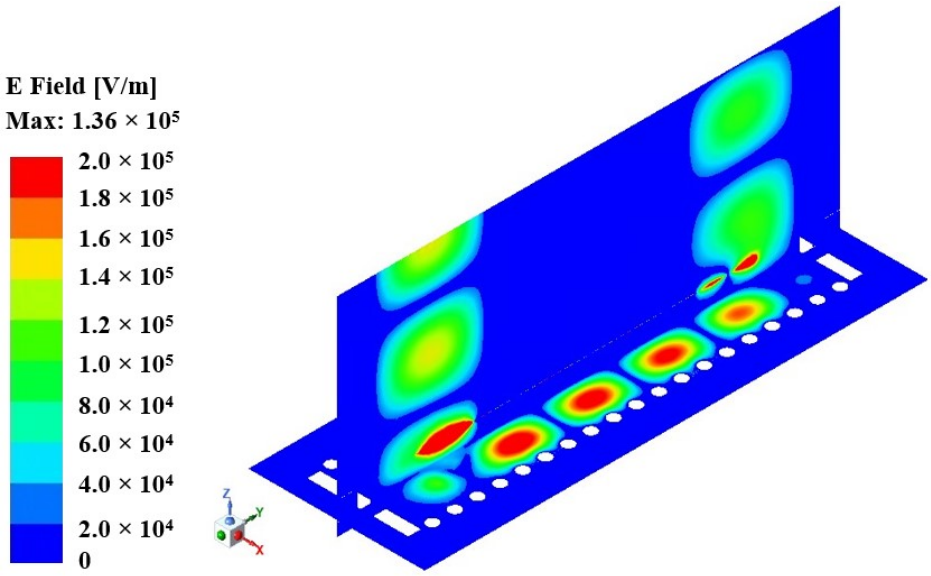


Figure 4.28: Isometric representation of the e-field distribution of the mode converter at 505 GHz

4.7 Chapter Summary

This chapter highlights that no single converter universally dominates across all performance metrics. Instead, the optimal choice depends on system-level requirements. The Probe-less stepped SIW (Section 4.5) design excels in minimizing loss, the zigzag antenna converter (Section 4.3) maximizes bandwidth and multi-functionality, and the perpendicular dipole (Section 4.6) design uniquely addresses vertical integration challenges. Collectively, these architectures demonstrate the diverse strategies available for enabling RWG TE_{10} mode to SIW TE_{20} mode transitions at THz frequencies, and they form complementary solutions for future on-chip and inter-chip THz communication systems.

Chapter 5

Terahertz On-Chip Antennas and Transceiver Design for Wireless Network-on-Chip Architecture

While the Chapter 4 established an efficient mode conversion technique for exciting higher-order SIW modes, the broader impact of such components lies in their application to practical THz systems. In particular, on-chip communication requires compact, wideband, and integrable antenna solutions capable of supporting high data rates within and between chips. Building upon the advances in SIW horn antennas and mode converters, chapter 5 explores the application of on-chip THz communication systems, demonstrating how these techniques can be leveraged to overcome the limitations of conventional wired interconnects and enable high-speed intra- and inter-chip wireless links.

This chapter consolidates the outcomes of two complementary studies. The first contribution focused on the design and analysis of a THz dipole antenna for intra-chip communication, providing proof-of-concept demonstrations of wireless connectivity

across multiple cores within a flip-chip package. Building upon this foundation, the second contribution advanced the research toward a complete transceiver model that incorporates both intra-chip and inter-chip communication scenarios. By comparing dipole and zigzag antennas in realistic chip environments, analyzing path loss and electric field distributions, and performing link budget estimates, the study validates the feasibility of achieving sub-pJ-per-bit energy consumption in WNoC systems. Together, these works provide a comprehensive evaluation of antenna configurations, system-level performance, and design trade-offs necessary for enabling THz wireless interconnects in future multi-core processors.

This chapter presents the author's contributions toward realizing THz-enabled WiNoCs, focusing on the design and simulation of on-chip antennas and transceiver architecture for intra- and inter-chip communication. The chapter synthesizes findings from two major studies: (i) initial exploration of THz dipole antennas for intra-chip communications and (ii) extended work on transceiver design and performance evaluation across both intra- and inter-chip scenarios.

5.1 System Setup

The first stage of this work focused on demonstrating the feasibility of using THZ on-chip antennas to enable wireless intra-chip communication. A simple dipole antenna was selected due to its compact footprint, omnidirectional radiation characteristics, and compatibility with micron-scale integration. The antenna length was designed to be 0.009 mm with a radius of 1μm, optimized to resonate near 1 THz, which aligns with the desired operating band for Wireless Network-on-Chip (WNoC) systems.

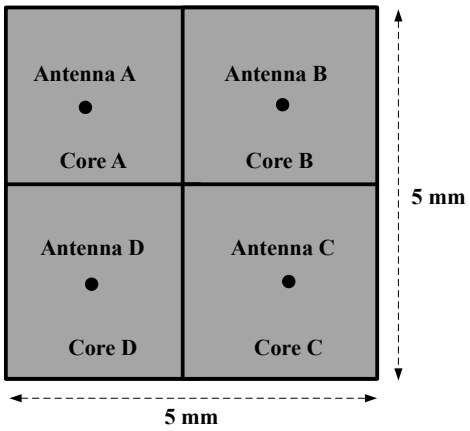


Figure 5.1: Top view of the multi-core processor

To account for realistic chip conditions, the antenna was integrated into a 5×5 mm^2 chip package that contained four processing cores as shown in Figure 5.1. The package included multiple layers such as silicon substrate, dielectric layers, and flip-chip interconnects, reflecting typical System-on-Chip (SoC) packaging. Since modeling thousands of interconnect wires in full detail would create prohibitive computational complexity, they were condensed into an equivalent conductive layer representation, capturing their electromagnetic shielding effects and excessive meshing requirements.

5.2 Simulation Framework

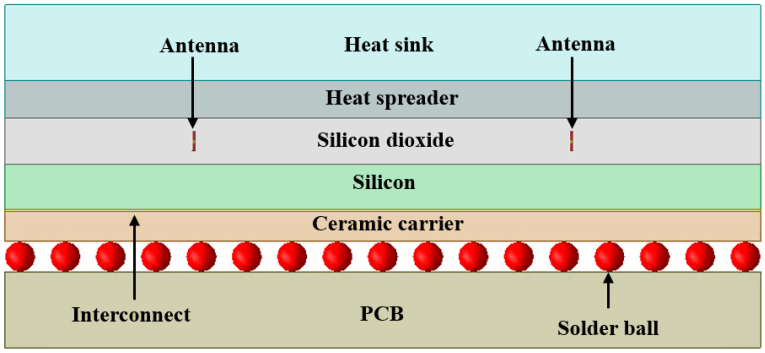


Figure 5.2: Side view of the flip-chip package with embedded dipole antenna

Full-wave EM simulations were conducted in Ansys HFSS, which allowed for 3D modeling of antenna performance and e-field propagation. The antenna was embedded in a flip-chip structure (material property is available in Table 5.1), as illustrated in side view schematics (Figure 5.2), and excitation was applied using a lumped port. Three representation cores (labeled A, B, and C) were selected for performance evaluation, as these presented different distances and orientations, thus forming worst-case scenarios for intra-chip communications.

Table 5.1: Layers of materials and their characteristic within a chip package

Name	**Thickness (mm)**	**Materials/Properties**
Heat sink	0.5	Aluminum
Heat spreader	0.25	Aluminum nitride (AIN) ($\epsilon_r = 8.6, \tan\delta = 0.0003$)
Polyimide	0.5	$\epsilon_r = 3.5, \tan\delta = 0.008$
Silicon	0.5	$\epsilon_r = 11.9, \tan\delta = 0.2$
Silicon dioxide	0.5	$\epsilon_r = 4, \tan\delta = 0.0001 - 0.001$
Interconnect	0.013	copper
Ceramic carrier	0.5	Alumina ($\epsilon_r = 9.4, \tan\delta = 0.006$)
Solder balls	0.32	Perfectly electric conductor
Antenna	-	Copper

5.3 Results and Observations

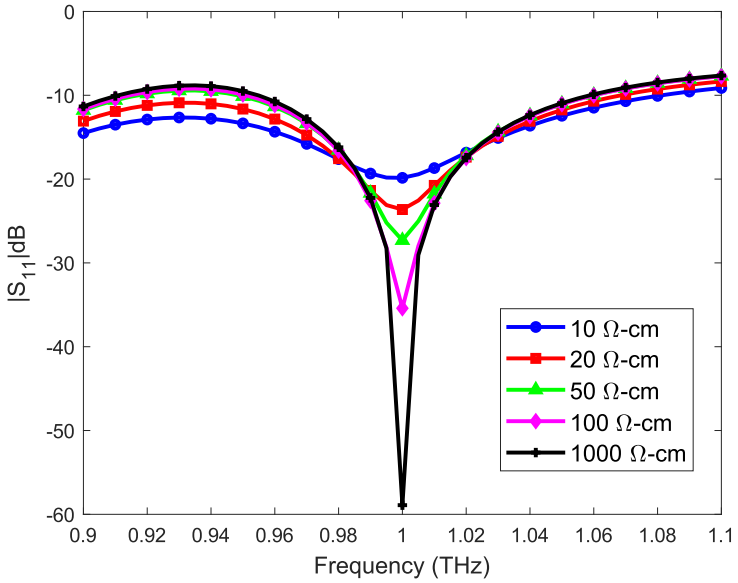


Figure 5.3: Dipole antenna $|S_{11}|$ for varying SiO_2 resistivity

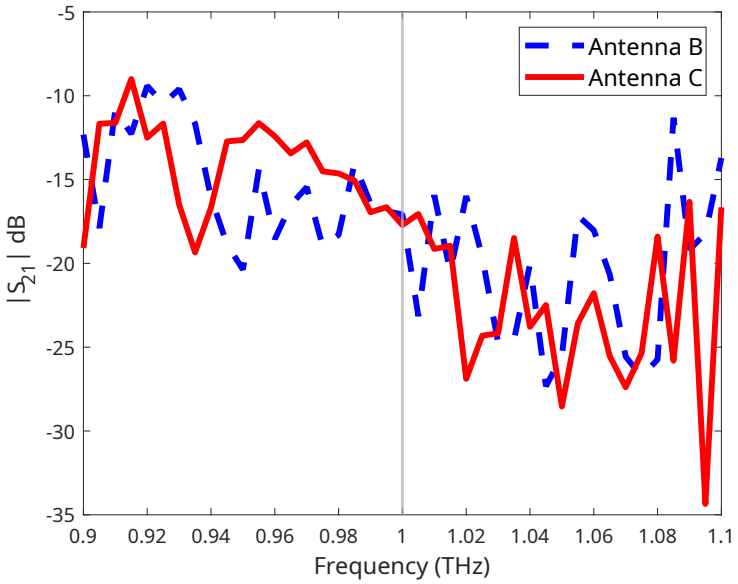


Figure 5.4: Transmission coefficient ($|S_{21}|$) with Antenna A as the transmitter

The simulated reflection coefficient $|S_{11}|$, shown in Figure 5.3, demonstrates good impedance matching, with values remaining below -10 dB around 1 THz for all examined

SiO_2 resistivity levels. As the substrate resistivity increases, the overall magnitude of $|S_{11}|$ improves, indicating reduced reflection and better impedance matching. This improvement is attributed to lower substrate conductivity, which suppresses dielectric losses and surface-wave propagation, two major factors that degrade on-chip antenna performance at terahertz frequencies [107]. Conversely, lower-resistivity substrates introduce greater conduction losses, resulting in slightly poorer matching. These results confirm that optimizing SiO_2 resistivity is critical for minimizing substrate-induced losses and achieving stable, high-efficiency operation within THz integrated systems. The transmission coefficient $|S_{21}|$ results, shown in Figure 5.4, indicate a coupling magnitude of approximately -17 dB between Antenna A and both Antenna B and Antenna C. Interestingly, although Antenna C is physically farther from Antenna A than Antenna B, the transmission magnitudes remain nearly identical. This phenomenon is attributed to multiple reflections within the package structure, which effectively redirect the propagating waves and compensate for distance-related attenuation.

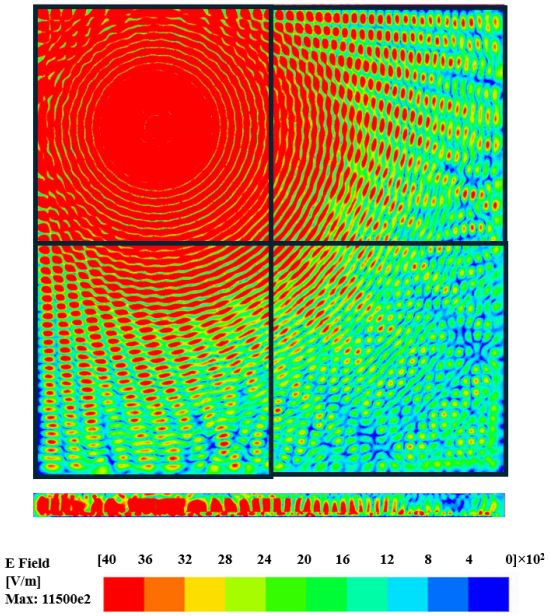


Figure 5.5: Simulated electric field distribution (V/m) across the top and side views of the chip with an integrated antenna at 1 THz

The e-field distribution plots provided in Figure 5.5 provide further insight into propagation mechanisms. Cross-sectional views revealed that strong fields were confined within the chip package layers, and significant reflections occurred at the boundaries of silicon and dielectric materials. This suggested that intra-chip THz communication primarily relies on wave reflections and surface-wave propagation, rather than direct line-of-sight transmission.

5.4 WiNoC Architecture and Design Concept

Building upon the antenna-level proof-of-concept, the second stage of this research extended the design toward a complete transceiver model capable of supporting both intra-chip and inter-chip communications. The architecture follows the principles of Wireless Network-on-Chip (WiNoC), where antennas are embedded within cores to enable single-hop or broadcast communication.

5.4.1 Antenna Configurations

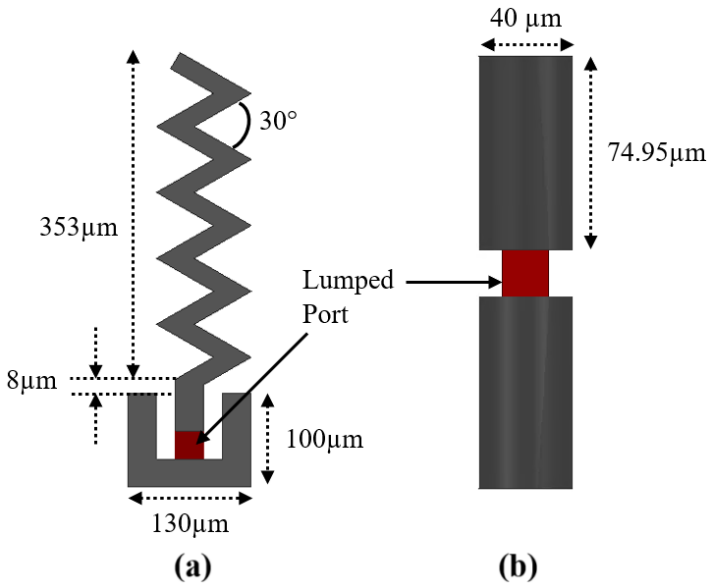


Figure 5.6: On-chip **(a)** zigzag antenna and **(b)** dipole antenna

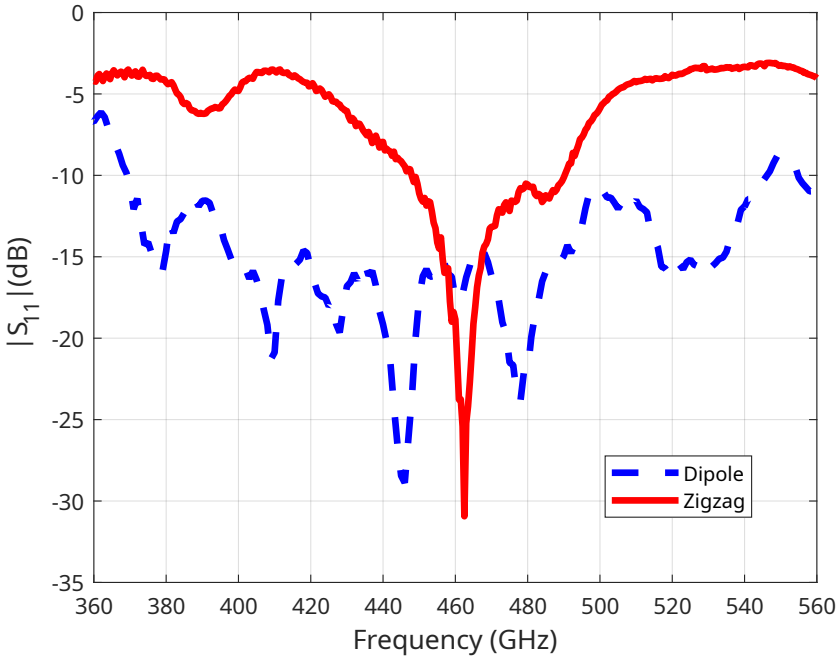


Figure 5.7: $|S_{11}|$ of dipole and zigzag antenna under polyimide substrate

Two types of on-chip antennas were designed and analyzed for THz intra-chip communication: a dipole antenna and a zigzag antenna, as illustrated in Figure 5.6**(a-b)**.

- **Dipole Antenna**: The dipole antenna, with a total length of 149.9μm, resonates at approximately 446 GHz. Its reflection coefficient ($|S_{11}|$), shown in Figure 5.7, confirms good impedance matching within the operational band.

- **Zigzag Antenna**: The zigzag antenna has an unfolded Length of 353μm, and exhibits resonance at 462.5 GHz. The corresponding $|S_{11}|$ demonstrates stable impedance performance and wideband matching characteristics suitable for THz integration.

Both antennas were implemented within a $20 \times 20\text{mm}^2$ multi-core chip environment that incorporates realistic packaging layers, including heat spreaders, silicon substrates, and polyimide dielectric films. Polyimide was selected as the primary substrate due to its low dielectric constant ($\epsilon_r = 3.5$) and low loss tangent, which minimize surface-wave

propagation and substrate losses at THz frequencies. For comparative evaluation, silicon dioxide (SiO_2) substrates were also simulated to investigate the effect of dielectric loss and resistivity on antenna performance [107]. The complete list of materials used in the chip stack, along with their corresponding electrical properties, is summarized in Table 5.1.

5.4.2 Intra-Chip Communication Performance

In the simulations, each core (A, B, C, D, E, F, G, H, and I) was configured with both zigzag and dipole antennas. For analysis, cores A, B, C, E, and I were selected, as they represent the worst-case scenarios in terms of inter-core transmission performance. All transmission coefficients presented in this study at 462.5 GHz (zigzag antenna) and 446 GHz (dipole antenna) are measured relative to Antenna A.

5.4.2.1 Simulated Transmission Coefficient

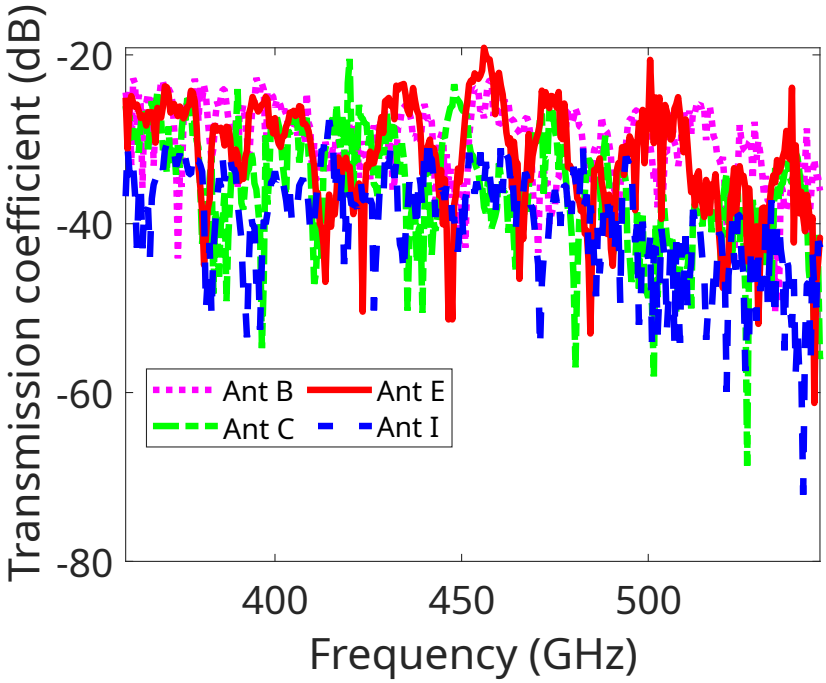


Figure 5.8: $|S_{21}|$ of zigzag antenna with Antenna A as the transmitter

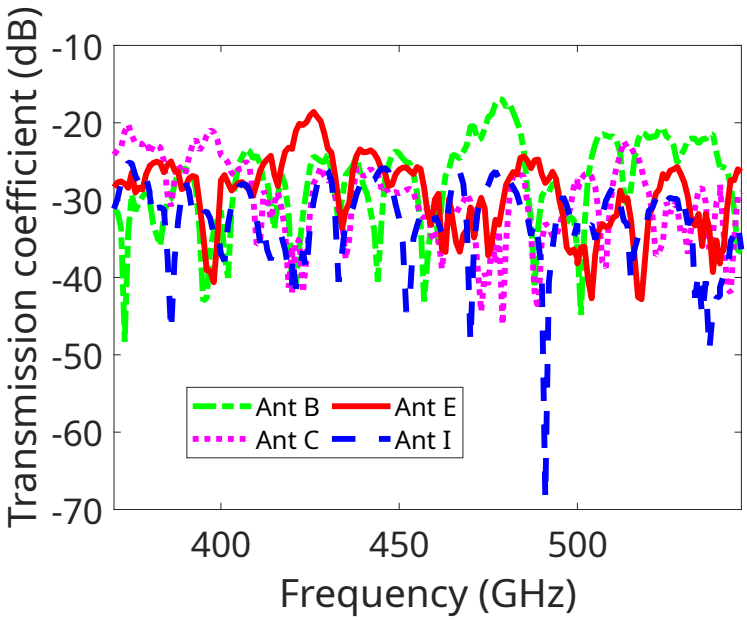
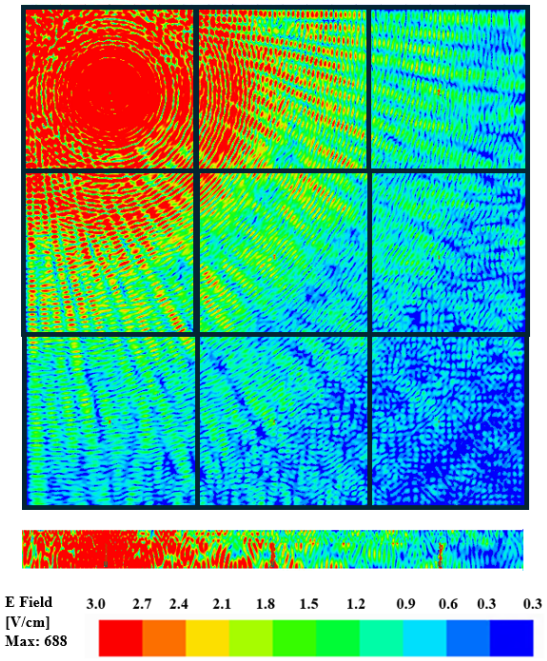


Figure 5.9: $|S_{21}|$ of dipole antenna with Antenna A as the transmitter

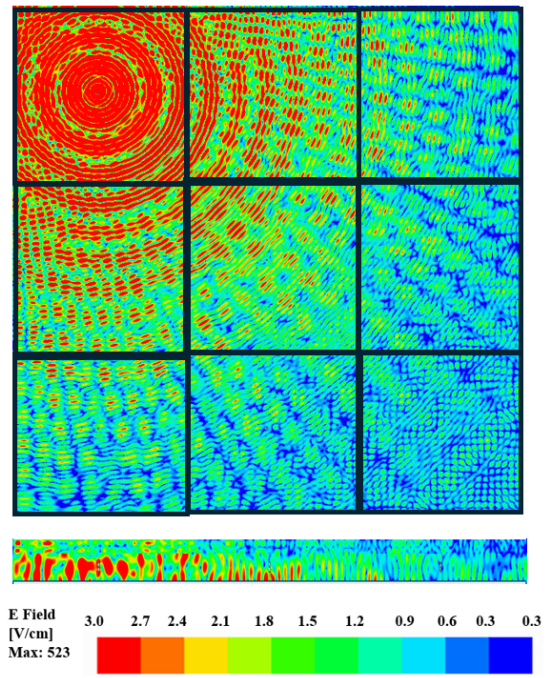
As shown in Figure 5.8, for the zigzag antenna at 462.5 GHz, the transmission coefficient $|S_{21}|$ between Antenna A and Antenna I is -33 dB, while that between Antenna A and Antenna C is -41 dB. These values indicate stronger reflection and attenuation in the case of Antenna I, as more of the transmitted wave is scattered from the enclosed chip surface before reaching the receiver. Similarly, Figure 5.9 shows the dipole antenna case at 446 GHz. Here, the transmission coefficients $|S_{21}|$ between Antenna A and Antenna I and between Antenna A and Antenna C are -28.26 dB and -28.98 dB, respectively. Despite Antenna I being located farther from Antenna A, the similarity of the transmission coefficients suggests that the wave experiences stronger reflections from the chip structure in the case of Antenna I.

The low transmission coefficient $|S_{21}|$ observed in both antenna cases is mainly due to (i) on-chip introduces losses due to substrate absorption and reflections from the chip packages and surrounding structures, (ii) the antenna gains and coupling efficiency between transmitting and receiving antennas also influence the transmission coefficient. The combined effect of these factors leads to a relatively low transmission coefficient.

5.4.2.2 Simulated E-field Distribution



(a)



(b)

Figure 5.10: Surface distribution of E-field magnitude (V/cm) on the die under **(a)** zigzag antenna excitation at 462.5 GHz and **(b)** dipole antenna excitation at 446 GHz

This observation is further validated by the e-field distributions across the surface of the chip, illustrated in Figures 5.10**(a)** and 5.10**(b)** for the zigzag and dipole antennas, respectively. The cross-sectional view demonstrates that the field intensity is highly concentrated near the excitation region of the antenna, while the lower-intensity waves extend across the chip surface and become significant for communication with other cores. In the case of intra-chip communication, these results confirm that surface waves constitute the dominant mechanism, consistent with prior findings [226].

A comparison of the field patterns indicates that the e-field distribution produced by the dipole antenna is more distorted than that of the zigzag antenna. This suggests that when designing on-chip antennas for intra-chip communication among processor cores in a multi-core architecture, careful evaluation of the field distribution is essential. Furthermore, if directional or phased-array antennas are employed for communication, diffraction effects arising from the compact chip environment and closely spaced components could distort the radiation beams, ultimately degrading the antenna gain.

It is also evident that the field distributions vary with frequency, as each antenna resonates at a distinct frequency corresponding to its maximum reflection coefficient. This frequency dependence highlights the importance of optimizing antenna design for the intended operational band.

5.4.2.3 Simulated Transmission Gain in Intra-Chip Communication Channels

Since there is no relative motion between the cores of a multi-core chip, the propagation channel under investigation can be regarded as time-invariant. The transmission gain (G_a) is defined as the cumulative gain that incorporates the transmit antenna gain, the receive antenna gain, and the propagation (path) gain. Experimentally, it is equivalent to the scattering parameter $|S_{21}|$, which quantifies the transmission efficiency from port 1 to port 2.

The transmission gain can be expressed using the Friis transmission equation [227]:

$$G_a = \frac{|S_{21}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_r G_t \left(\frac{\lambda}{4\pi r}\right)^2 e^{-2\alpha r} = \frac{P_r}{P_t} \tag{5.1}$$

where $|S_{21}|$ represents the coupling between the transmitter and receiver, while $|S_{11}|$ and $|S_{22}|$ denote the reflection coefficients at each end. G_t and G_r correspond to the transmitter and receiver antenna gains, respectively, P_t and P_r are the transmitted and received powers, λ is the free-space operating wavelength (648μ m and 672μ m for the zigzag and dipole antennas, respectively), α is the attenuation constant, and r is the separation distance between the antennas.

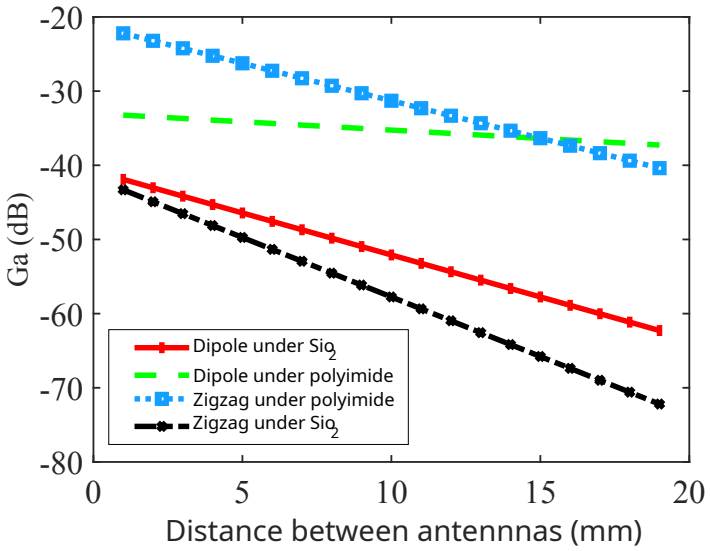


Figure 5.11: Simulated PDF for transmission-gain (G_a) dispersion.

Because these antennas operate within the confined and fixed physical environment of the chip, measurements are constrained by the structural characteristics of the medium. Consequently, the intra-chip channel model is inherently coupled with both the antenna design and the chip's electromagnetic environment. For this reason, a series of simulations and measurements of transmission gain (G_a) were performed between different antenna pairs as a function of distance. All results were obtained at

the resonant frequencies of the antennas, i.e., 462.5 GHz for the zigzag antenna and 446 GHz for the dipole antenna. The data were then post-processed using Equation (5.1), and the results are presented in Figure 5.11.

This study examined the effects of two distinct dielectric materials on antenna-to-antenna transmission gain by using silicon dioxide and polyimide as die substrates. As shown in Figure 5.11, the higher resistivity of silicon results in reduced transmission gain compared to polyimide. The maximum measurable separation was constrained to approximately 19 mm, corresponding to the longest possible path across a 13×13 mm^2 chip, where the maximum diagonal distance between centrally placed antennas is 18.38 mm.

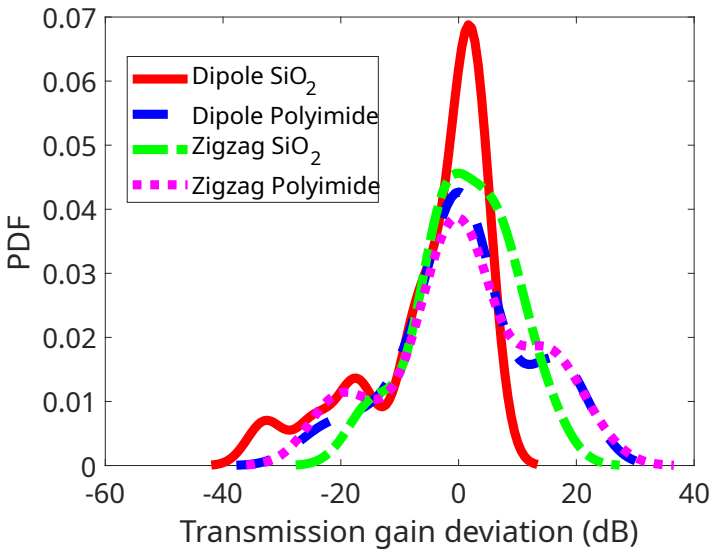


Figure 5.12: Simulated PDF for transmission-gain (G_a) dispersion.

The probability density function (PDF) of the transmission gain (G_a) variations is presented in Figure 5.12. The results indicate that the path loss in the simulated THz band ranges from approximately -40 dB to $+35$ dB. Notably, the dipole antenna beneath silicon dioxide exhibits greater fluctuations in transmission gain than the zigzag antenna. This analysis provides valuable insights for determining the link budget and estimating channel gain for intra-chip communication, enabling more accurate

performance prediction for specific configurations of antenna placement and orientation.

5.4.2.4 Link Budget Estimation for Intra-Chip Communication

The target of the analysis is to determine the achievable transmission performance between on-chip antennas by evaluating key parameters such as transmission coefficient (|S21|), insertion loss, and transmission gain across the operating THz frequency range. These metrics provide a direct measurement of coupling efficiency between antennas, propagation loss, and link reliability within the chip environment. By analyzing these parameters, the study establishes whether the proposed architecture can support practical intra- and inter-chip wireless communications.

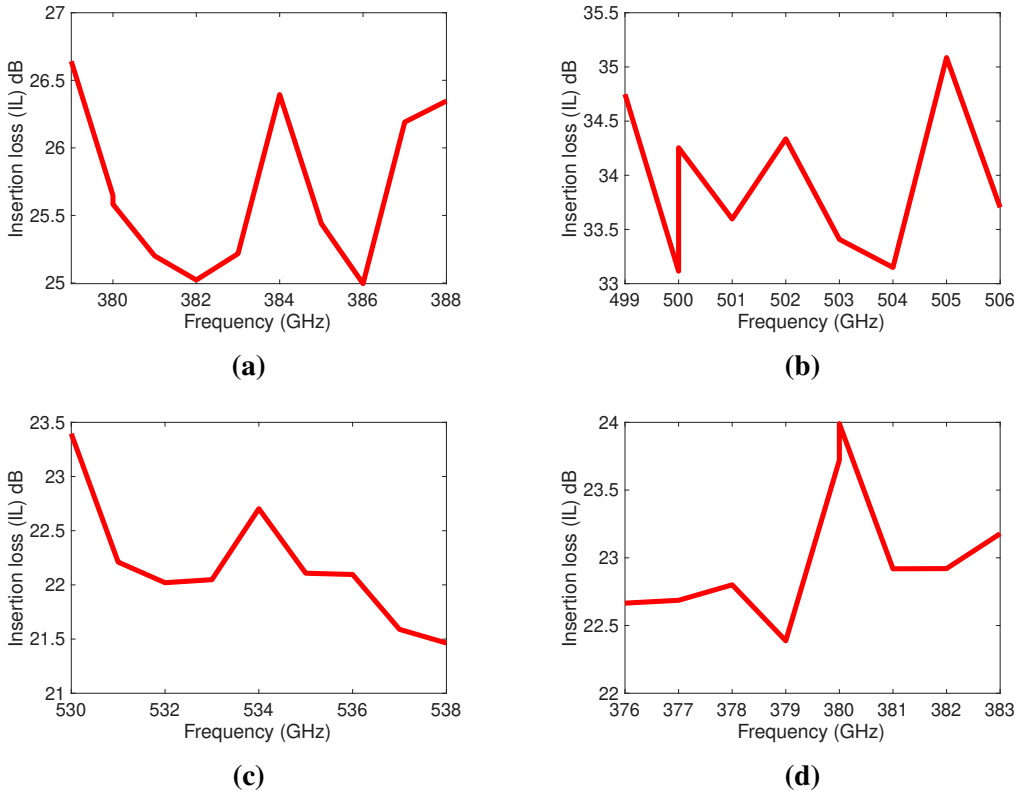


Figure 5.13: Simulated insertion loss (< 2 dB) of dipole antenna pairs with Antenna A transmitting to: **(a)** B, **(b)** C, **(c)** E, and **(d)** I.

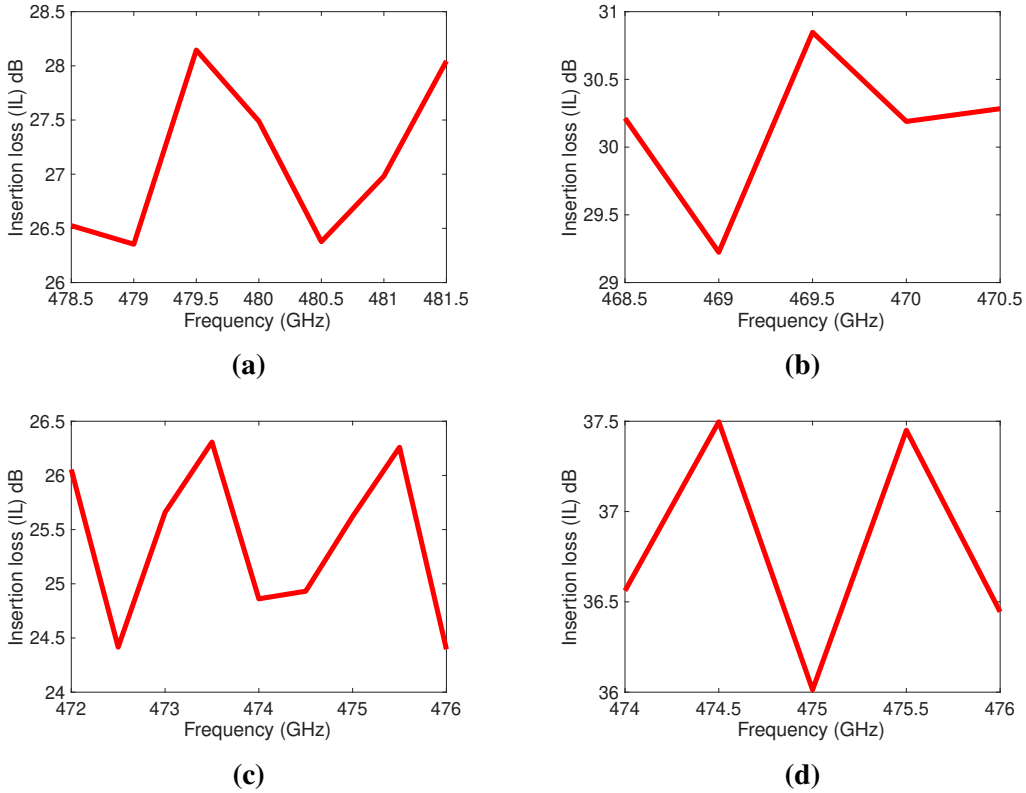


Figure 5.14: Simulated insertion loss (< 2 dB) of zigzag antenna pairs with Antenna A transmitting to: **(a)** B, **(b)** C, **(c)** E, and **(d)** I.

Figures 5.8 and 5.9 show the transmission coefficient S_{21} as a function of frequency, with Antenna A chosen as the reference. In this context, IL_{BA}, IL_{CA}, IL_{EA}, and IL_{IA} denote the insertion loss (IL) relative to Antenna A. The channel bandwidth is defined as the frequency range in which insertion loss satisfies $IL_{iA} < 2$ dB (where $i =$ B, C, E, I). A 2 dB threshold is commonly adopted to indicate a channel with minimal distortion [10].

Table 5.2: Bandwidth comparison of dipole and zigzag antennas for intra-chip communication

Core	Dipole BW (GHz)	Zigzag BW (GHz)
B	9 (379–388)	2 (468.5–470.5)
C	7 (499–506)	3 (478.5–481.5)
E	8 (530–538)	4 (472–476)
I	7 (376–383)	2 (474–476)

These results are presented in Figures 5.13 and 5.14, where the insertion loss remains below the 2 dB threshold. Importantly, all reported frequency bands fall within the -10 dB reflection coefficient region of the prospective antennas, ensuring reliable matching performance.

From the transmission characteristics provided in Table 5.2, a dedicated communication channel was established for each antenna pair. For the analysis of binary On-Off Keying (OOK) modulation, the minimum signal-to-noise ratio (SNR) required to achieve an error probability of 10^{-14} is assumed as $\text{SNR}_{\text{min}} = 24$ dB. This error probability indicates the likelihood that noise, interference, or other channel impairments cause the received signal to be incorrectly detected.

The noise power P_n is calculated as:

$$P_n = -174\,\text{dBm/Hz} + 10\log_{10}(BW) + NF \tag{5.2}$$

where -174 dBm/Hz is the thermal noise floor at room temperature, bW is the system bandwidth in Hz, and NF is the receiver noise figure (assumed to be 10 dB). The required received power and corresponding transmit power are then determined as:

$$P_{rx} = P_n + SNR_{\text{min}} \text{ and } P_{\text{tx}} = P_{rx} + \text{IL} \tag{5.3}$$

where IL represents the insertion loss between the antenna pair.

Finally, the energy-per-bit at the receiver and transmitter is given by:

$$E_{rx} = \frac{P_r}{R_b} \text{ and } E_{tx} = \frac{P_t}{R_b} \tag{5.4}$$

where P_r and P_t are the received and transmitted powers expressed in watts, and R_b is the bit rate. Using the measured insertion loss and bandwidths of each antenna configuration with Antenna A as the reference, the bit rate and the corresponding transmitter and receiver energy-per-bit values were computed according to Equation 5.2–5.4. The results are summarized in Table 5.3.

Table 5.3: Link-budget analysis with Antenna A as the transmitter for dipole and zigzag configurations.

Antenna Type	**Receiving Antennas**	**BW (GHz)**	**IL (dB)**	**Bit Rate (Gbps)**	**Energy per bit (J/bit)**	
					E_{tx}	E_{rx}
Dipole	B	9	-26.64	71.81	5.78e-16	1.25e-18
	C	7	-35.08	55.85	4.04e-15	1.25e-18
	E	8	-23.39	63.83	2.74e-16	1.25e-18
	G	7	-23.99	55.85	3.14e-16	1.25e-18
Zigzag	B	2	-28.14	15.96	8.17e-16	1.25e-18
	C	3	-30.84	23.94	1.52e-15	1.25e-18
	E	4	-26.30	31.91	5.35e-16	1.25e-18
	G	2	-37.49	15.96	7.03e-15	1.25e-18

5.5 Inter-chip Architecture

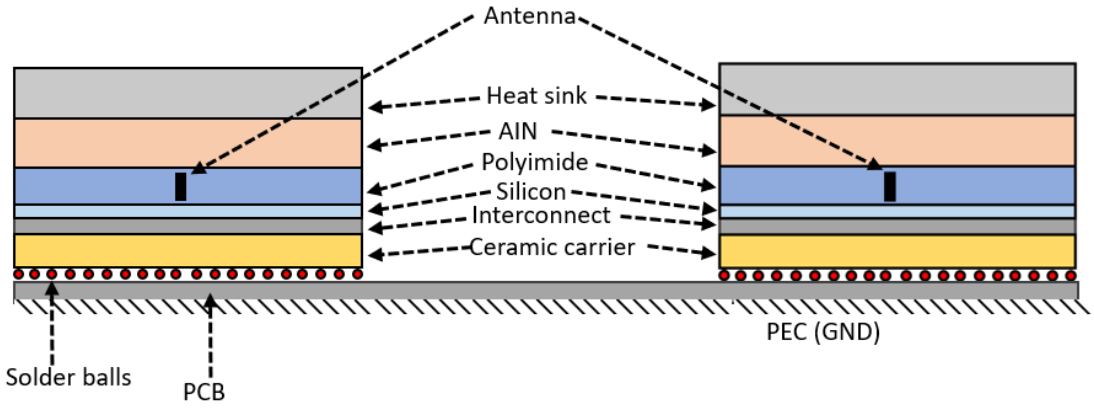


Figure 5.15: Inter-chip communication configuration [36]

The architecture was further extended to an inter-chip communication scenario, where two chips were mounted on a PCB substrate separated by 14 mm. Antennas positioned at the edges of each chip communicated through the package and PCB layers as illustrated in Figure 5.15. The PCB substrate was modeled using FR408 laminate with a relative permittivity of $\epsilon_r = 3.66$ and a loss tangent of $\tan\delta = 0.012$. The bottom surface of the PCB was defined as a perfect electric conductor (PEC) to emulate the ground plane. To account for the flip-chip packaging effects, a solder-ball array was incorporated, consisting of 25 balls with a diameter of 0.1 mm and a pitch of 0.25 mm. This configuration captures the structural and electromagnetic behavior of the inter-chip channel in a realistic packaging environment.

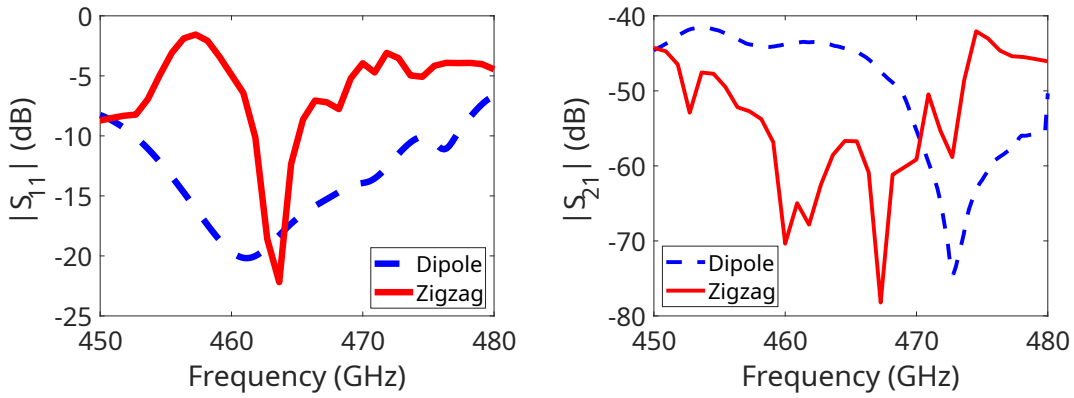
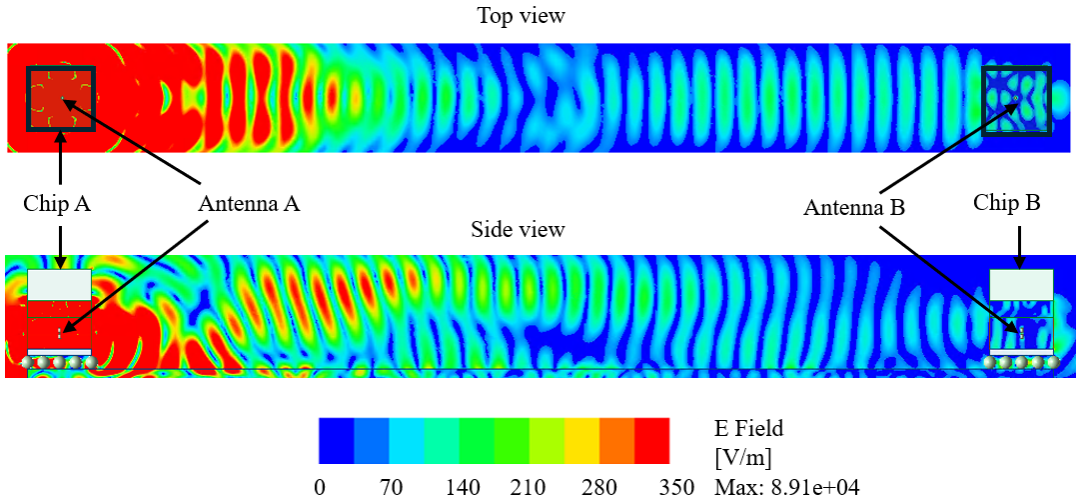
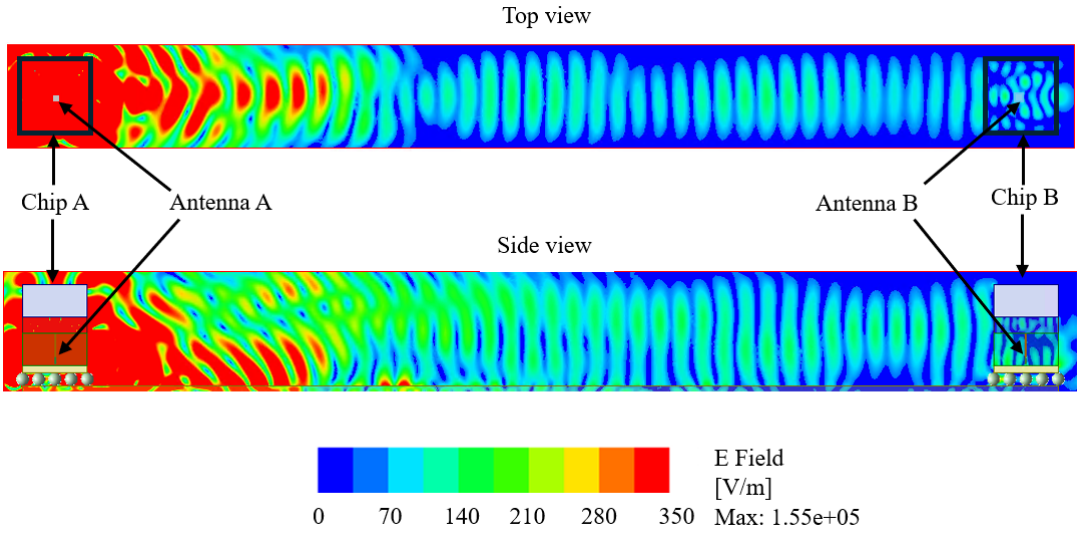


Figure 5.16: Simulated performance under inter-chip communication **(a)** $|S_{11}|$ and **(b)** $|S_{21}|$

The reflection coefficient ($|S_{11}|$) characteristics of both antennas are illustrated in Figure 5.16**(a)**. A minor variation in the inter-chip |S11| compared to the intra-chip case (Figure 5.7) is primarily attributed to the influence of the surrounding inter-chip packaging and structural environment. To simplify the simulation process and reduce computational complexity, only the antennas positioned along the chip edges were analyzed. The corresponding transmission performance between Antenna A and Antenna B is depicted in Figure 5.16**(b)**. The results indicate that the zigzag antenna exhibits a transmission coefficient near -60 dB, whereas the dipole antenna achieves approximately -43 dB. Although such elevated insertion losses can be challenging for practical implementations, a detailed assessment confirming the feasibility of communication under these loss conditions is presented in Appendix A.



(a)



(b)

Figure 5.17: Simulated e-field distribution across the inter-chip communication in the case of: **(a)** Dipole antenna and **(b)** Zigzag antenna [36]

We further analyzed the variation of the electric field distribution across the inter-chip communication structure. The top and side views of the field patterns for both the dipole and zigzag antennas are shown in Figures 5.17, where only Antenna A is excited. From the side view, it is evident that part of the radiated field is reflected by the aluminum heat sink (used in the simulation) and subsequently bounces back from the PCB substrate.

Under otherwise identical structural conditions, the maximum electric field magnitude is observed to be higher for the zigzag antenna compared to the dipole antenna. This indicates that the geometry of the inter-chip model, the die substrate properties, and the operating frequency all strongly influence the field distribution.

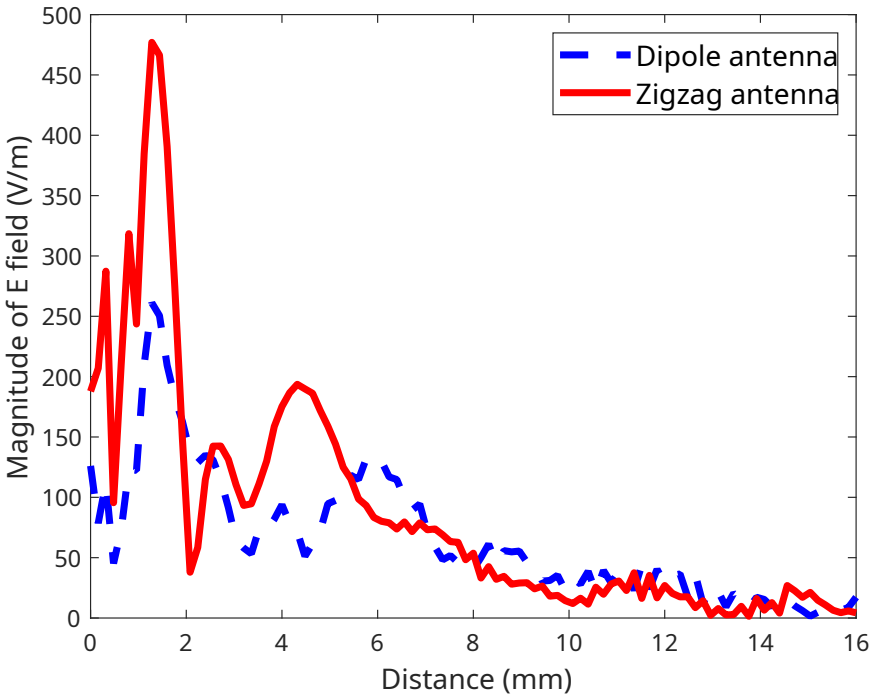


Figure 5.18: Electric field (V/m) along the line between Antennas A and B (A on)

In addition, Figure 5.18 presents the simulated electric field magnitude along the line connecting Antenna A and Antenna B. A distinct rise in field intensity is observed at approximately 4.5 mm for the zigzag antenna and 6 mm for the dipole antenna, which corresponds to reflections of the electric field from the bottom PCB structure. These observations highlight the importance of substrate interactions and package geometry in shaping inter-chip electromagnetic propagation.

5.6 Measurement Setup

In the measurement setup, through-silicon vias (TSVs) can be utilized to route RF signals from the source located on the top or outer layer to the antenna positioned on another layer of the chip package. TSVs serve as vertical electrical conduits that pass completely through a silicon die, enabling vertical interconnection and efficient signal delivery in multilayer structures [228]. A ground-signal-ground (GSG) probe is used to establish electrical contact with the top metal layer of the structure. The probe is connected to a vector network analyzer (VNA), which facilitates accurate S-parameter measurements [229].

Using this setup, the transmission coefficient (S_{21}) between the transmitting and receiving antennas can be measured, providing an estimate of the coupling and path loss between chips [230]. This allows the characterization of inter-chip RF communication performance in terms of signal transmission efficiency. Prior studies have reported inter-chip transmission coefficients in the range of -20 dB to -60 dB at THz frequencies, validating the use of S_{21} as a key performance indicator [231].

In addition to S-parameter measurements, the overall communication performance can be further evaluated through link budget analysis [232], and in a complete system, metrics such as bit error rate (BER) and data rate can be assessed by integrating the antenna with THz transceiver circuits. Although such system-level measurements are beyond the scope of this work, the obtained antenna characteristics, such as gain, radiation pattern, and $|S_{21}|$, provide a reliable indication of the feasibility of THz inter-chip communication.

5.7 Chapter Summary

This chapter has presented a consolidated investigation into the feasibility of employing terahertz (THz) wireless communication for intra- and inter-chip connectivity in multi-core processor architectures. By integrating the findings from two complementary studies, the discussion progressed from antenna-level characterization to system-level transceiver modeling within realistic flip-chip environments.

The first part of the work established the design and analysis of micron-scale dipole antennas for intra-chip wireless communication, demonstrating acceptable reflection and transmission coefficients and confirming the role of surface-wave propagation across the chip substrate. The results highlighted the importance of substrate selection and package layers in determining path loss and electric field distribution.

Building on this foundation, the subsequent study introduced a complete THz transceiver architecture and compared dipole and zigzag antenna designs for both intra- and inter-chip communication scenarios. While the dipole antenna exhibited wider bandwidths and higher data rates, the zigzag antenna achieved stronger and more uniform electric field distributions. Link budget analysis confirmed that both antenna configurations can achieve energy-per-bit values below 1 pJ/bit, validating their competitiveness with conventional wired interconnects even under high insertion-loss conditions.

Overall, the contributions presented in this chapter demonstrate that THz wireless links are not only technically viable but also energy-efficient alternatives to traditional metallic interconnects. These findings establish a solid foundation for the transition from proof-of-concept antenna designs to more integrated WNoC transceiver architectures. The broader implications, challenges, and future research directions will be discussed in the final concluding chapter of this thesis.

Chapter 6

Conclusion and Recommendations for Future Work

6.1 Conclusion

This thesis presented a comprehensive investigation into the design and modeling of advanced terahertz (THz) antenna systems and communication channels suitable for next-generation wireless and on-chip applications. Three major research contributions were addressed: (i) a stacked substrate integrated waveguide (SIW) pyramidal horn antenna, (ii) a broadband rectangular waveguide (RWG) to SIW mode converter antenna, and (iii) an on-chip THz communication channel model integrating antenna-based links. In Chapter 3, a five-layer stacked SIW-based pyramidal horn antenna was proposed to achieve compactness, high gain, and beam symmetry at $210\,\text{GHz}$. The design employed optimized slot coupling, Gaussian excitation, and dielectric loading to realize equal half-power beamwidths (HPBWs) in both the E- and H-planes. Full-wave simulations confirmed a peak gain of $10\,\text{dBi}$ and sidelobe levels of approximately $-17\,\text{dB}$, demonstrating efficient TE_{10}-mode propagation and suitability for THz front-end integration. Chapter 4 introduced a broadband, probe-less RWG-to-SIW mode converter enabling

efficient TE_{10}–to–TE_{20} mode transformation. The optimized transition exhibited low reflection, high coupling efficiency, and wideband impedance matching. The proposed converter provides a compact and planar interface between conventional metallic waveguides and integrated SIW structures, offering an effective feeding mechanism for on-chip or multilayer antenna systems.

In Chapter 5, a detailed analysis of intra- and inter-chip THz wireless communication channels was conducted. Using full-wave electromagnetic simulations, the study characterized propagation loss, coupling strength, and substrate influence on channel behavior. The results validated that on-chip antennas operating in the THz band can enable high-speed, low-interference data transfer for future wireless network-on-chip (WiNoC) architectures.

Collectively, the research advances the understanding of compact, high-performance, and integrable antenna structures for THz systems. The developed designs demonstrate that SIW-based architectures can overcome conventional fabrication and integration challenges, paving the way for efficient front-end modules and chip-level THz communication links.

6.2 Recommendations for Future Work

Although this research successfully demonstrated the theoretical design and full-wave simulation of several THz SIW-based mode converters and antenna structures, the experimental realization and system-level integration were beyond the present project's scope. The limitations primarily stemmed from restricted access to terahertz measurement facilities, high-precision micro-fabrication tools, and the significant cost associated with wafer-level processing. Consequently, the study focused on simulation-driven validation to establish the electromagnetic feasibility of the proposed designs. Nonetheless, the

identified future works are essential to advance the current outcomes toward practical THz systems. They address critical gaps such as fabrication verification, bandwidth optimization, active circuit integration, and on-chip channel characterization, ensuring that the developed concepts can transition from simulated prototypes to experimentally validated, fully functional THz interconnect and antenna modules. These recommendations can be outlined as follows:

1. **Fabrication and Measurement:** Future work should focus on micro-fabrication of the proposed SIW horn and mode converter using MEMS or deep reactive-ion etching (DRIE) processes. Experimental validation of gain, radiation patterns, and impedance characteristics will be crucial for verifying simulation accuracy at THz frequencies.

2. **Bandwidth Enhancement:** Further optimization using metamaterial or metasurface loading could improve bandwidth and reduce sidelobe levels. Incorporating reconfigurable or tunable dielectric layers may also enable frequency agility.

3. **Integration with Active Circuits:** The proposed SIW and mode converter structures should be co-designed with THz amplifiers, detectors, or mixers to realize complete transceiver modules compatible with CMOS or BiCMOS processes.

4. **Thermal and Material Characterization:** As THz systems operate at high frequencies and densities, analyzing the impact of temperature, conductor loss, and substrate anisotropy on performance will be valuable for practical deployment.

5. **On-Chip Channel Optimization:** Future research may explore multi-hop and multi-antenna configurations within chip packages to improve coverage, reduce coupling losses, and enhance data throughput in wireless network-on-chip systems.

6. **Experimental Channel Modeling:** Physical measurements of chip-to-chip propagation at THz frequencies can validate the simulation-based channel models presented, providing insights for future link-level and system-level design.

7. **Extension to Integrated Sensing and Communication (ISAC):** The developed antenna architectures can be further adapted for joint communication and sensing (JCAS) applications in the THz band, enabling simultaneous data transmission and environmental perception.

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Appendix A

Possibility of Communication with High Insertion Loss

This section examines the viability of achieving reliable communication when the transmission coefficient or insertion loss (IL) falls below -40 dB. It presents a quantitative evaluation of the required transmitted power and outlines possible strategies to optimize system performance under such high-loss conditions. The analysis begins with the following fundamental equations:

$$\text{Insertion Loss } (\text{IL}_{\text{dB}}) = 10 \times \log_{10}\left(\frac{P_{in}}{P_{out}}\right), \tag{A.1}$$

$$\text{Nosie Figure } (\text{NF}_{\text{dB}}) = 10 \times \log_{10}(F), \tag{A.2}$$

where, F is the noise factor and is given as $F = \frac{SNR_{in}}{SNR_{out}}$.

$$NoisePower(N_0) = KTBF, \tag{A.3}$$

where K denotes the Boltzmann constant (1.38×10^{-23} J/K), T represents the absolute

temperature (taken as 273.15 K plus an additional $50°$C to account for ambient conditions), and *F* corresponds to the linear noise factor, expressed as $10^{\frac{NF}{10}}$ from its dB value. Converting the noise power density, N_0, into dBm yields:

$$N_0(dBm) = 10 \times \log_{10}\left(\frac{KT_0BF}{1mW}\right), \tag{A.4}$$

Upon simplifying

$$N_0(dBm) = -173.5 + 10 \times \log_{10}(B) + NF \tag{A.5}$$

The required transmission power can now be determined for an insertion loss, $ILdB$, of 40 dB and a noise figure, *NF*, of approximately 10 dB, a representative value for terahertz (THz) communication systems. Under these conditions, the transmitted power ($P_{t(dBm)}$) is expressed as:

$$\begin{aligned} P_{t(dBm)} &= P_{r(dBm)} + IL_{dB} \\ &= N_{0(dBm)} + SNR_{dB} + IL_{dB} \\ &= -173.5 + 10 \times \log_{10}(B) + NF + SNR_{dB} + IL_{dB} \\ &= -173.5 + 10 \times \log_{10}(4 \times 10^9) + 10 + 24 + 40 \\ &= -3.479dBm \end{aligned} \tag{A.6}$$

A transmit power of -3.48 dBm is therefore feasible for modern THz links, even in the presence of high insertion loss.