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Low-Voltage Solid State DCCB Design Based on Bypassed Bidirectional Thyristor-Capacitor Suppressor

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***Abstract*—This article introduces a novel technique known as Bidirectional Thyristor Capacitor (BiTriCap) designed to interrupt DC currents effectively and mitigate power surges in low-voltage (LV) solid-state DC circuit breakers (SS-DCCB). The method employs parallel snubber capacitors to absorb switching effects, subsequently releasing stored energy during the subsequent switch operation. The model incorporates considerations for both line and load inductances, offering a realistic portrayal of a DC system and ensuring authentic protective measures. To validate the efficacy of this approach, practical results from the system are cross-referenced with simulation outputs, validating the credibility of the research findings. Additionally, an ARM microcontroller is programmed to control the sequence of actions among the active SS switches, optimizing their performance. The proposed LV SS-DCCB operates at a voltage level of *48 VDC* and nominal current of *8 A*. However, the design is scalable and can be extended to accommodate higher voltage and current ranges.**

***Index Terms*— Solid State-DCCB, Snubber Capacitor, Surge Absorption, DC Microgrid, Switching Effect, DC system Protection.**

I. INTRODUCTION

THE DC Circuit Breaker (DCCB) plays a crucial role in DC Microgrids (MGs) [1], protecting the load, line, and power supply [2]. In recent years, substantial research has been dedicated to refining SS-DCCB utilizing various surge absorption techniques. Notable among these are the SCR-BCB [3] with transformer, Metal Oxide Varistor (MOV), and several active components. Despite their effectiveness, these designs exhibit certain drawbacks, including increased complexity, cost, weight, and the introduction of additional surge sources, particularly in the primary winding of the transformer. Similarly, the TCB model proposed in [4] incorporates components such as MOV, transformer, thyristor, and diode. This design also channels surges through a transformer path, which results in similar weaknesses as the SCR-BCB design, including increased complexity and cost. Another technique, the SCBT and RB-IGCT models discussed in [5], employs an MOV-C snubber and MOV energy absorption parallel to the integrated gate-commutated thyristor (IGCT) structure. This approach emphasizes the role of capacitors in damping high-frequency voltage oscillations. DCCBs possess several critical characteristics that must be carefully considered during the design process. A primary concern, as highlighted in [6], is switching action time, which has been addressed through the development of a novel switch driving method. Equally important is the minimization of component count to enhance both cost-effectiveness and reliability. In [7], a passive clamping technique combining metal oxide varistors (MOVs) and capacitors is proposed to mitigate switching surges while minimizing component usage. The bidirectional capability of DCCBs, as explored in [8], offers significant advantages for medium-voltage and grid applications due to its ability to handle current flow in both directions. A comprehensive review in [9] evaluates the current state of solid-state circuit breakers (SSCBs) for low-voltage DC distribution systems, comparing various approaches in terms of fault response time, reliability, conduction losses, and complexity.

Regarding snubber circuits, [10] proposes a charged capacitor to accelerate switch action by providing a negative charge to rapidly absorb surges. In contrast, [11] introduces a novel oscillating-commutation SS-DCCB to enhance the switch performance and withstand shock. Moreover, [12] introduces the eMOV model, which decouples peak clamping from nominal DC voltage, allowing for lower voltage class devices and reduced conduction losses.

Concerted efforts are directed towards specialized components assigned the responsibility of absorbing the switching impact of the main switch, providing a protective shield to prevent damage [13]. Within this category of components, the MOV stands out as a widely adopted choice for mitigating surges in DCCBs [13]. However, in some of the surge absorption techniques, an LC branch is embedded in the

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design to commutate the current for the next action of providing the zero cross [13],[14].

The voltage and current characteristics of MOVs display nonlinear behavior, captured by the formulation presented in Eq. (1). The MOV activates when the circuit voltage exceeds the clamping voltage threshold. This crucial role in surge protection underscores its importance in ensuring the reliable operation of DCCBs [15].

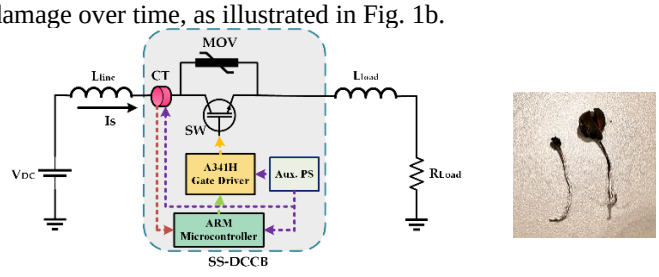
$$\log(v_{MOV}) = P_1 + P_2 log_{10}(i_s) + P_3 e^{-log_{10}(i_s)} + P_4 e^{log_{10}(i_s)} \quad (1)$$

The voltage across the MOV is represented by v_{MOV}, while the line current flowing through the MOV is denoted by i_s, with coefficients P_1 to P_4 being manufacturer-specified parameters.

However, the use of MOVs for DC surge absorption presents several limitations [15]. These include gradual deterioration, increased clamping voltage, current leakage, and heightened capacitance, all of which pose potential hazards to the system in DCCB application [15]. This letter proposes a significant advancement by eliminating MOV from DCCB designs and instead utilizing a snubber capacitor-based subcircuit to directly absorb the switching surge and block the passing current, thus reducing the stress on the main switch. This approach aims to address the issues associated with MOV, leveraging the low degradation rate of capacitors through simple charge and discharge sequences, thereby improving the overall safety and reliability of the system.

From a cost perspective, the total cost of a capacitor-based DCCB is cheaper than an MOV-based DCCB. Due to the high degradation rate of MOV, the lifespan and reliability of SS-DCCBs using capacitor surge absorbers would be higher than those using MOV. Although capacitor-based DCCBs require more active components compared to basic MOV-based DCCBs, their overall cost remains lower over time.

Fig. 1a illustrates the basic model of an MOV-based SS-DCCB. During a fault, the current level measured by the current sensor (CT) is transmitted to the ARM microcontroller. Subsequently, the ARM microcontroller sends a disconnection command to the gate driver of the active switch [13]. The released energy results in a surge across the switch, which is absorbed by the MOV. While this technique yields acceptable results, the degradation of the MOV can lead to component damage over time, as illustrated in Fig. 1b.



(a) (b)

Fig. 1. (a) MOV-based SS-DCCB circuit topology. (b) MOV damage observed during experimental testing.

As it can be seen from Fig. 2, MOV absorbs the surge in level of clamping voltage of the MOV. So, three stages of operation are defined in the switch operation, Normal operation, fault assessment, and energy absorption. After receiving the voltage level to the clamping voltage, MOV conducts, and the surge mitigates in this component. In consideration of MOV-based DCCB, the recommended clamping voltage rate is $1.5V_{DC} < V_{Clamp} < 2.5V_{DC}$ [16].

A primary challenge in DC circuits during fault scenarios stems from the absence of zero-crossing [17]. To effectively address this issue, this article introduces an innovative solution in the form of an active parallel subcircuit, utilizing thyristor-capacitor components. This designed subcircuit serves a dual purpose: it mitigates the surges induced by switching events and enhances fault detection capabilities within the DC system. By incorporating thyristor-capacitor elements, the proposed approach aims to offer a robust and efficient means of tackling challenges related to microprocessor-based fault detection and minimizing the impact of switching-induced surges in DC circuits.

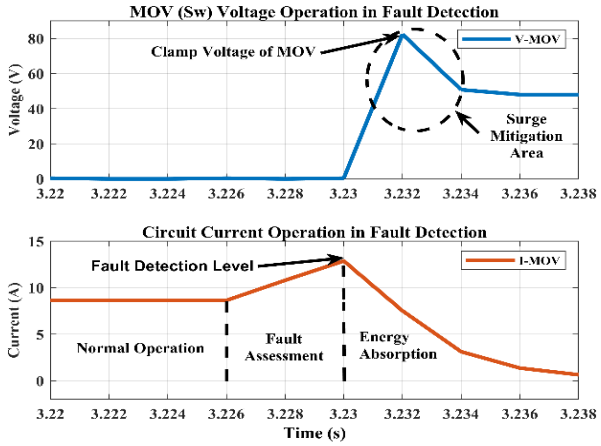


Fig. 2. Experimental Result: MOV (SW) voltage and line current in fault detection operation.

In this article, two separate tests are conducted to validate the proposed model of SS-DCCB. Initially, the phenomenon of DC circuit switching is explored, followed by an examination of fault detection within the model. In both instances, practical results are compared with simulation outcomes to validate their accuracy and alignment. This comparative analysis serves to affirm the credibility and robustness of the findings across both tests. The proposed model is tested with *48 VDC* and an *8 A* line current. However, the design can be expanded to higher voltage and current levels, considering the design prospects.

II. Proposed BiTriCap Technique Principal

The energy generated during the switching process in DCCBs is closely tied to the release of inductance within the circuit and distribution system. Previous discussions have centered around capacitor-based circuits acting as commutators to facilitate zero crossing with a series inductance in DCCBs [18]. However, this article presents a novel approach where the primary switching surge is redirected and mitigated through a capacitor-based subcircuit by activating a thyristor in its forward operation.

In this sequence, the aluminum film electrolytic snubber capacitor takes on the responsibility of absorbing the surge,

becoming fully charged in the process. Subsequently, in the ensuing operation, a backward thyristor is activated to discharge the capacitor through the designated resistor. This action readies the absorption circuit for subsequent performance, ensuring a controlled and optimized process for handling switching surges within DCCBs.

The fundamental role of a circuit breaker is to safely disconnect the circuit during system faults and maintenance operations. However, transients induced by current and voltage fluctuations resulting from faults and switching processes pose potential risks to the main switch, potentially leading to damage during disconnection.

Taking this concept into account, ensuring the safe performance of the switch becomes imperative. To achieve this, the surge current is rerouted away from the main switch through a bypassed snubber capacitor subcircuit, initiated by triggering a forward thyristor. This proactive measure diverts the surge current away from the main switch, protecting it from potential damage during circuit disconnection.

The entire process of mitigating surges is summarized in the bidirectional absorption and release or discharge of the capacitor's energy. The results are verified and compared with simulations. Furthermore, the suggested method demonstrates its capability to counteract faults in the reverse direction effectively.

Fig. 3 illustrates the blueprint of the envisioned model, featuring the strategic integration of the forward bypass thyristor (Tr_f). Its role is pivotal, absorbing any surge within the series capacitor. Conversely, during the backward flow, the thyristor in the reverse path (Tr_b) becomes active, discharging the accumulated energy within the system. To facilitate this intricate operation, precise control is maintained over all active switches, including the IGBT as the primary switch, along with both thyristors. This control is orchestrated by the STM32F407VG ARM microprocessor, which transmits commands through the gate driver systems.

The goal is to recreate an authentic DC system setup in the proposed model. As a result, both line and load inductances are thoroughly considered to ensure the realism and accuracy of the proposed model. This inclusion enables the simulation and analysis of the system's behavior under real-world conditions, ultimately enhancing its applicability and reliability in practical scenarios.

In the proposed model, the A341H IGBT Gate Drivers are employed to efficiently operate and initiate both the IGBT and thyristors within the circuit. Given the nature of thyristors as components reliant on current for triggering, a strategic setup is incorporated in the design. Two resistors are intentionally positioned along the connection path between the gate of the Thyristor and the gate drivers. This placement serves a dual purpose: firstly, to limit the output current of the gate driver, and secondly, to act as a protective measure for the microprocessor, thereby preventing any potential damage. This considerate arrangement ensures the controlled and safe activation of the thyristors, mitigating risks and optimizing the functionality of the entire circuit.

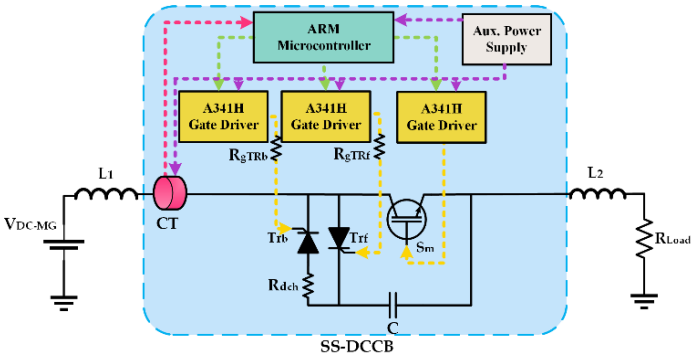


Fig. 3. The proposed BiTriCap based SS-DCCB

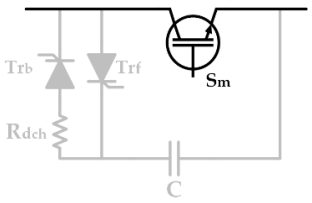
Effectively managing the IGBT involves both activation (ON) and deactivation (OFF) signals. However, only the ON signal is required when triggering the thyristor, as the thyristor autonomously switches off once the current crosses zero.

The duration for the thyristor to turn off depends on the charging (surge absorption) duration of the series capacitor. After the capacitor's charging cycle, it transitions into an open circuit, indicating the end of its conducting state. This characteristic behavior ensures that the thyristor's deactivation aligns with the completion of the capacitor's charging process, synchronizing the operational phases within the circuit.

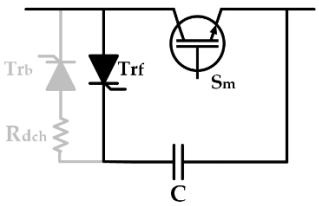
The sequential operation of the active switches within the proposed model is visually depicted in Fig. 4. During the standard operation of the SS-DCCB, the primary switch (S_m) remains connected. When it is time to switch, the forward path activates concurrently as the main switch begins its shutdown process. The energy released during this switch is then diverted into the forward path, as illustrated in Fig. 4.2. Subsequently, in the third step, the main switch is safely turned off without experiencing any disruption in the operation.

Moving on to the fourth operational step, following the absorption of any surge by the paralleled snubber capacitor, the forward thyristor automatically switches off, resulting in the successful disconnection of the entire system. To prepare for absorbing potential surges in the next switch, the capacitor discharges in the subsequent step, synchronizing this discharge with the brief activation of the IGBT.

Once the bypassed capacitor is fully discharged, the backward thyristor turns off, allowing the system to seamlessly resume its regular operation. This accurate sequence of steps ensures a smooth and controlled transition through various operational phases, effectively managing energy redirection, surge absorption, and system disconnection within the SS-DCCB setup.



1: S_m is ON



2: S_m and Tr_f are ON

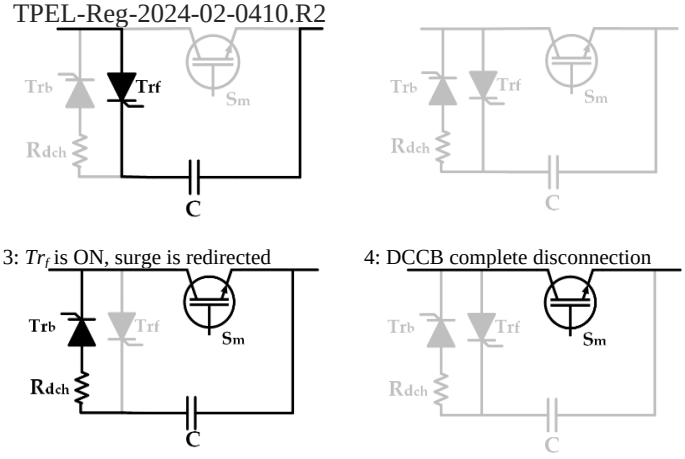


Fig. 4. Operational modes in the proposed circuit

Fig. 5 illustrates a switching diagram, elucidating the precise timing of each switch activation within every sequence. This diagram offers a visual representation that enhances understanding the synchronized switching instances throughout the operation.

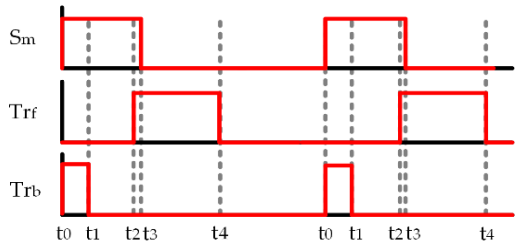


Fig. 5. Active components switching sequence

The calculation of the capacitor is grounded in the energy transformation between the circuit inductance and the capacitor. In fault detection scenarios, the stored inductive energy of the line and load side inductance is rapidly released. If this energy is not controlled, it can lead to damage to the main switch. In the proposed technique, the released energy is redirected into a mitigation path based on capacitors through the following circuit: $V_{DC\text{-}MG}$ - L_1 – Tr_f – C – L_2 - R_{Load}, ensuring this redirection occurs until the circuit current reaches zero.

As the energy released during the switching process is sourced from the stored energy in the circuit inductance (E_L), it can be represented using Eq. (2) as follows:

$$E_L = \frac{1}{2}(L_1 + L_2)I_L^2 \tag{2}$$

In this context, L_1 represents the inductance on the line side, while L_2 corresponds to the load side inductance. The computed level of stored energy relies on the square of the line current, I_L.

In the proposed circuit, the threshold tripping current is designated as I_L=*15 A*.

Upon disconnecting the main switch, it is imperative to dissipate the entire energy within the circuit. To protect the main switch from potential damage, this energy must be absorbed and redirected to the designated snubber capacitor. Consequently, the capacitance's energy ($E_{C_{min}}$) capacity should be at least equivalent to the inductive released energy, as outlined in Eqs. (3) and (4) in the following:

$$E_L = E_{C_{min}} \tag{3}$$

$$\frac{1}{2}C_{min}V_C = \frac{1}{2}(L_1 + L_2)I_L^2 \tag{4}$$

In this context, V_C signifies the maximum voltage across the capacitor.

Given the maximum current of *15.1 A* from the main path, the capacitor's maximum voltage would be *50 V* (An overvoltage exceeding *4.1%* above the nominal voltage is deemed acceptable across the snubber capacitor). Consequently, the capacitance (C) of the snubber capacitor to absorb the switching effect in the circuit can be computed as greater than *52 µF* using Eq. (5).

$$C \geq \frac{(L_1 + L_2)I_{L_{max}}^{\ 2}}{V_{L_{max}}^{\ 2}} \tag{5}$$

In the subsequent calculations, to determine the optimal amount of snubber capacitor (C) discharge resistance (R_{dch}) and the capacitor voltage during the discharge sequence (t_{dch}), Eq. (6) can be employed.

$$V_C(t) = v_0 e^{\left(\frac{-t_{dch}}{R_{dch}C}\right)} \tag{6}$$

TABLE I
PROPOSED SS-DCCB PARAMETERS

Parameter	Acronym	Value	Unit
Input DC Voltage (Chroma 6200H-100P)	$V_{DC\text{-}MG}$	48	V
Snubber Capacitor	C	470	µF
Microprocessor	ARM Microcontroller	STM32F407VG	-
Forward Thyristor	Tr_f	SKKT27B12E	-
Backward Thyristor	Tr_b	SKKT27B12E	-
Main Switch	S_m (IGBT)	IRGB4620D	-
Gate Driver	GD	A341H	-
Line Side Inductance	L1	21	µH
Load Side Inductance	L2	565	µH
Load Resistance (Chroma 63204)	R_{load}	6	Ω
Gate Resistance F	$RgTr_f$	20	Ω
Gate Resistance B	$RgTr_b$	20	Ω
Discharge Resistance	R_{dch}	50	Ω
Current Transformer	CT	LEM 100P	-

In this condition, the initial voltage of the capacitor (v_0) is v_0=Vc_{max}, and subsequently, the discharge resistance can be determined using Eq. (7).

$$R_{dch} = \frac{-t_{dch}}{C \times Ln(\frac{V(t)}{V_{C_{max}}})} \tag{7}$$

Therefore, based on Eq. (7), configuring the capacitor at *470 µF* will result in the attenuated current surge discharging through a *50* Ω resistor within *0.2 msec*.

For evaluation of DC system released energy, line and load inductors depending on being underground or overhead and the length of the lines therefore inductor have been calculated based on Eq. (8) per Kilometre (H/km), for an overhead transmission line [19]:

$$L = \frac{2 \times 10^{-4}}{\ln\left(\frac{D}{r}\right)} \quad (8)$$

And for underground line, Eq. (9), the inductor can be calculated as the equation below:

$$L = \frac{\mu_0}{2\pi} ln(\frac{2h}{r}) \times 1000 \quad (9)$$

In Eq. (8) and Eq. (9), L is the inductance per kilometre (in Henries per kilometre), r and D are the radius and diameter of the conductor (in meters) respectively, h is the depth of the conductor below the earth's surface (in meters), and μ_0 is the permeability of free space, approximately $4\pi \times 10-7\ H/m$.

The values of circuit components are presented in Table 1.

III. Circuit Switching Test

In this section, a switching test has been conducted to demonstrate the stability of the proposed technique. In this test, the main switch repeatedly connects and disconnects at a frequency of *0.5 Hz*, which represents the worst-case scenario for a DCCB. Subsequently, the capacitor and the main switch currents and voltages were monitored. The obtained results are subsequently validated through experimental testing. The measured values from this test confirm that the various sequences of the proposed technique operate as expected.

A. Simulation Analysis of Circuit Switching

This section discusses the MATLAB simulation results for the suggested model. Fig. 6 illustrates the voltage and current across the main switch. As observed, in both the ON and OFF states of operations, surges and switching spikes are redirected to the bypassed snubber subcircuit. The switching overcurrent is measured around *0.18 A*, and there are no voltage surges during the switching time. This indicates that the proposed model affirms the effectiveness of switching surge suppression through the suggested technique.

The switching test undergoes a voltage at *48 VDC*, with a nominal circuit current of *8 A*. This test validates the switching surge absorption before proceeding to the subsequent tests for fault detection and circuit interruption in DC systems. The entire surge is rerouted to the bypassed snubber subcircuit during this test.

Fig. 7 depicts the operation of the forward thyristor and snubber capacitor during surge redirection. Upon receiving the disconnection command, the forward thyristor activates a few milliseconds earlier to absorb the released energy from the circuit. Consequently, the main switch is successfully disconnected from the circuit without experiencing surges or overvoltage.

Additionally, Fig. 8 illustrates the performance of the snubber capacitor discharge during the second cycle of the main switch while in the ON-state, offering insights into the operation of the backward thyristor.

B. Practical Results of Circuit Switching

The laboratory prototype of the proposed SS-DCCB, utilizing the designed BiTriCap technique, is depicted in Fig. 9.

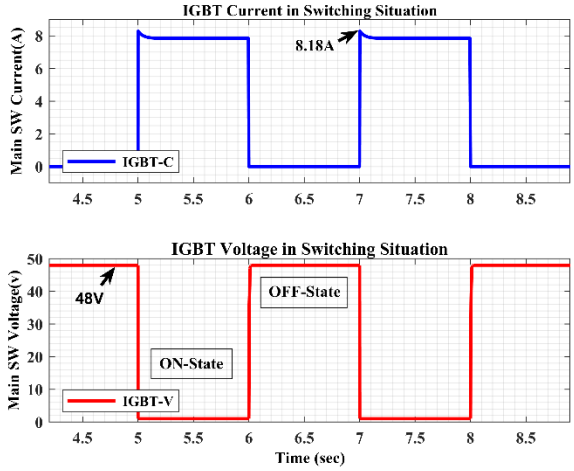


Fig. 6. Simulation Result: Main switch (IGBT) switching operation

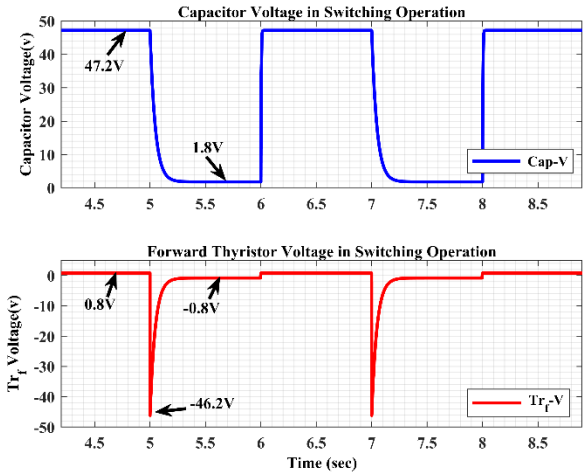


Fig. 7. Simulation Result: Forward thyristor and snubber capacitor voltage in switching operation

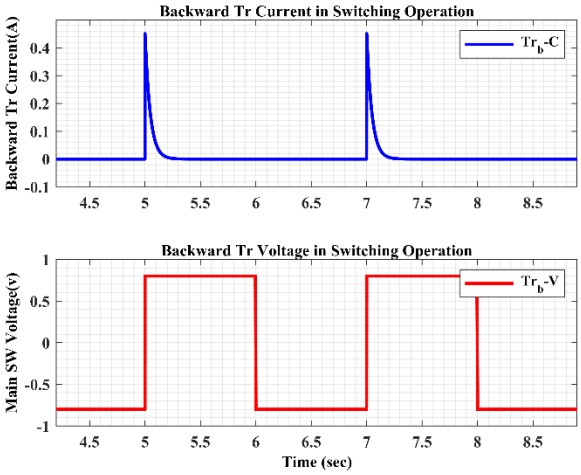


Fig. 8. Simulation Result: Backward Tr voltage and capacitor discharge current

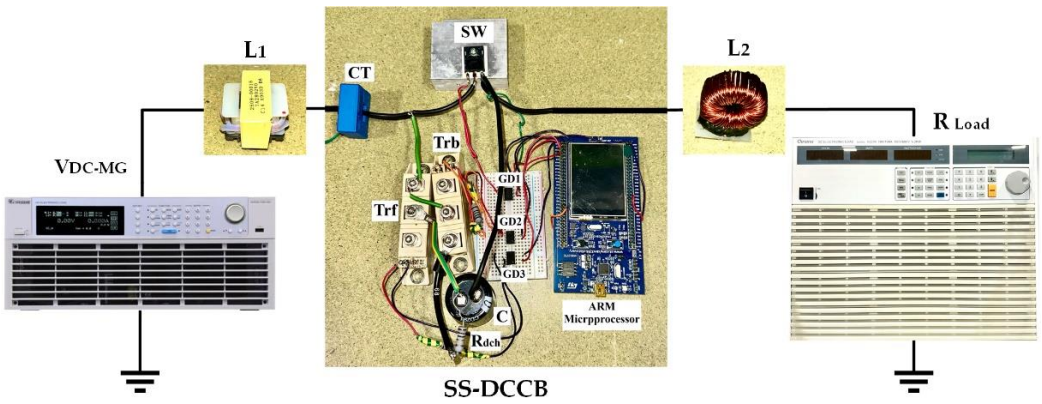


Fig. 9. Practical setup of the proposed SS-DCCB with BiTriCap surge absorption technique

In practical terms, the discharge time and switching speed are determined by the amount of released energy, contingent on the circuit inductance. For this test, inductances on both the line and load sides are considered within *20 μH* and *565 μH* to maximize the switching surge and accurately model the inductance of real-world low-voltage distribution systems.

The results illustrated in Fig. 10 validate the viability of the proposed technique. In previous research efforts, the current commutation technique employed parallel capacitor inductance to induce current fluctuations, facilitating the achievement of current zero-crossings, and subsequently absorbing the released energy through other parallel MOV branches [20].

However, the technique proposed in this article introduces a novel approach where the entirety of the surge and current surge is redirected into the snubber capacitor, leading to the elimination of MOV from the design.

During the interruption of the main system using the BiTriCap Technique, there is no tension or surge present across the main power (IGBT) switch. By employing this technique, the main switch is able to prolong its lifespan, while the SS-DCCB demonstrates reliable performance. This is because surges are directed away from the switch and redirected to the snubber subcircuit. Additionally, the capacitor undergoes a straightforward charge and discharge process, contributing to enhanced reliability.

IV. Fault Detection Analysis Test

In this section, a fault detection analysis test has been conducted to demonstrate the reliability and effectiveness of the proposed technique in identifying and responding to short-circuit faults. This test is necessary to ensure that the DCCB can accurately detect short-circuit conditions and disconnect the load as quickly as possible.

During this test, the circuit operates under normal conditions with a current of *8 A*, and a short-circuit is simulated as well. The fault detection mechanism is designed to sense an overcurrent above *15 A* and send a disconnecting signal to the circuit breaker. Additionally, the capacitor and main switch voltage and current are monitored to assess the effectiveness of the circuit.

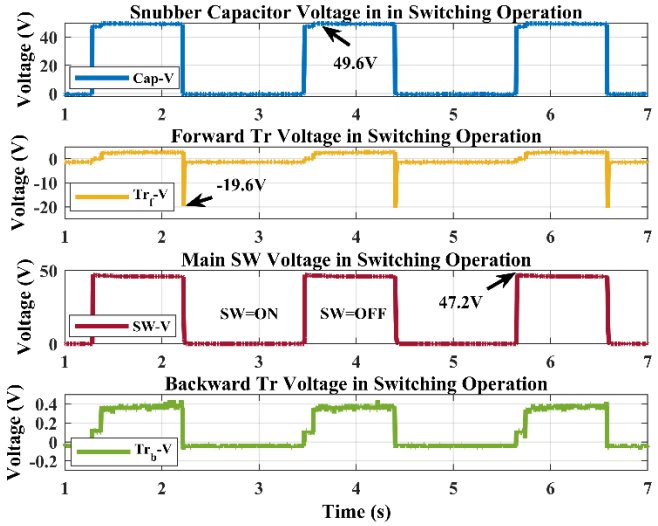


Fig. 10. Experimental Result: Test validation of switching operation

The obtained results, which were validated through experimental testing, indicate that the proposed technique, due to its simplicity in control, can immediately sense the overcurrent and effectively suppress the fault surge, providing robust protection against fault conditions as intended.

A. Simulation Analysis of Fault Detection

During the short-circuit or fault detection test of the BiTriCap technique, the nominal circuit voltage is set at *48 V*, the circuit current is specified as *8 A* (based on the defined *6* Ω load), and the fault detection trigger level by the microprocessor is established at *15 A*. The fault current *(I_f)*, illustrated in Fig. 11, flows from the short-circuited load through the line and load side inductances (L_1 and L_2), forward thyristor, and the bypassed snubber capacitor (C) and then to the power supply ($V_{DC\text{-}MG}$) when the IGBT switch is disconnected.

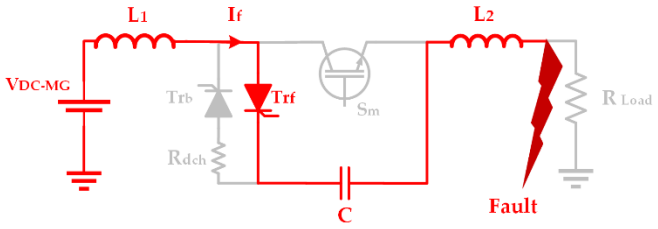


Fig. 11. SS-DCCB Fault current path

Therefore, it can be computed by Eq. (10) as follows.

$$I_f = \frac{V_{DC-MG}}{C(L_1 + L_2)s^2 + 1} \tag{10}$$

The initial inductance current (I_{L0}) during the fault period can be determined using the Eq. (11) provided below. In this formulation, t_{det} represents the fault detection time.

$$I_{L_0} = i_s + \frac{V_{DC-MG} t_{det}}{(L_1 + L_2)} \tag{11}$$

In this scenario, the calculation of the forward thyristor voltage (V_{Trf}) involves the consideration of the input voltage (V_{DC-MG}), system series inductances (L_1 and L_2), the snubber capacitor (C), and the initial inductance current (I_{L0}) during the fault time, as outlined in Eq. (12).

$$V_{Tr_f} = \frac{V_{DC-MG}}{s} - \left(\frac{2(L_1 + L_2)Cs^2 + 1}{Cs}\right) I_{L_0} \tag{12}$$

By employing the inverse Laplace transform, the temporal variation in the voltage across the forward thyristor during the fault time can be determined by Eq. (13) as follows.

$$v_{Tr_f}(t) = v_{DC-MG} - 2LI_{L_0}\cos(\omega_f t) - I_{L_0}\sin(\omega_f t) \tag{13}$$

Where $L=L_1+L_2$ represents the total system inductance, I_{L0} is the initial current of the system in fault condition, and $\omega_f=2\pi f$ is fault frequency dependent parameter.

Fig. 12 presents the flowchart of the programmed ARM microprocessor STM32F407VG. The SS-DCCB determines its course of action by measuring the current of the main system line in accordance with the defined restrictions and permissions in the circuit.

Upon detecting a fault through the embedded current transformer (CT) in the main current path, the microprocessor issues a breaking command, leading to the disconnection of the main switch following the sequences outlined in Fig. 3 and the flowchart presented in Fig. 12.

Fig. 13 illustrates one cycle of the circuit operation. A manual fault is introduced at *1.5* sec. Notably, when the measurement device detects a *15 A* threshold, the controller issues a trigger command to Tr_f, redirecting the fault effect and transmitting a disconnection command to the IGBT, which serves as the main circuit switch. The overvoltage during the breaking time, compared to the circuit voltage level, is approximately *2* volts, falling within an acceptable range.

During a fault occurrence, the capacitor voltage undergoes an instantaneous increase, effectively absorbing the circuit surge, and the current in the bypassed path drops to zero as the capacitor becomes charged. Subsequently, the thyristor turns off in accordance with its operating principle.

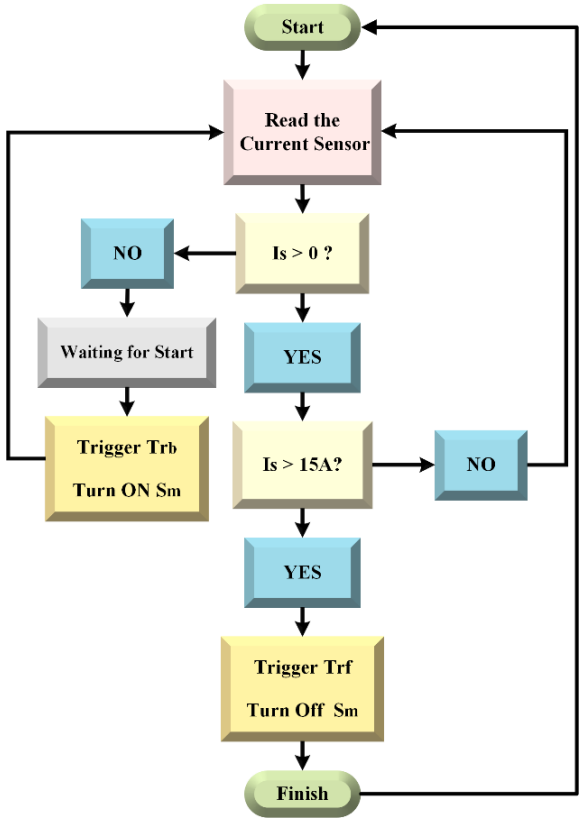


Fig. 12. Fault and short-circuit detection flowchart

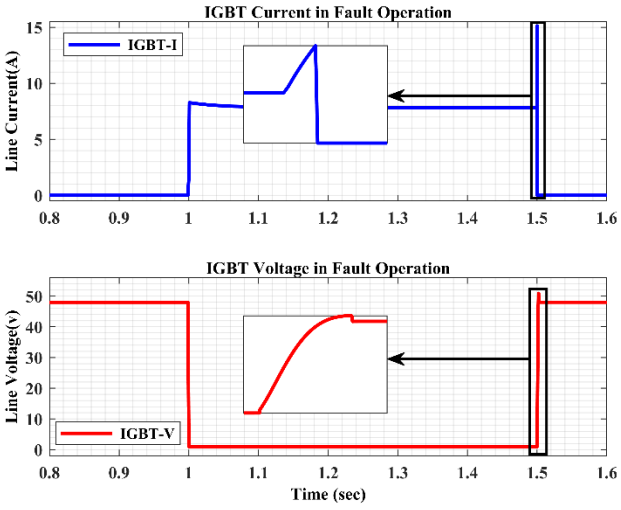


Fig. 13. Simulation Result: Main switch fault detection performance

Fig. 14 illustrates the behavior of the snubber capacitor and the voltage variation across the forward thyristor during the normal operation and at the time of fault detection. In the illustrated scenario, the capacitor discharges to *1.8 V*. At *1.5 sec* after the fault event begins, the capacitor voltage increases to *50 V* when the microprocessor triggers the forward thyristor to divert the surge. This dynamic reaction exemplifies how the system responds to the fault condition.

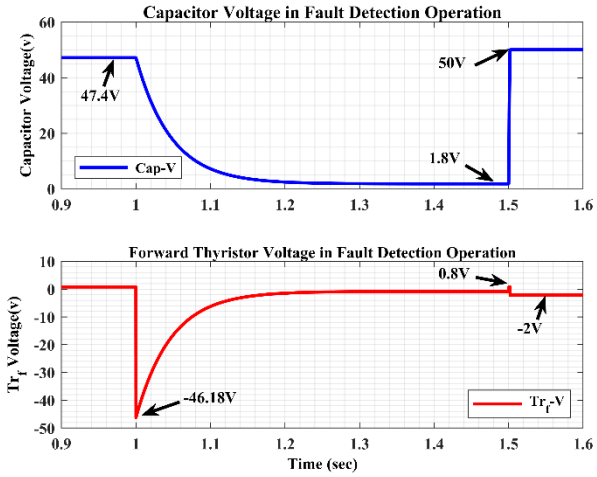


Fig. 14. Simulation Result: Capacitor and Tr_f voltage in fault detection operation

B. Experimental Validation of Fault Detection and Circuit Protection Capability

The experimental phase of the research validates the interruption test, as depicted in Fig. 15, which illustrates the voltage and current characteristics of the main switch in the proposed model. The outcomes closely align with the simulated results. The presented results indicate minimal overvoltage ($V_{max\text{-}Sm}$=*50 V*) and precise current interruption (I_f=*15.2 A*) observed at the main switch during fault detection. According to the circuit topology, when the microprocessor detects the current threshold, it immediately interrupts the main current path via S_m. In the proposed model, the rise time/fault clearing time, depicted in Fig. 15 as the time taken to increase the voltage from *10%* to *90%* of the input voltage ($V_{DC\text{-}MG}$), measures *116 µs*. Additionally, the main switch voltage rises to *50 V* quickly, without significant overvoltage. With this rise time, the fault frequency falls within the range of *8.62 kHz*. Therefore, when selecting the main switch, CT, and bypassed forward thyristor, it is crucial to consider covering this fault bandwidth. According to the datasheets of the components utilized in this research, the IGBT operates at a frequency of *5.8 MHz*, while both the CT and the Tr_f operate within a frequency range of *100 kHz*.

As shown in Fig. 16, the snubber capacitor effectively mitigated the short-circuit surge, resulting in the voltage level rising to full charge. When S_m is switched ON, a voltage of *-45.6 V* is observed across the forward Tr, which remains inactive. However, Tr_f operates instantaneously to redirect the surge into the snubber capacitor, stabilizing its voltage at *47.8 V*. During the switch operation, the capacitor discharges through the S_m-C-R_{dch}-Tr_b loop.

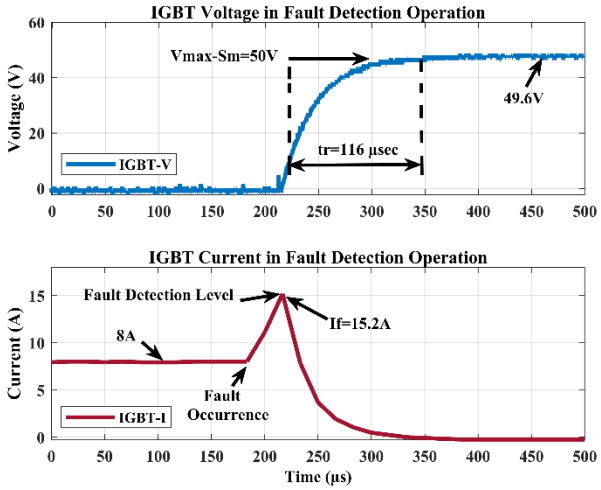


Fig. 15. Experimental Result: Validating Fault Detection for the Main Switch.

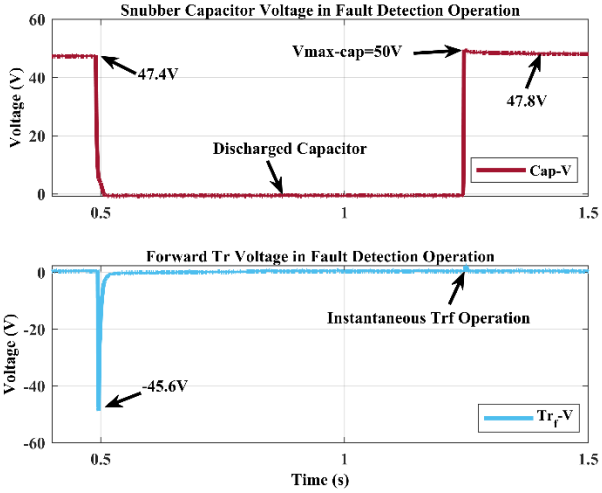


Fig. 16. Experimental Result: Snubber Capacitor and Forward Tr voltage

Tests were conducted using both aluminum film electrolytic capacitor and polypropylene film capacitor, producing consistent and comparable results. Due to the low cost of electrolytic capacitors in lower voltage ranges, it was included in this test. For designs requiring voltages above *500 VDC*, polypropylene capacitors are suitable.

Table 2 presents a concise comparison with previous research studies and a summary of the circuit topology and performance. It demonstrates the use of a straightforward design with minimal active components, achieving satisfactory results in mitigating the switching effects of SS-DCCB during fault detection operations in DC MGs. The real model of the DC system, considering line and load inductances, is employed in the presented DC system to observe the switch action in a real-world setting.

TABLE 2
TOPOLOGY COMPARISON

Reference	Proposed Model	[6]	[7]	[8]	[21]	[22]	[23]	[24]
Category	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB
Normal reclosing capability	Yes	YES	YES	YES	Yes	No	Yes	No
Switch Type	IGBT	IGBT	MOSFET	Thyristor	SiC MOSFET	SiC MOSFET	Thyristor	IGBT
Total Active components	2× Thyristor 1× IGBT	1 IGBT	>2 MOSFET	3×Thyristor 4× IGBT	2× SiC MOSFET	2× SiC MOSFET	6× Thyristor	6× Thyristor 3× IGBT
Diode	0	4	0	4	1	2	0	0
Capacitors	1	2	1	1	2	3	1	1
Inductors	0	6	0	0	1	0	0	1
Resistors	1	0	0	1	2	5	2	1
Level of circuit control complexity	Medium	LOW	Medium	High	Medium	Medium	High	High
Surge Absorber type	Capacitor	RLC	MOV-C	RC	MOV-RC	MOV-RC	TVS-RC	RLC
Mechanical Switches	0	0	0	0	0	3	1	0
Surge arresters	0	0	1	0	1	0	1	0

V. Conclusion

This research introduces an innovative and enhanced design of SS-DCCB based on the BiTriCap technique, aiming to provide enhanced protection and reduce overvoltage levels compared to MOV-based DCCBs. The effectiveness of the proposed design is evaluated through a series of switching and fault detection tests, and the results are systematically compared with simulation outcomes to validate the approach.

The orchestrated process is meticulously managed by a programmed microprocessor, which oversees and controls the DC line current in real-time. The microprocessor triggers interruption commands at predefined levels, ensuring the effective protection of the load. Notably, the observed overvoltage across the main switch is minimal, measuring only *2 volts*, a level well within the acceptable range.

The achieved success in zero current crossing is attributed to the innovative strategy of redirecting the surge into the bypassed snubber capacitor. This approach not only demonstrates the feasibility and efficacy of the proposed BiTriCap technique but also highlights its potential in enhancing the overall performance and reliability of SS-DCCBs in DC MGs.

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