Analysis of DC Breaking Phenomenon in DC Microgrids

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Preface

This thesis was developed at the School of Engineering, Computer and Mathematical Sciences, Auckland University of Technology, New Zealand, to satisfy the requirements for obtaining a Doctor of Philosophy (PhD) degree. The research was conducted from August 2021 to December 2024 under the guidance of Prof. Tek Tjing Lie and A/Prof. Kosala Gunawardane. This thesis aimed to develop the design of DC circuit breakers to effectively absorb DC surges in DC microgrids.

This exploration encompasses a mix of experimental and simulation inquiries and the formulation of theoretical models to propose an effective surge absorption technique. Furthermore, it underscores the impact of incorporating line and load inductances in solid state DCCB (SS-DCCB) performance. Several techniques including Bidirectional Thyristor- Capacitor (BiTriCap) Technique, Divided Surge Absorption Technique (DSAT) and Bidirectional Passive Techniques (BPT) are proposed in this research.

The insights garnered from this thesis have been encapsulated into manuscripts. Each chapter of the thesis begins with a clear delineation of the connection between the manuscript's content and the overarching theme of the thesis. Furthermore, every chapter is dedicated to elucidating the research presented within these manuscripts.

Acknowledgement

Completing this PhD journey has been an incredible endeavor, and it would not have been possible without the invaluable support, encouragement, and love of numerous individuals.

First and foremost, I wish to express my deepest gratitude to my supervisor, **Professor Tek Tjing Lie**, for his dedicated guidance, encouragement, and invaluable support throughout this research. His expertise and constructive feedback have been instrumental in shaping the direction and quality of my work.

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I owe a profound debt of gratitude to my **family**, who have been a constant source of support and inspiration. My **mother**, whose unconditional love and prayers have always been my beacon of hope, and my **father**, whose memory remains a guiding light in my life. My heartfelt thanks also go to my sister, **Somayyeh**, who taught me the true essence of resilience and how to live with purpose.

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To each of you, I am eternally grateful for your unwavering support, encouragement, and belief in my abilities. This thesis is not merely the culmination of my academic journey but also a reflection of the collective contributions, sacrifices, and guidance that you have generously offered me. It stands as a testament to your faith in me and the profound impact you have had on shaping my path to success.

Abstract

This PhD thesis explores the pivotal role of the switching phenomenon in the operational dynamics of DC microgrids (DC MGs), emphasizing the design and optimization of Solid-State DC Circuit Breakers (DCCBs) to manage switching surges. Predominantly switching surges pose significant challenges in DC systems, necessitating innovative solutions for effective mitigation. This research bridges the existing knowledge gap by introducing and evaluating advanced surge absorption techniques, aiming to enhance the reliability and protection of DC MG systems.

The study's central focus lies in the design, modeling, and experimental validation of 48VDC solid-state circuit breakers, with a threshold interruption current ranging between 10A and 20A. This selection corresponds to the voltage level specified in the Future Architecture of Network (FAN) Project and the capabilities of the laboratory's experimental facilities, providing a practical basis for testing. Various solid-state switches, including Insulated Gate Bipolar Transistors (IGBTs), Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), and Thyristors, along with their gate drivers, are utilized to investigate their performance under worst-case scenarios and real-world conditions.

To address the challenges of surge absorption, three novel techniques are proposed and extensively analyzed:

1. **Bidirectional Thyristor-Capacitor (BiTriCap) Technique**

This technique introduces a bypassed path with a snubber subcircuit comprising two antiparallel thyristors. These thyristors absorb the current surge during fault conditions and discharge a capacitor during normal operation. The BiTriCap technique effectively bypasses the surge through the capacitor, leveraging its charge-discharge dynamics. Its scalability across a wide voltage and current range makes it a versatile solution. Experimental validation considers worst-case scenarios with inductances in the millihenry range to simulate high-surge conditions.

2. Divided Surge Absorption Technique (DSAT)

The DSAT employs surge division principles, redirecting the load-side surge through a load-side diode and the line-side surge into a bypassed thyristor-RC subcircuit. This technique demonstrates high reliability and rapid surge absorption, significantly reducing voltage stress across the main switch.

3. Bidirectional Passive Technique (BPT)

Designed for bidirectional DC applications, the BPT uses a passive RCD subcircuit to filter and absorb surges. This method minimizes surge voltage across the main switch while simplifying circuit complexity by relying on fewer active components, making it a cost-effective and efficient solution for complex systems.

The thesis includes comparative analyses of these proposed techniques against conventional models, highlighting their efficacy in surge absorption, operational reliability, and scalability. Experimental results confirm the superiority of the proposed methods, offering significant improvements in performance and resilience.

This research contributes a comprehensive framework for the design and implementation of advanced DCCBs, paving the way for more robust and efficient DC MG systems. The proposed techniques demonstrate potential applicability across various voltage and current ranges, establishing a foundation for further exploration and commercialization in DC power systems.

Contents

Nomenclature

Description	Symbol	Description	Symbol
Microgrid	MG	Active Injected Circuit	AIC
Distributed Energy Resources	DER	Current Transformer	CT
DC Circuit Breaker	DCCB	Switch	Sw
Metal Oxide Varistor	MOV	Forward Thyristor	T_{rf}
Solid-State DCCB	SS-DCCB	Backward Thyristor	T_{rb}
Hybrid DCCB	H-DCCB	Main Switch	S_m
Circuit Breaker	CB	Line Inductance	L_1
AC Circuit Breaker	ACCB	Load Inductance	L_2
Surge Protection Device	SPD	Gate Resistance	R_g
Transient Voltage Suppressor	TVS	Load Resistance	R_L
Multi-Level DC-DC	ML DC-DC	Discharge Resistance	R_{dch}
High Voltage DC	HVDC	Gate Driver	GD
Bidirectional Thyristor-Capacitor	BiTriCap	Input Voltage	$V_{DC\text{-}MG}$ /V_s/V_{DC}
Divided Surge Absorber Technique	DSAT	Silicon Controlled Rectifier	SCR
Bidirectional Passive Technique	BPT	Medium Voltage	MV
Low Voltage	LV	Zero Current Source	ZSC
Photovoltaic	PV	Threshold Current	I_{th}

Bidirectional Breakover Device	BBD	Switching Time	t_{sw}
Common Mode	CM	Fault Current	I_f
Molded Case Circuit Breaker	MCCB	Damping Time	t_d
Mechanical DCCB	M-DCCB	Solid-State Circuit Breaker	SSCB
Ultra-fast Disconnector	UFD	Unidirectional SSCB	U-SSCB
Load Commutation Switch	LCS	Bidirectional SSCB	B-SSCB
Magnetic Coupling Fault Current Limiter	MC FCL	Surge Absorber	S.A.
Zero Source DCCB	Z-s DCCB	Control Circuit Complexity	C.C.C.
Active Thyristor CB	AT-CB	Passive Component	P.C.

Attestation of Authorship

I hereby declare that this submission is my own work and that the work presented in this thesis is solely based on my own research. The content of this PhD work is original, except where the work is referenced. I also declare that this work has not been submitted in whole or in part for the purpose of a degree or qualification at any degree-awarding institute. I declare that this thesis is my own work and contains nothing as an outcome of work done in internal and/or external collaboration.

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Mehdi Moradian

December 2024

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By signing you are confirming that the co-author contributions stated in the table(s) below are accurate.

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Manuscript Title:	DC Circuit Breaker Evolution, Design, and Analysis
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Chapter 4: Enhanced LV Solid-State DC Circuit Breaker Design with Divided Surge Absorption Technique	Mehdi Moradian	85
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I. Chapter 1:

Introduction

1 Background

A Microgrid (MG) integrates distributed energy resources (DERs) and controllable loads, enabling it to operate both with and without the main grid [1]. DC MGs facilitate the integration of renewable energy sources and use DC distribution systems, offering advantages such as negligible reactive power and low harmonics. The protection of DC MGs relies on DCCBs, which are crucial for maintaining system reliability and performance. However, the effects of switching phenomena in DC MGs need to be effectively addressed [2],[3].

The implementation of DC MGs presents significant challenges related to system protection, which has let to recent research focusing on improving DCCB designs. The primary challenge in DC MGs is the occurrence of arcs during current interruption, which does not cross zero and is more severe than in traditional AC networks with sinusoidal currents [4]. Consequently, the focus is on enhancing DCCB designs to prevent voltage and current surges that could damage the system. This can be approached in two ways: (i) by installing surge protection devices in all low-value circuit components in the grid, which is not technically viable, or (ii) by designing a novel circuit breaker that redirects the surge path internally, thus reducing its severity through advanced techniques.

To address these DC circuit protection challenges, DC Circuit Breaker technology has seen significant improvements, with three main topologies currently presented [5],[6],[7]: 1. Mechanical (Resonance) DCCBs, 2. Solid-state (Static) DCCBs, and 3. Hybrid DCCBs. However, mechanical DCCBs do not meet the fast-switching requirements of DC systems, as their interruption time is in the millisecond range. As a result, solid-state (SS-DCCBs) and hybrid (H-DCCBs) models are more commonly used and remain under research for various voltage levels and applications in DC MGs.

In terms of design topologies, recent advancements have introduced various surge absorption techniques, such as Metal Oxide Varistor (MOV)-based surge absorption [8],[9],[10], MOV-RC techniques [11],[12],[13], and Z-Source topologies [14],[15], applied to both unidirectional [16],[17] and bidirectional DCCB configurations [18]. However, the use of MOV's in DC applications is limited due to their inherent weakness such as a high rate of gradual degradation, leakage current, increased clamping voltage, and elevated capacitance, which restrict its effectiveness in such environments [19]. To mitigate these limitations, some designs propose

reducing the continuous presence of MOVs by adding a switch in series with the MOV [18]. While this approach helps minimize MOV usage, it introduces the complexity of an active switch, which increases the overall circuit control complexity [20]. Despite the effectiveness of these designs, there are still significant gaps in DCCB design, necessitating improvements to make these solutions more applicable to real-world scenarios.

2 Significance of DC Circuit Breaker Surge Absorption

The enhancement of renewable energy systems, DC MGs, and multi-port DC grids and DC applications necessitates an urgent requirement for DCCB technology with faster switching speed, robust switching capacity, higher reliability, and an economical design. However, designing a DCCB poses several challenges, including the need to break a high current within microseconds due to the high fault current in DC grids compared to AC grids caused by the low line impedance of DC lines. In addition, unlike AC grids, the arc in the circuit breaker (CB) under current interruption is not naturally extinguished by the system in DC grids, so the CB itself must provide the zero current crossing (see Figure 1), and the circuit must be designed for damping the shocks [21]. Furthermore, in DC grids, the magnetic energy is stored in the system inductance, and the DCCB must dissipate this energy. Also, the DC breaker must withstand the residual over-voltages after current interruption. These challenges make the DCCB topology fundamentally different from ACCBs, as they are typically fabricated based on semiconductor technology, MOVs, and ultra-fast switches. To address these challenges, our research focuses on developing novel DCCB designs and techniques aimed at enhancing surge damping and enabling rapid energy dissipation.

3 Faults in DC Systems

If we consider a DC system with a two-pole setup, there are two primary types of faults that can occur: pole-to-ground fault and pole-to-pole fault. These faults are illustrated in Figure 2. Pole-to-ground fault is more frequent, whereas pole-to-pole fault is more severe as it causes voltage and current shocks [22]. The predicted behaviour of the fault types discussed in DC circuits can be categorized into three sectors such as

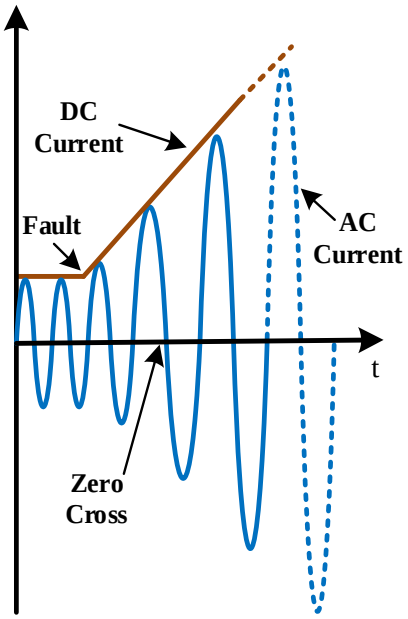


Figure 1. Conceptual Waveform of Current in DC vs AC systems

1. The capacitor discharge phase, in which the DC side capacitor rapidly discharges as soon as the fault occurs.
2. The freewheeling diode phase, where the converter voltage drops to zero, and currents flow through the diodes of the converter station since the solid-state components in the converter are probably blocked. In this phase, the converter behaves like an uncontrolled rectifier.
3. Finally, the AC side feeding phase, the fault is eventually supplied by the AC grid.

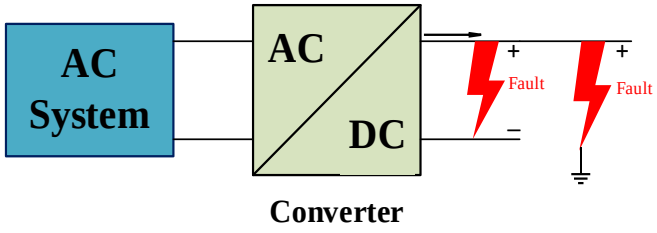


Figure 2. Different kinds of faults in DC systems.

Due to the fast escalation of fault currents, achieving the necessary interruption speed criteria for fault protection is challenging. The abrupt surge in fault currents in DC systems has the potential to cause harm to the freewheeling diodes located in converter stations. Therefore, it is vital for the DCCB to trip before any damage occurs to the diodes. The protective system must be devised to eliminate faults in a matter of milliseconds [23].

4 Components Used in Surge Protection Circuits

A summary of used components in surge protection devices (SPD's) is compared in Table 1. So far, MOV due to its characteristics similarity to a variable resistor being the most applicable component in DC surge protection. However, other components are also used to absorb overvoltage surges in SPDs. The IEEE C62.41L standard provides a detailed comparison of different SPDs.

When designing circuits to protect against surges, the designer must ensure two significant factors:

1. The surge protectors don't interfere with the normal operation of the power conversion circuit.

2. The components used to absorb, divert, or attenuate surges are strong enough to handle them.

Table 1. IEEE C62.41Location Categories, Frequency of Occurrences, and Surge Waveforms [3]

Suppression Element	Advantage	Disadvantage	Expected Life
Gas Tube	Very high current handling capability	Very high firing voltage	Limited
	Low capacitance	Finite life cycle	
	High insulation resistance	Slow Response times	
		Non restoring under DC	
MOV	High current handling capability	Gradual degradation	Degrades
		High clamping voltage	
	Broad current spectrum	High capacitance	
	Broad voltage spectrum		
	Low clamping voltage	Limited surge current rating	Long

TVS Diode	Does not degrade	High capacitance for low voltage types	
	Broad voltage spectrum		
	Extremely fast response time		
TVS Thyristor	Does not degrade	Non-restoring under DC	Long
	Fast response time	Narrow voltage range	
	High current handling capability	Turn-off delay time	

It's also important for the surge protection system to be reliable, since a very powerful surge could destroy the surge protection components. There are two main types of transient suppressors: those that reduce the strength of transients and prevent them from reaching critical devices, and those that redirect transients away from sensitive loads while minimizing the residual voltage.

Gas tubes- which can also be referred to as GDTs, utilize an inert gas within their structure to ionize and conduct during a brief occurrence. The ionization process of the gas takes a certain amount of time, resulting in gas tubes taking multiple microseconds to activate or "fire."

Two fundamental types of p-n junction devices that can be used for protecting against transient surges are **TVS diodes and TVS thyristors**. These devices can be acquired as bidirectional devices with back-to-back configurations, making them appropriate for protecting against positive or negative surges that may occur at power or signal entry points. A TVS diode functions as a clamping device by blocking any voltages that go beyond its breakdown voltage, while a TVS thyristor operates as a crowbar device that triggers when over-voltages reach the break-over voltage. If the TVS diode experiences surges that exceed its rating, it has the potential to malfunction just like any other stressed semiconductor component.

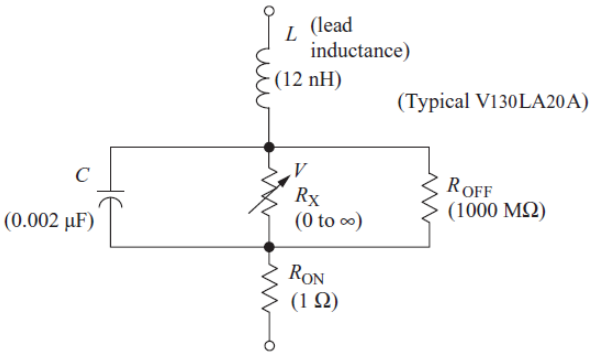
Once the TVS thyristors are switched on, the current flowing through them needs to be stopped or reduced below a specific threshold to restore their nonconductive state after the transient has passed. These thyristors are typically not suitable for DC power protection or low impedance

voltage sources because they may not return to nonconduction. For these types of applications, a TVS diode would be more appropriate.

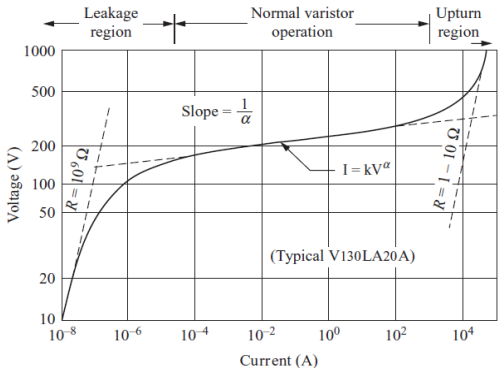
Capacitors and Inductors- Most AC surge protection designs incorporate capacitors and inductors as means of diverting and absorbing surges, which also serve as LC filters. By considering the mathematical form of $2\pi fL$ and $1/2\pi fC$ to calculate the impedance of an inductor and capacitor, respectively, we can determine their ability to filter out high-frequency surges that may be present on a 50 or 60 Hz power frequency waveform. However, In DC applications, the inductor acts as a source of surge energy during switching operations, making it essential to account for its shocks in the design process. Additionally, the capacitor, with its ability to absorb surges, serves as a valuable component in such designs.

MOV- Unlike the fuse or circuit breaker which offers over-current protection, the varistor provides over-voltage protection by means of voltage-clamping in a similar way to the back-to-back Zener diode. The word "Varistor" is a combination of the words VARI-able resi-STOR used to describe their mode of operation way back in their early days of development which is a little misleading since a varistor could not be manually varied like a potentiometer or rheostat.

Basic model and general evaluation of MOV is presented by GE, 1983 according to Figure 3a. In leakage region as illustrated in Figure 3b, circuit equivalent could be defined as Figure 3c and flow current in this region is very small. Furthermore, in normal operation (Figure 3d), MOV acts as a variable resistor. The behaviour of the component changes based on the circuit current and voltage value.



a. generalized equivalent



b. current-voltage characteristics curve

c. Leakage region equivalent d. Normal operation

Figure 3. MOV characteristics [3], [27]

As a weakness, MOV does not provide complete protection for electrical equipment. It provides no protection from sustained over-voltages that may result in damage to that equipment as well as to the protector device. Other sustained and harmful over-voltages may be lower and therefore ignored by a MOV device. MOV provides no equipment protection from inrush current surges (during equipment startup), from overcurrent (created by a short circuit), or from voltage sags (brownouts); it neither senses nor affects such events. Susceptibility of electronic equipment to these other electric power disturbances is defined by other aspects of the system design, either inside the equipment itself or externally by means such as a UPS, a voltage regulator or a surge protector with built-in overvoltage protection (which typically consists of a voltage-sensing circuit and a relay for disconnecting the AC input when the voltage reaches a danger threshold).

4.1 DCCB Principles

The primary objective of having a DCCB in DC systems is to protect the system against intentional or unintentional faults and voltage or current switching surges. Figure 4 provides a depiction of future flexible hybrid DC/AC microgrid protection scheme. The DCCBs are strategically situated in different areas of the grid, such as close to the distribution line, renewable energy sources, primary grid, battery storage, and loads, with the aim of protecting and maintenance of the microgrid [24]. There are various levels of current paths in the loop and from generation to load. Therefore, the types of DCCB are different. For instance, Schneider Electric presents a wide range of types of NW-DC, NSX-DC, C65H-DC, C65L-DC, and NG125 CBs for the applications of DC power supply, rail transit and photovoltaic (PV) power generation etc. in 500 up to 1000 V_{DC}. Or Eaton brand HMDLDC code is especially for photovoltaic industry in application range of 1000 V_{DC} [25].

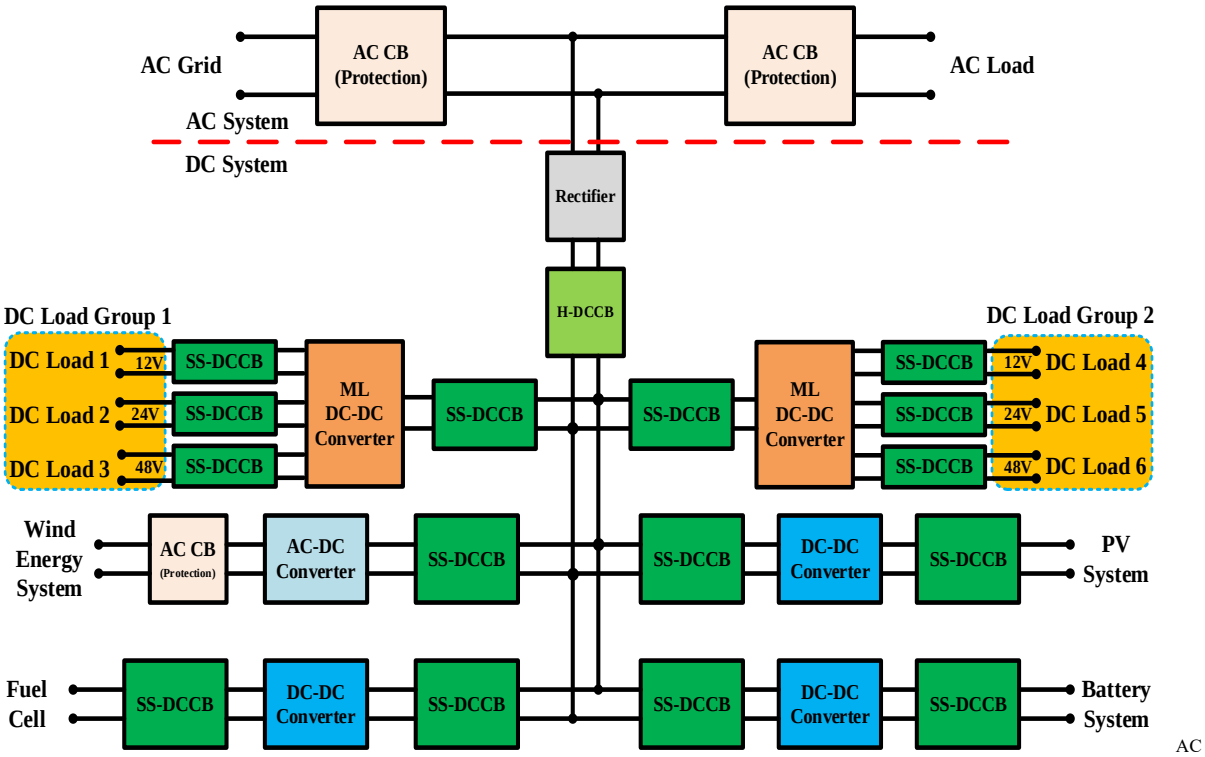
Figure 4 also illustrates the essential significance of DCCBs within the emerging DC MG framework. These microgrids, shaping future infrastructure development, depend greatly on commercially available SS-DCCBs to guarantee resilient circuit protection, as emphasized in [2]. A range of circuit breakers will be utilized, including the specialized Hybrid DCCB (H-DCCB) designed for high voltage situations, and the SS-DCCB primarily catering to medium and low voltage needs [26]. This varied selection of circuit breakers highlights the dynamic nature of DC MG design and functionality.

From the control perspective of DC systems, since all SS-DCCBs are controlled using microprocessors, an additional option is to connect all DCCBs to a central system controller. This allows for the implementation of DC MG control strategies, such as load shedding, and other techniques affecting generation, transmission, and consumption aspects.

Since, the placement of the DCCB in DC MGs is not predetermined, the maximum released energy is used to assess line and load inductances. However, system inductances can still be estimated based on whether the lines are overhead or underground [27].

Various existing DCCB designs, including the T-DCCB [28], soft SS-DCCB [9], and AT-CB [12] models, integrate components such as capacitors, MOVs, and other active elements. Although these designs are effective, they increase system complexity, cost, weight, and may introduce additional surge sources. Similarly, the TIM-Pack model [17], which uses MOV-C snubbers and parallel energy absorption components, faces comparable issues. Moreover, previous designs relying on capacitors for surge absorption have not sufficiently addressed cost concerns or accounted for the effects of load or line inductance on DCCB performance in real-world applications [27].

Furthermore, DCCBs are also utilized for maintaining the devices within the DC system. When a component of the system requires maintenance, the DCCB can safely interrupt the circuit, allowing the maintenance work to be carried out without posing a risk to personnel or damaging the equipment.



CB: AC Circuit Breaker, H-DCCB: Hybrid DCCB, SS-DCCB: Solid State DCCB, ML DC-DC Converter: Multi-Level DC-DC Converter,

Fig. 4: Future Flexible Hybrid DC/AC Microgrid Protection Scheme

Expanding of DC MGs in recent years due to its advantages compare with AC systems, has led to researchers focusing on various aspects of these systems. Specifically, this research focuses on the phenomenon of DC circuit breaking and to address the following questions.

5 DCCB Applications

As DC power technology advances, its application across various transmission systems has become increasingly widespread. DCCBs are now essential components in a range of settings. Additionally, the specific requirements for DCCBs vary significantly between different systems [29],[30].

5.1 DC Distribution Systems

DC distribution systems are commonly employed in urban and industrial settings due to their compatibility with renewable energy sources and energy storage systems. Circuit breakers ensure system safety by isolating faults promptly and maintaining uninterrupted operation of interconnected loads and energy sources [31].

5.2 DC Transmission

High-voltage DC (HVDC) transmission is a preferred solution for transferring power over long distances with minimal losses, especially when connecting remote renewable energy sites. Circuit breakers are critical for isolating faults, preventing system-wide disruptions, and enabling maintenance without halting power flow [32].

5.3 DC MGs

DC MGs are prevalent in isolated areas, military installations, and urban environments with a high reliance on renewable energy and batteries. Circuit breakers protect these systems from faults, facilitate smooth transitions between grid-connected and islanded modes, and support dynamic energy flows [33].

5.4 Rail and Traction Applications

Railway and metro systems heavily rely on DC power for traction motors and regenerative braking. Circuit breakers ensure operational safety by quickly clearing faults, protecting electrical equipment, and enabling seamless sectionalizing during maintenance or emergencies [34],[35].

5.5 Shipboard Systems

Modern ships incorporate DC-based integrated power systems to enhance efficiency and reduce environmental impact. Circuit breakers play a vital role in safeguarding propulsion systems, critical navigation controls, and communication networks, ensuring reliable operation even in challenging maritime conditions [36].

6 DC Aircraft

The shift toward more electric and all-electric aircraft designs depends on DC systems for powering avionics, propulsion, and other subsystems. Circuit breakers enhance onboard safety by isolating electrical faults, enabling modular system configurations, and ensuring consistent power distribution for essential operations [37].

7 Research Gaps and Questions

Despite the significant advancements in DC circuit breaker (DCCB) technologies, several critical gaps remain unaddressed in the context of surge absorption and system reliability. This research

identifies and categorizes these gaps as follows:

Part 1 – Surge Absorption with Minimal Degradation

- Conceptual Limitations: Existing DCCB designs primarily rely on MOVs for surge absorption, which are prone to degradation in DC applications. This limitation reduces their long-term reliability and necessitates the exploration of alternative components or configurations.

- Design Challenges: To extend the MOV lifespan, MOV-based techniques often require additional active components to disconnect MOVs post-surge, increasing circuit complexity. There is a need for simpler, more reliable surge absorption designs.

- Experimental Gaps: Current experimental studies inadequately address the scalability of DCCBs for real-world applications, particularly in terms of their ability to withstand repeated surge conditions without degradation.

- Validation Needs: Comparative analysis between conventional MOV-based designs and alternative solutions is limited, highlighting a need for more robust validation methodologies.

Part 2 – Passive Surge Absorption in Flexible Designs

- Conceptual Insights: Most studies focus on active subcircuits for surge management, which increases cost and control complexity. Passive solutions with comparable efficacy are underexplored.

- Design Limitations: The impact of passive elements, such as resistors, capacitors, and diodes, in reducing circuit complexity while maintaining surge absorption efficiency, needs further exploration.

- Mathematical Modeling: Existing models lack generalizability, often confined to specific voltage and current ranges, limiting their application to diverse DC systems.

Part 3 – Mitigating Line and Load Inductance Effects

- Conceptual Gaps: The role of line and load inductances in contributing to surge phenomena is well-known, but existing designs often overlook their comprehensive integration into DCCB performance models.

- Design Adaptability: Few studies propose scalable solutions capable of addressing the varying inductances of overhead and underground DC lines.

- Experimental Validation: The interaction between DCCBs and inductive components remains underexplored, particularly for bidirectional applications in complex DC microgrid environments.

To address these gaps, the following research questions are formulated:

1. What are the primary design and performance constraints of current DCCB technologies, particularly in terms of surge absorption and degradation?

2. How can the proposed DCCB designs mitigate issues such as zero-crossing challenges and surge absorption in DC switching phenomena?

3. Which components or configurations offer the most effective solution for managing DC surges with improved reliability and reduced degradation?

This research aims to bridge these gaps by proposing novel surge absorption techniques, validating their efficacy through modeling, simulation, and experimental testing, and providing scalable solutions adaptable to diverse DC microgrid applications. Through addressing these questions, the study contributes to the advancement of robust and reliable DCCB designs for the next generation of DC power systems.

8 Methodological Approach Overview

This research investigates the enhancement of surge absorption techniques in DCCBs to address challenges in DC MG systems. The methodological approach adopted in this thesis is structured around a blend of theoretical modeling, experimental validation, and simulation-based analyses, allowing for a comprehensive evaluation of novel DCCB designs. The methodology is divided into several interconnected phases:

8.1 Literature Review and Gap Identification

A thorough review of existing research on DC MGs and DCCB technologies was conducted to identify limitations in current surge absorption techniques. This phase established the foundation for the study by:

- Analyzing mechanical, solid-state, and hybrid DCCB topologies.

- Evaluating surge absorption techniques based on MOV, MOV-RC, and MOV-RCD surge absorbers, and identifying their limitations, including high degradation rates and complexity in active control schemes.

- Highlighting the need for innovative techniques that address real-world applications and scalability.

8.2 Design of Advanced Surge Absorption Techniques

The study proposes three innovative surge absorption methods:

- Bidirectional Thyristor-Capacitor (BiTriCap) Technique: Designed to manage surges through antiparallel thyristors and capacitors, this method leverages charge-discharge dynamics to mitigate high-current surges effectively.

- Divided Surge Absorption Technique (DSAT): Focused on unidirectional DC applications, DSAT divides surges into line-side and load-side components, minimizing voltage stress on the main switch.

- Bidirectional Passive Technique (BPT): Aimed at bidirectional DC systems, this method utilizes a fully passive RCD subcircuit to filter and absorb surges with high efficiency.

8.3 Theoretical Modeling and Simulation

The proposed techniques were modeled using MATLAB/Simscape simulation tool. The modeling phase included:

- Developing mathematical representations of the proposed techniques and DCCB switching phenomena.

- Simulating worst-case scenarios with varying line and load inductances to test the scalability and reliability of the techniques.

- Comparing the performance of proposed techniques against conventional designs.

8.4 Experimental Validation

Experimental studies were conducted to validate the theoretical models and simulations:

- A 48VDC solid-state circuit breaker was designed and tested, focusing on interruption currents between 10A and 20A.

- Components such as IGBTs, MOSFETs, and thyristors, along with their gate drivers, were assessed under controlled laboratory conditions.

- Scenarios involving inductances in the millihenry (mH) and microhenry (μH) range were created to replicate real-world high-surge conditions.

8.5 Comparative Analysis

The effectiveness of the proposed techniques was benchmarked against existing models:

- Performance metrics such as surge absorption capacity, reliability, scalability, and cost-efficiency were analyzed.

- Results were presented in terms of surge voltage reduction, fault isolation speed, and the ability to handle high fault currents.

8.6 Framework Development

Based on the findings, a comprehensive framework for DCCB design and implementation in DC MGs was developed:

- The framework integrates the proposed techniques into practical applications.

- It provides a scalable solution adaptable to various DC voltage and current ranges.

8.7 Manuscript Integration and Dissemination

The research outcomes were organized into individual manuscripts, each dedicated to a specific

technique or aspect of the study. These manuscripts were prepared for publication, ensuring rigorous peer review and academic dissemination.

9 Dissertation Structure Overview

This PhD Thesis is organized into six chapters, each contributing to the exploration and development of advanced DCCBs for DC MG applications. The structure aligns with the "Manuscript Format" as specified by Auckland University of Technology, ensuring that core chapters are self-contained and prepared for publication, while the introductory and concluding chapters provide a comprehensive narrative of the research.

Chapter 1: General Introduction

The opening chapter establishes the context for the research, detailing the challenges posed by switching surges in DC MGs and the significance of robust DCCB technology. It outlines the objectives, scope, and research questions, providing a foundation for the study. Key advancements in renewable energy systems and their implications on DC systems are discussed, emphasizing the necessity of novel surge absorption techniques.

Chapter 2: DC Circuit Breaker Evolution, Design, and Analysis

This chapter reviews the evolution of DCCB technology, contrasting traditional and contemporary designs. It provides a critical analysis of mechanical, solid-state, and hybrid DCCBs, identifying their advantages and limitations. The chapter highlights research gaps, particularly in surge absorption and scalability, setting the stage for the novel techniques proposed in subsequent chapters.

Chapter 3: Low-Voltage Solid State DCCB Design Based on Bypassed Bidirectional Thyristor-Capacitor Suppressor

This chapter introduces the **Bidirectional Thyristor-Capacitor (BiTriCap) Technique**, detailing its design and functionality. Experimental results are presented to validate its performance in mitigating surges under worst-case scenarios, showcasing its potential for scalable applications in DC MGs.

Chapter 4: Enhanced LV Solid-State DC Circuit Breaker Design with Divided Surge Absorption

Technique

The focus of this chapter is the **Divided Surge Absorption Technique (DSAT)**, a novel approach for unidirectional surge absorption. The chapter discusses its implementation, operational reliability, and effectiveness in reducing voltage stress across switches. Comparative analyses with conventional methods highlight its advantages.

Chapter 5: Bidirectional Solid State Circuit Breaker with Passive Surge Absorber for LV Applications

This chapter introduces the **Bidirectional Passive Technique (BPT)** for bidirectional DC applications. The design's simplicity and efficiency are emphasized, with experimental validation confirming its suitability for complex DC systems. Its cost-effectiveness and applicability to various voltage and current ranges are discussed in detail.

Chapter 6: Conclusion and Future Research Directions

The final chapter synthesizes the research findings, summarizing the contributions of the proposed techniques to the field of DCCB design. It reflects on the objectives, evaluates the research's impact, and identifies potential avenues for further exploration, such as the integration of advanced materials and real-time adaptive systems in DCCB technology.

Each chapter is designed to be self-contained while contributing to the overarching theme of enhancing DCCB performance and reliability. The combination of theoretical insights, simulation analyses, and experimental validations ensures a holistic approach to addressing the challenges in DC MG protection.

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II. Chapter 2:

Manuscript 1 – Literature Review

This chapter reviews the evolution, design, and performance analysis of DCCBs with a focus on solid-state technologies for DC microgrids. It highlights the challenges in designing DCCBs, such as rapid fault interruption and energy absorption, emphasizing their critical role in protecting modern power systems. The text classifies DCCB topologies into mechanical, solid-state, and hybrid types, examining their features, advantages, and limitations. Additionally, it explores energy absorption techniques, including MOV-based, capacitor-based, and hybrid designs, while proposing improvements for reliability, efficiency, and cost-effectiveness in DCCB systems to support future power systems.

Review

DC Circuit Breaker Evolution, Design, and Analysis

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Abstract: While traditional AC mechanical circuit breakers have been competent for protecting AC circuits, high penetration of DC power distribution technologies like DC microgrids (MGs) obligate better disruption performance features such as quick and reliable switching speeds. However, a DC circuit breaker (DCCB) novel design is challenging due to the need to quickly break high currents within milliseconds, caused by the high fault current rise in DC grids compared to AC grids. In DC grids, the circuit breaker must provide zero current crossing and be designed for absorbing surges since the arc is not naturally extinguished by the system. Additionally, the DC breaker must mitigate the magnetic energy stored in the system inductance and withstand residual over-voltages after current interruption. These challenges require a fundamentally different topology for DCCBs, which are typically made using solid-state semiconductor technology, metal oxide varistors (MOV), and ultra-fast switches. This study aims to provide a comprehensive review on development, design, and performance description of DCCBs in parallel with a specific concentration on analysis of internal topology, energy absorption path and sub-circuits in Solid-State (SS)-based DCCBs. The research explores various novel designs that introduce different structures for energy dissipation solution. The classification of these designs is based on the fundamental principles of surge mitigation and a detailed analysis of the techniques employed in DCCBs. In addition, our framework offers an advantageous reference point for the future evolution of SS-circuit breakers in numerous developing power delivery systems.

Keywords: DC circuit breaker, Mechanical DCCB, Sloid-state DCCB, Hybrid DCCB, DC Microgrids, DC circuit breaker topology, Metal oxide varistor, Surge absorption.

1 Introduction

DC microgrids (MGs) are a modern form of electricity distribution system that use DC instead of AC to transmit and distribute electrical energy. In a DC MG, various distributed energy resources (DERs) such as photovoltaic (PV) systems, wind turbines, and energy storage devices are connected to a common DC bus through power electronics interfaces. In recent years, DC MGs are becoming increasingly popular due to their numerous advantages over traditional AC grids, including improved energy efficiency, higher power quality, greater flexibility, and economical reasons in integrating renewable energy sources [1]-[3]. They are also considered to be an important solution for addressing the challenges of the increasing demand for electricity, energy security, and climate change mitigation.

However, the design and operation of DC MGs pose unique challenges, such as controlling power flow and maintaining stability and reliability, which require innovative solutions. As a result, research and development efforts in the field of DC MGs are ongoing, with the aim of improving their performance and expanding their application [4]- [6].

An overview of a typical DC MG is presented in Figure 1. DC circuit breakers are placed at various locations in the grid, near to the renewable energy resources, transmission line, main grid, battery bank, and load sides to ensure microgrid protection and maintenance. The DC circuit breaker (CB) types vary due to the presence of different levels of voltage and current paths within the network, ranging from generation to load. The primary objective of having a DCCB in DC systems is to protect the system against intentional or unintentional faults and voltage or current switching surges [7]-[10]. Table 1 provides a brief comparison between DCCBs specification of some manufacturers [11]-[15]. The selection of DCCBs will be based on the working conditions, voltage and current level, and thermal capacity which is substantially affected by I^2t of the beaker. The AC system can endure the fault current for a little while longer when it is experiencing thermal overload or overcurrent since the fault current rise rate is comparatively slow. Due to the DC system's low short-circuit impedance and rapid rising time of the fault current, it must be stopped immediately [16]-[18].

Furthermore, DCCBs are also utilized for maintaining the devices within the DC system. When a component of the system requires maintenance, the DCCB can safely interrupt the circuit,

allowing the maintenance work to be carried out without posing a risk to personnel or damaging the equipment.

Table 1. Comparison of different types of commercialized DCCB's applications

Description	Schneider Electric	Eaton	Siemens	ABB	LS
Model	Power PacT JDC	CJGPVS, CKDPV	HDGD	SACE Emax	Susol
Rated Current	30~1200 A	150~3000 A	50~1600 A	Up to5000 A	16~1600 A
Performance voltage	500 VDC	600~1000 VDC	600 VDC	250~1000 VDC	500-1500 VDC
Breaking Capacity	20 up to 50 KA	1.5 up to 42 KA	42 KA	65 KA	20 up to 50 KA
Ambient Conditions	-10 to 60 ºC	-40 to 70 ºC	-25 to 70 ºC	-40 to 70 ºC	-25 to 55 ºC
Operation time	≤30 ms	1 ms	70-300 ms	≤70 ms	≤40 ms

The DCCBs system makes it possible for some studies [19]-[21] to focus on DC MG fault current limiting, control, and clearing. These areas of study have been widened to include DC MG clusters.

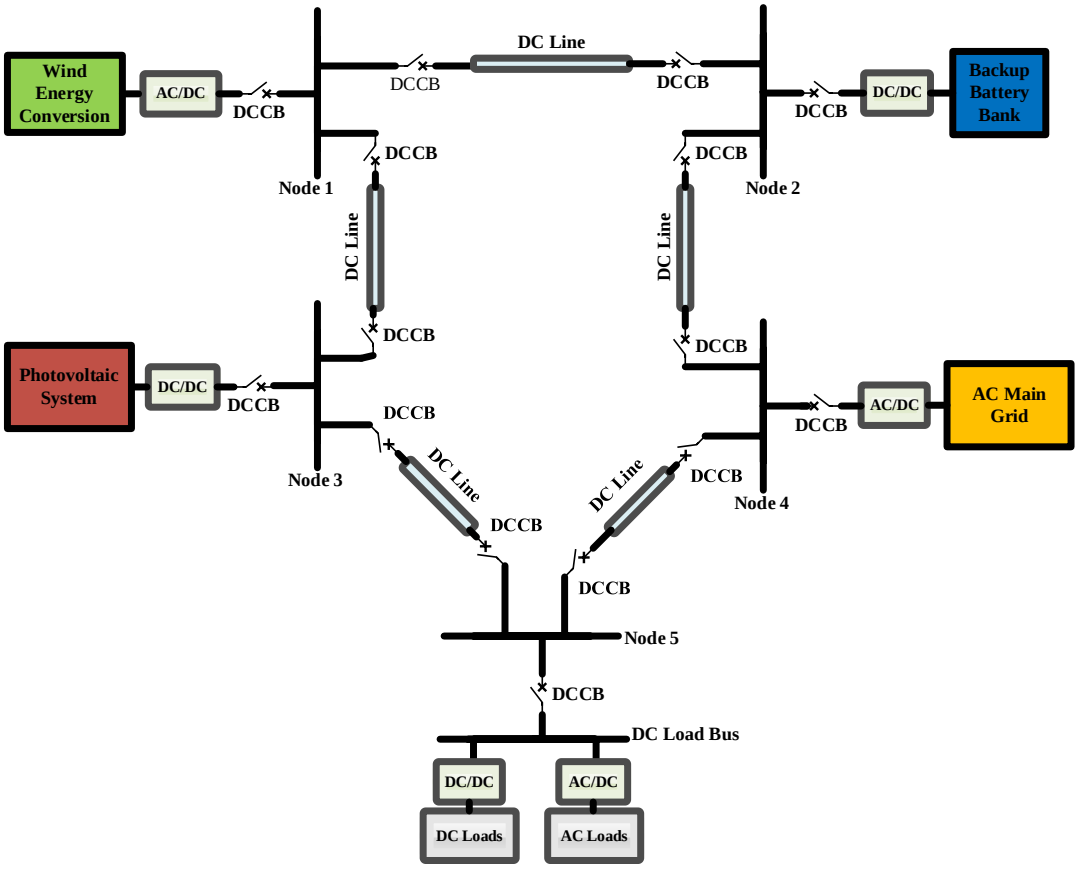


Figure 1. Overall topology of DC Microgrids

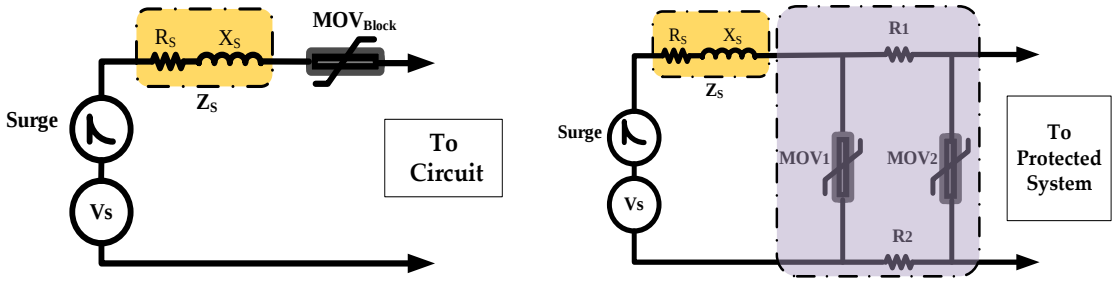
2 Surge Absorption Design Principle for DC Circuits

Surge voltages are voltage increases that usually occur for a duration from approximately one signal cycle to 1.5 second. These overshoots are typically triggered by the switching of high range loads and main grids. Although they are not as intense as sharp spikes, surges usually surpass the line voltage by around 20%, which can lead to data corruption of computers, harm of devices, and inaccurate readings in supervisions systems. If a surge persists for more than two seconds, it is generally known as an overvoltage. Therefore, to protect a circuit against transients, it is necessary to restrict the voltage amplitude of the surge at each part of the circuit and deviate the current and voltage of the surge through protection-specific components to absorb the released energy. The likelihood of experiencing damage from a power surge is typically associated with the size of the sudden increase and time span of the surge. Electric discharges and other transients in power systems exhibit rapid and intense properties in terms of both speed and magnitude (often several thousands of volts), hence, surge protection device (SPDs) needs to react promptly and manage considerable energy levels shortly to be effective. Typically, upstream circuit breakers or fuses cannot react quickly enough in response to the activation of the surge diverter because their reaction time is not fast as the span of the transient impulse [22], [23].

Essentially, all SPDs operate as voltage dividers [24]. Figure 2 demonstrates this concept with a series line impedance, Z_S. The source impedance, Z_S, is always present due to the impedance of system wiring and transient source. Since load impedance, Z_L is significantly larger than Z_S, a greater voltage is generated across the load, which leads to detrimental consequences. When an impedance-blocking device like Metal-Oxide Varistor (MOV_{block}) is linked in series, as depicted in Figure 2a, its impedance rises in response to the surge's frequency components dependents. This causes a decrease in the load voltage. Thus, this type of series SPD topology is not conventional. When a shunt SPD element, such as MOV_{shunt} with impedance of Z_{MOV} in Figure 2b, is used, its impedance decreases during high-voltage surges, allowing a shunt current to flow through it and absorb the surge energy. If possible, components of Z_S should be selected to increase its value and mitigate the surge, thereby reducing the stress on the bypass device.

An optimal SPD should minimize the transmitted surge energy to the load to protect both the load and the SPD against any hazard. This transmitted energy can be determined by integrating

the surge voltage and current over time, represented as $\int vi\,dt$. An effective SPD should achieve a lower voltage across the load (known as clamping voltage) to restrict the current flowing through the load. It should also possess characteristics such as low dynamic resistance and quick response time. Additionally, extra factors like longevity, repeatability, board size, cost, reliability, and a fail-safe mechanism are crucial considerations in the design of an SPD.



a. with blocking device in series configuration

b. with shunting device configuration

Figure 2. Voltage division methodology in transient surge protector design

In DC calculations, due to zero frequency (*f=0*), impedance is considered as pure resistance. But, in case of high frequency surge occurrence, impedance behavior changes by created inherent inductance. Surge frequency for 20 µsec length time is 50 kHz, and for 50 µsec is 20 kHz. Thus, the impedance amount of the circuit ($Z = R + jX$) should be calculated if the inductance is negligible or not.

Since shunt structures are more suitable for SPD designs, the dissipated energy in MOV can be computed using the following method for estimation of voltage, V_{MOV}, and current, I_{MOV} of the MOV as expressed in Eqs. (1) and (2):

$$V_{MOV} = \frac{Z_{MOV}}{Z_{MOV} + Z_S} \times V_{Surge} \tag{1}$$

$$I_{MOV} = \frac{Z_L}{Z_L + Z_{MOV}} \times i_{Surge} \tag{2}$$

Therefore, the energy that is dissipated across the MOV, E_{MOV}, during the surge time denoted as t_{surge} , can be expressed in Eq. (3) as follows:

$$E_{MOV} = V_{MOV} I_{MOV} t_{surge} = \frac{Z_{MOV} Z_L}{(Z_{MOV} + Z_S)(Z_L + Z_{MOV})} V_{Surge} i_{Surge} t_{surge} \quad (3)$$

The above calculation could assist the designers in choosing the appropriate components for their SPD design.

A typical practical protector design with nonlinear devices such as MOV and bidirectional breakover devices (BBDs) for a two-wire DC system is illustrated in Figure 3. capacitors represent additional near short-circuit paths to the surges and offer exceptional protection as well. If the maximum induced voltage is greater than the corresponding MOV's firing voltage, the MOV will activate and conduct a high current immediately. This causes a clamping voltage to form across the MOV terminals, and it absorbs the released energy over the surge duration. This protects the critical load from the surge voltage danger. Additionally, the surge energy is further filtered by the *LC* filters on the path. The series inductor's $L\omega$ impedance and the parallel capacitor's $\frac{1}{C\omega}$ impedance absorb more energy of the HV transient. If there is any residual HV transient, the BBDs at the end of the protection path will absorb it by firing, provided that the peak of the remaining surge surpasses the BBD's trigger voltage [25].

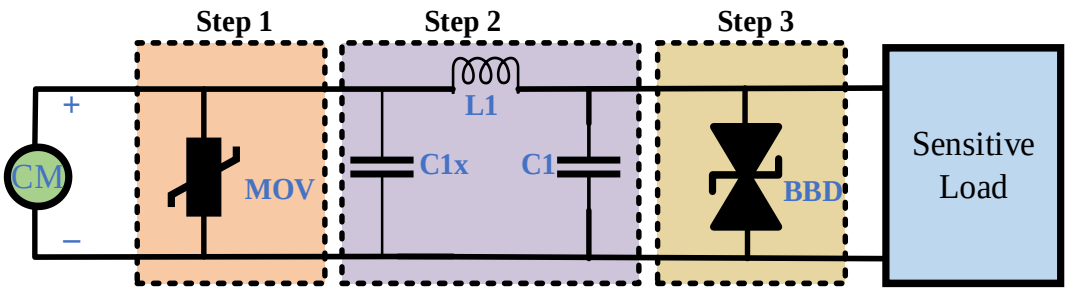


Figure 3. practical surge protector topology against common mode (CM) surge

Where total dissipated energy (E_D) in the system will be determined as the sum of the dissipated energy during the three steps of surge protection as expressed in Eq. (4).

$$E_D = E_{step1} + E_{step2} + E_{step3} \quad (4)$$

$$V_{MOV} = \frac{Z_{MOV}}{Z_S + Z_{MOV}} V_{Surge} \quad (5)$$

$$V_{C1} = \frac{Z_{C1}}{Z_{C1} + Z_{L1}} V_{MOV} \tag{6}$$

$$V_{SL} = V_{BBD} = V_{C1} = \frac{Z_{MOV} \times Z_{C1}}{(Z_S + Z_{MOV}) \times (Z_{C1} + Z_{L1})} \times V_{Surge} \tag{7}$$

$$i_{surge} = i_{MOV} + i_{C1x} + i_{L1} \tag{8}$$

$$i_{L1} = i_{C1} + i_{BBD} + i_{SL} \tag{9}$$

$$i_{MOV} = \frac{Z_s}{Z_S + Z_{MOV}} i_{surge} \tag{10}$$

$$i_{C1x} = \frac{Z_s}{Z_S + Z_{C1x}} i_{surge} \tag{11}$$

$$i_{C1} = \frac{Z_{L1}}{Z_{L1} + Z_{C1}} i_{L1} \tag{12}$$

$$i_{BBD} = \frac{Z_{L1}}{Z_{L1} + Z_{BBD}} i_{L1} \tag{13}$$

$$i_{L1} = \frac{(Z_{L1} + Z_{C1})(Z_{L1} + Z_{BBD})}{Z_{BBD} Z_{C1} - Z_{L1}^2} \times i_{SL} \tag{14}$$

$$i_{L1} = X i_{SL} \tag{15}$$

Given the component impedances and a constant value, X, the surge current can be calculated using the Eq. (14), which can then be used to determine the sensitive load current (Eq. (16)).

$$i_{SL} = Y \times i_{surge} \tag{16}$$

$$Y = \frac{Z_{BBD} Z_{C1} - Z_{L1}^2}{(Z_{L1} + Z_{C1})(Z_{L1} + Z_{BBD})} \times \frac{Z_{MOV} Z_{C1x} - Z_S^2 - Z_S Z_{C1x}}{(Z_S + Z_{MOV})(Z_S + Z_{C1x})} \tag{17}$$

Therefore, the amount of dissipated energy in each component in the circuit can be determined separately by considering the provided estimated values of voltage, and current of each component multiply with the time such as the formulation is Eq. (3).

3 DC Circuit Breaker Topologies

There are three fundamental topologies of DC circuit breakers [26]-[28]. Mostly, other researchers developed these designs. Although electromechanical based circuit breakers are not used in DC topology system designs anymore due to the significant disadvantage of their low-speed performance.

1. Mechanical (Resonance) DC circuit breakers (M-DCCB)

2. Solid state (Static) DC circuit breakers (SS-DCCB)

3. Hybrid DC circuit breakers (H-DCCB)

In the subsequent stage, there will be an examination and thorough discourse on the structure and efficiency of various topologies.

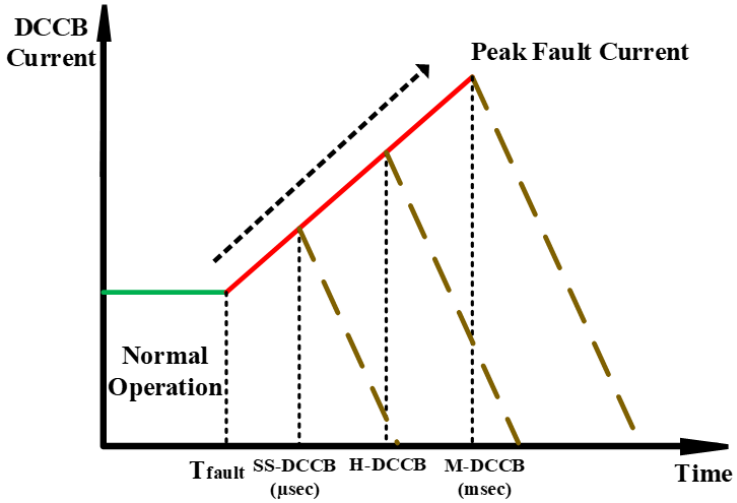


Figure 4: response time comparison between DCCBs in fault absorption

The objective of Figure 4 is to demonstrate the significant contrast in both reaction time and current-limiting capacity between different topologies of DCCBs. Since control of semiconductor devices as active components is governed by a comparatively low-power external signal, the activation of SS-DCCB turn-off and current-limiting mechanism can take place in a matter of microseconds.

Efforts to develop DCCBs that utilize resonance began in the 1980s. Table 2, Topology 1 (M-DCCB) provides an overview of the topology, which involves mechanical switches that interrupt the current when a zero crossing is created through an LC path (known as forced current diverted commutation line) that runs in parallel with the main electromechanical breaker. The topology also comprises an energy absorption branch, which consists of MOVs. Although newer topologies mentioned in this section may have advantages over the resonance topology, such as lower resistive on-state loss, it may still have practical applications for load switching. The resonance DC breaker topology is comprised of three primary branches [34]:

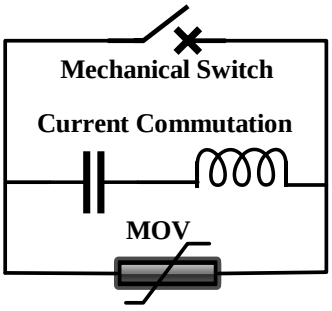
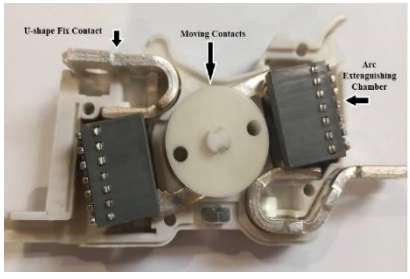
1. The normal current flow line

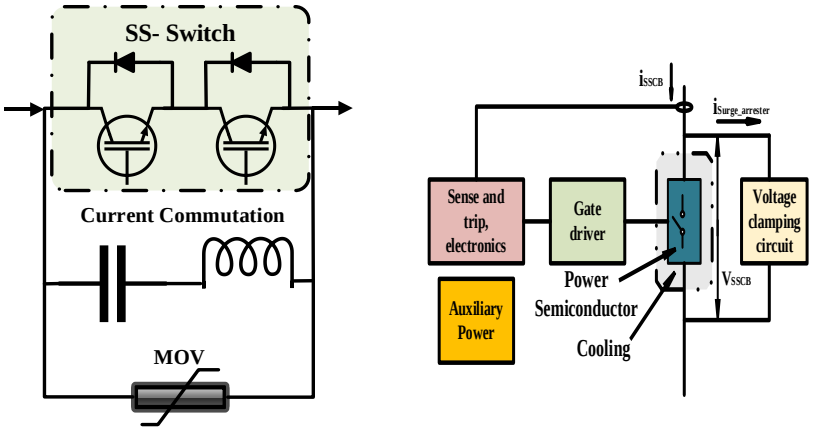
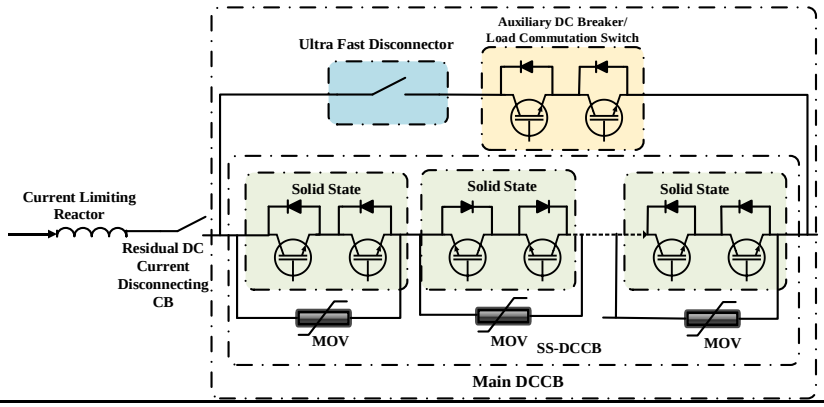
2. The forced current diverted commutation line

3. The surge mitigation sub-circuit

During a typical operation, the current follows the intended line. However, if the breaker is instructed to interrupt the current, a mechanical switch will open, resulting in an arc and a change in current direction into a different path. This change generates current oscillations. The arc causes a voltage drop that contributes to these oscillations, which in turn help to extinguish the arc by crossing the zero current point. Afterward, the current flows into an absorption sub-circuit to dissipate any remaining induced energy of the system.

Table 2. Fundamental topology of DCCBs

Topology 1: M-DCCB [16],[29]			**Advantage:** High breaking capacity **Disadvantage:** Low speed- Large size- Huge arc production

Topology 2: SS-DCCB [30],[31]		**Advantage:** Very fast- Small size- Low loss **Disadvantage:** Low Capacity
Topology 3: H- DCCB [28],[32],[33]		**Advantage:** Relatively High Breaking Capacity, Fast **Disadvantage:** Expensive

Internal structure of electrical contact in a Molded Case Circuit Breaker (MCCB) double break operating mechanism is presented in Table 2, Topology1. The double-breaking contact system is a highly advanced design for low voltage circuit breakers contacts and was patented by Siemens in 2007. The U-shaped contact points help to reduce the intensity of the shock caused by a surge in the breaker by producing a magnetic field that rotates 180 degrees in the opposite direction. This design simplifies the disconnection of the double-breaking mechanism [29,35].

To improve and supply the quick interruption during the fault or surges in DC systems, SS-DCCBs presented. The solid-state topology employs semiconductor devices such as IGBT, MOSFET, GTO, and Thyristor in conjunction with MOV and/or capacitor to interrupt the flow of electrical current. During regular operation, the current flows through the semiconductor devices. To halt the current, the devices are deactivated, and the current is rerouted into the paralleled sub-circuit, which acts as both the commutation and energy-absorbing path. The MOVs discharge the energy accumulated in the system, much like in the resonance topology. SS-DCCB topology illustrates a solid-state based configuration that employs IGBTs and diodes

for bi-directional applications. The figure demonstrates a solid-state DC breaker for unidirectional configuration. The topology of bi-directional current interruption could be achieved by positioning the same range IGBT in anti-series with an anti-parallel diode. More breaker cells can be added in series to raise the rated voltage level [36]. Even though the SSCB can break the current swiftly enough for fault current disruption, the semiconductors conduct current during typical working conditions, causing high losses due to the voltage drop over the breaker, particularly in high voltage applications [31], [37].

A typical SSCB comprises several crucial elements, including power semiconductor devices, gate drivers, cooling mechanisms, voltage clamping circuits, fault detection systems, sense and trip electronics, and an auxiliary power supply. In Table 2 a theoretical performance of a standard SSCB is depicted. The number of power semiconductors needed will vary depending on the application's voltage and current ratings, the power semiconductor technology, and the breaker's topology. Even though gate drivers with auxiliary power supply are already on the market, several researchers are investigating ways to enhance the gate driver's capabilities to create high-performance SSCBs and integrate multiple functions into a single unit [31].

Hybrid topologies combine both mechanical switches and semiconductor devices. Recent research papers suggest that ABB and ALSTOM have created DC circuit breaker prototypes using this approach, which show potential as promising technologies. H-DCCB topology provides an overview of the hybrid DC circuit breaker, which can be viewed as an extension of an IGBT-based solid-state topology. The utilization of thyristors in the design enables this topology to be appropriate for HVDC circuit breaker designs, as it can handle large voltage and current levels effectively [38]-[43]. The breaker includes an additional branch with a mechanical low resistance ultra-fast disconnector (UFD) and a load commutation switch (LCS). The LCS, same as the solid-state DC breaker, is designed to interrupt current flow, but it has a limited number of breaker cells that can only transfer current to the main breaker. To address the issue of conduction losses in solid-state topology, hybrid topology allows for nominal current to flow through the LCS and a UFD under regular operation. When an interruption command is received, the LCS turns off and transfers current to the main breaker, same as the solid-state breaker. Following the commutation, the UFD opens to isolate and protect the LCS from voltage drops caused by the main breaker's interruption of current. The UFD is a crucial element in minimizing losses during regular operations and achieving rapid current interruption. It operates as an

electromagnetic actuator, utilizing magnetic forces to achieve the fast-switching speed necessary for efficient circuit protection. According to ABB, their DC circuit breaker can eliminate faults within 5 milliseconds. The role of the current limiting reactor is to restrict the high slope of the fault current. In addition, a switch that operates in parallel with the hybrid DC breaker is also present to provide physical isolation following the clearance of the fault current. To determine the current and energy dissipation in these circuit breakers during a fault, certain circuit parameters must be considered. Following a circuit fault in a DC system, most of the fault current redirected through the H-DCCB is attributable to the IGBTs within the breaker [44]-[46]. The fault current can be denoted in Eq. (18) as follows:

$$i_f = I_{line} + \frac{V_{IGBT}}{L_{line} + L_{CLR}} \times (t - t_1) \tag{18}$$

Where I_{line}, is the pre-fault current, L_{CLR} is current limiting reactor inductance, and $t_1$is the fault time. And current of the IGBT switch will be calculated by Eq. (19) as:

$$i_{IGBT} = I_{line} + \frac{V_{IGBT}}{L_{line} + L_{CLR}} \times t_2 \tag{19}$$

Where t_2 is the performance time of the IGBT switch.

To calculate the dissipated energy of the MOV, the voltage at the protection level during t3 (MOV performance time) is assumed to remain constant. The maximum amount of energy dissipated by the MOV in each series part is then determined by Eq. (20) as:

$$E_{MOV} = [I_{line} + \frac{V_{IGBT}}{L_{line} + L_{CLR}} \times t_2] \times V_{MOV} \times \frac{t_3}{2} \tag{20}$$

Thus, the dissipated energy between each individual series cell in H-DCCB could be calculated separately by the presented formula [47], [48].

4 Design Improvements of DCCBs for DC Microgrids Application

The upcoming section will examine three novel and distinct classifications of the DCCB's energy absorption techniques:

4.1. MOV-based DCCB

4.2. Capacitor-based DCCB

4.3. Hybrid MOV-Cap DCCB

The most crucial section in DCCBs for absorption of the released energy during switching and faults is the energy absorption part. In this Section, we compared a wide range of studies that suggested several designs to redirect the surge through solid state components to technically absorb the released energy. The constructed DCCB worked admirably in each of the approaches that were discussed, and the outcomes are pleasing. The difference is between their technology, performance voltage and current level, and the response time which is a key factor in DCCB designs.

5 MOV-Based DCCB

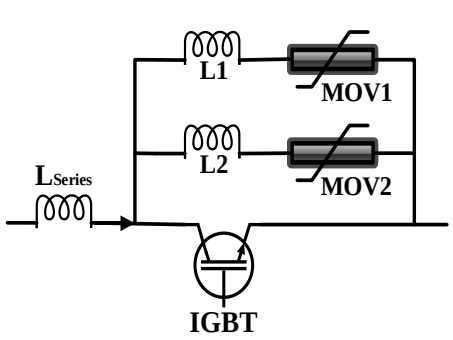
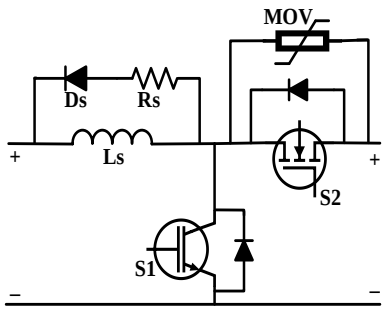
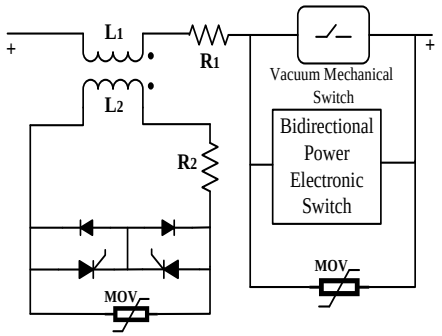
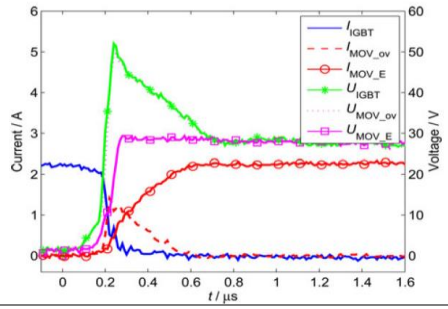
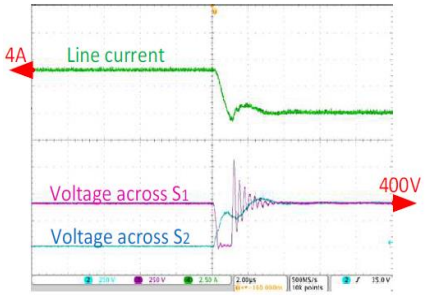
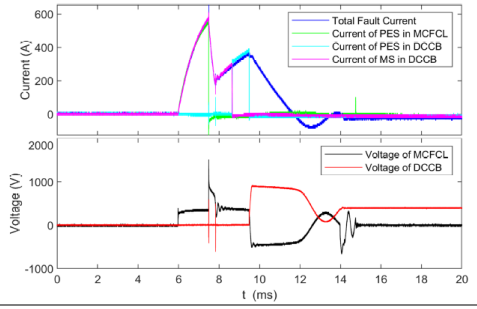
For DCCBs based on MOVs, the circuit breaker's embedded MOV completely handles surge absorption. Different designs define the strategy for absorbing the released energy [49]-[52].

The significant drawback of these designs is that the MOVs deteriorate over time when exposed to surges [22],[30].

The separated MOV technique in Table 3 has put forward an approach that involves using two distinct MOVs placed in specific locations within a circuit, to isolate the two functions of the MOV, namely voltage clamping and energy absorption. This proposed approach aims to separate the two functions of MOVs, allowing them to operate independently and more efficiently. The result shows the successful test and surge absorption through paralleled MOV's circuit. But the test is restricted to a small range of voltage and current amplitudes.

Alongside, ground clamping strategy illustrates a new DCCB design that uses a current limiter to absorb the surge voltage [54]. This SSCB design consists of several components including a main switch (S_2) that conducts the line current and prevents source voltage before and after breaker operation. Additionally, the design includes a MOV to demagnetize the energy stored in the system inductor, a ground clamping switch (S_1) that bypasses the DC bus, and a current-limiting inductor (L_2) with its resistive energy absorber.

Table 3. A comparative study on three conventional MOV-based design of DCCB's

Description	Topology 1 [53]	Topology 2 [54]	Topology 3 [55]
Proposed model			
Model Verification			
Technique	Separated MOV	Ground Clamping	MC FCL
Technology	MOV- IGBT	MOV- MOSFET, IGBT	MOV- IGBT
V_{dc}/I_{dc}	30 v/ 2.5 A	400 v/4 A	500 v/ 380 A
Response Time	0.4 µsec	50 msec	1.8 ms
Number of Passive Components	4	6	8
Number of Active Components	1	2	≥4

In this design, minimum current limiting inductance could be determined by Eq. (21) according to the bus voltage, V_{DC}, breaking time, T_{Break}, zero current detection time, T_{det}, saturation current of inductor, I_{Lsat}, and threshold current of I_0 :

$$L_s > \frac{V_{DC}(T_{Break} + T_{det})}{I_{Lsat} - I_0} \tag{21}$$

Furthermore, magnetic coupling fault current limiter (MC FCL) technique proposed a fault current limiting design with magnetic coupling auxiliary circuit in the input of the circuit breaker to limit the severity of the current shocks. In this study released energy is coordinated to be dissipated in both MOV and resistance in the secondary of the transformer.

Overall, while various techniques for surge absorption have been successful in damping surges and fault currents, there are design issues that need to be addressed. For example, many designs rely on MOVs for surge absorption, but often fail to consider the limitations of MOVs, which can weaken their ability to damp surges or will be degraded over time.

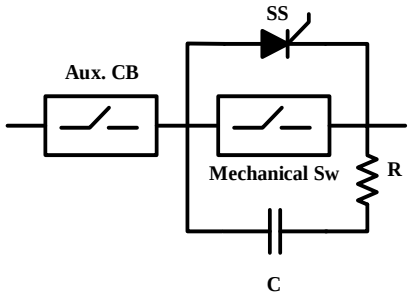
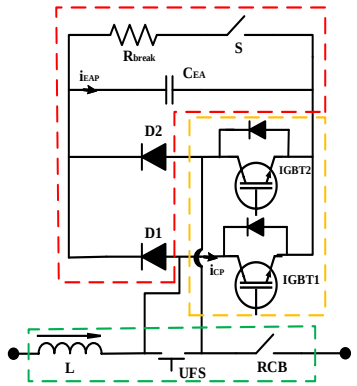
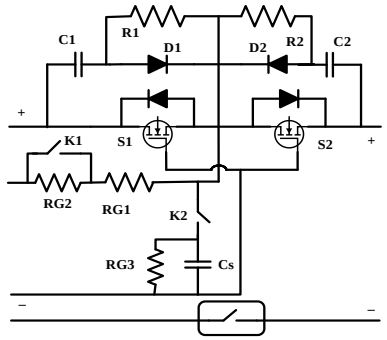
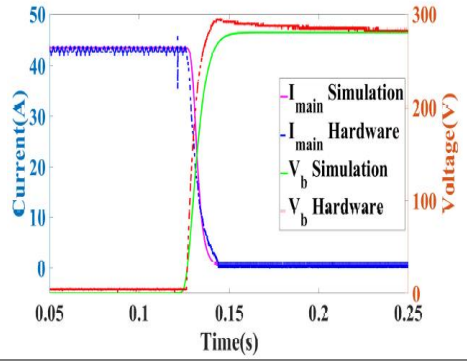
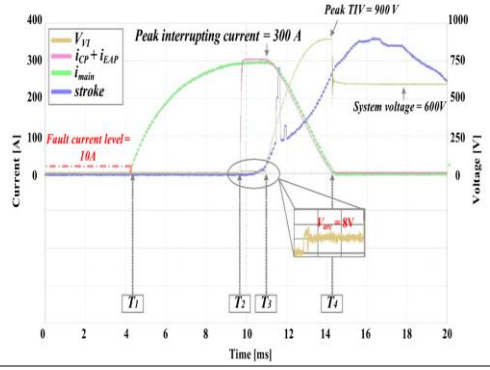
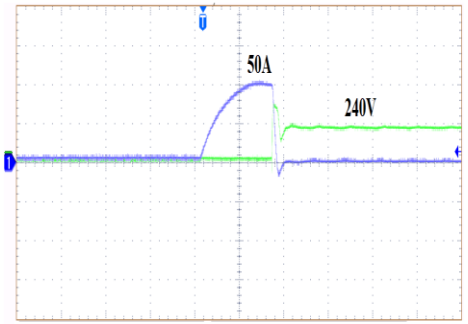
5.1 Capacitor-Based DCCB

To enhance the design of DCCBs, some studies have explored the use of capacitor-based technology for both commutating and surge absorption purposes. This approach involves a bridge-type capacitor-commutation unit that serves to buffer the device voltage and is considered an independent method for improving DCCB design [56], [57]. Table 4 provides a concise overview of the recent designs, highlighting their points of comparison.

All three-capacitor based DCCB designs mentioned in Table 4 redirect surges to a subcircuit to reduce the impact of energy released during DC system faults or surges. They effectively absorb energy using specific techniques. However, the designs differ in terms of their response time, voltage and current levels, and the components used in the circuit.

Other studies have followed unidirectional and bidirectional Z-source DCCB (Z-s DCCB) designs, which the strategy is focused on capacitor-based design [61]-[66].

Table 4. A comparative study on three conventional capacitor-based design of DCCB's

Description	Topology 1 [58]	Topology 2 [59]	Topology 3 [60]
Proposed Model			
Model Verification			
Technique	A/C Circuit	VI- PMA	Soft-switched
Technology	Cap- IGBT	Cap- IGBT	Cap- MOSFET
V_{dc}/I_{dc}	283 v/ 43.5 A	750 v/ 300 A	240 v/ 50 A
Response Time	15 msec	9.6 msec	20 msec
Number of Passive Components	2	7	12
Number of Active Components	3	5	5

Z-s DCCBs show potential as suitable options for protect low and medium-voltage distribution networks, along with DC equipment, among the various configurations available, because of their uncomplicated structure, control mechanism, and economical price [67]. As shown in Fig. 5 the general layout of bidirectional Z-s DCCB, where two sets of isolated thyristors are arranged in parallel to facilitate the flow of current in both directions.

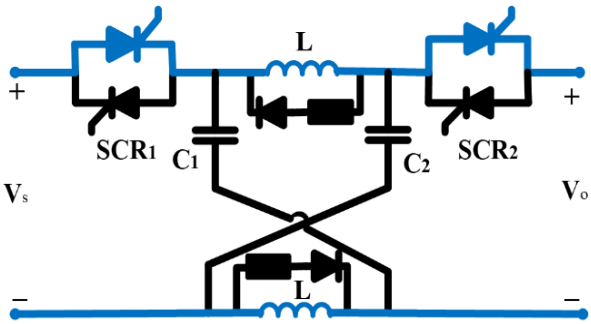


Figure 5. bidirectional Z-s DCCB [67]

In the mentioned designs electrolytic capacitors for surge absorption are utilized, but these components have limited capacity and cannot dissipate the energy released by high voltage longer duration faults and have a limited lifespan due to their chemical structure.

5.2 Hybrid MOV-Cap. DCCB

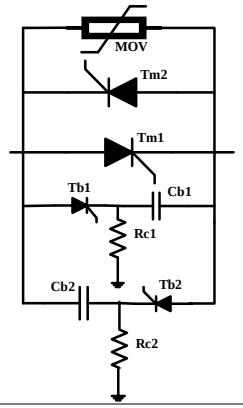
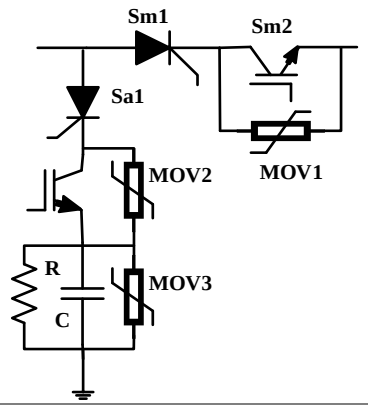
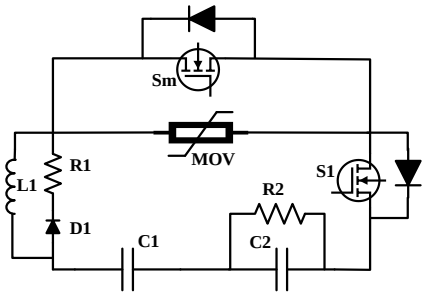
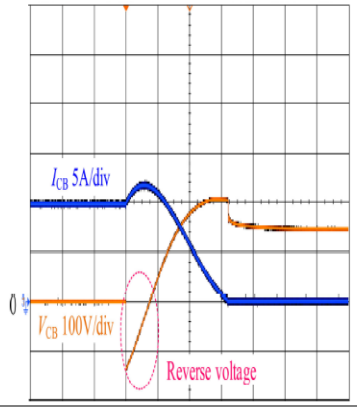
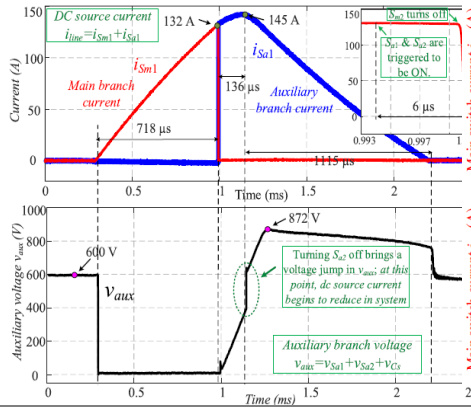
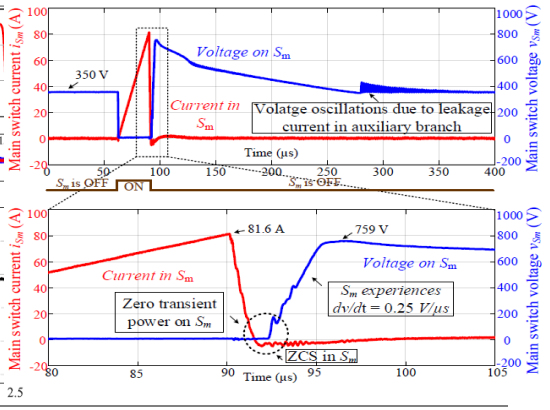
Several studies have proposed novel designs of hybrid MOV-Cap DCCB to overcome the weakness of degradation of MOV and restricted capability of capacitors to absorb the energy [68]- [71].

In Table 5, all designs effectively performed fast through different techniques. capacitor discharge path is considered for all models and the level of voltage and current in the circuits are different.

In active thyristor CB (AT-CB) technique, bidirectional, low loss DCCB with a reliable opening process based on a simple hybrid design for capacitor and MOV is implemented. This technique is more suitable for medium voltage DC systems [72].

$$t_q = \frac{C_b V_n}{\alpha I_{fmax}} \tag{22}$$

Table 5. A comparative study on three conventional hybrid MOV-Cap design of DCCB's

Description	**Topology 1 [72], [73]**	**Topology 2 [74]**	**Topology 3 [75]**
Proposed Model			
Model Verification			
Technique	AT CB-DCCB	TIM-Pack	LCC-AIC
Technology	MOV-Cap Thyristor	MOV-Cap Thyristor-IGBT	MOV-Cap SiC MOSFET
V_{dc}/I_{dc}	150 v/10 A	600 v/145 A	350 v /90 A
Response Time	1.6 msec	6 µsec	4 µsec
Number of Passive Components	5	5	9
Number of Active Components	4	4	2

$$C_b = \frac{\alpha t_q I_{fmax}}{V_n} \tag{23}$$

Therefore, the value of the bypass capacitor can be approximated using Eq. (23), which involves determining the recovery time, t_q, which will calculated by Eq. (22), inserting the values for the maximum allowable fault, I_{fmax}, and the desired coefficient, α.

Other techniques of Thyristor-IGBT-MOV (TIM-Pack) and inductor capacitor-capacitor based active injection circuit (LCC-AIC) in Table 5 switched fault currents into the designed sub-circuits within a couple of microseconds to improve the reliability.

6 Discussion on the Design Improvement

Various techniques of surge absorption have been discussed in the literature for designing DCCBs in nominal voltage ranges that span from a few hundred volts to tens of kV. The power rate, voltage, and flowing current level in a DC microgrid are directly linked to the semiconductor device utilized in its design. As a result, the design and techniques employed should be adapted for varying levels of power in the microgrid. During the DCCBs circuits design, the number of passive and active components used plays a crucial role in determining the most cost-effective topologies for the rate of DC system power. Additionally, it is important to consider the lifespan of the circuit components by assessing the weaknesses of each part during the design process. Regarding the reliability of the circuit, it has been mentioned that there is a lack of detailed comparison in literature, specifically in terms of the vulnerabilities of the components such as deterioration, chemical-based materials, and limited energy capacity.

This paper focuses on proposing new ideas to improve the design of the surge absorption sub-circuit in the evolution of DCCB designs. Table 3 concentrates on the performance of the circuit and the task of energy absorption, which currently relies on MOV-based subcircuits. However, the weakness in the performance of MOV degradation and protection is not taken into consideration. MOV alone is unable to protect the circuit against short circuits and overcurrent situations. Therefore, when designing a DCCB for DC protection with an MOV energy absorber, it is crucial to consider current limitations. This aspect is addressed in the designs presented by ground clamping strategy and MC FCL techniques.

Hybrid designs are typically employed to address the performance limitations of previous designs and enhance their features. A hybrid design in the energy absorber can mitigate the degradability and overcurrent and short circuit protection issues associated with MOV in Table 3, as well as the low capacity and chemical-based weaknesses of capacitors, in Table 4. In a hybrid design, the tension in the circuit is divided among various shock absorber components, effectively covering these weaknesses. This concept is most evident in the designs proposed by TIM-Pack and LCC-AIC techniques.

7 Prospective Future Advancement

Here are a few possible future advancements that have the potential for future research:

- Research on the surge absorption techniques and sub-circuits in DCCB design to cover the existing limitations.

- Integrated design of DCCBs in terms of performance, and higher breaking capacity against faults and switching of the DC circuits.

- Improve the reliability and lifetime of the DCCB's by using non-chemical, non-degradable components for surge, fault and switching effect absorption.

- Cost reduction by substituting minimal amount of the degradable components, and utilization of alternative components like resistance instead of expensive like MOV.

- Power loss can be minimized through design improvements, which involve reducing both switching power loss resulting from semiconductor switching and passive component loss from elements like current limiters and snubber resistors during regular system operation. This can lead to more efficient performance with reduced power dissipation.

8 Conclusion

DCCB as a significant part of the DC MG topology takes over the protection and improving the reliability of modern power systems. In this article, surge absorption principle in DC systems were reviewed to illustrate the process of limiting the voltage and current transients that occur in DC systems due to switching operations or lightning strikes. Furthermore, three level SP design

estimations for sensitive load are determined, which ensure that sensitive loads are protected from transients.

Three main topologies of DCCB design evolution including M-DCCB, SS-DCCB, and H-DCCB topologies were investigated and reviewed. Each topology has its advantages and disadvantages, and the choice of topology depends on the specific application requirements. Particularly, the energy absorption subcircuits of DCCBs were focused, which were separated into three sub-designs: MOV-based, capacitor-based, and hybrid MOV-Cap based designs. Then, various techniques were examined and discussed to identify the optimal design approach for different applications. Finally, design improvement factors and future development of DCCBs were discussed. These include the use of advanced materials, such as wide-bandgap semiconductors, and the integration of DCCBs with other protection devices to improve the overall system reliability.

Surge absorption technique and design plays a critical role in ensuring the reliable performance of DC MG and DCCB. The protection of modern power systems primarily depends on the employed techniques in DCCBs. Enhancing the subcircuit design responsible for energy absorption and considering design improvement factors will contribute to the advancement of DCCBs in the context of future power systems.

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III. Chapter 3:

Manuscript 2 – BiTriCap Technique Surge Absorption

In this chapter, the published manuscript delves into the innovative BiTriCap (Bidirectional Thyristor-Capacitor) technique for surge absorption in low-voltage SS-DCCBs. The study presents a design leveraging thyristors and snubber capacitors to redirect and dissipate switching surges, addressing limitations of traditional MOV-based solutions. Experimental and simulation analyses validate the model's performance in fault detection and energy absorption, showcasing its scalability for higher voltage applications. The research highlights the advantages of reduced degradation, cost-effectiveness, and improved reliability, making the BiTriCap-based SS-DCCB a promising solution for DC microgrid protection.

Low-Voltage Solid State DCCB Design Based on Bypassed Bidirectional Thyristor-Capacitor Suppressor

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***Abstract*—**This article introduces a novel technique known as Bidirectional Thyristor Capacitor (BiTriCap) designed to interrupt DC currents effectively and mitigate power surges in low-voltage (LV) solid-state DC circuit breakers (SS-DCCB). The method employs parallel snubber capacitors to absorb switching effects, subsequently releasing stored energy during the subsequent switch operation. The model incorporates considerations for both line and load inductances, offering a realistic portrayal of a DC system and ensuring authentic protective measures. To validate the efficacy of this approach, practical results from the system are cross-referenced with simulation outputs, validating the credibility of the research findings. Additionally, an ARM microcontroller is programmed to control the sequence of actions among the active SS switches, optimizing their performance. The proposed LV SS-DCCB operates at a voltage level of *48 VDC* and nominal current of *8 A*. However, the design is scalable and can be extended to accommodate higher voltage and current ranges.

Index Terms— Solid State-DCCB, Snubber Capacitor, Surge Absorption, DC Microgrid, Switching Effect, DC system Protection.

1 INTRODUCTION

THE DC Circuit Breaker (DCCB) plays a crucial role in DC Microgrids (MGs) [1], protecting the load, line, and power supply [2]. In recent years, substantial research has been dedicated to refining SS-DCCB utilizing various surge absorption techniques. Notable among these are the SCR-BCB [3] with transformer, Metal Oxide Varistor (MOV), and several active components. Despite their effectiveness, these designs exhibit certain drawbacks, including increased complexity, cost, weight, and the introduction of additional surge sources, particularly in the

primary winding of the transformer. Similarly, the TCB model proposed in [4] incorporates components such as MOV, transformer, thyristor, and diode. This design also channels surges through a transformer path, which results in similar weaknesses as the SCR-BCB design, including increased complexity and cost. Another technique, the SCBT and RB-IGCT models discussed in [5], employs an MOV-C snubber and MOV energy absorption parallel to the integrated gate-commutated thyristor (IGCT) structure. This approach emphasizes the role of capacitors in damping high-frequency voltage oscillations. DCCBs possess several critical characteristics that must be carefully considered during the design process. A primary concern, as highlighted in [6], is switching action time, which has been addressed through the development of a novel switch driving method. Equally important is the minimization of component count to enhance both cost-effectiveness and reliability. In [7], a passive clamping technique combining metal oxide varistors (MOVs) and capacitors is proposed to mitigate switching surges while minimizing component usage. The bidirectional capability of DCCBs, as explored in [8], offers significant advantages for medium-voltage and grid applications due to its ability to handle current flow in both directions. A comprehensive review in [9] evaluates the current state of solid-state circuit breakers (SSCBs) for low-voltage DC distribution systems, comparing various approaches in terms of fault response time, reliability, conduction losses, and complexity.

Regarding snubber circuits, [10] proposes a charged capacitor to accelerate switch action by providing a negative charge to rapidly absorb surges. In contrast, [11] introduces a novel oscillating-commutation SS-DCCB to enhance the switch performance and withstand shock. Moreover, [12] introduces the eMOV model, which decouples peak clamping from nominal DC voltage, allowing for lower voltage class devices and reduced conduction losses.

Concerted efforts are directed towards specialized components assigned the responsibility of absorbing the switching impact of the main switch, providing a protective shield to prevent damage [13]. Within this category of components, the MOV stands out as a widely adopted choice for mitigating surges in DCCBs [13]. However, in some of the surge absorption techniques, an LC branch is embedded in the design to commutate the current for the next action of providing the zero cross [13],[14].

The voltage and current characteristics of MOVs display nonlinear behavior, captured by the formulation presented in Eq. (1). The MOV activates when the circuit voltage exceeds the

clamping voltage threshold. This crucial role in surge protection underscores its importance in ensuring the reliable operation of DCCBs [15].

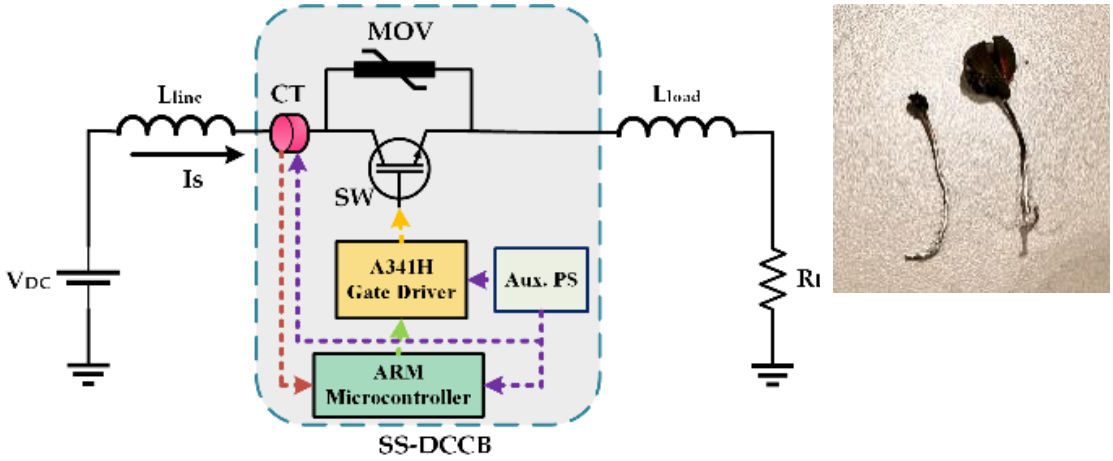
$$\log(v_{MOV}) = P_1 + P_2 log_{10}(i_s) + P_3 e^{-log_{10}(i_s)} + P_4 e^{log_{10}(i_s)} \quad (1)$$

The voltage across the MOV is represented by v_{MOV}, while the line current flowing through the MOV is denoted by i_s, with coefficients P_1 to P_4 being manufacturer-specified parameters.

However, the use of MOVs for DC surge absorption presents several limitations [15]. These include gradual deterioration, increased clamping voltage, current leakage, and heightened capacitance, all of which pose potential hazards to the system in DCCB application [15]. This letter proposes a significant advancement by eliminating MOV from DCCB designs and instead utilizing a snubber capacitor-based subcircuit to directly absorb the switching surge and block the passing current, thus reducing the stress on the main switch. This approach aims to address the issues associated with MOV, leveraging the low degradation rate of capacitors through simple charge and discharge sequences, thereby improving the overall safety and reliability of the system.

From a cost perspective, the total cost of a capacitor-based DCCB is cheaper than an MOV-based DCCB. Due to the high degradation rate of MOV, the lifespan and reliability of SS-DCCBs using capacitor surge absorbers would be higher than those using MOV. Although capacitor-based DCCBs require more active components compared to basic MOV-based DCCBs, their overall cost remains lower over time.

Fig. 1a illustrates the basic model of an MOV-based SS-DCCB. During a fault, the current level measured by the current sensor (CT) is transmitted to the ARM microcontroller. Subsequently, the ARM microcontroller sends a disconnection command to the gate driver of the active switch [13]. The released energy results in a surge across the switch, which is absorbed by the MOV. While this technique yields acceptable results, the degradation of the MOV can lead to component damage over time, as illustrated in Fig. 1b.



(a) (b)

Fig. 1. (a) MOV-based SS-DCCB circuit topology. (b) MOV damage observed during experimental testing.

As it can be seen from Fig. 2, MOV absorbs the surge in level of clamping voltage of the MOV. So, three stages of operation are defined in the switch operation, Normal operation, fault assessment, and energy absorption. After receiving the voltage level to the clamping voltage, MOV conducts, and the surge mitigates in this component. In consideration of MOV-based DCCB, the recommended clamping voltage rate is $1.5V_{DC} < V_{Clamp} < 2.5V_{DC}$ [16].

A primary challenge in DC circuits during fault scenarios stems from the absence of zero-crossing [17]. To effectively address this issue, this article introduces an innovative solution in the form of an active parallel subcircuit, utilizing thyristor-capacitor components. This designed subcircuit serves a dual purpose: it mitigates the surges induced by switching events and enhances fault detection capabilities within the DC system. By incorporating thyristor-capacitor elements, the proposed approach aims to offer a robust and efficient means of tackling challenges related to microprocessor-based fault detection and minimizing the impact of switching-induced surges in DC circuits.

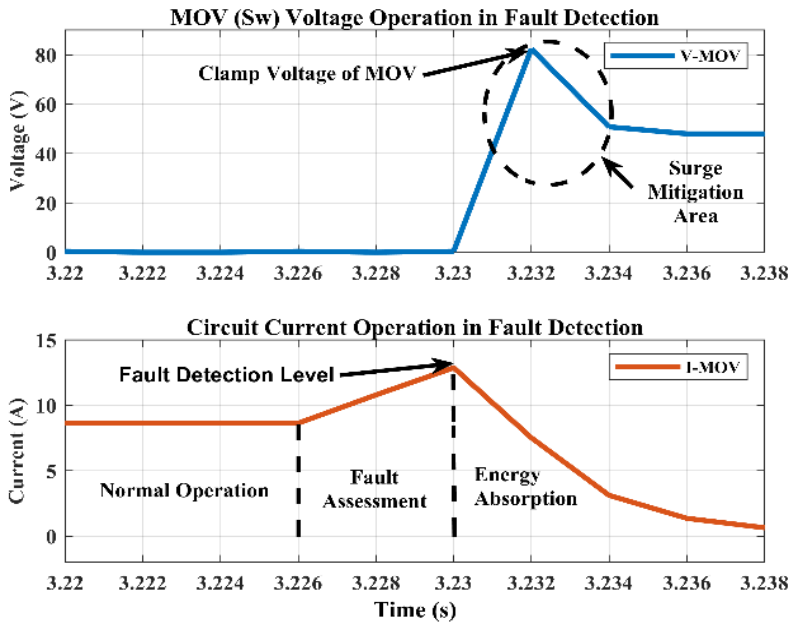


Fig. 2. Experimental Result: MOV (SW) voltage and line current in fault detection operation.

In this article, two separate tests are conducted to validate the proposed model of SS-DCCB. Initially, the phenomenon of DC circuit switching is explored, followed by an examination of fault detection within the model. In both instances, practical results are compared with simulation outcomes to validate their accuracy and alignment. This comparative analysis serves to affirm the credibility and robustness of the findings across both tests. The proposed model is tested with *48 VDC* and an *8 A* line current. However, the design can be expanded to higher voltage and current levels, considering the design prospects.

2 Proposed BiTriCap Technique Principal

The energy generated during the switching process in DCCBs is closely tied to the release of inductance within the circuit and distribution system. Previous discussions have centered around capacitor-based circuits acting as commutators to facilitate zero crossing with a series inductance in DCCBs [18]. However, this article presents a novel approach where the primary switching surge is redirected and mitigated through a capacitor-based subcircuit by activating a thyristor in its forward operation.

In this sequence, the aluminum film electrolytic snubber capacitor takes on the responsibility of absorbing the surge, becoming fully charged in the process. Subsequently, in the ensuing

operation, a backward thyristor is activated to discharge the capacitor through the designated resistor. This action readies the absorption circuit for subsequent performance, ensuring a controlled and optimized process for handling switching surges within DCCBs.

The fundamental role of a circuit breaker is to safely disconnect the circuit during system faults and maintenance operations. However, transients induced by current and voltage fluctuations resulting from faults and switching processes pose potential risks to the main switch, potentially leading to damage during disconnection.

Taking this concept into account, ensuring the safe performance of the switch becomes imperative. To achieve this, the surge current is rerouted away from the main switch through a bypassed snubber capacitor subcircuit, initiated by triggering a forward thyristor. This proactive measure diverts the surge current away from the main switch, protecting it from potential damage during circuit disconnection.

The entire process of mitigating surges is summarized in the bidirectional absorption and release or discharge of the capacitor's energy. The results are verified and compared with simulations. Furthermore, the suggested method demonstrates its capability to counteract faults in the reverse direction effectively.

Fig. 3 illustrates the blueprint of the envisioned model, featuring the strategic integration of the forward bypass thyristor (Tr_f). Its role is pivotal, absorbing any surge within the series capacitor. Conversely, during the backward flow, the thyristor in the reverse path (Tr_b) becomes active, discharging the accumulated energy within the system. To facilitate this intricate operation, precise control is maintained over all active switches, including the IGBT as the primary switch, along with both thyristors. This control is orchestrated by the STM32F407VG ARM microprocessor, which transmits commands through the gate driver systems.

The goal is to recreate an authentic DC system setup in the proposed model. As a result, both line and load inductances are thoroughly considered to ensure the realism and accuracy of the proposed model. This inclusion enables the simulation and analysis of the system's behavior under real-world conditions, ultimately enhancing its applicability and reliability in practical scenarios.

In the proposed model, the A341H IGBT Gate Drivers are employed to efficiently operate and initiate both the IGBT and thyristors within the circuit. Given the nature of thyristors as components reliant on current for triggering, a strategic setup is incorporated in the design. Two resistors are intentionally positioned along the connection path between the gate of the Thyristor and the gate drivers. This placement serves a dual purpose: firstly, to limit the output current of the gate driver, and secondly, to act as a protective measure for the microprocessor, thereby preventing any potential damage. This considerate arrangement ensures the controlled and safe activation of the thyristors, mitigating risks and optimizing the functionality of the entire circuit.

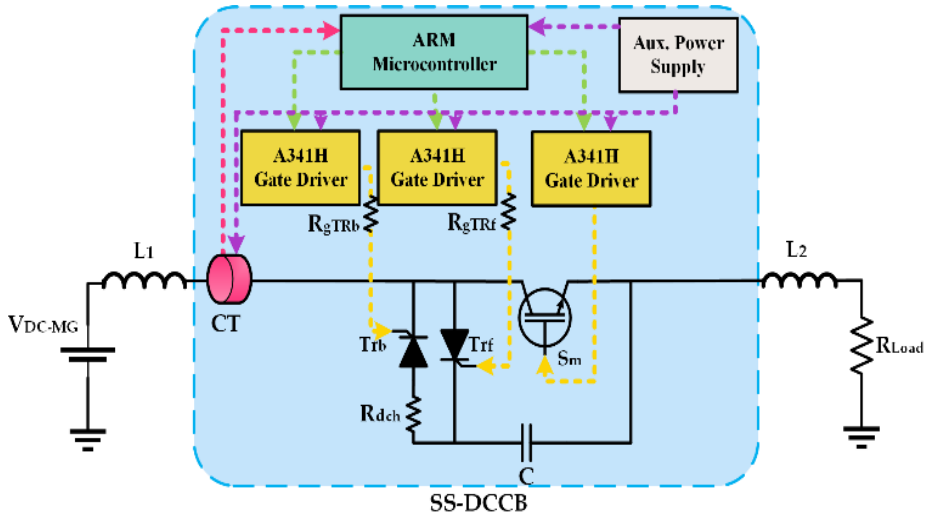


Fig. 3. The proposed BiTriCap based SS-DCCB

Effectively managing the IGBT involves both activation (ON) and deactivation (OFF) signals. However, only the ON signal is required when triggering the thyristor, as the thyristor autonomously switches off once the current crosses zero.

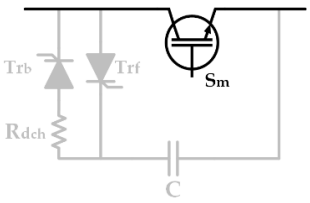
The duration for the thyristor to turn off depends on the charging (surge absorption) duration of the series capacitor. After the capacitor's charging cycle, it transitions into an open circuit, indicating the end of its conducting state. This characteristic behavior ensures that the thyristor's deactivation aligns with the completion of the capacitor's charging process, synchronizing the operational phases within the circuit.

The sequential operation of the active switches within the proposed model is visually depicted in Fig. 4. During the standard operation of the SS-DCCB, the primary switch (S_m) remains

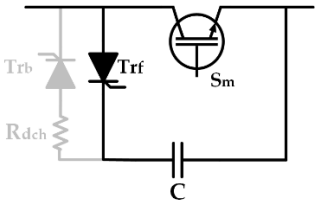
connected. When it is time to switch, the forward path activates concurrently as the main switch begins its shutdown process. The energy released during this switch is then diverted into the forward path, as illustrated in Fig. 4.2. Subsequently, in the third step, the main switch is safely turned off without experiencing any disruption in the operation.

Moving on to the fourth operational step, following the absorption of any surge by the paralleled snubber capacitor, the forward thyristor automatically switches off, resulting in the successful disconnection of the entire system. To prepare for absorbing potential surges in the next switch, the capacitor discharges in the subsequent step, synchronizing this discharge with the brief activation of the IGBT.

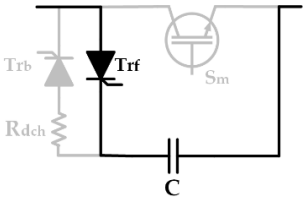
Once the bypassed capacitor is fully discharged, the backward thyristor turns off, allowing the system to seamlessly resume its regular operation. This accurate sequence of steps ensures a smooth and controlled transition through various operational phases, effectively managing energy redirection, surge absorption, and system disconnection within the SS-DCCB setup.



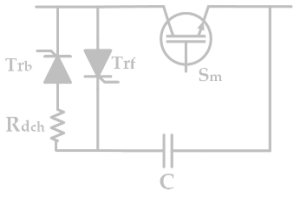
1: *Sm* is ON



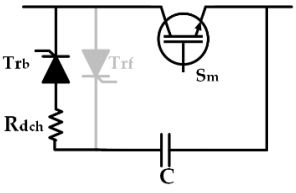
2: *Sm* and *Trf* are ON

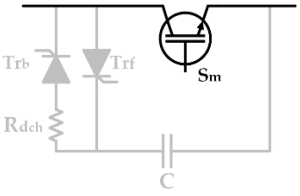


3: *Trf* is ON, surge is redirected



4: DCCB complete disconnection





5: Tr_b and S_m are ON, discharging path is activated.

6 (1): S_m is ON, normal operation

Fig. 4. Operational modes in the proposed circuit

Fig. 5 illustrates a switching diagram, elucidating the precise timing of each switch activation within every sequence. This diagram offers a visual representation that enhances understanding the synchronized switching instances throughout the operation.

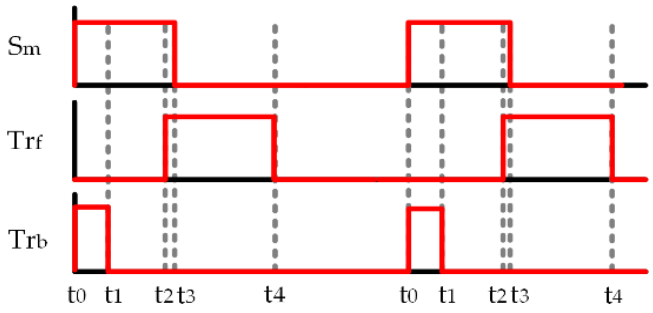


Fig. 5. Active components switching sequence

The calculation of the capacitor is grounded in the energy transformation between the circuit inductance and the capacitor. In fault detection scenarios, the stored inductive energy of the line and load side inductance is rapidly released. If this energy is not controlled, it can lead to damage to the main switch. In the proposed technique, the released energy is redirected into a mitigation path based on capacitors through the following circuit: $V_{DC\text{-}MG}$ - L_1 – Tr_f – C – L_2 - R_{Load}, ensuring this redirection occurs until the circuit current reaches zero.

As the energy released during the switching process is sourced from the stored energy in the circuit inductance (E_L), it can be represented using Eq. (2) as follows:

$$E_L = \frac{1}{2}(L_1 + L_2)I_L^2 \tag{2}$$

In this context, L_1 represents the inductance on the line side, while L_2 corresponds to the load side inductance. The computed level of stored energy relies on the square of the line current, I_L.

In the proposed circuit, the threshold tripping current is designated as I_L=*15 A*.

Upon disconnecting the main switch, it is imperative to dissipate the entire energy within the circuit. To protect the main switch from potential damage, this energy must be absorbed and redirected to the designated snubber capacitor. Consequently, the capacitance's energy ($E_{C_{min}}$) capacity should be at least equivalent to the inductive released energy, as outlined in Eqs. (3) and (4) in the following:

$$E_L = E_{C_{min}} \tag{3}$$

$$\frac{1}{2} C_{min} V_C^2 = \frac{1}{2} (L_1 + L_2) I_L^2 \tag{4}$$

In this context, V_C signifies the maximum voltage across the capacitor.

Given the maximum current of *15.1 A* from the main path, the capacitor's maximum voltage would be *50 V* (An overvoltage exceeding *4.1%* above the nominal voltage is deemed acceptable across the snubber capacitor). Consequently, the capacitance (C) of the snubber capacitor to absorb the switching effect in the circuit can be computed as greater than *52 μF* using Eq. (5).

$$C \geq \frac{(L_1 + L_2) {I_{L_{max}}}^2}{{V_{L_{max}}}^2} \tag{5}$$

In the subsequent calculations, to determine the optimal amount of snubber capacitor (C) discharge resistance (R_{dch}) and the capacitor voltage during the discharge sequence (t_{dch}), Eq. (6) can be employed.

$$V_C(t) = v_0 e^{(\frac{-t_{dch}}{R_{dch} C})} \tag{6}$$

In this condition, the initial voltage of the capacitor (v_0) is $v_0 = Vc_{max}$, and subsequently, the discharge resistance can be determined using Eq. (7).

$$R_{dch} = \frac{-t_{dch}}{C \times Ln(\frac{V(t)}{V_{C_{max}}})} \tag{7}$$

Therefore, based on Eq. (7), configuring the capacitor at *470 μF* will result in the attenuated current surge discharging through a *50* Ω resistor within *0.2 msec*.

For evaluation of DC system released energy, line and load inductors depending on being underground or overhead and the length of the lines therefore inductor have been calculated based on Eq. (8) per Kilometre (H/km), for an overhead transmission line [19]:

$$L = \frac{2 \times 10^{-4}}{\ln\left(\frac{D}{r}\right)} \tag{8}$$

TABLE I

PROPOSED SS-DCCB PARAMETERS

Parameter	Acronym	Value	Unit
Input DC Voltage (Chroma 6200H-100P)	$V_{DC\text{-}MG}$	48	V
Snubber Capacitor	C	470	µF
Microprocessor	ARM Microcontroller	STM32F407VG	-
Forward Thyristor	Tr_f	SKKT27B12E	-
Backward Thyristor	Tr_b	SKKT27B12E	-
Main Switch	S_m (IGBT)	IRGB4620D	-
Gate Driver	GD	A341H	-
Line Side Inductance	L1	21	µH
Load Side Inductance	L2	565	µH
Load Resistance (Chroma 63204)	R_{load}	6	Ω
Gate Resistance F	$RgTr_f$	20	Ω

Gate Resistance B	$RgTr_b$	20	Ω
Discharge Resistance	R_{dch}	50	Ω
Current Transformer	CT	LEM 100P	-

And for underground line, Eq. (9), the inductor can be calculated as the equation below:

$$L = \frac{\mu_0}{2\pi} ln(\frac{2h}{r}) \times 1000 \quad (9)$$

In Eq. (8) and Eq. (9), L is the inductance per kilometre (in Henries per kilometre), r and D are the radius and diameter of the conductor (in meters) respectively, h is the depth of the conductor below the earth's surface (in meters), and μ_0 is the permeability of free space, approximately $4\pi \times 10-7\ H/m$.

The values of circuit components are presented in Table 1.

3 Circuit Switching Test

In this section, a switching test has been conducted to demonstrate the stability of the proposed technique. In this test, the main switch repeatedly connects and disconnects at a frequency of *0.5 Hz*, which represents the worst-case scenario for a DCCB. Subsequently, the capacitor and the main switch currents and voltages were monitored. The obtained results are subsequently validated through experimental testing. The measured values from this test confirm that the various sequences of the proposed technique operate as expected.

3.1 Simulation Analysis of Circuit Switching

This section discusses the MATLAB simulation results for the suggested model. Fig. 6 illustrates the voltage and current across the main switch. As observed, in both the ON and OFF states of operations, surges and switching spikes are redirected to the bypassed snubber subcircuit. The switching overcurrent is measured around *0.18 A*, and there are no voltage surges during the switching time. This indicates that the proposed model affirms the effectiveness of switching surge suppression through the suggested technique.

The switching test undergoes a voltage at *48 VDC*, with a nominal circuit current of *8 A*. This test validates the switching surge absorption before proceeding to the subsequent tests for fault detection and circuit interruption in DC systems. The entire surge is rerouted to the bypassed snubber subcircuit during this test.

Fig. 7 depicts the operation of the forward thyristor and snubber capacitor during surge redirection. Upon receiving the disconnection command, the forward thyristor activates a few milliseconds earlier to absorb the released energy from the circuit. Consequently, the main switch is successfully disconnected from the circuit without experiencing surges or overvoltage.

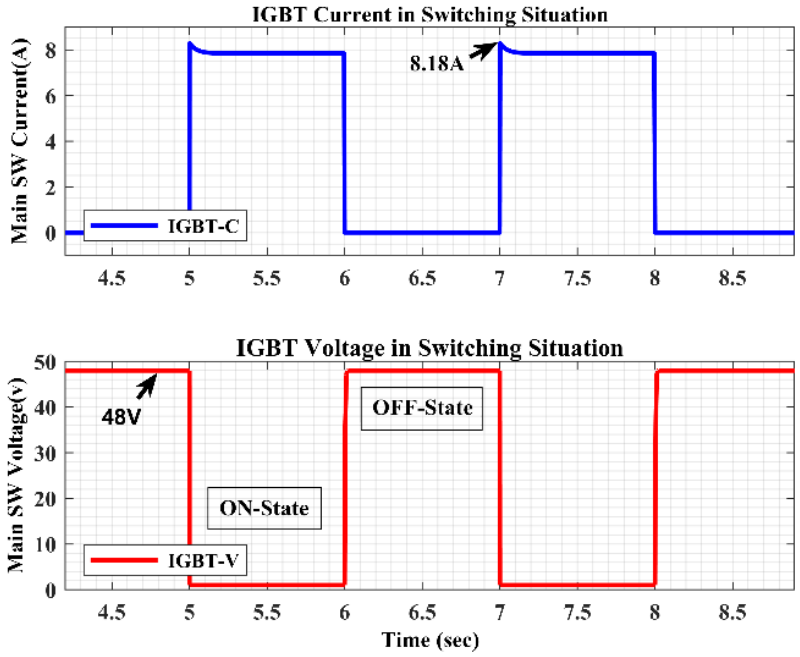


Fig. 6. Simulation Result: Main switch (IGBT) switching operation

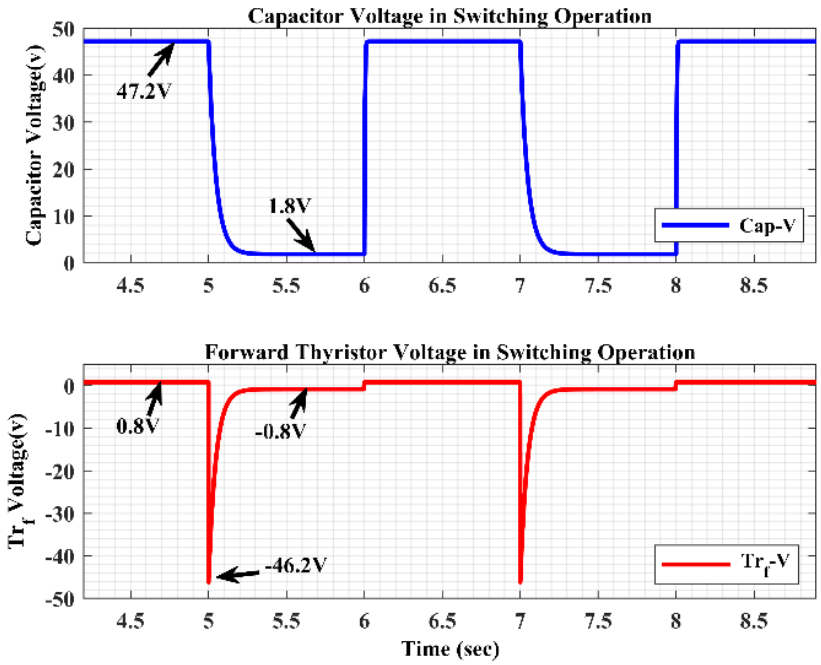


Fig. 7. Simulation Result: Forward thyristor and snubber capacitor voltage in switching operation

Additionally, Fig. 8 illustrates the performance of the snubber capacitor discharge during the second cycle of the main switch while in the ON-state, offering insights into the operation of the backward thyristor.

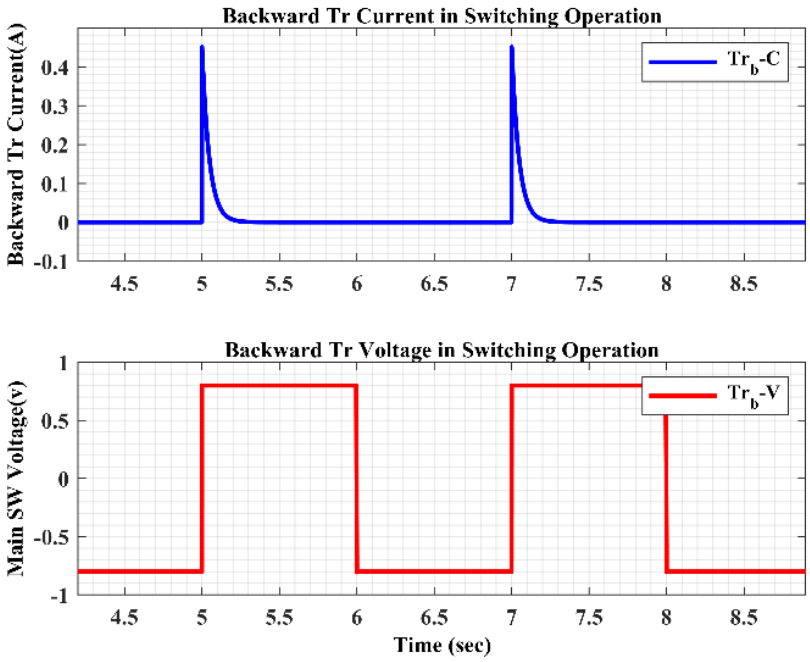


Fig. 8. Simulation Result: Backward Tr voltage and capacitor discharge current

3.2 Practical Results of Circuit Switching

The laboratory prototype of the proposed SS-DCCB, utilizing the designed BiTriCap technique, is depicted in Fig. 9.

In practical terms, the discharge time and switching speed are determined by the amount of released energy, contingent on the circuit inductance. For this test, inductances on both the line and load sides are considered within *20 μH* and *565 μH* to maximize the switching surge and accurately model the inductance of real-world low-voltage distribution systems.

The results illustrated in Fig. 10 validate the viability of the proposed technique. In previous research efforts, the current commutation technique employed parallel capacitor inductance to induce current fluctuations, facilitating the achievement of current zero-crossings, and subsequently absorbing the released energy through other parallel MOV branches [20].

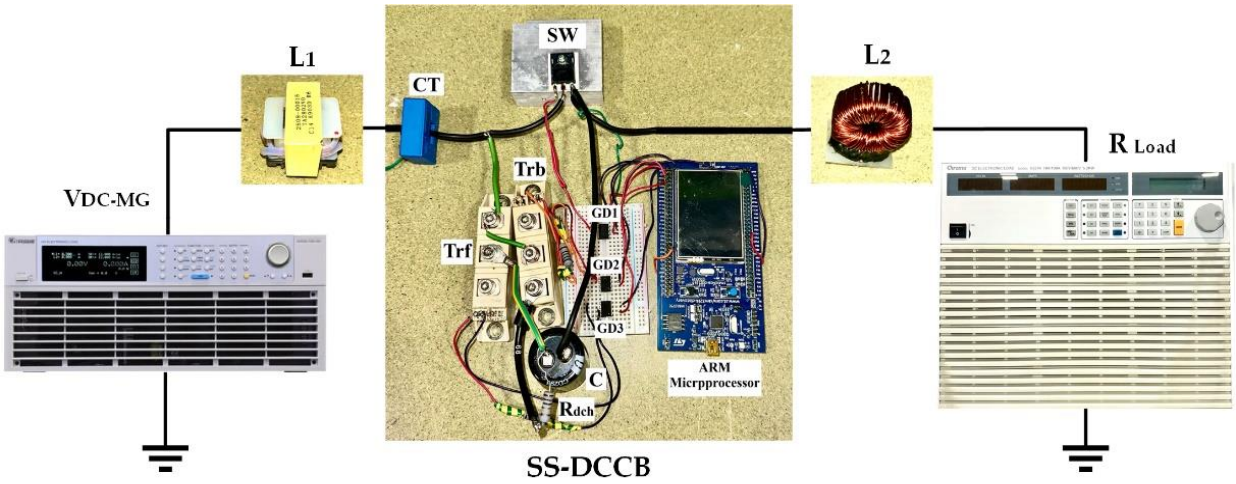


Fig. 9. Practical setup of the proposed SS-DCCB with BiTriCap surge absorption technique

However, the technique proposed in this article introduces a novel approach where the entirety of the surge and current surge is redirected into the snubber capacitor, leading to the elimination of MOV from the design.

During the interruption of the main system using the BiTriCap Technique, there is no tension or surge present across the main power (IGBT) switch. By employing this technique, the main switch is able to prolong its lifespan, while the SS-DCCB demonstrates reliable performance. This is because surges are directed away from the switch and redirected to the snubber subcircuit. Additionally, the capacitor undergoes a straightforward charge and discharge process, contributing to enhanced reliability.

4 Fault Detection Analysis Test

In this section, a fault detection analysis test has been conducted to demonstrate the reliability and effectiveness of the proposed technique in identifying and responding to short-circuit faults. This test is necessary to ensure that the DCCB can accurately detect short-circuit conditions and disconnect the load as quickly as possible.

During this test, the circuit operates under normal conditions with a current of *8 A*, and a short-circuit is simulated as well. The fault detection mechanism is designed to sense an overcurrent above *15 A* and send a disconnecting signal to the circuit breaker. Additionally, the capacitor and main switch voltage and current are monitored to assess the effectiveness of the circuit.

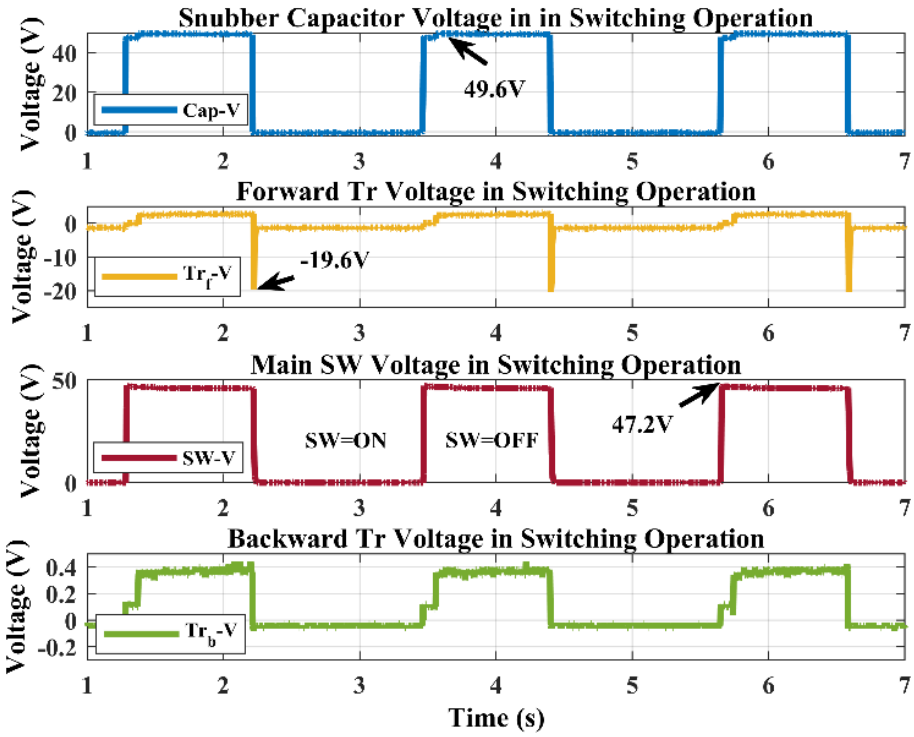


Fig. 10. Experimental Result: Test validation of switching operation

The obtained results, which were validated through experimental testing, indicate that the proposed technique, due to its simplicity in control, can immediately sense the overcurrent and effectively suppress the fault surge, providing robust protection against fault conditions as intended.

4.1 Simulation Analysis of Fault Detection

During the short-circuit or fault detection test of the BiTriCap technique, the nominal circuit voltage is set at *48 V*, the circuit current is specified as *8 A* (based on the defined *6* Ω load), and the fault detection trigger level by the microprocessor is established at *15 A*. The fault current *(I_f)*, illustrated in Fig. 11, flows from the short-circuited load through the line and load side inductances (L_1 and L_2), forward thyristor, and the bypassed snubber capacitor (C) and then to the power supply ($V_{DC\text{-}MG}$) when the IGBT switch is disconnected.

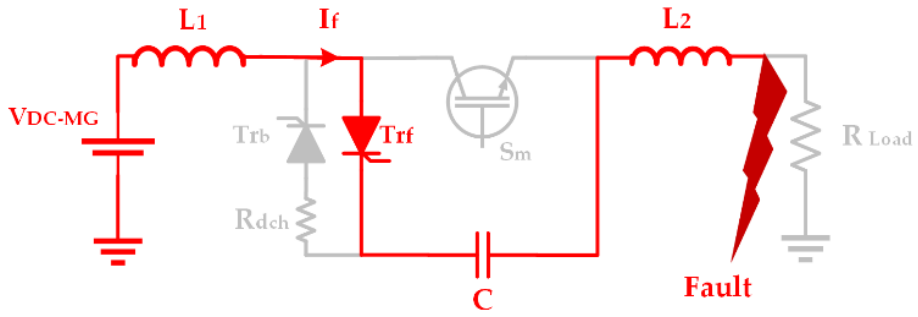


Fig. 11. SS-DCCB Fault current path

Therefore, it can be computed by Eq. (10) as follows.

$$I_f = \frac{V_{DC-MG}}{C(L_1 + L_2)s^2 + 1} \tag{10}$$

The initial inductance current (I_{L0}) during the fault period can be determined using the Eq. (11) provided below. In this formulation, t_{det} represents the fault detection time.

$$I_{L_0} = i_s + \frac{V_{DC-MG} t_{det}}{(L_1 + L_2)} \tag{11}$$

In this scenario, the calculation of the forward thyristor voltage (V_{Trf}) involves the consideration of the input voltage (V_{DC-MG}), system series inductances (L_1 and L_2), the snubber capacitor (C), and the initial inductance current (I_{L0}) during the fault time, as outlined in Eq. (12).

$$V_{Tr_f} = \frac{V_{DC-MG}}{s} - \left(\frac{2(L_1 + L_2)Cs^2 + 1}{Cs}\right) I_{L_0} \tag{12}$$

By employing the inverse Laplace transform, the temporal variation in the voltage across the forward thyristor during the fault time can be determined by Eq. (13) as follows.

$$v_{Tr_f}(t) = v_{DC-MG} - 2LI_{L_0} \cos(\omega_f t) - I_{L_0} \sin(\omega_f t) \tag{13}$$

Where $L=L_1+L_2$ represents the total system inductance, I_{L0} is the initial current of the system in fault condition, and $\omega_f=2\pi f$ is fault frequency dependent parameter.

Fig. 12 presents the flowchart of the programmed ARM microprocessor STM32F407VG. The SS-DCCB determines its course of action by measuring the current of the main system line in accordance with the defined restrictions and permissions in the circuit.

Upon detecting a fault through the embedded current transformer (CT) in the main current path, the microprocessor issues a breaking command, leading to the disconnection of the main switch following the sequences outlined in Fig. 3 and the flowchart presented in Fig. 12.

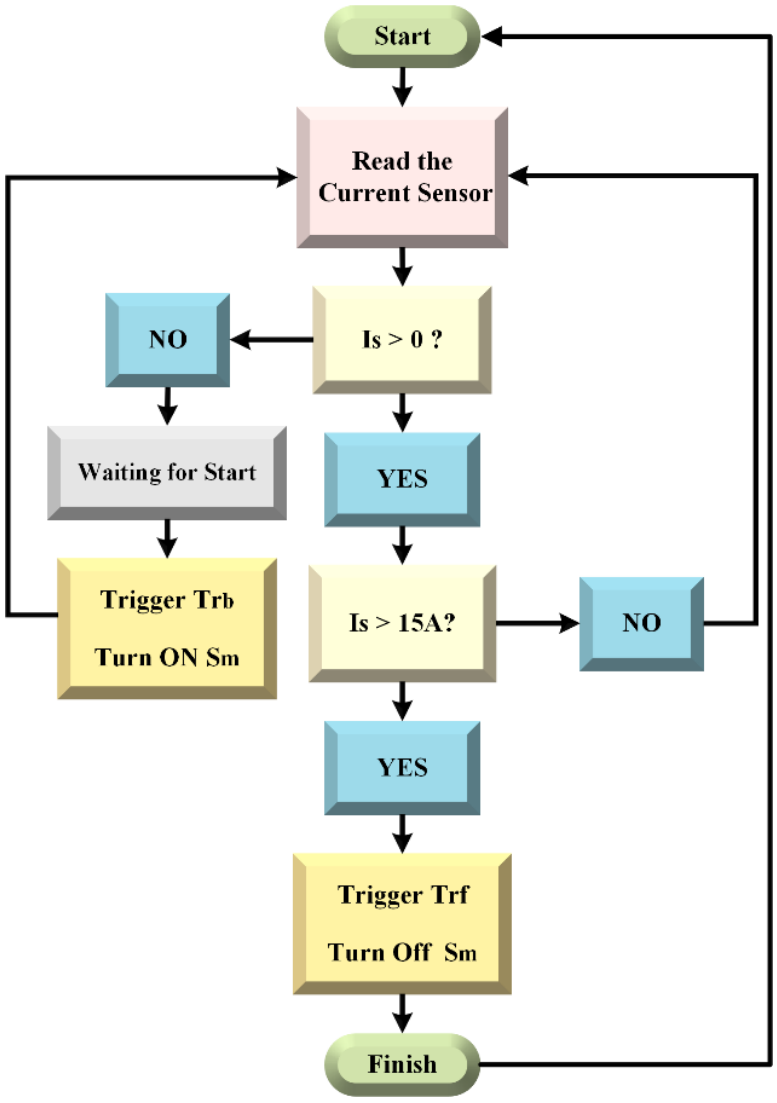


Fig. 12. Fault and short-circuit detection flowchart

Fig. 13 illustrates one cycle of the circuit operation. A manual fault is introduced at *1.5* sec. Notably, when the measurement device detects a *15 A* threshold, the controller issues a trigger

command to Tr_f, redirecting the fault effect and transmitting a disconnection command to the IGBT, which serves as the main circuit switch. The overvoltage during the breaking time, compared to the circuit voltage level, is approximately *2* volts, falling within an acceptable range.

During a fault occurrence, the capacitor voltage undergoes an instantaneous increase, effectively absorbing the circuit surge, and the current in the bypassed path drops to zero as the capacitor becomes charged. Subsequently, the thyristor turns off in accordance with its operating principle.

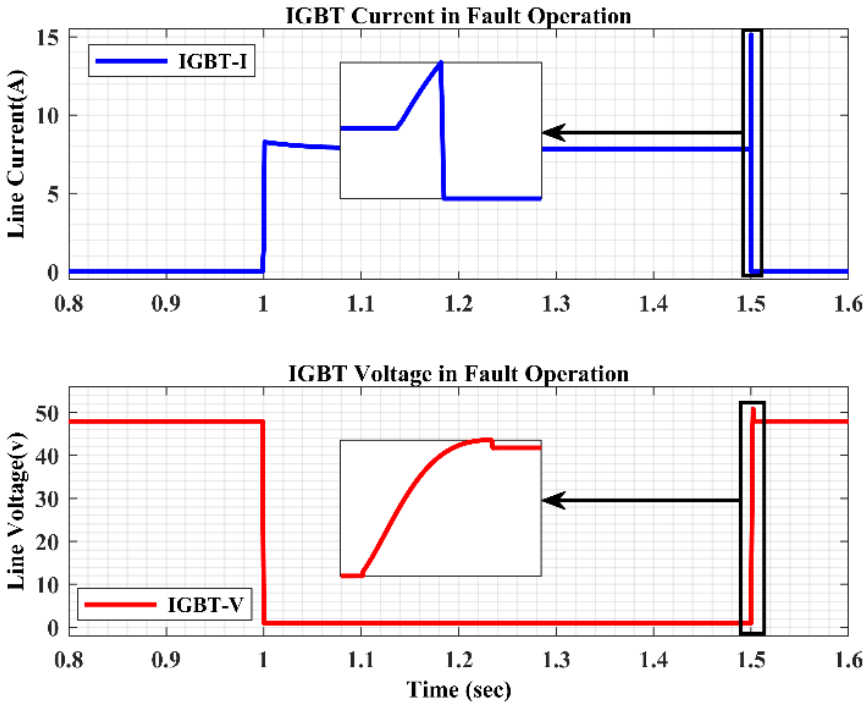


Fig. 13. Simulation Result: Main switch fault detection performance

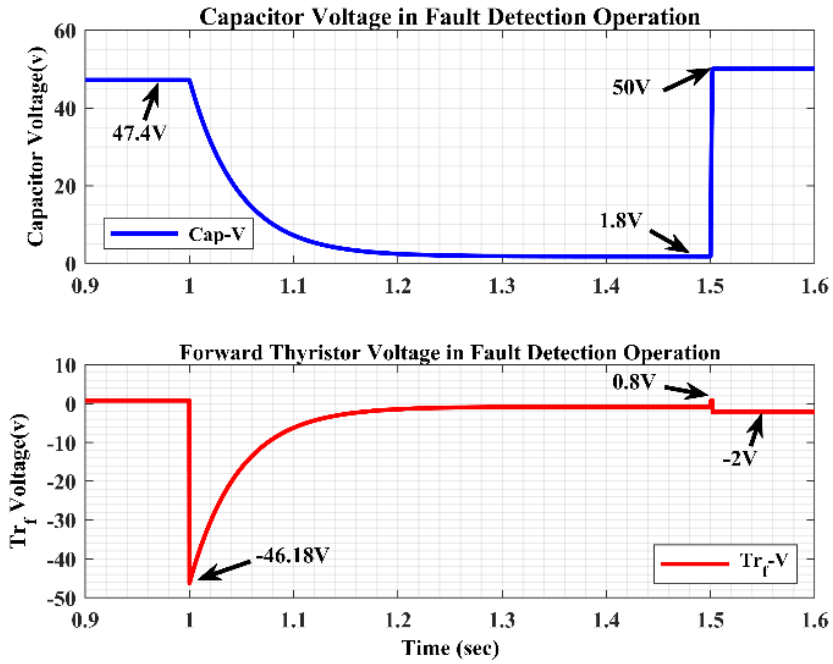


Fig. 14. Simulation Result: Capacitor and Tr_f voltage in fault detection operation

Fig. 14 illustrates the behavior of the snubber capacitor and the voltage variation across the forward thyristor during the normal operation and at the time of fault detection. In the illustrated scenario, the capacitor discharges to *1.8 V*. At *1.5 sec* after the fault event begins, the capacitor voltage increases to *50 V* when the microprocessor triggers the forward thyristor to divert the surge. This dynamic reaction exemplifies how the system responds to the fault condition.

4.2 Experimental Validation of Fault Detection and Circuit Protection Capability

The experimental phase of the research validates the interruption test, as depicted in Fig. 15, which illustrates the voltage and current characteristics of the main switch in the proposed model. The outcomes closely align with the simulated results. The presented results indicate minimal overvoltage ($V_{max\text{-}Sm}$=*50 V*) and precise current interruption (I_f=*15.2 A*) observed at the main switch during fault detection. According to the circuit topology, when the microprocessor detects the current threshold, it immediately interrupts the main current path via S_m. In the proposed model, the rise time/fault clearing time, depicted in Fig. 15 as the time taken to increase the voltage from *10%* to *90%* of the input voltage ($V_{DC\text{-}MG}$), measures *116 µs*. Additionally, the main switch voltage rises to *50 V* quickly, without significant overvoltage. With this rise time, the fault frequency falls within the range of *8.62 kHz*. Therefore, when selecting the main switch, CT, and

bypassed forward thyristor, it is crucial to consider covering this fault bandwidth. According to the datasheets of the components utilized in this research, the IGBT operates at a frequency of *5.8 MHz*, while both the CT and the Tr_f operate within a frequency range of *100 kHz*.

As shown in Fig. 16, the snubber capacitor effectively mitigated the short-circuit surge, resulting in the voltage level rising to full charge. When S_m is switched ON, a voltage of *-45.6 V* is observed across the forward Tr, which remains inactive. However, Tr_f operates instantaneously to redirect the surge into the snubber capacitor, stabilizing its voltage at *47.8 V*. During the switch operation, the capacitor discharges through the S_m-C-R_{dch}-Tr_b loop.

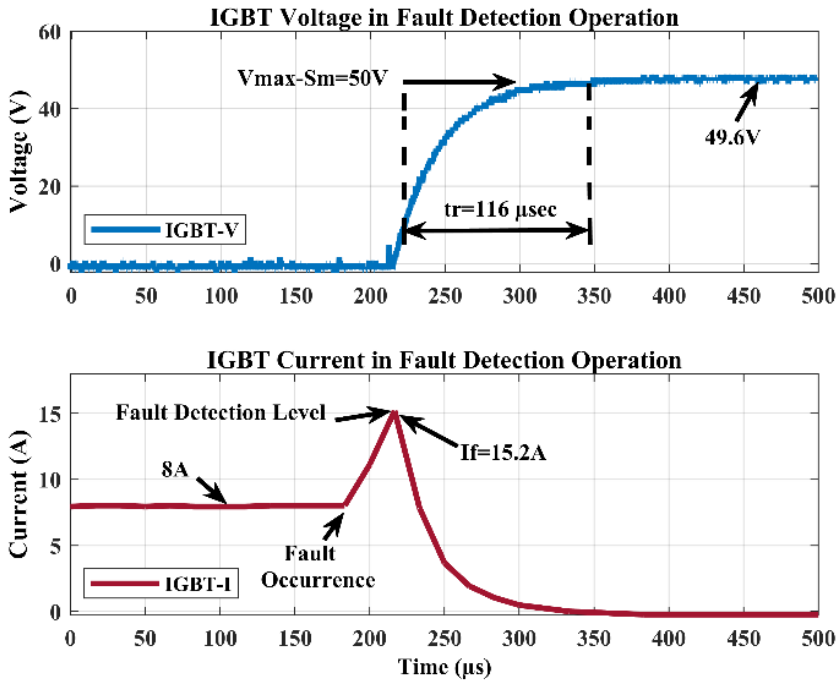


Fig. 15. Experimental Result: Validating Fault Detection for the Main Switch.

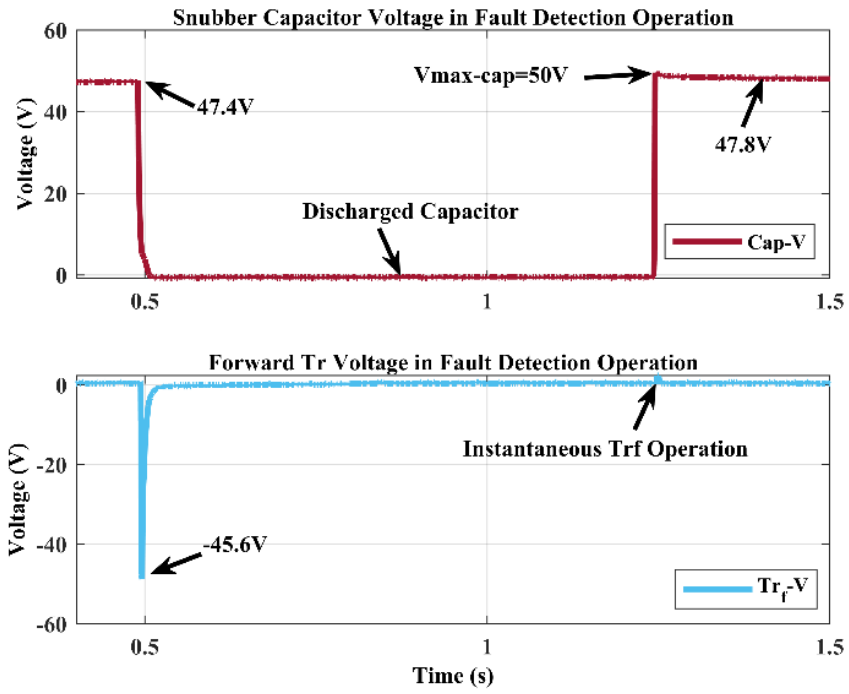


Fig. 16. Experimental Result: Snubber Capacitor and Forward Tr voltage

TABLE 2

TOPOLOGY COMPARISON

Reference	Proposed Model	[6]	[7]	[8]	[21]	[22]	[23]	[24]
Category	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB
Normal reclosing capability	Yes	YES	YES	YES	Yes	No	Yes	No
Switch Type	IGBT	IGBT	MOSFET	Thyristor	SiC MOSFET	SiC MOSFET	Thyristor	IGBT
Total Active components	2× Thyristor 1× IGBT	1 IGBT	>2 MOSFET	3×Thyristor 4× IGBT	2× SiC MOSFET	2× SiC MOSFET	6× Thyristor	6× Thyristor 3× IGBT
Diode	0	4	0	4	1	2	0	0
Capacitors	1	2	1	1	2	3	1	1
Inductors	0	6	0	0	1	0	0	1
Resistors	1	0	0	1	2	5	2	1
Level of circuit control complexity	Medium	LOW	Medium	High	Medium	Medium	High	High
Surge Absorber type	Capacitor	RLC	MOV-C	RC	MOV-RC	MOV-RC	TVS-RC	RLC
Mechanical Switches	0	0	0	0	0	3	1	0
Surge arresters	0	0	1	0	1	0	1	0

Tests were conducted using both aluminium film electrolytic capacitor and polypropylene film capacitor, producing consistent and comparable results. Due to the low cost of electrolytic capacitors in lower voltage ranges, it was included in this test. For designs requiring voltages above *500 VDC*, polypropylene capacitors are suitable.

Table 2 presents a concise comparison with previous research studies and a summary of the circuit topology and performance. It demonstrates the use of a straightforward design with minimal active components, achieving satisfactory results in mitigating the switching effects of SS-DCCB during fault detection operations in DC MGs. The real model of the DC system, considering line and load inductances, is employed in the presented DC system to observe the switch action in a real-world setting.

5 Conclusion

This research introduces an innovative and enhanced design of SS-DCCB based on the BiTriCap technique, aiming to provide enhanced protection and reduce overvoltage levels compared to MOV-based DCCBs. The effectiveness of the proposed design is evaluated through a series of switching and fault detection tests, and the results are systematically compared with simulation outcomes to validate the approach.

The orchestrated process is meticulously managed by a programmed microprocessor, which oversees and controls the DC line current in real-time. The microprocessor triggers interruption commands at predefined levels, ensuring the effective protection of the load. Notably, the observed overvoltage across the main switch is minimal, measuring only *2 volts*, a level well within the acceptable range.

The achieved success in zero current crossing is attributed to the innovative strategy of redirecting the surge into the bypassed snubber capacitor. This approach not only demonstrates the feasibility and efficacy of the proposed BiTriCap technique but also highlights its potential in enhancing the overall performance and reliability of SS-DCCBs in DC MGs.

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IV. Chapter 4:

Manuscript 3: DSAT Technique Surge Absorption

This manuscript presents the development of low-voltage SS-DCCBs, a novel Divided Surge Absorption Technique (DSAT) is introduced to enhance fault protection. The proposed design splits surge absorption into two segments: a line-side bypass circuit using SCRs and capacitors, and a load-side dissipation loop with diodes. This approach ensures rapid fault interruption within 10 μs while reducing overvoltage and improving component longevity. The technique is validated at 48V and 300V through simulations and practical tests, demonstrating superior reliability, simplified design, and scalability for DC microgrids and medium-voltage systems.

The proposed DSAT technique in this chapter, compared to the BiTriCap technique introduced in Chapter 3, reduces the number of active components in the bypass snubber surge absorber by one, resulting in lower control circuit complexity. It also divides surge handling into line-side and load-side components. On the load side, the surge is redirected through a diode–inductance–fault path, eliminating the need for a dedicated surge absorber. Only the line-side surge requires absorption, which is managed using a current blocker in series with a thyristor. Consequently, the capacitor used in this technique is smaller than that in the BiTriCap approach. Overall, the DSAT model reduces the cost, physical size, and complexity of the SS-DCCB compared to the BiTriCap technique.

Furthermore, the DSAT technique has been tested at two voltage levels and under varying system inductances and predefined current thresholds to evaluate its performance and confirm the flexibility of the proposed model.

Enhanced LV Solid-State DC Circuit Breaker Design with Divided Surge Absorption Technique

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Abstract- This article presents an innovative design for low-voltage (LV) solid-state DC circuit breaker (SS-DCCB), incorporating the divided surge absorption technique (DSAT). This novel approach divides the circuit-breaking process into two distinct sections: a line-side surge absorber and a load-side surge damper. Upon detecting a fault through embedded current transformer (CT) measurements and microprocessor-defined thresholds, the SS-DCCB rapidly protects the system by disconnecting the load, ensuring reliable performance. The line-side surge is absorbed via a bypassed path utilizing silicon-controlled rectifier (SCRs) and a series electrolytic capacitor based subcircuit, while the load-side surge is mitigated through a circulation diode pathway. The adaptability of the proposed DSAT technique is assessed at two voltage levels: $V_1=300V$ and $V_2=48V$, demonstrating its effectiveness and potential to extend in a wide range of LV and medium voltage (MV) levels. These findings validate the theoretical concept through MATLAB simulations and in-lab practical analysis demonstrated by the proposed model.

Keywords: SS-DCCB, DC Microgrid, Divided Surge Absorber, Zero Current Source, DC Protection, DC Fault Detection.

1 Introduction

The design of DC Circuit Breakers (DCCBs) for evolving network architectures presents a range of challenges, particularly with the rising integration of DC microgrids, where surge absorption is a crucial concern [1],[2]. As DC systems grow more prevalent, addressing the limitations of conventional surge management techniques becomes essential [3]-[5]. Existing solutions, such as Mechanical DCCBs (M-DCCBs) and Hybrid DCCBs (H-DCCBs), offer

potential methods for dealing with these challenges [6], [7]. However, they are constrained by their relatively slow response times, as M-DCCBs require milliseconds to disconnect, making them unsuitable for high-speed DC load interruptions where microsecond-scale responses are required [8].

Surge absorption technologies, particularly Metal Oxide Varistors (MOVs), have been widely used in DC systems [9]. However, these components come with significant drawbacks, including gradual degradation, increased clamping voltage, current leakage, and added capacitance, which can create safety risks in DCCB applications [10]. Despite advancements in DCCB design, a gap remains in achieving an MOV-free solution that enhances surge absorption while optimizing performance [11].

In terms of lifespan in DC applications, an MOV typically has a defined lifetime of 5.6 years [12], while an electrolytic capacitor is rated for 60,000 h at 60°C. It is also confirmed that the DC electrolytic capacitor's impedance is minimized within a frequency range of 40 kHz [13]. In this research, based on the selected parameter values, discharge time ($t= 5\times\tau = 5\times RC$), and considering that the capacitor is not continuously connected to the circuit, its lifespan is expected to reach around 120 million switching cycles and surge absorption events. However, factors such as temperature and humidity can affect the performance of the surge absorber [13].

This study introduces a novel topology for DCCBs, designed to overcome the speed limitations and complexity of existing models. The proposed model has been validated at 48V and 300V for current thresholds of 12A, 20A, and 30A, demonstrating improvements in overvoltage management across the main switch. In comparison to the BiTriCap technique, which relies on capacitors for surge absorption, the proposed design significantly increases switching speed, reduces the number of active components, simplifies control circuits, and lowers manufacturing costs [11].

Several existing DCCB designs, such as the SCR-BCB [14] and TCB [15] models, incorporate transformers, MOVs, and other active components. While these designs are effective, they introduce increased system complexity, cost, weight, and potential additional surge sources. Likewise, RB-IGCT model employing MOV-C snubbers and parallel energy absorption components face similar challenges [16]. Furthermore, previous designs that utilized capacitors for surge absorption have yet to adequately address cost concerns or

account for the impact of load or line inductance on DCCB performance in practical applications [17], [18].

The key innovation in this study is the development of SS-DCCB design that partitions DC surges caused by circuit interruptions into two distinct segments, one on the load side and the other on the line side. This approach ensures high-speed, reliable performance while addressing the shortcomings of existing designs. The proposed DSAT topology offers several highlighted advantages and contributions, as outlined below.

- Improved switch protection and reduced overvoltage across the main switch eliminate the need for parallel surge suppressors, thereby extending the switch's lifespan.
- The design principle has been validated for voltages up to $300V$ and offers potential for further studies to adapt the design for higher voltage levels in SS-DCCBs.
- The proposed SS-DCCB incorporating the DSAT technique exhibits reliable performance, effectively absorbing surges through the capacitor's charge and discharge operation.
- Consideration of both line and load inductances ensures effective suppression of released energy, making the SS-DCCB design applicable in real-world scenarios.
- Swift switch performance, with disconnection occurring within $10\mu sec$, ensures rapid protection of the system, SS switch, and load, thereby minimizing voltage surge.
- Efficient absorption and redirection of circuit inductive energy ensure optimal management of released energy through separate bypass routes.
- Minimization of active and passive components enhances efficiency and simplifies the design.

This study introduces an innovative model founded on the principle of dividing the effects of faults. The proposed model undergoes simulation for two distinct voltage and DC system configurations, encompassing both $V_1=300V$ and $V_2=48V$ scenarios. Additionally, practical experimentation is carried out specifically at $48V$, providing comprehensive validation of the model's flexibility across various voltage levels. The voltage levels of DC Microgrids are specified within the standards IEC60077-3, IEC61660-1, and IEC60947-2 [19].

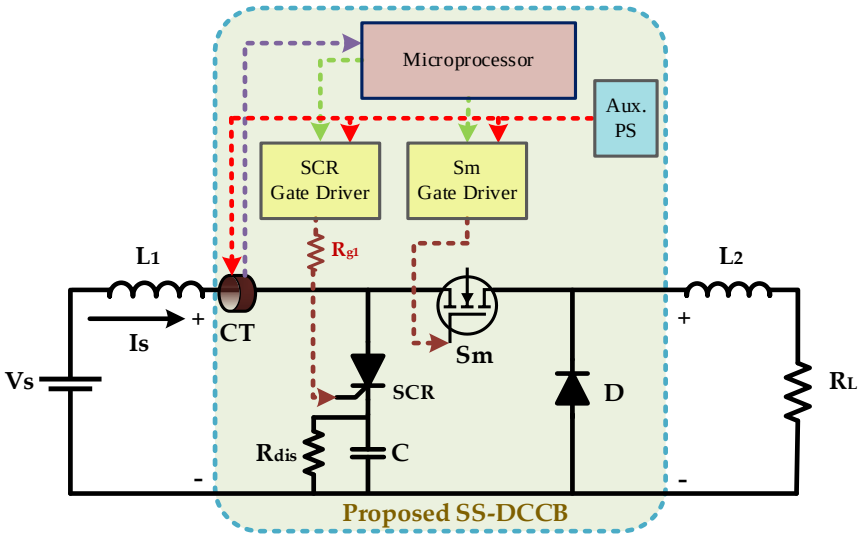


Fig. 1: Proposed SS-DCCB model scheme

In the proposed SS-DCCB model as shown in Fig. 1, the surges generated during switching and fault detection are carefully divided into two distinct sections: the line side and the load side. Within this design framework, the primary switch (S_m) receives protection through shock redirection employing the DSAT technique. The circuit achieves a switching frequency (rise time) of approximately *100 kHz*, corresponding to a switching time of *10 µsec*. Upon detecting a fault threshold, the STM controller issues commands to both switches—an ON command to the SCR and an OFF command to the MOSFET. A 1 µs delay in deactivating the MOSFET is applied to account for the differences in switching characteristics and operational speeds between the SCR and MOSFET.

This delay is accounted for in the ARM controller programming as a corresponding delay in turning on the MOSFET.

According to the SKKT27B12E SCR datasheet, the SCR has a switching speed of *1 µs* (equivalent to a *1 MHz* switching frequency). Meanwhile, the IXFP110N15T2 MOSFET has a rise time of *44 ns*, enabling it to handle circuit interruption. The overall switching operation of the proposed SS-DCCB occurs within the microsecond range. Upon receiving the SCR activation command, the released inductive energy on the line side is directed towards the electrolytic capacitor via a bypassed path, while on the load side, the discharged energy is channelled into the circulating loop created by the diode. In this design, the capacitor functions as a zero-current source (ZCS) or current-blocking element.

The circuit mechanism is visually represented in the flowchart depicted in Fig. 2. During normal operation of the SS-DCCB, the circuit's current (I_s) level is checked by collecting it's value by a line current transformer (CT) at intervals of *147* nanoseconds. Concurrently, the microprocessor continuously observes the circuit's performance at time intervals of $0.75\ \mu s$. Upon detection of a fault current exceeding the predefined threshold (greater than *20A*), protection command is swiftly sent to SCR, followed by a command to the S_m after $1\ \mu s$ to bypass the surge into the capacitor. In proposed model, as depicted in the flowchart presented in Fig. 2, a push button is considered to activate the gate signal of S_m.

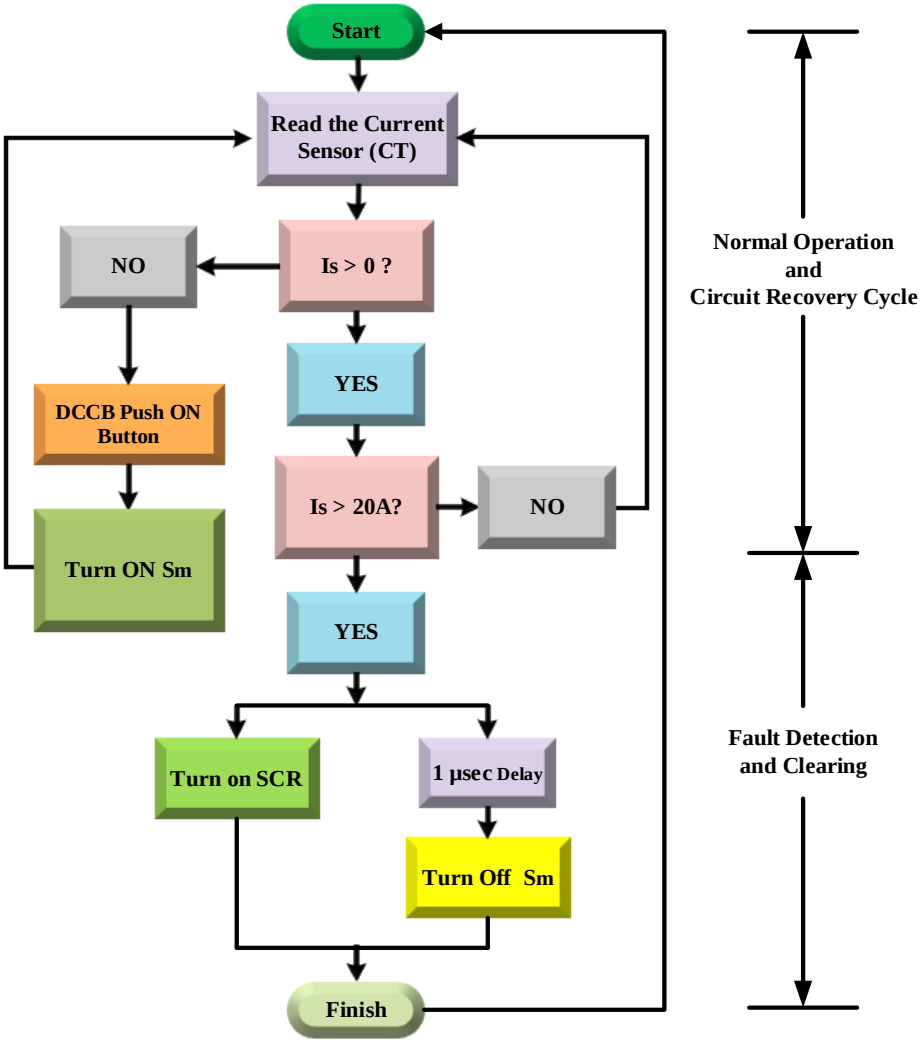


Fig. 2: Circuit operational control flowchart

In such scenarios, the line side loop functions to block the current on the line side after absorbing the switching effects induced by L_1, effectively mitigating its impact. Simultaneously, the load side loop automatically and efficiently discharges the energy stemming from the inductance of the load side, L_2, facilitated by the inclusion of a carefully

selected diode. This comprehensive approach ensures the seamless operation of the SS-DCCB, guaranteeing robust protection. In the proposed model, R_{g1} represents the gate resistance of the SCR and serves two key functions: first, it limits the output current from the gate driver, and second, it protects the microprocessor from potential damage. This strategic placement ensures the controlled and safe activation of the SCR, reducing risks and enhancing overall circuit performance. Unlike MOSFETs, which have a voltage-driven gate, the SCR gate is current-driven. To prevent current flow from the microprocessor to the thyristor, Rg1 is incorporated into the gate circuit. To maintain uniformity in the control side of the proposed model, identical A341H gate drivers are employed.

2 Design Methodology

In the process of circuit design and component selection, careful consideration must be given to two distinct categories of components: active and passive. When selecting active components, parameters such as voltage and current ratings, operational temperature limits, and the ability to handle circuit fault current based on manufacturer specifications are taken into account.

For the calculation and design of passive components, such as the line side ZCS capacitor, it is imperative that they have the capability to absorb and contain the surge originating from the line side while effectively blocking the passage of current. Consequently, it is essential for the capacitor's capacity to exceed the energy released by the inductance, ensuring optimal performance as presented in Eq. (1)

$$\frac{1}{2}CV_s^2 > \frac{1}{2}L_1I_s^2 \tag{1}$$

where, C represents the bypass ZCS capacitor, V_s denotes the voltage of the DC system, L_1 represents the inductance on the line side, and I_s signifies the maximum current flowing through the capacitor.

Taking into account Eq. (1), the calculation of C can be performed for both V_1 (as described in Eq. (2)) and V_2 (as outlined in Eq. (3)) SS-DCCB designs.

$$\frac{1}{2}C_{V1}(300^2) > \frac{1}{2}(15 \times 10^{-3})(30^2) \tag{2}$$

$$\frac{1}{2}C_{V2}(48^2) > \frac{1}{2}(0.67 \times 10^{-3})(20^2) \tag{3}$$

As the simulation of the proposed model covers both V_1 and V_2 voltage levels using the same formulation, the capacitor can be determined to be $C_{V1}=150\mu F$ for V_1 design and $C_{V2}=116\mu F$ for V_2 design.

As a critical component of the SS-DCCB design, careful consideration must be given to the discharge of the capacitor to ensure it has sufficient capacity to absorb the system surge. To assess the line and load inductances, whether for underground or overhead lines, the inductors can be calculated using the following formulas:

- For overhead transmission lines: $L = 2 \times 10^{-4} / \ln\left(\frac{D}{r}\right)$

- For underground lines: $L = \frac{\mu_0}{2\pi} ln(\frac{2h}{r}) \times 1000$

In these equations, L represents inductance per kilometre, r and D denote the radius and diameter of the conductor, h is the depth of the conductor, and μ_0 is the permeability of free space, approximately $4\pi \times 10-7\ H/m$ 0.

To discharge the capacitor after switching and fault detection surge absorption, the circuit utilizes a simple passive RC sub-circuit with a time constant for capacitor discharging, as implemented in this paper. Fig. 3 depicts the circuit performance during fault detection, highlighting that all current in the line side loop must flow through the capacitor, while the current through the thyristor must remain below its holding current. The holding current of the thyristor, specifically the SKKT27B12E, is *100mA*, so the current in the discharge resistor (R_{dis}) must not exceed this threshold according to the manufacturer's specifications. Therefore, once the capacitor is fully charged, the current flowing through the thyristor must remain below *100mA*, indicated as $I_1=I_H < 100mA$. If this condition is not met, the current could flow through the path comprising V_s-L_1-*SCR*–R_{dis}, potentially leading to damage to the system.

$$V_C = V_{R_{dis}} = R_{dis} I_H \tag{4}$$

where, V_C represents the voltage across the capacitor, R_{dis} denotes the discharge resistance, and I_H stands for the holding current of the SCR.

For the V_2 design with $V_S=48V$, the maximum voltage across the capacitor would be $V_C=76.8V$. Accordingly, R_{dis} is calculated as *768*Ω.

Using a similar calculation, in the scenario of V_1 application with V_S=300V, the capacitor voltage increases to $V_C=363V$ during fault detection. Consequently, the discharge resistor can be determined as $R_{dis} = 3630\Omega$.

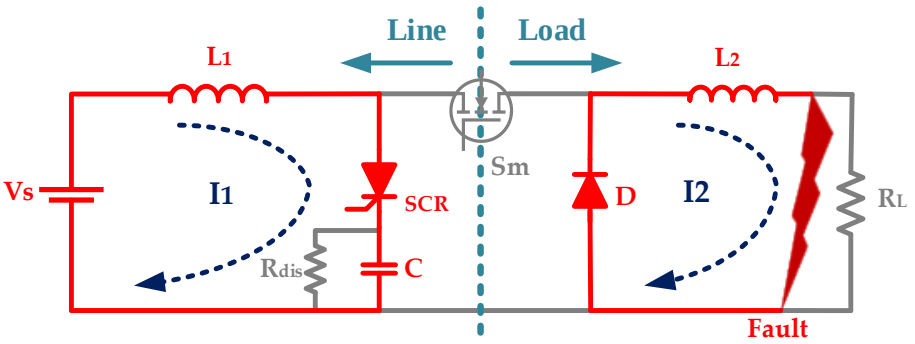
When designing the diode for the load side, it is imperative to ensure its capability to withstand the current released in the load side inductance. This consideration serves to minimize the complexity of the circuit design.

When a fault occurs across the load, such as a short circuit, the line current measured by the sensor (CT) is compared with a predefined setpoint within the controller. The controller conducts measurements of the current sensor value seven times per microsecond. Upon detecting a short circuit, indicated by the measured current exceeding the defined threshold, the controller commands the SCR connection and then main switch (MOSFET) disconnection.

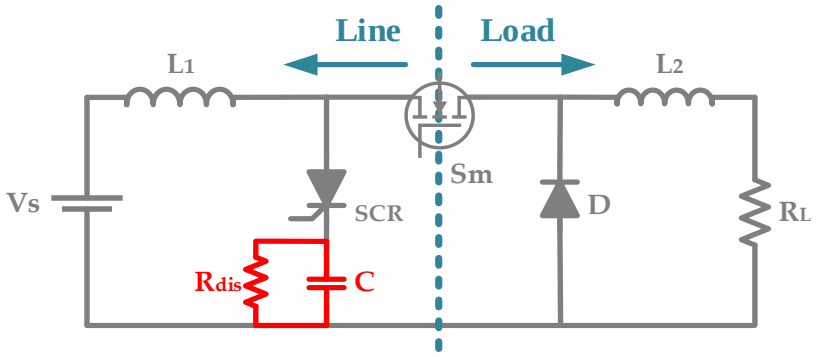
In this scenario, the circuit is divided into two sections, as depicted in Fig. 3a. As a result, two distinct loops emerge. The fault current and the released energy from the load side loop are discharged via the *D-L2-Fault* path. Meanwhile, on the line side, the released energy is redirected to the capacitor through the *Vs-L1-SCR-C* path. Subsequently, once the ZCS capacitor is fully charged, the current is obstructed from the path, effectively creating an open circuit.

Once the capacitor has fully absorbed the surge, the SCR automatically turns off, as the current is blocked in loop 1. The capacitor then discharges through the R_{dis}-*C* loop, as illustrated in Fig. 3b.

The primary achievements of this technique include: 1) load protection, 2) shielding the solid-state main switch from surges and shocks during switching operations, 3) simplifying the DCCB and circuit design, 4) fortifying the circuit's resilience against faults, whether they occur on the line or load side, 5) reliable operation, and 6) quick performance.



a. Fault Detection



b. Capacitor Discharge Process

Fig. 3: Circuit Fault Detection Operation

By considering the circuit performance depicted in Fig. 3, it becomes feasible to compute the currents circulating within each loop. In order to characterize the transient behaviour of I_1, Eq. (5) is employed based on KVL in V_S-L_1-SCR-C.

$$I_1(t) = \frac{1}{L_1}\int (V_s - V_{SCR} - V_C)dt + i_1(t_f) \tag{5}$$

where, I_1 represents the current flowing through loop 1 during fault time, with L_1 denoting the inductance on the line side. Additionally, V_s signifies the voltage of the DC system, V_{SCR} represents the voltage across the SCR, V_C stands for the capacitor voltage, and $i_1(t_f)$ indicates the initial current in the inductance during fault time.

Moreover, the calculation of the current in loop 2 can be conducted using Eq. (6).

$$I_2(t) = \frac{1}{L_2}\int V_D dt + i_2(t_f) \tag{6}$$

where, I_2 represents the current circulating through loop 2 during fault time, while V_D denotes the voltage across the diode. Furthermore, L_2 signifies the inductance on the load side, and $i_2(t_f)$ indicates the initial current of L_2 during fault time.

In the proposed DSAT, the maximum fault current can be determined using Eq. 7.

$$i_{f-max} \approx ((V_P + V_D)/((L_1 + L_2).\omega_f).e^{-\gamma t}\sin(\omega_f.t) \quad (7)$$

where, V_{sm} represents the switch voltage, and V_P, ω_f, ω_0, and γ can be computed using Eq. 8.

$$V_C = (V_{SCR} + V_C), \omega_f = \sqrt{\omega_0^2 - \gamma^2},\ \omega_0 = 1/\sqrt{(L_1 + L_2).C}, \gamma = R_{dis}.C, R_{eq} \approx R_{on,Sm} + R_{dis} \quad (8)$$

It has been established that the behaviour of the loop currents in both loops follows an exponential trend. Subsequent simulations and practical tests have been conducted to validate the formulations presented. The outcomes from these endeavours corroborate the theoretical predictions, lending further credence to the accuracy and reliability of the proposed models.

2.1 Switching operation of the proposed model:

to demonstrate the circuit switching performance by repeatedly operation of S_m, a test is carried out. The test utilized a command signal with a *20*-second symmetrical ON-OFF cycle for switching of S_m. During the interruption, the main switch voltage peaked at *51.25V*, resulting in a *3.25V* (*6.7%*) overvoltage. No current surge was detected in the main circuit path, validating the effectiveness of the proposed DSAT.

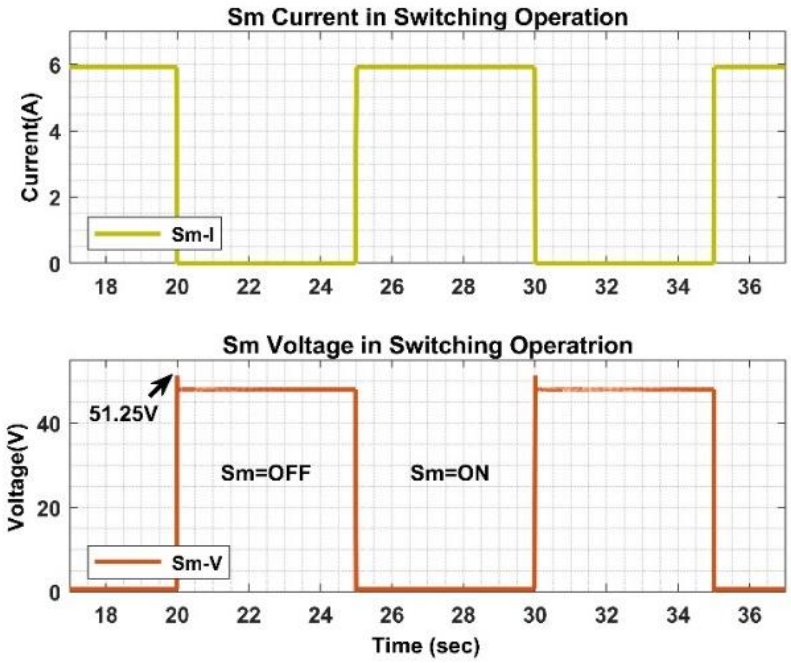


Fig. 4: S_m current and voltage in switching operation.

In this scenario, the energy released from the inductances is redirected into the corresponding sub-circuits. Fig. 5 illustrates the behavior of the SCR voltage and current during the switching operation of the S_m. When the OFF command is given, the energy released from the line inductance flows through the SCR (*5.98A*) and is absorbed by the capacitor. The ON and OFF operations are as follows:

$S_m = ON$: $V_{SCR} = -16.69V$, I_{SCR} and $I_{Cap} = 0$, *SCR=OFF.*

$S_m = OFF$ (Surge Absorption): $V_{SCR} = V_s - V_{Cap} = -2.42V$, $V_{Cap} = 50.42V$, I_{SCR} and $I_{Cap} = 5.98A$.

The current flowing through the SCR and capacitor in the OFF state demonstrates the capacitor's effectiveness in absorbing the switching surge.

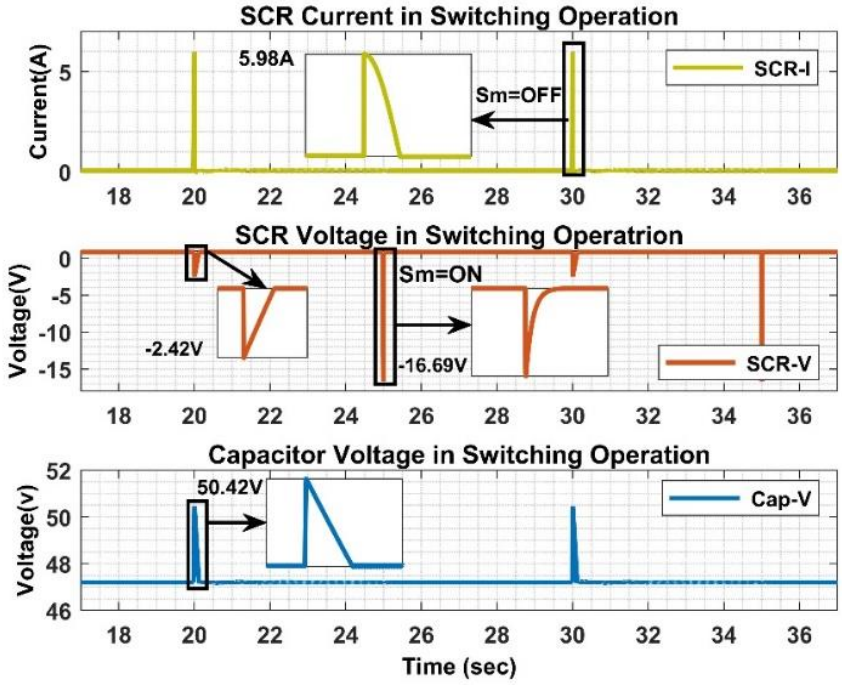


Fig. 5: SCR current and voltage, Capacitor voltage in switching operation

The circuit operation shows that the circuit is robust against multiple switching operation.

3 Simulation Results and Analysis

In this phase of the research, simulations were conducted to assess parameter variations for two input DC voltage levels ($V_1=V_s=300V$ and $V_2=V_s=48V$) and two set of parameters within the system. The inductance values were deliberately adjusted to observe the impact of the proposed model on the variation of energy release in the system.

For the V_1 voltage level, the threshold current is defined as $30A$, while for the V_2 voltage design, it is set at $20A$. The performance of the main switch (S_m) is depicted in both simulated models, as shown in Fig. 6.

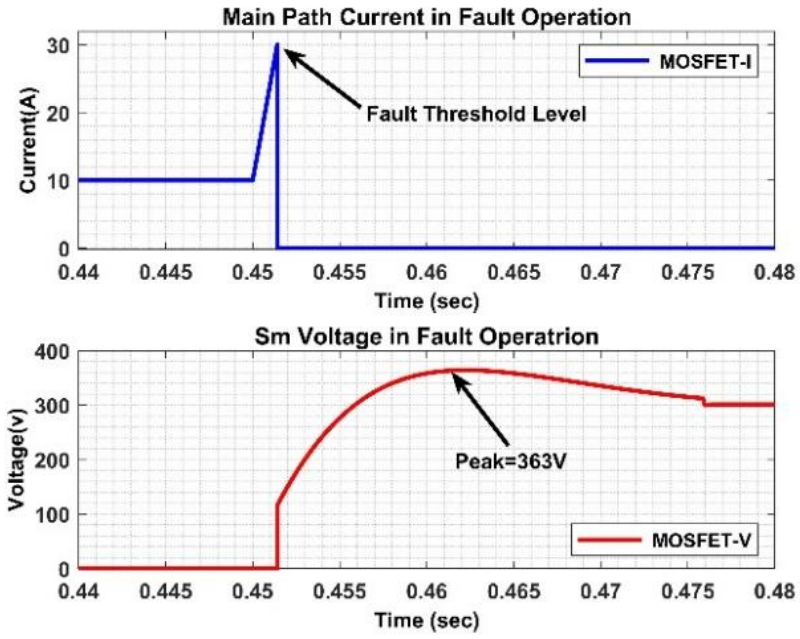
In both Fig. 6a and Fig. 6b, upon occurrence of a fault within the system, the current undergoes an increase, prompting the microprocessor to evaluate its magnitude and compare with the pre-defined setpoint. When the line current reaches the threshold level, the microprocessor issues distinct commands to both active switches. A deactivation command is sent to S_m while an activation command is dispatched to the SCR.

In Fig. 6a, the test is performed with parameters set as follows: $V_1=300VDC$, $L_1=15\ mH$, $L_2=6\ mH$, $R_L=30\Omega$, and $C=470\ \mu F$. Under these conditions, the overvoltage across the main

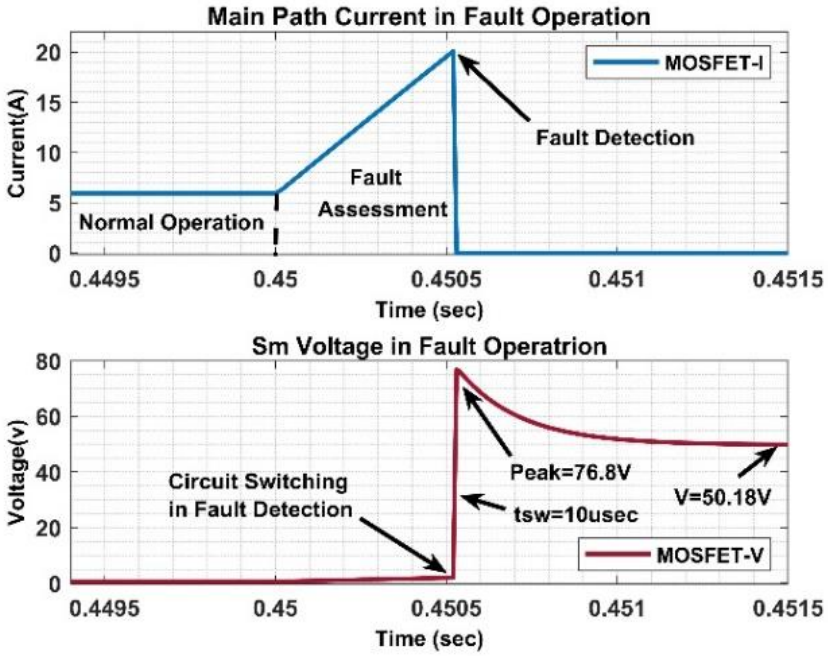
switch (S_m) of the safeguarded circuit registers at *63V*, approximately *21%* of the circuit's nominal voltage. This level falls within the acceptable range for circuit-breaking applications, and the voltage tolerance of the IXFP110N15T2 MOSFET remains within this range of shock. The threshold current (I_{th}) for fault detection in this test is configured at three times the nominal current (I_n) of the system, denoted as $I_{th} = 3 \times I_n$.

In Fig. 6b, the test is carried out with the parameters configured as follows: V_2=*48VDC,* L_1=*0.67 mH,* L_2=*1.03 mH,* R_L=*8*Ω, and *C=470 µF*. Under these conditions, the voltage overshoot of the protected circuit amounts to *28.8V*, which is approximately *60%* of the circuit's nominal voltage. In this scenario, the threshold current (I_{th}) for fault detection is set at 3.33 times the nominal current (I_n) of the system, expressed as $I_{th} = 3.33 \times I_n$.

Based on the IEC60898-3 and IEC60947-2 standards for Circuit Breakers it is evident that the selected fault current level of the DCCB should be chosen with caution to protect the system and prevent overvoltage of the switch [20],[21]. A higher threshold current level results in the release of more square energy as mentioned in and Eq. (1). Considering the threshold fault current as twice the line nominal current ($I_{th} = 2 \times I_n$) would lead to negligible voltage overshoot (in the range of *3.7V* or *7%* of the DC system voltage).



a) S_m (MOSFET) voltage and current in V_s=300V, L_1=15 mH, L_2=6 mH



b) S_m (MOSFET) voltage and current in V_s=48V, L_1=0.67 mH, L_2=1.03 mH

Fig. 6: Simulation Results: S_m voltage and current in a) V_1 design, and b) V_2 design

To emphasize the influence of the threshold fault current level on the overvoltage across the main switch, comparative results are presented in Table 1. It's evident that the overvoltage across the main switch is directly influenced by the chosen threshold for fault current, which in turn is tied to the energy released within the system. When the threshold current is set at $I_{th}=3.3\times I_n$, the maximum overvoltage reaches *60%* of the DC system voltage across the main switch. Conversely, the minimum overvoltage occurs at $I_{th} = 2\times I_n$, which is *7%*.

Table 1. Overvoltage Value vs Threshold Current Level

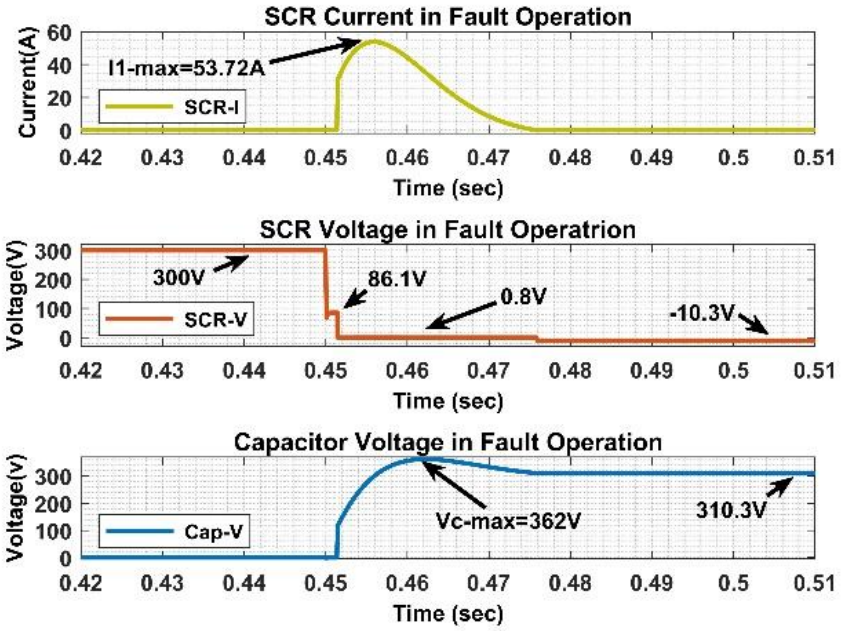
Voltage Level	Threshold Current	Overvoltage Value	Percentage
300V	$I_{th} = 3 \times I_n$	63V	21%
48V	$I_{th} = 3.3 \times I_n$	28.8V	60%
48V	$I_{th} = 2 \times I_n$	3.7V	7%

The design concept presented herein demonstrates a high degree of flexibility, rendering it suitable for deployment in both LVDC Microgrids and MVDC Microgrids. Notably, the circuit response time within V_2 systems is measured at $t_{sw}=10\mu sec$, an interval deemed sufficiently expedient to effectuate the disconnection of the load side and ensure the protection of the DC system from potential hazards.

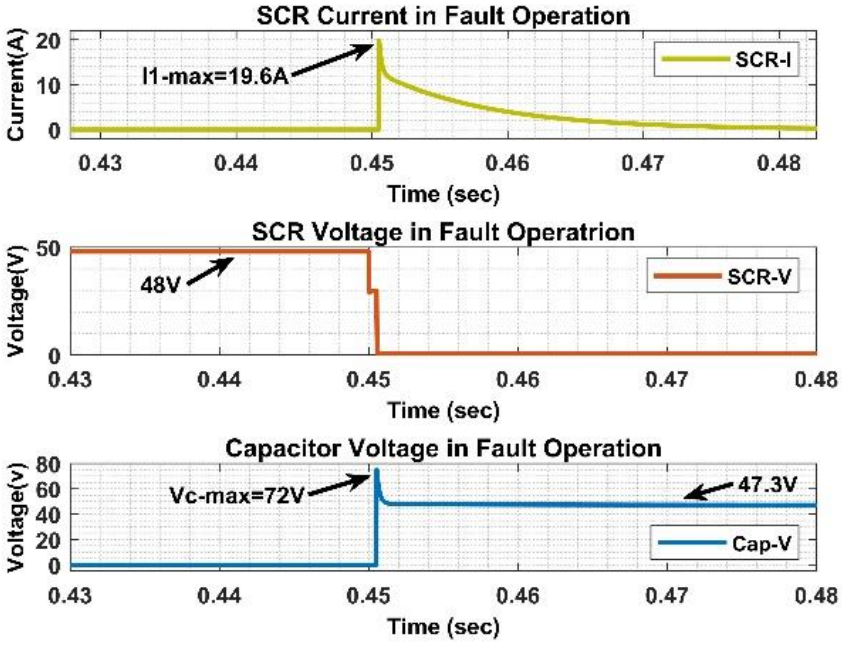
In a comprehensive analysis depicted in Fig. 7, the comparison of voltage and current characteristics between SCR and capacitor is provided, alongside an examination of the consequential impact stemming from the release of energy on the bypassed line side of the SS-DCCB within both V_2 and V_1 configurations. These results meticulously scrutinize the implications of varying voltage levels and system inductance on the overall switching performance, thereby elucidating crucial insights essential for informed decision-making in the realm of DCCB design and operation.

In Fig. 7a, an observation reveals that the transient bypassed current traversing through the thyristor surges to $53.7A$, surpassing the nominal line current by $23.7A$. This surge is attributed to the elevated level of inductance incorporated within the system, specifically denoted as $L_1=15\ mH$. During the period of SCR conduction in fault operation, the voltage across the capacitor escalates to $362V$, effectively absorbing the shock generated during switching.

Comparatively, in Fig. 7b, the transient shock is analysed in contrast to the findings in Fig. 7a. Herein, a transient shock measuring $I_{1\text{-}max}=19.6A$ is discerned within the bypassed branch, while concurrently, the capacitor voltage ascends to $V_{C\text{-}max}=72V$. Subsequently, the capacitor undergoes a full charge, stabilizing the capacitor voltage at $47.3V$. This comparative analysis between Figs. 7a and 7b elucidates the nuanced dynamics of transient shock responses and capacitor behaviour, furnishing insights for system optimization and performance enhancement.



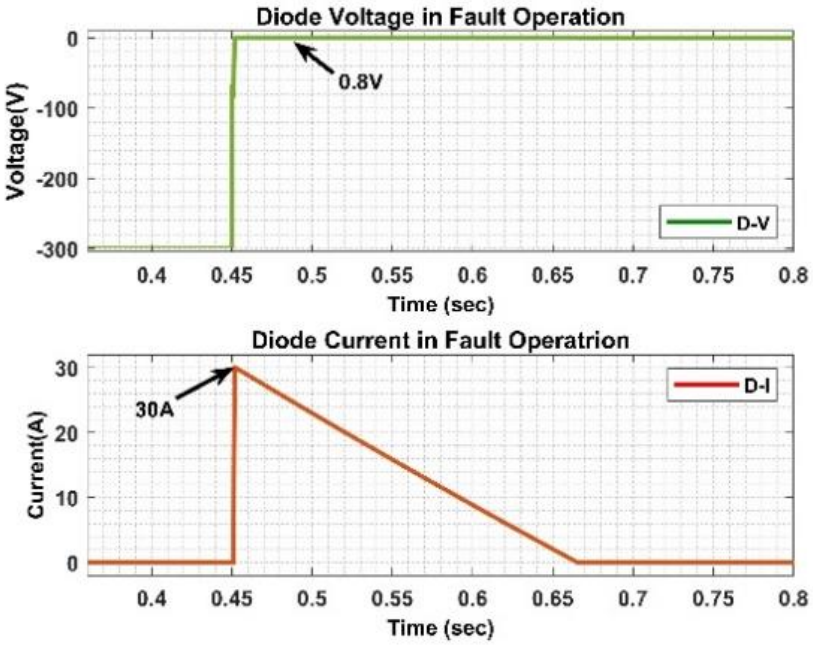
a) SCR and capacitor voltage and current (V_1 design)



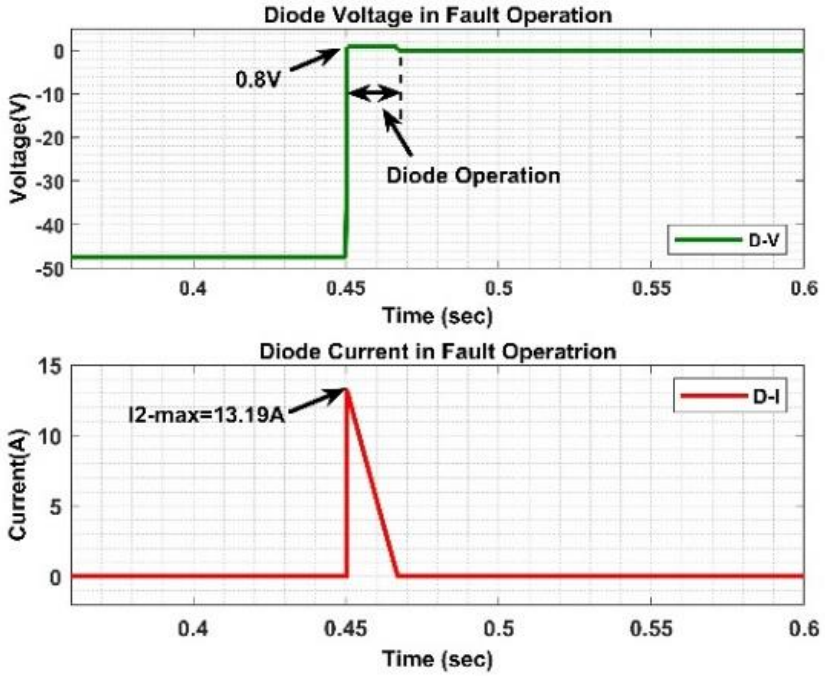
b) SCR and capacitor voltage and current (V_2 design)

Fig. 7: Simulation Results: comparison of voltage and current of SCR and capacitor and impact of released energy of SS-DCCB in V_1 and V_2 designs.

In Fig. 8, the voltage behaviour of the load side diode and its conduction characteristics are depicted, alongside the transient performance of the current within *L_2-Fault-D* loop.



a) Diode voltage and current in fault operation in V_1=300V



b) Diode voltage and current in fault operation in V_2=48V

Fig. 8: Simulation Results: Diode voltage and current in both designs

Both Fig. 8a and Fig. 8b illustrate the dissipation of released energy from the inductance, facilitated through the formation of the loop. Notably, in the V_2 DCCB design, the maximum

current within loop 2 is denoted as $I_{2\text{-}max}$= *30A*, whereas in the V_1 DCCB design, this maximum current is observed to be $I_{2\text{-}max}$= *13.19A*. These findings underscore the differential transient performance between V_1 and V_2 configurations.

4 Experimental Validation

The experimental test was carried out to assess the performance of the proposed SS-DCCB design operating at V_2= *48VDC*. The primary objective of this test was to validate both the proposed topology and the DSAT technique against simulation results.

For validation of the proposed model, the experimental setup utilized a Chroma DC Power Supply (62100H-100P) as the system's power source, while a Programmable DC Load (Chroma 63204-5.2KW) functioned as the load. Additionally, a *30V/2A* auxiliary power supply was integrated to provide power to the gate drivers and the STM ARM Controller.

The technical specifications and part numbers of the components are detailed in Table 2.

Table 2. Circuit Components Value

Parameter	Acronym	Value	Unit
Input DC Voltage	V_S	48	VDC
Snubber Capacitor	C	470	μF
Microprocessor	ARM Microcontroller	STM32F407VG	-
Main Switch	S_m (MOSFET)	IXFP110N15T2	-
Bypass Thyristor	SCR	SKKT27B12E	-
Diode	D	HER303	-
Gate Driver	GD	A341H	-
Line Side Inductance	L1	670	μH
Load Side Inductance	L2	1.03	mH
Load Resistance	R_{load}	9.6	Ω
Gate Resistance	R_{g1}	20	Ω
Current Transformer	CT	LEM 100P	-

The practical implementation of the proposed SS-DCCB integrated with the DSAT technique is visually depicted in Fig. 9, providing a tangible representation of the experimental setup, and facilitating further analysis and evaluation of its performance characteristics.

Another advantage of the proposed DSAT topology is its robustness when connected to a DC power supply or DC Microgrid with an integrated buck converter. During switching and fault detection operations, the surge generated by the L_B inductance is absorbed by the C_B shunt capacitor in Fig. 9, while the surge from L_1 is expected to be dampened in capacitor (C) after the SCR is triggered.

The threshold fault detection current level, denoted as $I_f=20A$, has been established, representing 3.33 times the nominal current of the DC system, which is $6A$, as depicted in Fig. 9. Upon the occurrence of a fault within the system, the STM32 controller initiates an evaluation process. Once the current threshold is detected, a response command is transmitted to the switch, prompting it to disconnect the load.

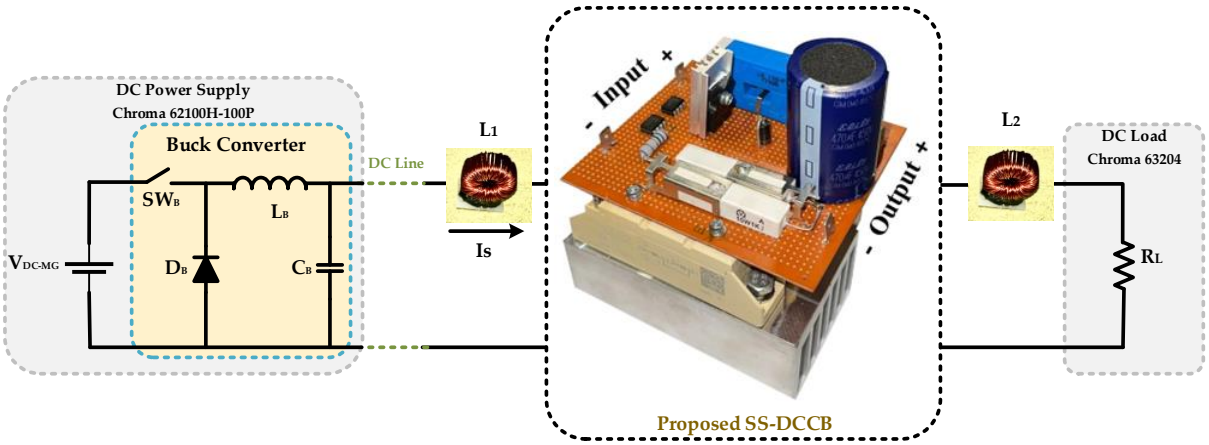


Fig. 9: Practical setup of proposed SS-DCCB with DSAT technique

The response time of the primary switch is recorded at $t_{sw}=10\ \mu sec$. While detecting faults, an overshoot in voltage of $68.8V$ is noted, comprising 43% of the system voltage (V_S) amplitude, which is 13% less than the simulation outcome. Notably, adjustments to the current threshold level can yield variations in the observed overshoot voltage, as evidenced by conducted tests. Lowering the threshold current level results in a commensurate reduction in the overshoot voltage, offering insights into real-world potential optimization strategies for system performance and reliability.

As shown in Fig. 10, the current slope is approximately *7A/ms*. According to the LEM-100P CT datasheet, the sampling interval for measuring circuit current is *147* nanoseconds, while the Arm Microprocessor's prescaler for this process is set to *0.75* µsec. Consequently, even during rapid current changes, the CT will consistently transmit measurement signals to the microprocessor, enabling the interruption command to accurately disconnect the circuit without affecting its operation. Furthermore, the *di/dt* of the SCR, based on the IXFP110N15T2 datasheet, is *150A/µsec*, which satisfies the circuit's interruption requirements.

In Fig. 11, analysis reveals a peak current flow through the bypass branch, marked as I_{1max}*=18.35A*. Concurrently, a transient voltage shock of *76V* amplitude is observed across the SCR. This voltage surge is likely attributed to system switching dynamics and the subsequent release of energy within the bypass route. Notably, a differential voltage of V_S-V_C*=-12.4V* is noted across the thyristor, stemming from the variance between the capacitor voltage of V_C*=60.2V* and the V_S*=48V* power supply voltage.

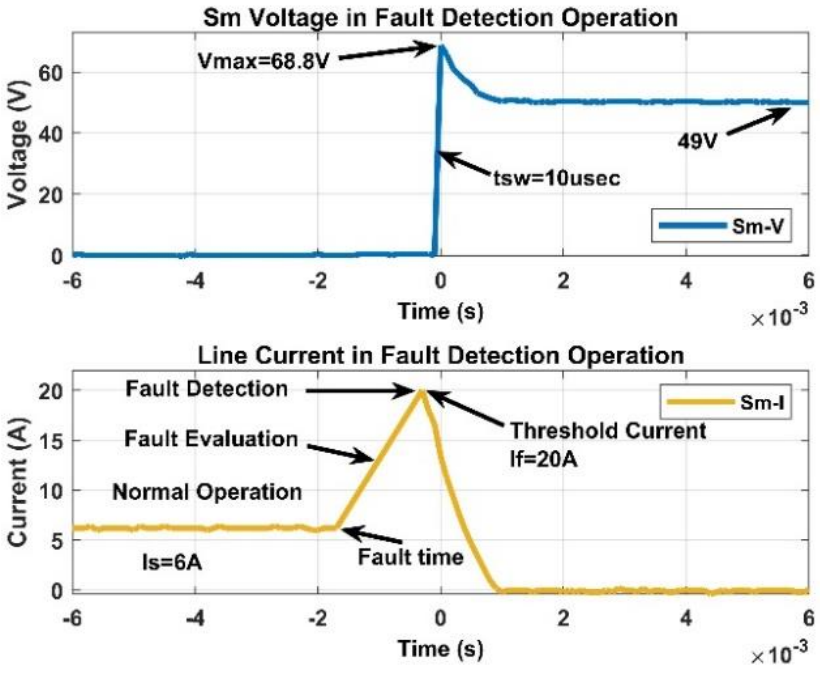


Fig. 10: Experimental Results: S_m (MOSFET) voltage and line current performance in fault detection operation

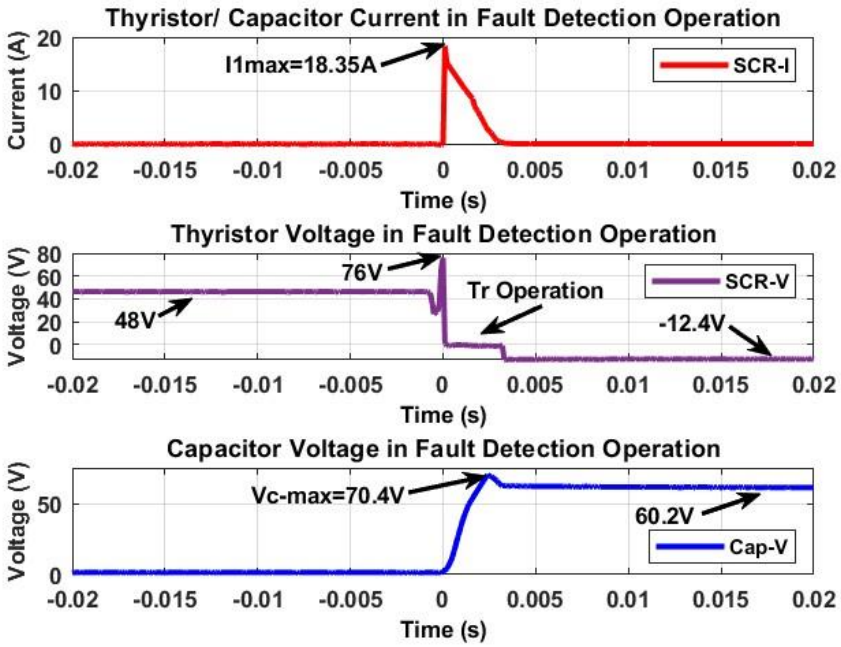


Fig. 11: Experimental Results: SCR Current, Voltage, Capacitor Voltage

In Fig. 12, the damping time (t_d) of the discharge for released energy on the load side is determined to be t_d=*1.6* msec. However, it becomes evident that upon the occurrence of a short circuit in the load, the formation of a loop on the load side ensues following the operation of the main switch. Consequently, the energy stored in the inductance dissipates rapidly along the path of *L2-Fault-D*.

During the design phase, it is crucial to verify that the components can withstand the circuit conditions. In this research, as shown in Fig. 12, the surge current circulating on the load side is *10.5A*. The selected HER303 diode has a peak surge current rating of *50A*, indicating that it can tolerate the instantaneous surge current generated by the load side inductance (L_2).

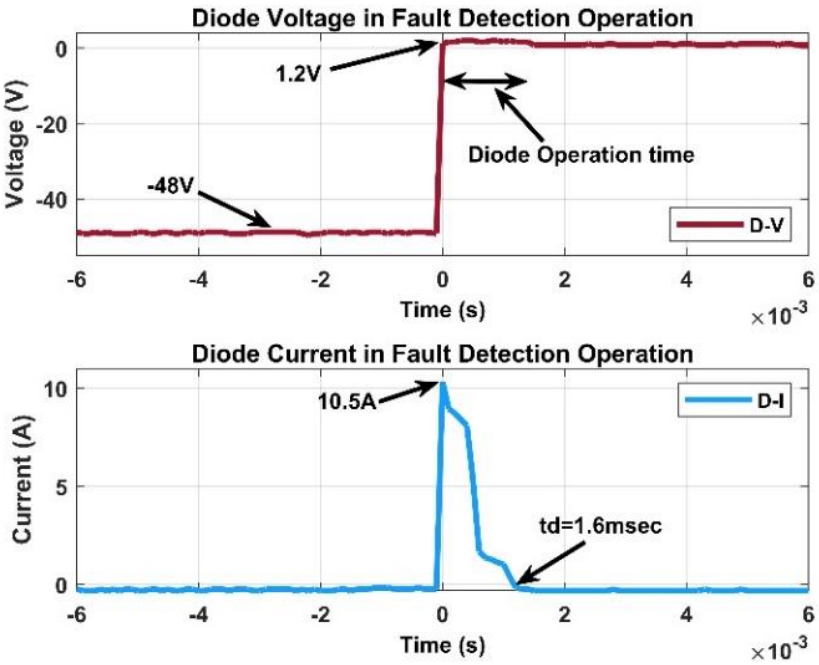


Fig. 12: Experimental Results: Diode voltage and loop 2 current in fault operation

5 Discussion

This section presents a comparative analysis to validate the proposed design by comparing it with existing techniques. The analysis highlights the simplicity and efficiency of the design, which uses minimal active components to mitigate switching effects in SS-DCCB during fault detection in DC microgrids. A real-world DC system model is employed to simulate realistic conditions, confirming the design's effective performance. Overall, the proposed model demonstrates robust and practical fault management, performing as well as or better than more complex designs.

TABLE 3

A COMPARISON STUDY WITH OTHER DCCB TECHNOLOGIES

Reference	Proposed Model	[11]	[14]	[15]	[16]
Category	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB
Technique	DSAT	BiTriCap	SCR-BCB1	TCB	RB-IGCT
Normal Reclosing Capability	Yes	Yes	Yes	Yes	Yes
Switch Type	MOSFET	IGBT	SCR	SCR	IGCT
Total Active Components	1×MOSFET	1×IGBT	4×SCR	3×SCR	4×IGCT
	1×SCR	2×SCR			
Diode	1	0	2	3	0
Capacitors	1	1	2	1	1
Inductors	0	0	2	2	0
Resistors	1	1	1	2	1
Circuit Control Complexity	Low	Medium	High	Medium	High
Surge Absorber Type	Capacitor	Capacitor	MOV-RC	MOV-RC	MOV-RC
Mechanical Switches	0	0	0	2	0
Surge Arresters	0	0	1	1	1

6 Conclusion

The study introduces a novel approach utilizing a SS-DCCB coupled with DSAT methodology for fault current interruption. Simulations were conducted for two distinct system setups: one with an input voltage of *300VDC*, a nominal circuit current of *10A*, and a threshold current of *30A*; the other with a system voltage of *48VDC*, a line current of *6A*, and a fault threshold current of *20A*. Meanwhile, experimental testing was carried out for the *48VDC* system to validate both the proposed model and the simulation outcomes. Results demonstrated successful circuit disconnection within a remarkable *10 µsec*. The proposed model partitions the circuit into two distinct line and load segments, ensuring swift switch operation and mitigating shock hazards. Response time of *10 µsec* was consistently achieved across simulation and experimentation. In the line side loop, fault current is absorbed and blocked by a ZCS capacitor through the V_S-L_1-*SCR*-*C* loop to prevent its flow, while in the load side loop, a diode discharges the released energy through the *L2*-*Fault*-*D* loop. Control of the proposed DSAT is facilitated by an ARM STM32 controller. The proposed model of SS-DCCB adopts a design approach that eliminates the necessity for a suppressor across the main switch. This is achieved through the implementation of the DSAT technique, which facilitates the separation of the circuit. The utilization of DSAT ensures efficient and reliable circuit interruption without the need for supplementary suppression components. This design innovation not only enhances the operational efficiency of the SS-DCCB but also contributes to its robustness and durability. The results of this paper are compared with recent studies to assess the performance of the proposed model against other techniques.

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V. Chapter 5:

Manuscript 4: Bidirectional SSCB with Passive Surge Absorber

This chapter introduces the Bidirectional Passive Technique (BPT), a novel method for managing surges in bidirectional DC systems. Emphasizing simplicity and efficiency, the BPT utilizes a passive RCD subcircuit to minimize surge voltage and enhance operational reliability. Experimental validations demonstrate its cost-effectiveness and adaptability across various voltage and current ranges, establishing its potential for complex DC applications.

The proposed BPT technique in this chapter, compared to the DSAT technique introduced in Chapter 4, features a bidirectional SSCB with a fully passive surge absorber, aimed at minimizing the number of active components in the DCCB. This results in significantly reduced control circuit complexity. Similar to the DSAT model, the BPT technique separates surge handling into line-side and load-side components. On the load side, the surge is redirected through a diode–inductance–fault path, eliminating the need for a surge absorber. The line-side surge, as in the DSAT technique, is absorbed using a current blocker in series with a thyristor.

In terms of bidirectional capability, the proposed SSCB with BPT supports a wider range of applications in DC microgrids by accounting for DCCB polarity and the direction of both the surge and the fault currents, thereby enhancing the overall reliability of the SSCB.

Bidirectional Solid State Circuit Breaker with Passive Surge Absorber for LV Applications

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Abstract- This letter introduces the Bidirectional Passive Technique (BPT), a novel topology for low-voltage solid-state circuit breakers (SSCBs). BPT achieves fast switching, minimizes surge voltage across the main switch, and reduces circuit complexity by limiting active components to the primary switch. The study details the working principles, operating modes, and design procedure, supported by key equations for time intervals, voltages, and currents. Validation through MATLAB simulations and practical tests demonstrates rapid interruption within *40 µsec*, ensuring effective protection for loads and DC microgrid (DC-MG) systems. The proposed model targets low-voltage systems (*48 V*) with a *10 A* threshold current for the Future Architecture of Network Project, demonstrating the high effectiveness of the BPT in DC microgrid protection.

Index terms- SSCB, Passive Surge Absorber, Snubber RC, Surge Mitigation, Fault Detection.

1 Introduction

THE advancement of DC-MGs in recent years has necessitated the development of DC protection devices capable of rapid and effective interruption to protect loads and main switches against switching surges caused by system inductance [1]. For all DC system voltage levels (even *12VDC*), the generated surge can damage the main switch and compromise system protection, making surge protection a crucial requirement in modern DC systems [2]. Despite progress, there remain gaps to enhance the design and performance of solid-state circuit breakers (SSCBs). Some research has focused on real-world systems and practical considerations, including circuit breaker designs that account for line or load inductances [3], [4], and the application of surge absorbers with high degradation rates [5], [6].

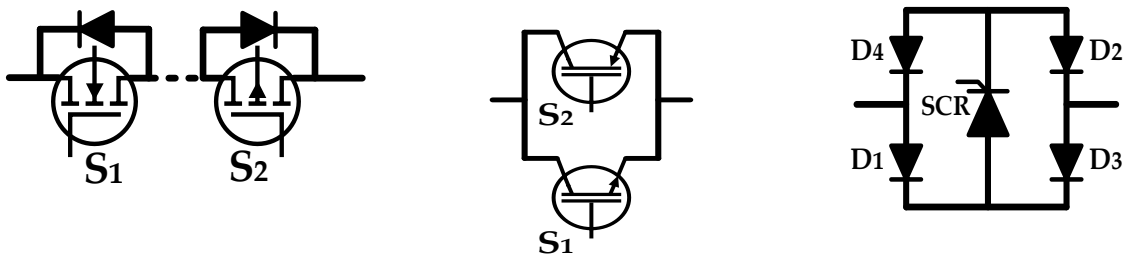
The bidirectional configurations of power electronic components are depicted in Fig. 1. MOSFETs and IGBTs are triggered using voltage-based signals, while SCRs/Thyristors function as current-based solid-state switches. The circuit configurations supporting

bidirectional operation include back-to-back (Fig. 1a) [7], antiparallel (Fig. 1b) [8], and bridged styles (Fig. 1c) [9].

The performance of a Metal Oxide Varistor (MOV) declines with repeated exposure to surge currents and their duration.

This degradation happens when the MOV is placed in a power line, enduring a VDC voltage during its inactive state. As the MOV deteriorates, its leakage current increases, leading to higher power consumption and elevated temperatures.

This heat buildup accelerates the leakage current, potentially resulting in thermal runaway. To overcome these challenges, MOV-free designs offer a solution to mitigate these limitations. Nonetheless, recent research has proposed various topologies to address and reduce these drawbacks. The T-type bidirectional SSCB presented in [10] and shown in Fig. 2(a) incorporates a module in the vertical bypass subcircuit, operating in series with an inductor as a current limiter to serve as a supportive surge absorber. The capacitors in this configuration are designed for dual purposes: absorbing surge during fault conditions and accumulating energy in steady-state conditions, requiring larger sizes compared to conventional snubber circuits. However, this design poses challenges due to the high number of switches and the presence of leakage currents in the main pathway.



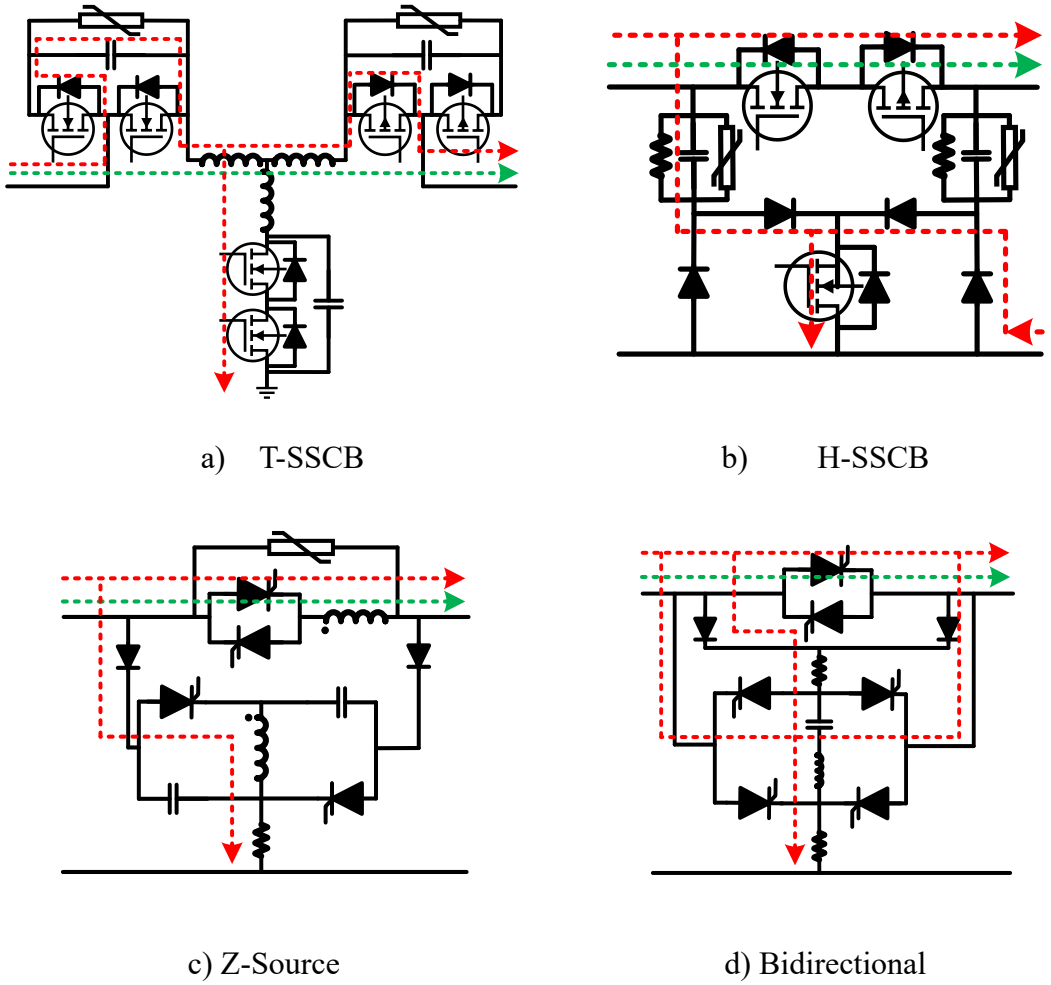
a) Back-to-Back (MOSFET) b) Antiparallel (IGBT) c) Bridged (SCR)

Fig. 1. Bidirectional connection topologies for power electronic switches

The H-type SSCB, depicted in Fig. 2(b), features a pair of back-to-back MOSFETs accompanied by an RC+MOV snubber [11]. An additional switch is incorporated to regulate the snubber, disconnecting the MOV from the power line to reduce its wear and extend the lifespan of the switches. However, integrating an extra solid-state switch in the bypassed subcircuit can add complexity to the control system.

To reduce control complexity, the SSCB design in [12] employs SCRs as snubber switches, enabling automatic turn-off when the current drops below the thyristors' holding current [see Fig. 2(c)]. This Z-source design includes additional switches to route the fault current through a bypass path and incorporates a transformer, which can introduce an additional source of surges.

In contrast, the bidirectional SSCB presented in [13] and shown in Fig. 2(d) employs six thyristors and an inductance module. While this design offers unique features, control system complexity remains a concern. In [13], three distinct operational sequences—charging, normal operation, breaking, and recharging—are incorporated into the model. To support surge mitigation, four additional switches operate in the bypass subcircuit.



a) T-SSCB b) H-SSCB

c) Z-Source d) Bidirectional

Fig. 2. recent research designs a) [10], b) [11], c) [12], d) [13]. Normal (Green) and Fault (Red) operations

However, in contrast to simpler designs, this approach introduces an inductance as an extra source of surges within the mitigation path. Furthermore, the study does not consider load-

side inductance, which may affect the results. Additional research studies and SSCB designs related to bidirectional configuration and performance are presented in [14]- [17].

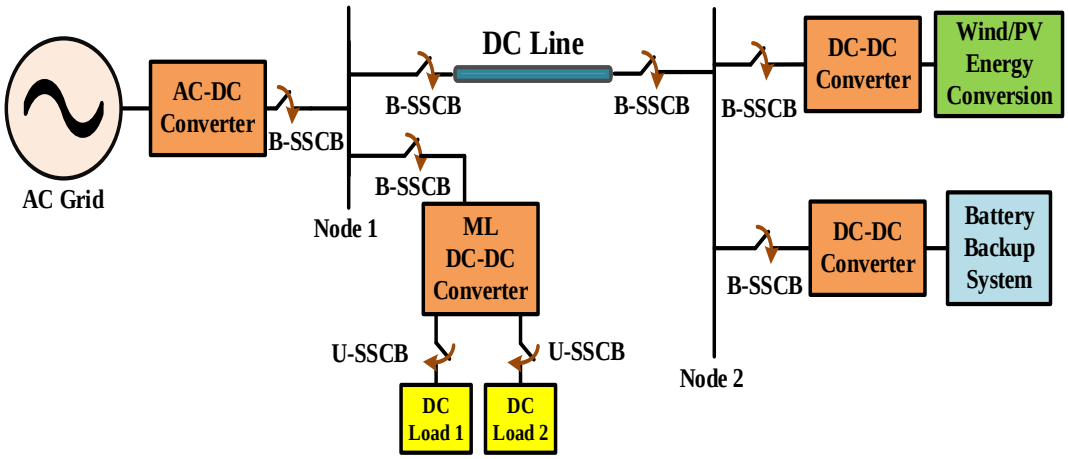
This paper introduces an innovative passive bidirectional model designed for effective surge absorption based on the RCD surge absorption principle. The proposed SSCB considers both line and load inductances, demonstrating its suitability for DC-MG applications. This paper focuses on applications for low-voltage (48 VDC) systems as defined in the Future Architecture of Network Project [3],[18],[19]. The presented fully passive model simplifies the control system, enhances reliability, reduces costs, enables fast response, and maintains operational simplicity. This design also introduces an effective surge absorption technique, utilizing a simple charge and discharge process for capacitors.

The key contributions of this research are:

1- Fully passive bidirectional surge absorption, ensuring robust protection without active control intervention. This makes the design multifunctional for both inter-bus and bus-to-load applications.

2- Separation of line-side and load-side surge absorption, enabling faster ($40\ \mu s$) and more reliable interruption.

3- Minimization of active switches, reducing control circuit complexity, increasing the overall lifespan of the switch, and facilitating scalability for medium- and high-voltage systems.



B-SSCB: Bidirectional SSCB, U-SSCB: Unidirectional SSCB, ML DC-DC Converter: Multilevel DC-DC Converter

Fig. 3. A typical DC Microgrid with highlighted role of Bidirectional SSCB.

In modern DC MG, SSCBs play a crucial role in system protection.

As shown in Fig. 3, the system incorporates both Bidirectional SSCBs (B-SSCBs) and Unidirectional SSCBs (U-SSCBs) to ensure reliable fault isolation and protection. Given the presence of multiple power sources, including the AC grid and renewable energy resources operating at different voltage levels, DC-DC converters are employed to standardize and regulate voltage levels. Additionally, multilevel DC-DC converters enable seamless integration with loads requiring different voltages, enhancing system flexibility and efficiency. The combination of B-SSCBs and U-SSCBs ensures robust protection, making them essential components in modern DC systems.

The design showcases how the surge filter discharges surges through a discharge resistor, providing an efficient mitigation mechanism. While the circuit concept builds on the approach presented in [19], the proposed model offers a fully passive and bidirectional solution, marking a significant advancement.

Capacitors, by their nature, can be charged as current flows into them. This characteristic allows them to bypass surges by directing excess energy into the component. Additionally, research studies [3],[19] have confirmed the surge absorption capability of capacitors. These studies also discuss various capacitor models, such as polypropylene film and electrolytic capacitors, and their ability to handle surge absorption [3]. It has been established that surge absorption in capacitors is a charge-discharge process that operates based on the current-blocking technique.

2 Proposed Model Analysis

The proposed passive SSCB model, along with its control system, is illustrated in Fig. 4. Two back-to-back MOSFET switches, S_1 and S_2, serve as the main switches, enabling circuit power flow conduction. Both switches are equipped with internal reverse diodes. In this design, capacitors C_1 and C_2 are essential for surge mitigation, while resistors R_1 and R_2 are included as a safety measure in case a maintenance break occurs. Alongside a mechanical discharge mechanism, they ensure prevent residual charge from remaining in the system, reducing the risk of electric shock during maintenance of the SSCB. The connection between the common point of the diodes and the system's negative polarity serves as a pathway for surge discharge. Additionally, diode D_3 creates a loop to circulate the fault on the load side and discharge the surge from L_2.

The circuit's operational sequence and various modes of the proposed SSCB are illustrated in Fig. 5, offering a clear foundation for performance analysis.

In the first stage of the design (refer to Fig. 5a), the capacitor charging operation is considered.

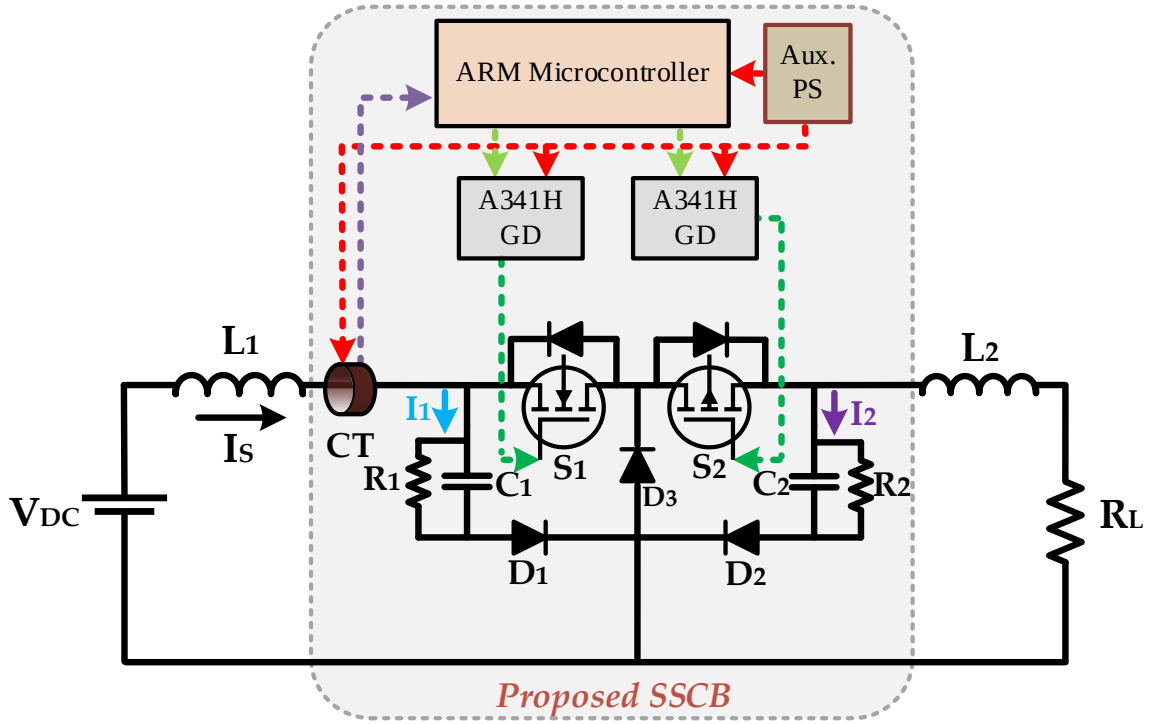
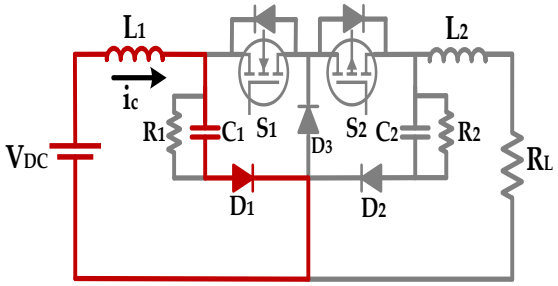


Fig. 4. Proposed Bidirectional SSCB with passive surge absorber.

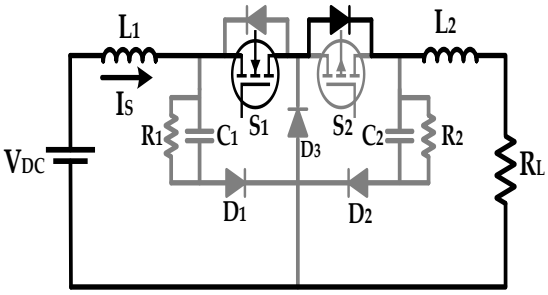
In this scenario, by analyzing the loop V_{DC}-L_1-C_1-D_1, the voltage across the capacitor reaches the input voltage level ($V_{c1} = V_{DC}$), and the capacitor charging current, $i_c(t)$, can be calculated by Eq. (1) as follows:

$$i_{c1}(t) = {V_{DC}}/{L_1 C_1 . \omega_d}\, e^{\frac{R_{L1} t}{2L_1}} \sin(\omega_d t)\ ,\ \omega_d = \sqrt{\frac{1}{L_1 C_1} - \frac{R_{L1}^2}{4L_1^2}} \quad (1)$$

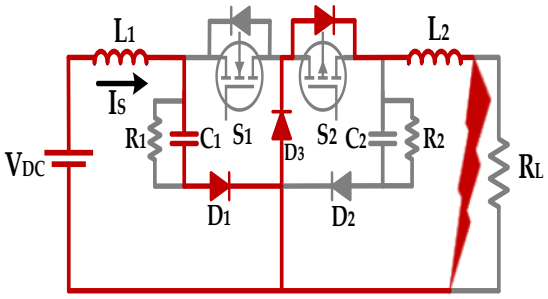
Equation (1) describes the sinusoidal and exponential nature of the capacitor current waveform in an RLC circuit, which depends on the values of the DC system's inductance, capacitance, and loop resistance (R_L). In this equation, ω_d is a constant which is a coefficient to present the oscillation of the waveforms.



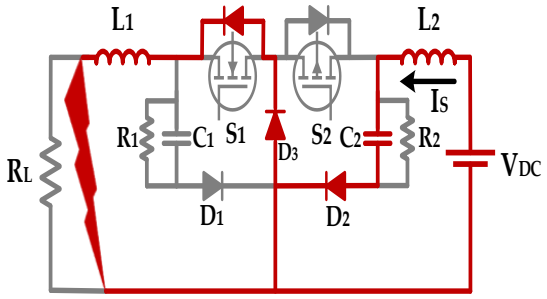
a) Capacitor charge cycle



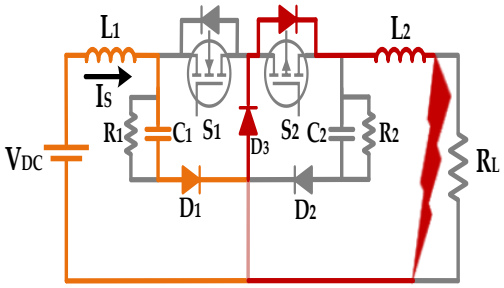
b) Normal operation



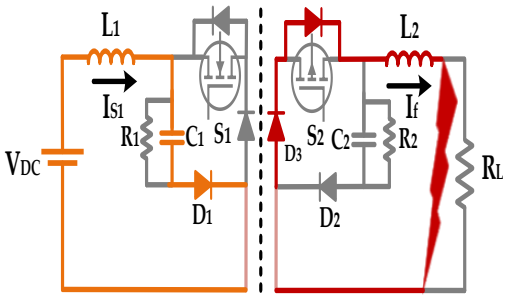
c) Forward Direction Power Flow Fault Operation



d) Reverse Direction Power Flow Fault Operation



e) Circuit in fault operation



f) Superposition principle

Fig. 5. Proposed SSCB operational sequence

It is important to note that the values of L_1 and L_2 correspond to the DC system's inductance, so the capacitor selection should be proportional to the system inductance. For reverse circuit operation, the values of C_2 and L_2 should be taken into account when calculating the capacitor charging operation.

In normal operation, as shown in Fig. 4b, the circuit follows a first-order differential equation.

However, during fault conditions (Fig. 5c, and Fig. 5d), the load is short-circuited, and is expressed in Eq. (2).

$$V_{DC} = (L_1 + L_2)\frac{di_s}{dt} \tag{2}$$

In this case, with initial value of $i_s(0) = i_s$, the fault current (i_{s-f}) can be calculated by Eq. (3) as follows.

$$i_{s-f} = \frac{V_{DC}t}{(L_1 + L_2)} + i_s \tag{3}$$

During fault operation, the circuit functions as two separate parts as expressed in Eqs. (4) – (6), depending on the circuit times constant and the superposition principle, as depicted in Fig. 5e and Fig. 5f.

$$V_{DC} = L_1\frac{di_{s1}}{dt} + V_{C1} + V_{R3} \tag{4}$$

$$V_{D3} = L_2\frac{di_f}{dt}\ , V_{D3} = R_{L2}(i_{s1} - i_f) \tag{5}$$

$$L_2\frac{di_f}{dt} + R_{L2}i_f = R_{L2}i_{s1} \tag{6}$$

Where, R_{L2} is the load side loop resistance. As a result, the load-side fault current (i_f) can be calculated by Eq. (7) as follows:

$$i_f = i_{s1} + (i_{L1(0)} - i_{s1})e^{-\frac{R_{L2}}{L_2}t_f} \tag{7}$$

Where The term $i_{L1(0)}$ refers to the initial value of the current in the line-side inductance (L_1) before fault occurrence.

Consequently, by assuming $V_{c1-0} = V_{DC}$ and $i_{L1}(0) = I_{L1}$, the capacitor voltage during the fault can be calculated by Eq. (8) as:

$$v_c = e^{-\alpha t}\left(\left(\frac{I_L}{C_1} + \frac{R_{L1}}{2L_1}V_{DC}\right)\frac{\sin(\omega_d t)}{\omega_d} - V_{DC}\cos(\omega_d t)\right) + V_{DC} \tag{8}$$

Hence, to calculate the optimized value of the capacitor (C_1) during the surge absorption (SA) interval (T_{SA}), Eq. (8) simplifies by considering $\frac{R_{L1}}{2L_1}V_{DC} >> \frac{I_L}{C_1}$, $e^{-\alpha T_{SA}} \approx 1$, and T_0 (the time from normal operation to the threshold level of the fault). Thus, it can be expressed as Eq. (9).

$$C_1 = \frac{T_{SA}}{V_{DC}}\left(\frac{T_0 V_{DC}}{L_1 + L_2} + I_{L1}\right) \tag{9}$$

In a similar process to C_1, C_2 can be estimated by considering circuit reverse operation.

The simulation results of the proposed model, using component values similar to those in the experimental setup, are shown in Fig. 6. When the fault current reaches the threshold level, it is detected via the measured current by the LEM 100P current transformer (CT). The STM32 microprocessor then sends an interruption command, causing the main switch (S_1) to disconnect the DC circuit. In this scenario, the voltage across the main switch rises to *57 V* instantaneously, and the surge generated by the circuit inductances is bypassed through the designated routes, including L_1-C_1-D_1 and L_2-D_3-(D_{S2}). The forward capacitor (C_1) voltage increases to *55 V*, and the surge current flows through this capacitor in *140 µsec*. In a similar situation, the surge current (*10 A*) passes through the circular backfeed diode D_3 in *140 µsec*.

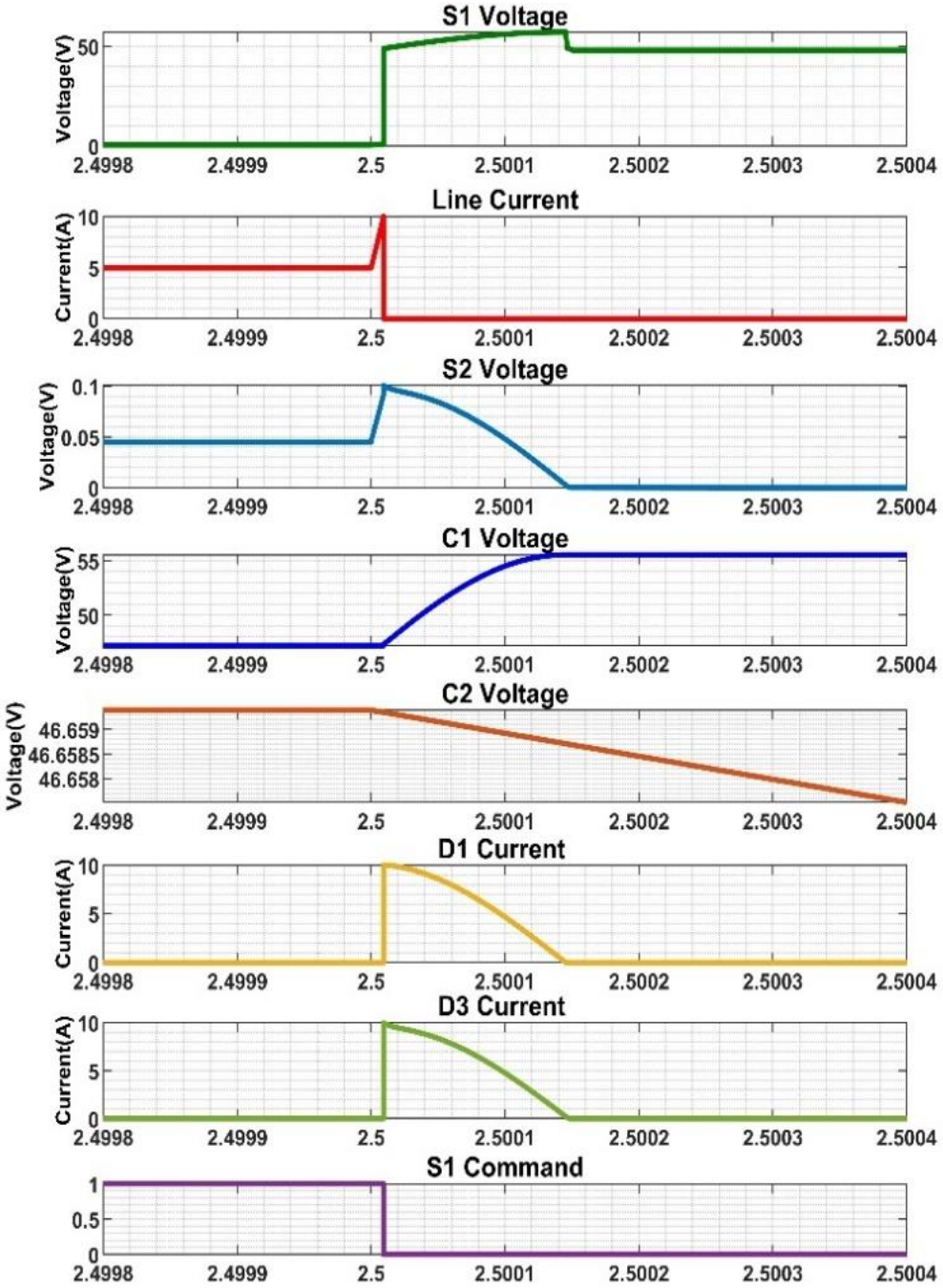


Fig. 6. Simulation results: conceptual waveforms of the proposed SSCB

3 Experimental Evaluation

The proposed design is validated through experimental testing of the SSCB in the laboratory, with the testbed shown in Fig. 7.

The input voltage is supplied by the Chroma 6200H-100P, while a programmable load, the Chroma 63204, is used as the load. The values of the circuit components are listed in Table 1.

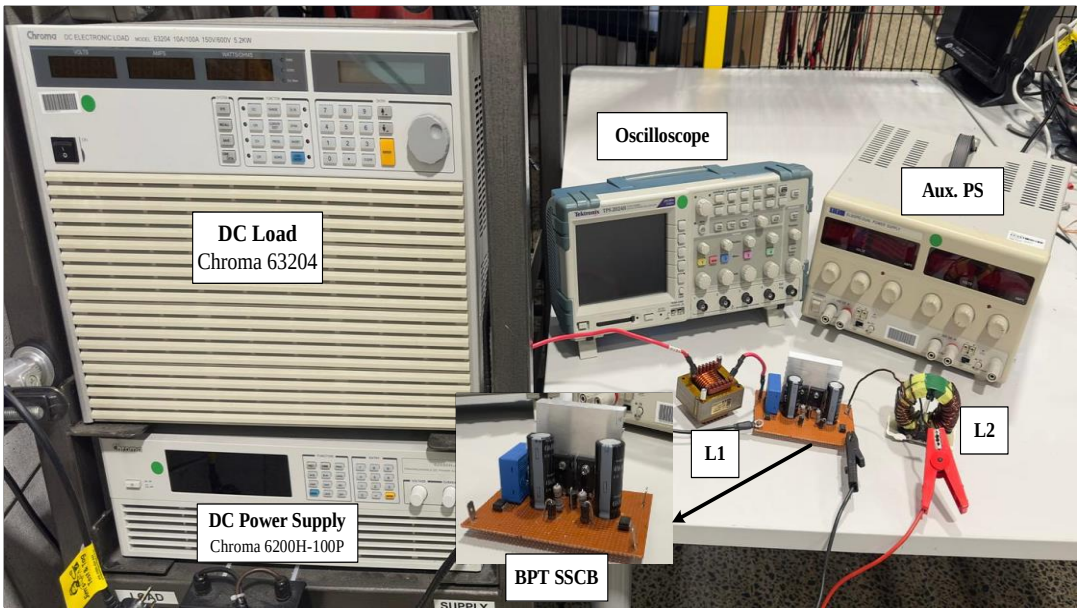


Fig. 7. Experimental Hardware Setup

The fault current takes *130 µsec* to rise from *5 A* to *10 A* and *90 µsec* to drop from the maximum value to zero (fault clearing time), as shown in Fig. 8. The discharge time depends on the circuit inductance. Once the STM microprocessor detects the current threshold, it promptly interrupts the main switch, which disconnects the circuit in *40 µsec* (t_r).

TABLE 1: CIRCUIT COMPONENTS VALUE

Component	Value	Component	Value
V_{DC}	48 V	D_1, D_2, D_3	HER303
C_1, C_2	120 µF	R_L	Chroma63204
R_1, R_2	250 KΩ	Gate Driver	A341H
Microprocessor	STM32F407VG	L_1, L_2	73µH- 12µH
S_1, S_2	IXFP110N15T2	CT	LEM 100P

Fig. 8 also demonstrates the detailed waveforms of the C_1 bypassed capacitor voltage and current. The maximum current passing through the capacitor is *8.8 A*, and its voltage experiences a slight increase (*3 V*) from *48 V* to *51 V*. The instantaneous overvoltage during surge absorption process occurs when it is switched from the main path to the surge absorber sub-circuit. However, it's peak reaches only *56 V*, representing *16%* of the input voltage (*48*

V), which does not impact the operation of the main switch. Notably, the interruption/rise time (t_r) of the main switch (S_1) is *40 µs*.

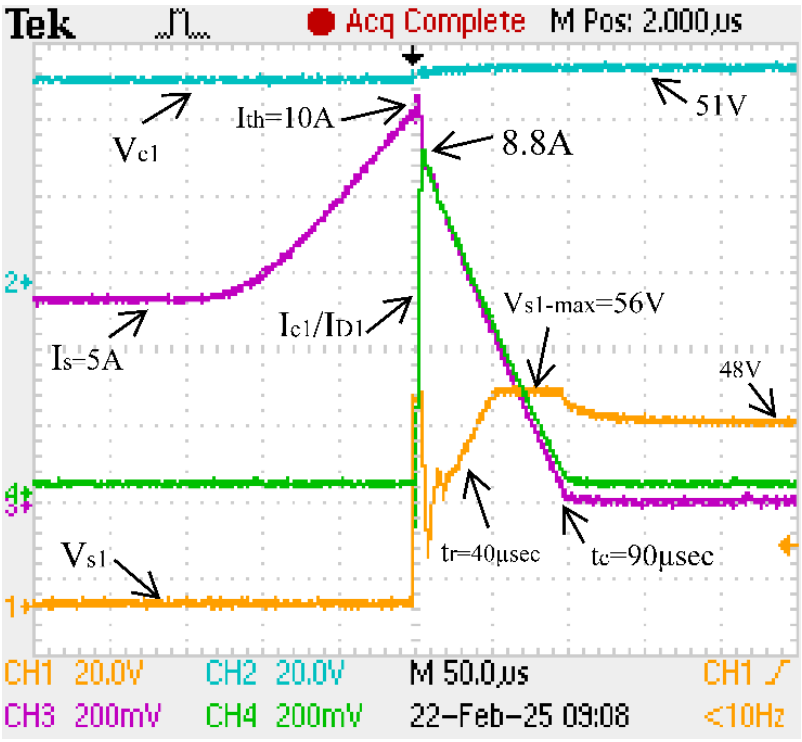


Fig. 8. Main Switch voltage (V_{S1}) and line current (I_s), bypassed capacitor 1 voltage (V_{c1}) and current (I_{c1}/I_{D1}) in forward direction.

Fig. 9 illustrates the behavior of the D_3 reverse diode (I_{d3}) and the S_2 reverse switch (V_{s2}, I_{s2}) during fault operation, along with the voltage across the main switch (V_{s1}). After circuit interruption, the system splits into two sections according to the superposition principle (Fig. 5f), causing the current through S_2 to behave differently compared to S_1. The voltage across the reverse switch is equal to its internal diode conduction voltage, and the current passing through the reverse diode (D_3) experiences a brief surge of *4.2 A*.

In the proposed model, the current flowing through the parallel resistors (R_1 and R_2) is negligible due to their high resistance values. Once the capacitors are fully charged, the resistor current is calculated as $I_{R1,R2}=48V/250\ K\Omega=0.000192A$, which is minimal and does not cause substantial power loss ($P_{loss\text{-}R1,R2}=0.0092\ Watt$) for the model.

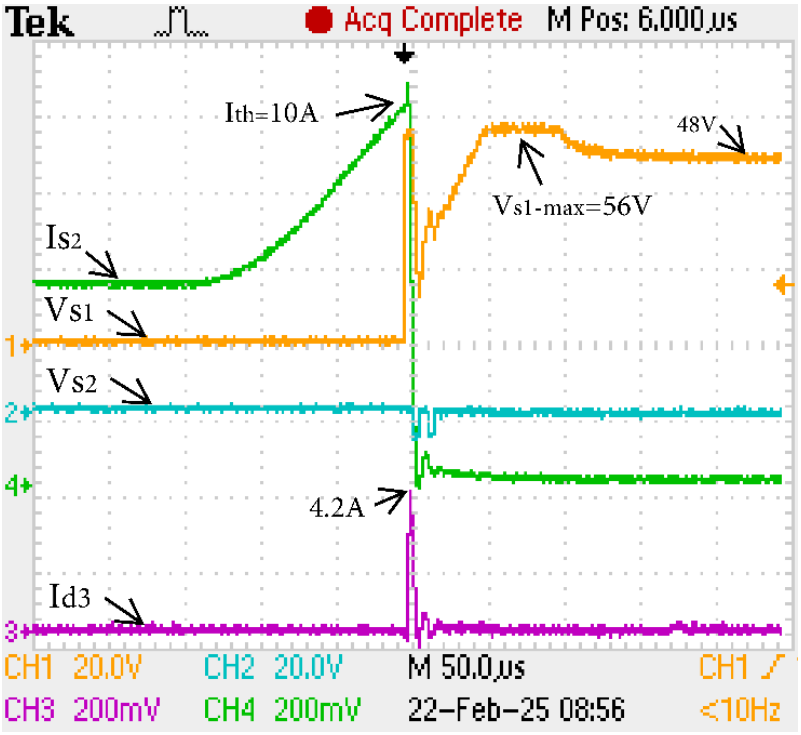


Fig. 9. V_{s1}, V_{s2}, I_{s2}, and I_{D3} (reverse diode current)

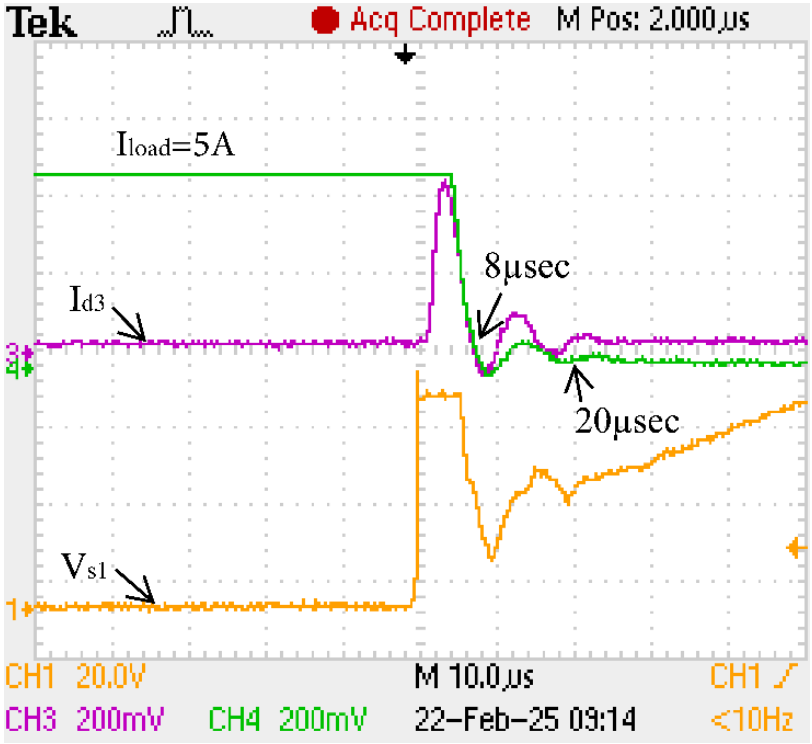


Fig. 10. Load interruption during the fault detection.

Fig. 10, shows that the current of the load crosses the zero in *8 µsec* and the current subsequently drops to zero in *20 µsec* (load interruption time) which approves the effectiveness of the proposed model.

The experimental and simulation results presented validate the effectiveness of the proposed BPT technique for SSCBs.

4 Comparative Study and Discussion

To evaluate the advantages of the proposed solution, the key features of four other LV SSCB designs are compared and discussed in Table II. It is evident that the BPT SSCB requires the least number of power devices to effectively interrupt faults with a fully passive surge absorber. Consequently, compared to existing breakers, the BPT SSCB offers advantages such as a minimized circuit complexity, lower costs, improved power efficiency, and greater reliability. The proposed SSCB filters surge currents through an RCD path, protecting both the DC load and the main power switch from surges generated by circuit inductances. Notably, the BPT-based SSCB, relying on a fully passive surge absorber, can interrupt the load within *20 µsec,* providing rapid protection for DC-MGs.

TABLE II

PERFORMANCE COMPARISON OF VARIOUS SSCBS TOPOLOGIES

Category	Proposed Model	[10]	[11]	[12]	[13]
No. Switches	2	4+2	2+1	2+2	2+4
S.A.	RCD	RC-MOV	RCD-MOV	RCD-MOV	RCD
V_{DC}/I_{th}	48V/10A	150V/2KA	500V/180A	50V/6.2A	380V/150A
C.C.C	Low	High	Medium	High	High
Interruption time	40 µsec	50 µsec	16 µsec	100 µsec	237 µsec
Passive SA	Yes	No	No	No	No
No. of P.C.	7	8	10	8	6
Cost	Low	High	Medium	High	High

S.A. Surge Absorber C.C.C.: Control Circuit Complexity P.C.: Passive Components

In DC applications, the absence of an inherent zero-crossing renders fault current interruption time a critical factor in ensuring effective circuit protection. For SSCB's, this interruption

time should ideally be in the microsecond range [1]. In the design of SSCBs, the interruption time is influenced by various factors, including voltage and current levels, the type of main solid-state switch (IGBT, MOSFET, or Thyristor), and circuit inductance. To validate that the results of the BPT technique meet this requirement, the interruption time in this research is compared with findings from other studies, as detailed in Table II.

5 Conclusion

This letter introduces a novel SSCB design for LVDC applications, capable of fully interrupting the load within *20 µsec*, with a switching time of *40 µsec* and a fault clearing time of *90 µsec*. Compared to traditional solutions, the proposed BPT-based SSCB offers a simple, bidirectional, fully passive structure, low cost, high efficiency, and enhanced reliability, making it a promising option for DC-MG protection. The fault-interruption principle and detailed design guidelines are thoroughly explained, and the feasibility of the proposed solution is validated through both experimental and simulation tests for the proposed model, which operates with a *48 VDC* system voltage and a *10 A* threshold fault current.

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VI. Chapter 6:

Conclusions and Future Research Directions

1 Introduction

This chapter consolidates the findings of this research and discusses the achieved results, emphasizing their contributions to the development of advanced DCCBs for DC microgrid (MG) applications. The study addressed the pressing challenges in surge absorption, scalability, and cost efficiency through the introduction of three innovative techniques: Bidirectional Thyristor-Capacitor (BiTriCap), Divided Surge Absorption Technique (DSAT), and Bidirectional Passive Technique (BPT). This chapter reflects on the broader implications of these findings and outlines prospective directions to further enhance the reliability and functionality of DCCB systems in future DC networks.

2 Discussion and Results Assessment

In this PhD thesis, three different techniques—BiTriCap, DSAT, and BPT—are proposed to enhance the design of SS-DCCBs by providing reliable and effective surge absorption while using components with lower degradation rates. The progression of the designs begins with the BiTriCap topology, which incorporates two active components in a bypassed snubber circuit. This design is improved in the DSAT technique by reducing the number of active components to one and employing a smaller capacitor, thereby lowering the overall cost and simplifying the control circuit.

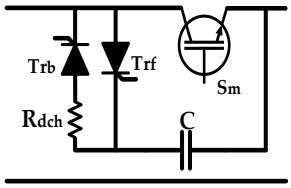
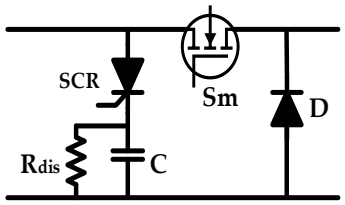
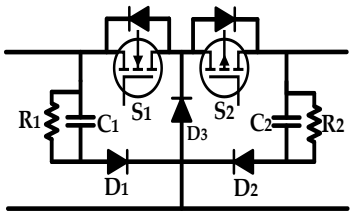
Building upon the DSAT's foundation, the BPT technique is developed to absorb surges using a fully passive subcircuit tailored for bidirectional applications. Notably, this model includes no active components in the bypass subcircuit, resulting in a significantly simplified control system.

All models were evaluated under the same voltage level (48 V) to ensure a fair comparison of interruption times. These results, summarized in a table, show that all three techniques achieve interruption within the μsec range, demonstrating their reliability for a wide range of DCCB applications.

In terms of cost assessment, the DSAT technique is more cost-effective than BiTriCap due to the removal of one capacitor and a reduction in component size. The BPT model, while evaluated under a different cost category (due to its use of bidirectional switches), is suitable for broader applications and represents a promising candidate for the commercialization of DC MG systems.

TABLE I

PERFORMANCE COMPARISON OF THE PROPOSED TECHNIQUES

Technique	BiTriCap	DSAT	BPT
Circuit Structure			
No. of S.A. Switches	2	1	0
S.A.	RC-SCR	RCD-SCR	RCD
V_{DC}/I_{th}	48V/15A	48V/20A	48V/10A
C.C.C	High	Medium	Low
Interruption time	116 µsec	10 µsec	40 µsec
Passive SA	No	No	Yes
No. of P.C.	2	3	7
Cost	High	Medium	Low

S.A. Surge Absorber C.C.C.: Control Circuit Complexity P.C.: Passive Components

It is worth noting that all three proposed topologies are scalable to higher voltage and current levels, provided that accurate circuit estimations are applied during the design process.

From another perspective, the BPT model offers greater robustness against potential high-frequency disturbances in the system, as it requires only a single switching command during normal DCCB operation.

All three techniques operate based on the charge-discharge principle of the capacitor during the surge absorption process.

In the event of a fault using the BiTriCap technique, even if the bypassed thyristor fails, the capacitors can still absorb surges multiple times. However, the overall effectiveness of the

technique will be reduced. As a potential solution for commercialization, an alarm can be implemented on the control side to notify the users to replace the faulty thyristor.

Regarding the DSAT technique, as mentioned in the chapter 5, the original design of DSAT is enhanced to develop the BPT technique. Therefore, removing the thyristor in this context can also contribute to design improvement. However, in the DSAT technique, the lifespan of the capacitor as a surge absorber is longer than in the BPT technique, as it is not directly connected to the power supply, resulting in reduced gradual degradation.

3 Summary of Research Contributions

3.1 Surge Absorption Innovations

The proposed techniques demonstrated significant improvements in handling switching surges, which are a critical challenge in DC MGs. Key contributions include:

- BiTriCap Technique: This method utilized antiparallel thyristors and capacitors to provide a dynamic charge-discharge mechanism, effectively reducing stress on circuit components during fault conditions. Unlike traditional surge absorption approaches reliant on MOVs, BiTriCap minimized degradation risks and extended operational durability.
- DSAT: By dividing the surge absorption into line-side and load-side paths, this technique effectively protected critical components while maintaining rapid response times. Its application in unidirectional systems showcased exceptional reliability under high-stress scenarios.
- BPT: The simplicity of this fully passive method, relying on RCD subcircuits, proved highly effective for bidirectional applications. Its cost efficiency and adaptability across varying voltage and current ranges made it a promising solution for complex systems.

3.2 Theoretical and Practical Validation

Through rigorous modeling using MATLAB/Simscape and extensive experimental testing, this research validated the efficacy of the proposed techniques under various conditions. Key findings include:

- The BiTriCap method achieved an improvement in surge voltage mitigation compared to conventional MOV-based designs with a certain clamping voltage.

- DSAT demonstrated a quick circuit interruption and minimized voltage stress across switches, highlighting its protective capabilities.

- BPT reduced the complexity and cost of bidirectional circuit designs by integrating passive components while maintaining high surge absorption efficiency.

3.3 A Framework for Next-Generation DCCBs

This research laid the groundwork for a comprehensive design framework, integrating advanced surge absorption techniques into scalable, cost-effective DCCB designs. The framework addresses critical gaps in existing DCCB technologies, ensuring their applicability to a wide range of DC MG scenarios, from low-voltage systems in residential applications to high-voltage industrial and transportation networks.

4 Implications for DC Microgrids

The proposed solutions directly address the critical requirements of modern DC MGs, including:

1. Reliability and Resilience: By mitigating the risks associated with switching surges and system faults, the techniques enhance the overall reliability of DC networks.

2. Cost Efficiency: The integration of passive components and the reduction of MOV reliance contribute to more economical designs.

3. Scalability: The adaptable nature of these methods ensures their compatibility with diverse applications, from small-scale renewable systems to expansive industrial grids.

These contributions not only strengthen the operational stability of DC MGs but also support the global transition toward sustainable energy systems.

5 Challenges and Limitations

While the research achieved significant advancements, several challenges remain:

- Scalability for High Voltage Applications: Although the techniques proved effective for low to medium voltage ranges, their application in high voltage systems requires further investigation.

- Thermal Management: The thermal performance of components, particularly under prolonged fault conditions, warrants additional study to ensure long-term reliability.

- Integration with Control Systems: While the proposed techniques focus on hardware innovations, their seamless integration with advanced control strategies, such as real-time monitoring and adaptive fault isolation, remains an area for future exploration.

6 Future Research Directions

6.1 DC Systems Noise Assessment

Switching noise and DC bus noise may present challenges to the performance and reliability of DCCBs. These forms of electrical noise can originate from rapid switching events, electromagnetic interference (EMI), and fluctuations within the DC bus, adversely affecting DCCB operation and overall system stability. Future research should prioritize a comprehensive investigation of these noise sources and their impacts, as well as strategies for mitigation.

Switching noise is inherent to solid-state components like IGBTs and MOSFETs used in DCCBs. It is often exacerbated in MV and HV systems due to higher switching frequencies and greater energy levels, leading to:

Mis-operation Risks: High-frequency noise can cause unintended tripping or failure to trip, undermining system reliability.

Thermal Effects: Persistent noise can increase power dissipation in the form of heat, reducing the lifespan of components.

Control Signal Interference: Noise can disrupt communication between the DCCB and control systems, delaying fault isolation or triggering false alarms.

6.2 AI and Machine Learning Integration

Integrating AI-driven systems for real-time fault prediction and adaptive control can significantly enhance the responsiveness and efficiency of DCCBs. Machine learning models could analyze historical fault data to optimize circuit breaker settings dynamically.

6.3 Enhanced Surge Absorption Techniques

Exploration of hybrid techniques that combine the benefits of BiTriCap, DSAT, and BPT could lead to a universal solution applicable across a broader range of DC MG configurations. Additionally, investigating new passive and active components for energy absorption could further improve efficiency.

6.4 Interdependency in Multi-DCCB and Multi DC-DC Converter Systems

In interconnected DC MGs, understanding the interdependency of multiple DCCBs and their collective impact on system stability is essential. This necessitates the development of coordinated protection strategies and effective communication protocols. Additionally, evaluating the influence of DCCB operation in the presence of DC-DC converters—common in real-world systems—can enhance overall system reliability. This objective can be achieved by studying various DC-DC converter topologies, analyzing their input and output inductance, and investigating their impact on the proposed DCCB technique. Moreover, the interaction between high-frequency switching in DC converters and its effect on DCCB operation (specifically control signal of the DCCB), along with a more detailed investigation into the surge absorbers used in these converters, presents a promising direction for future research. It is reasonable to expect some similarities among all solid-state-based circuits in terms of surge absorber topologies; however, their purposes—protection versus switching—are fundamentally different.

6.5 Environmental Sustainability

As the demand for sustainable technologies grows, future research should focus on eco-friendly materials and designs. This includes developing recyclable components and minimizing the environmental footprint of DCCBs.

7 Final Reflections

This thesis makes a substantial contribution to the advancement of DCCB technologies, addressing critical gaps in surge absorption, reliability, and scalability. The proposed techniques not only improve the performance of DCCBs but also pave the way for innovative applications in modern power systems.

By bridging the gap between theoretical advancements and practical implementations, this research sets the stage for the development of more robust, efficient, and cost-effective solutions. As DC systems continue to gain prominence in the global energy landscape, the findings of this study will play a pivotal role in shaping the future of power system protection.