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Design and performance evaluation of low-voltage solid-state DCCB using capacitor-based surge mitigation techniques

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ABSTRACT

This article conducts practical tests on four different configurations of solid-state DC circuit breakers (SS-DCCBs), investigating fault detection and circuit interruption phenomena in DC systems. It analyses circuit formulations and design principles, compares the topologies, and evaluates results. Since all circuit operation results are considered acceptable, the article scrutinizes circuit configurations and selects the most effective surge absorption technique based on active and passive components and surge mitigation complexity. The primary switch in the proposed models is a MOSFET, while the bypass switches are IGBT and Thyristor. The traditional surge absorption method using Metal Oxide Varistor (MOV) is contrasted with three topologies employing the capacitor current block technique (CBT). Practical testing and discussion of the effects of circuit inductance on switching speed and operation are also included. Real-world modeling incorporating inductance on both the line and load sides is utilized throughout all experiments to assess realistic outcomes. The optimal surge absorption configuration will be chosen based on its ability to meet various criteria, including efficient operation, rapid response, minimal complexity on both power and control sides, and the involvement of active and passive components. The tests were carried out on a system with a *48* V DC supply.

1. Introduction

In recent years, there has been a significant transformation in the structure of Microgrids, particularly with the evolution of DC Microgrid concepts and the exploration and expansion of flexible AC-DC systems (Gomis-Bellmunt et al., 2020; Moradian et al., 2019). In the emerging generation of Future Architecture of Networks, the importance of DCCBs has been increasingly emphasized (Liu et al., 2018). DCCBs are essential for protecting DC systems across a range of current and voltage levels, including LV, MV, and HVDC systems (Watson et al., 2021). The effectiveness of DCCBs for protection is crucial for the successful implementation and operation of future flexible hybrid AC-DC systems.

Fig. 1 illustrates the essential significance of DCCBs within the emerging DC Microgrid framework. These microgrids, shaping future infrastructure development, depend greatly on commercially available SS-DCCBs to guarantee resilient circuit protection, as emphasized in M. Moradian et al. (2023). A range of circuit breakers will be utilized, including the specialized Hybrid DCCB (H-DCCB) designed for high voltage situations, and the SS-DCCB primarily catering to medium and low voltage needs (Zheng et al., 2021). This varied selection of circuit breakers highlights the dynamic nature of DC Microgrid design and functionality.

From the control perspective of DC systems, since all SS-DCCBs are controlled using microprocessors, an additional option is to connect all DCCBs to a central system controller. This allows for the implementation of DC Microgrid control strategies, such as load shedding, and other techniques affecting generation, transmission, and consumption aspects.

Recent studies have predominantly focused on the use of MOVs and capacitors as key components for surge absorption in DCCBs, owing to their effectiveness in mitigating switching and fault-induced surges. The primary distinctions between these approaches lie in the circuit topologies and the methods employed for integrating the surge absorbers (M. Moradian et al., 2023; Moradian et al., 2024).

The main contributions of this paper are:

1. Discussing a capacitor-based surge absorption technique in SS-DCCB and proposing an optimal model.
2. Examining the impact of system inductance on switching interruption time.

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3. Investigating the optimal conditions for capacitor-based surge absorption in DCCB applications.
4. Providing a comprehensive analysis of both power and control elements in DCCB design, demonstrated on real-world systems.

Various existing DCCB designs, including the T-DCCB (Zhang et al., 2021), soft SS-DCCB (Rahimpour et al., 2022), and AT-CB (Shu et al., 2021) models, integrate components such as capacitors, MOVs, and other active elements. Although these designs are effective, they increase system complexity, cost, weight, and may introduce additional surge sources. Similarly, the TIM-Pack model, which uses MOV-C snubbers and parallel energy absorption components, faces comparable issues (Yan et al., 2023). Moreover, previous designs relying on capacitors for surge absorption have not sufficiently addressed cost concerns or accounted for the effects of load or line inductance on DCCB performance in real-world applications (Sen & Mehraeen, 2019).

Since the placement of the DCCB in DC microgrids is not predefined, the maximum released energy is utilized to evaluate line and load inductances (Moradian et al., 2024). While system inductances can be estimated based on overhead or underground line configurations, they act as surge sources during switching and fault interruption (Moradian et al., 2025). Effective surge damping is essential in the absorber circuit to ensure system stability. Although system inductance can be calculated, future research should focus on developing adaptive techniques for intelligent line inductance estimation. This advancement would enhance the reliability and efficiency of DC microgrid protection systems.

This article explores the testing of a conventional DCCB with an MOV to examine the effect of system inductance. However, due to the limitations of MOV in DC surge absorption, a capacitor based DCCB is proposed, and four different scenarios are evaluated:

Topology A: A typical MOV-based DCCB is tested, and the variation in system inductance is investigated.
Topology B: A thyristor-capacitor surge absorber is proposed. This method introduces a parallel sub-circuit that diverts the surge into a branch containing a thyristor in series with a capacitor.
Topology C: Similar to topology B, but the bypass switch is replaced with an IGBT. The results remain consistent with the previous model, but the control circuit becomes more complex. Unlike a thyristor, which turns off naturally, an IGBT requires an explicit turn-off command.
Topology D: This setup mirrors topology B, but the capacitor is precharged to analyse the surge absorber's behaviour with an initial charge.

To further validate the circuit's performance, a range of line and load inductances is considered, assessing their impact on switching speed. The findings emphasize the importance of optimal surge absorption design, requiring accurate estimation of line and load inductances for improved performance.

2. Analysis of DCCB MOV-Based topology

MOV-based DCCB is a conventional type of DCCB that has been extensively discussed in numerous research studies and forms the fundamental topology of DCCBs for absorbing DC circuit switching surges through the MOV mitigation path (M. Moradian et al., 2023; Ravi et al., 2022). MOVs are also recognized as cost-effective surge absorbers (M. Moradian et al., 2023). The Topology A model illustrated in Fig. 2 is straightforward, requiring only one active component and a gate driver to operate the system. This paper discusses the MOV-based circuit breaker for two main reasons: first, to illustrate circuit performance with a conventional DCCB, and second, to explore the impact of circuit inductance variation on DCCB operation. A microprocessor-based controller monitors the circuit's condition and, based on the switch voltage and main path current, releases control signals to implement circuit protection measures. Upon deactivation of the main switch (IRFP4227 MOSFET), the energy stored in the circuit needs to be dissipated during the transient switching phase, potentially endangering the switch. To protect both the main switch and the DC circuit from switching shocks, the MOV is triggered when the switch voltage reaches to the MOV's clamping voltage. This action allows the MOV to dissipate the surge, thereby protecting the circuit (Khanmiri et al., 2016).

In conjunction with the main switch's successful operation, the MOV possesses several weaknesses, including rapid degradation, high clamping voltage, potential failure due to leakage current and heat dissipation, and high capacitance, which adversely affects circuit performance. Furthermore, the MOV is unable to limit current shocks and functions solely based on voltage (Nogueira et al., 2023), (Kheirollahi et al., 2022).

The voltage across the switch (V_{SW}) in the Laplace domain can be defined using circuit parameters such as line current (I_s) and the inductances of both the line and load (L_{line}, L_{load}) during the transient switching period. When the main switch is ON, the system behaves as an

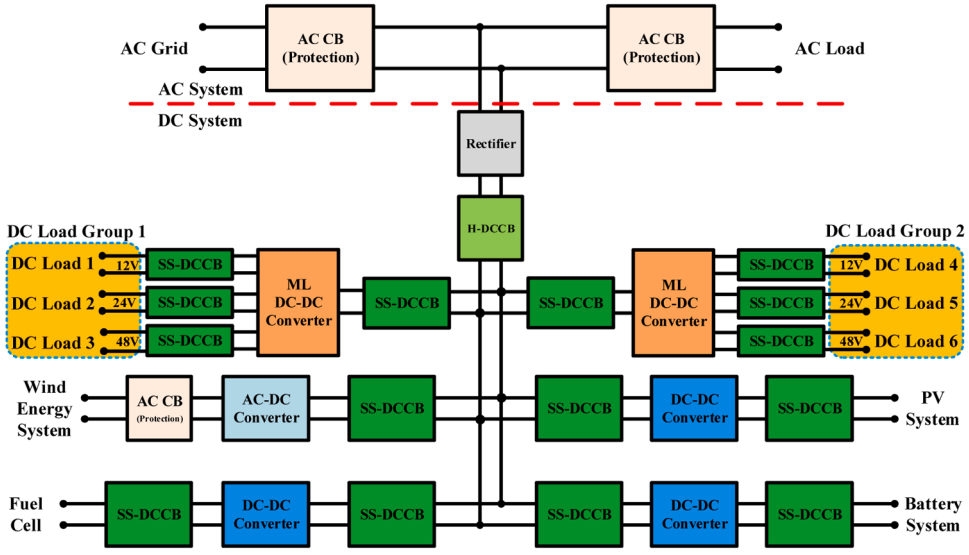
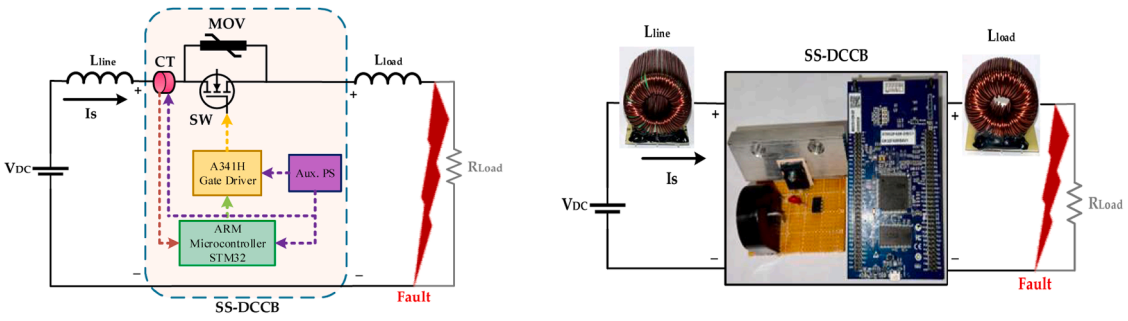


Fig. 1. Future Flexible Hybrid DC/AC Microgrid Protection Scheme.



a) Schematic of MOV-Based SS-DCCB b) Experimental setup of MOV-Based SS_DCCB

Fig. 2. MOV-based SS-DCCB circuit topology during a fault condition.

RL circuit, as shown in Eq. (1).

$$V_{Sw} = \frac{V_{DC}}{[(L_{Line} + L_{Load})s^2 + R_{Load}s]I_s} \quad (1)$$

Additionally, the voltage across the MOV, upon disconnection of the circuit, can be determined using Eq. (2).

$$i_f(v) = \beta v_{MOV}^{\gamma} \quad (2)$$

Where v_{MOV} and i_f denote the MOV voltage and line fault current respectively, "β" represents a constant coefficient determined by the spatial configuration of the MOV, and "γ" denotes the nonlinearity value ranging between *15* and *30* (Kularatna et al., 2018).

The selected MOV (EMX12080) has a clamping voltage of *80* V, which is *1.67* times the nominal DC system voltage of *48* V. The test was conducted at *48* V with a nominal circuit current of *8A* and a fault detection threshold of *13A*.

During a fault, as the current rises to *13A*, the switch is triggered to turn off, resulting in a voltage surge across the switch. Once the voltage reaches the MOV's clamping level, the MOV activates and suppresses the surge, as illustrated in Fig. 3. This surge absorption process occurs within microseconds.

When selecting the appropriate MOV for DC surge absorption, key factors include nominal current, peak voltage, clamping voltage, temperature tolerance, and the ability to withstand energy surges within a *2* ms timeframe (Kheirollahi et al., 2022).

2.1. SS-DCCB transition time analysis

Given the critical necessity for rapid switching within DC systems, the following tests are dedicated to exploring the impact of circuit inductance on switching speed. Fig. 4 presents the results of tests evaluating the switching characteristics of an identical circuit under consistent load conditions, yet varying circuit inductance.

In the initial test, the circuit's inductance is calculated as the sum of the line inductance and the load inductance, L_{eq}=L_{Line}+L_{Load}=*1.7mH*. Notably, the rise time of the voltage signal, spanning between *10 %* and *90 %* of the nominal voltage, measures at t_r=*180μsec*. Additionally, the total clamping time for fault detection under these conditions stands at

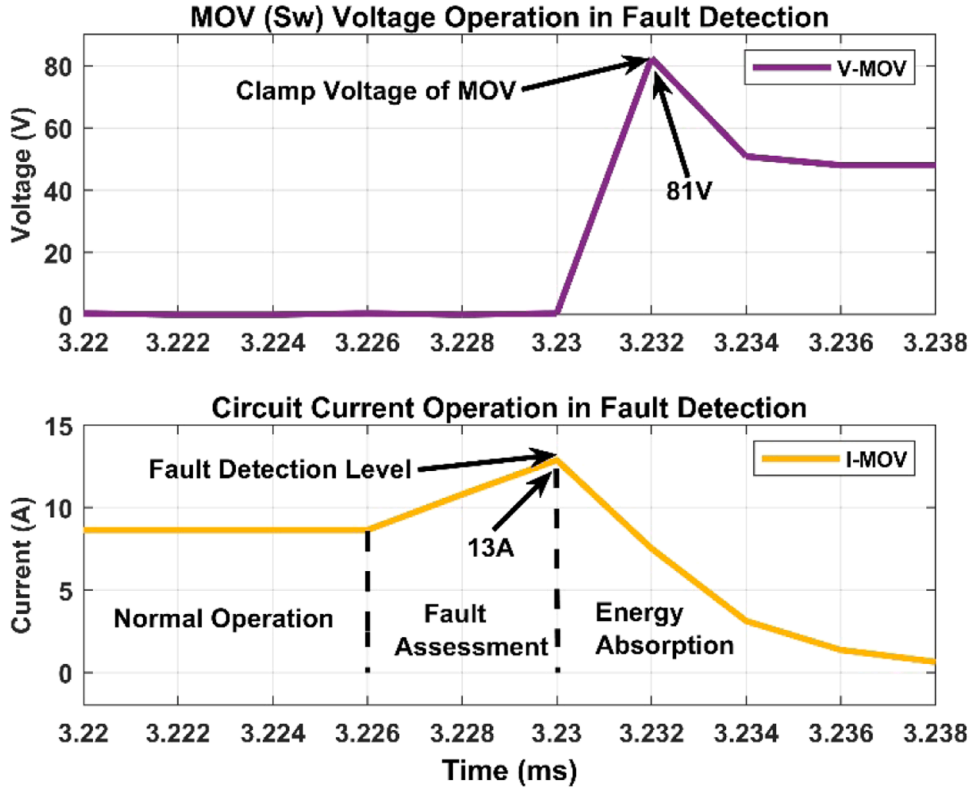


Fig. 3. Experimental Results: MOV (SW) voltage and line current.

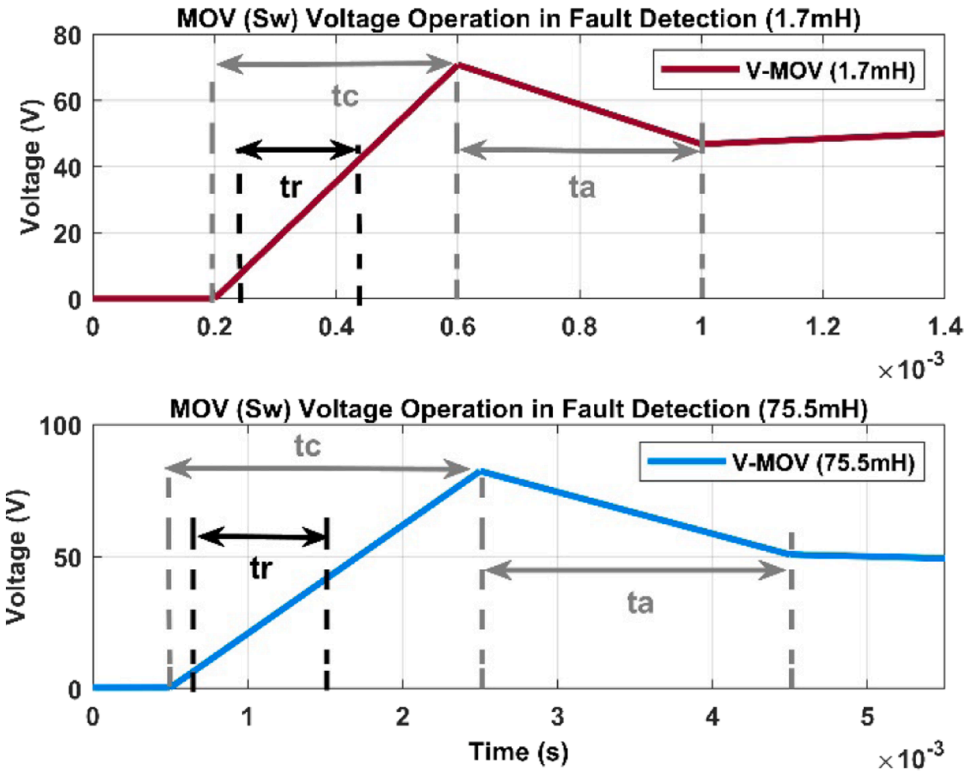


Fig. 4. Experimental Results: Assessing the impact of circuit inductance on switching speed.

t_c=*400μsec*, along with a surge absorption time of t_a=*400μsec*.

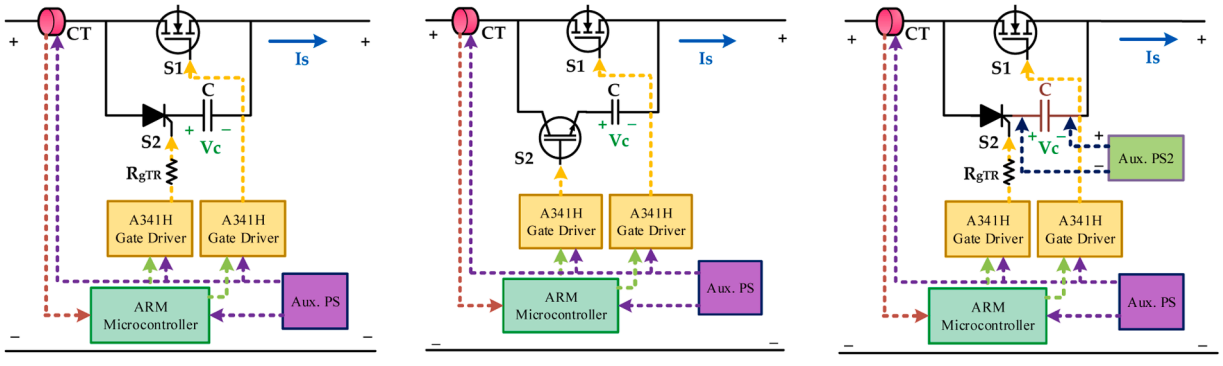
In contrast, when the circuit's inductance (L_{eq}) is increased to *75mH*, the rise time of the MOV voltage elongates to t_r=*1.1msec*. Similarly, the clamping time extends to t_c=*2msec*, accompanied by a surge absorption time of t_a=*2msec*. The primary reason for variations in system rise time, clamping time, and surge absorption time in this test is that the MOV functions as a variable resistor. As a result, the time constant of the RL circuit changes, impacting overall circuit performance in switching operation.

As a result of these tests, it could be analysed that circuit inductance impacts on switching speed, especially affects fast surge protection in fault detection of DC systems. It also demonstrates how variations in circuit inductance led to discernible changes in key parameters such as rise time, clamping time, and surge absorption time. Additionally, the comparison between the two scenarios, one with lower inductance and the other with higher inductance, highlights the consequential differences in switching behaviour, with higher inductance resulting in slower response times. Furthermore, these findings emphasize the significance circuit inductance in switching transition time and directly affects efficient fault detection and surge protection mechanisms.

3. Evaluation and validation of proposed DCCB models

Three topologies, shown in Fig. 5, are analysed to evaluate the snubber subcircuit's effectiveness in absorbing switching and fault detection surges. The topologies in Fig. 5a and Fig. 5b exhibit similar performance; however, the control mechanism in Fig. 5a is simpler than in Fig. 5b In Fig. 5a, the thyristor turns off automatically without requiring an OFF command, whereas in the bypassed subcircuit of Fig. 5b, both ON and OFF commands are needed for the IGBT. However, switching speed of IGBT is faster than Thyristor.

This paper evaluates the performance and operational principles of three proposed circuit configurations, focusing on their surge handling capabilities, control complexities, and overall effectiveness in mitigating



(a) Topology B (b) Topology C (c) Topology D

Fig. 5. Schematics of the discussed SS-DCCB's.

overvoltage during switching operations in solid-state DCCBs.

3.1. Topology B: thyristor-capacitor (TriCap) based topology

In Topology B (Fig. 5a), the configuration comprises a capacitor connected in series with a thyristor, paralleled with the primary switch. This arrangement is designed to mitigate surges associated with circuit switching effectively. The thyristor's activation during the switching period allows the surge to be redirected into the capacitor. Upon complete charging of the capacitor, the current diminishes to zero, causing the thyristor to switch off automatically. The primary switch successfully disconnects with minimal shock and negligible overvoltage, as evidenced by the recorded voltage surge of only *0.8* V across the switch during operation. This method, referred to as the BiTriCap Technique, is discussed in reference (Moradian et al., 2024).

In this configuration as illustrated in Fig. 5a, the current flowing through the main pathway is sampled seven times per microsecond, as per the microprocessor's settings. Upon detection of a fault by the controller, a turn-off command is simultaneously issued to the MOSFET while a turn-on command is sent to the thyristor, redirecting the released switching energy into the snubber capacitor. For control purposes in the proposed model, an auxiliary power supply is necessary to supply power to the microprocessor and gated drivers. To trigger the active components, two identical 8-pin A341H gate drivers are employed. However, since the thyristor operates based on current triggers, a *20* Ω resistor (R_{gTR}) is placed at the input of the thyristor's gate to limit the current injected from the gate driver and protect the STM32 microprocessor.

The circuit formulation in this technique during normal operation remains consistent with the previous model. However, during switching operations, there is an RLC circuit, and the maximum fault current ($i_{f\text{-max}}$) can be determined using the Eq. (3) and Eq. (4).

$$i_{f-max} \approx (V_{SW} / ((L_{line} + L_{load}).\omega_d).e^{-\gamma t}\sin(\omega_d.\ t) \tag{3}$$

$$\omega_d = \sqrt{\omega_0^2 - \gamma^2},\ \ \omega_0 = \frac{1}{\sqrt{(L_{line} + L_{load}).C}},\ \ \gamma = R_{eq}.C,\ \ R_{eq} \approx R_{on-SW} + R_f \tag{4}$$

where, V_{sw} is switch voltage, $R_{on\text{-}sw}$ is the switch ON resistance, and R_f is the fault path resistance.

In an alternative approach to calculating circuit components, determining the capacitance (C) necessary for designing the circuit breaker involves ensuring that the energy released from inductance is lower than the capacity of the capacitor.

$$E_C > E_L \tag{5}$$

$$\frac{1}{2}CV_{DC}^2 > \frac{1}{2}L_{eq}I_{th}^2 \tag{6}$$

In this equation, L_{eq} is loop inductance, L_{eq}=(L_{Line}+L_{Load}), and V_{DC} and I_{th} are the circuit voltage and short circuit threshold current.

For this examination, with the system's inductance at *2.03mH*, the snubber capacitor's voltage reaches to *55* V, and the predefined detection fault threshold level (I_{th}) fixed at *10A*, the capacitor's determination will rely on Eq. 9.

$$C > (1.7\ \times 10^{-3})\left(\frac{10}{55}\right)^2 = 56\mu F \tag{7}$$

Using the manufacturer's information for the selected switch (S_1) and the Thyristor (S_2), the conduction power dissipations are *1.34* W and *2* W respectively. In this case, the SS-DCCB switching power loss is $P_{L,SS\text{-}DCCB} = 3.34$ W, and the efficiency is given as follows:

$$\eta_{SS-DCCB} = \left(1 - \frac{P_{L,SS-DCCB}}{V_{DC}I_{DC-max}}\right) \times\ 100\% = \left(1 - \frac{3.34}{48\ \times\ 10}\right) \times\ 100\% = 99.30\% \tag{8}$$

3.2. Topology C: Capacitor- IGBT (Cap-IGBT) based circuit

Topology C (Fig. 5b) introduces an IGBT in place of the thyristor while retaining the capacitor in the subcircuit configuration. Although the fundamental approach to surge absorption remains similar to Topology B, the complexity of the control mechanism increases slightly. Unlike the thyristor, which requires only a turn-on command, the IGBT necessitates both turn-on and turn-off commands for effective operation. During the switching process, the bypassed IGBT turns on concurrently with the main switch turning off, absorbing the surge energy into the snubber capacitor. However, the timing of the IGBT's disconnection is critical; if it turns off prematurely before the capacitor is fully charged, it can induce significant stress on the bypassed switch, risking its integrity.

The primary challenge in this configuration lies in the need to manage the turn-off command accurately, given the varying inductance across different DC systems. The complexity of command management in this test makes it inherently more sophisticated than Topology B, as it demands precise timing to prevent undesirable voltage surges. The test on Topology C is conducted to demonstrate the feasibility of using an IGBT in the bypass path for surge absorption. However, it increases the complexity of the control circuit, as the IGBT requires an external turn-off command, unlike a thyristor, which switches off automatically.

3.3. Topology D: thyristor-capacitor (TriCap) with negative charge configuration

In Topology D (Fig. 5c), a capacitor with an initial negative charge *(−20* V) series with a thyristor is employed to absorb surges. This configuration diverges from the previous topologies, utilizing the capacitor not only as a surge absorber but also as a current blocker. The negative energy released by the charged capacitor aids in mitigating the surge during the switching operation.

However, the initial charge of the capacitor requires careful consideration, as it impacts the surge handling capability and overall circuit performance.

Fig. 6 indicates the conceptual waveform of the proposed CBT during fault interruption for Topologies B, C, and D, showcasing the operation of S_1 and S_2, as well as the behaviour of the circuit current and capacitor voltage. Before $t = t_0$ the SS-DCCB is in the steady state operation (ON state). Once the fault occurs, the line current rises to its maximum level by t=$t_{f\text{-max}}$. At this point, S_2 switches ON, followed by the delayed switching off of S_1. In this state, the bypass capacitor absorbs the redirected interruption surge by charging up, effectively blocking the current flow. The capacitor voltage variations demonstrate the efficiency of surge absorption.

The operational logic of the circuit is illustrated in the flowchart provided in Fig. 7. The microprocessor continuously measures the circuit's current through the CT and compares it with the predetermined fault current level, set at *10A* in this model. If the circuit's current exceeds the threshold, the STM32F407VG ARM microprocessor sends two commands to activate S_2 and deactivate S_1, thereby absorbing the surge generated by switching of the detected short circuits.

The selection of the main switch (S_1) and the bypassed thyristor (S_2) among IGBT (Zhang et al., 2023), IGCT (Zhuang et al., 2022), Thyristor (Nandakumar et al., 2022), and MOSFET (Wu et al., 2024) must ensure adequate coverage of system voltage, current, and fault bandwidth. Another key criterion is the switch's ability to break the threshold current (Zhuang et al., 2022). Based on the datasheets of the components used in this study, the IRFP4227 MOSFET operates at *50* MHz (with a rise time of *20* ns), while both the CT and S_2 function within a *100* kHz frequency range.

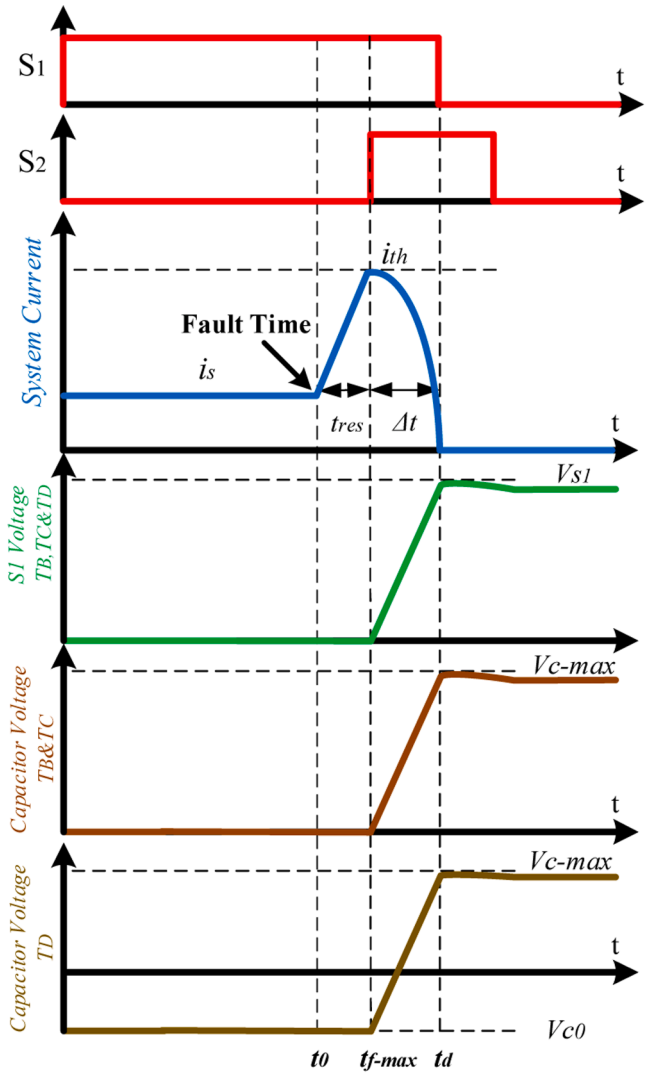


Fig. 6. Conceptual waveform of the capacitor-based topologies.

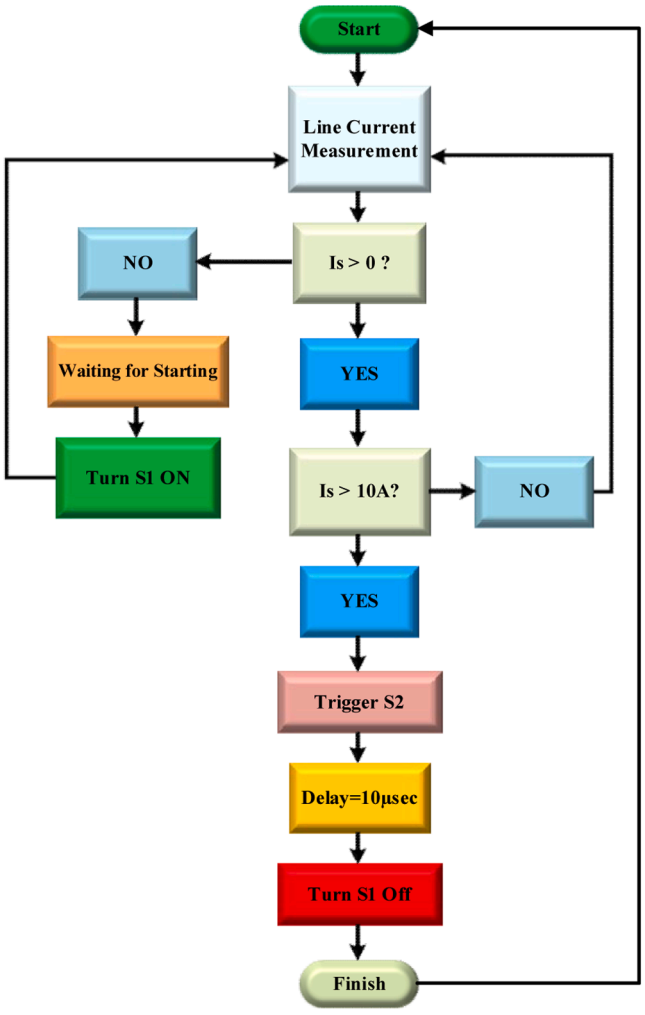


Fig. 7. Control system of the proposed models.

4. Experimental evaluation of the capacitor based topologies

The proposed model for Topologies B and D is shown in Fig. 5, with practical implementations depicted in Fig. 8. Fig. 8a illustrates the system setup for Topologies B and D, while Fig. 8b shows the setup for Topology C. In Topology D, an external auxiliary power supply is needed to charge the snubber capacitor with reverse polarity. However, this addition increases the circuit complexity while providing only minor advantages. Another drawback associated with this approach is the adverse effect on the DC capacitor polypropylene films due to the initial charge with inverse polarity, consequently diminishing the component's lifespan. On the other hand, supplying an extra auxiliary power source (Aux. PS 2) to initially charge the capacitor poses another issue.

The values of the circuit components are listed in Table 1. Chroma machines are utilized for both power supply and load.

In the next section, tests are performed with different line and load inductances, while the capacitor voltage is adjusted to analyse the effects of parameter variations on the test results.

4.1. Test scenarios

Since the results of the IGBT-based technique are similar to those of the TriCap model, the tests in this section primarily focus on the proposed techniques for Topologies B and D. Key variables, including inductance, capacitance, and the capacitor's initial voltage, are adjusted to evaluate the surge absorption performance of the proposed model. Additionally, it is concluded that modifying the circuit's time constant directly impacts the system's rise time and surge mitigation, emphasizing the significance of optimal design. The tests are categorized as shown in Table 2.

According to the results shown in Fig. 9a, the voltage across the switch during the switching phase is measured at *66* V, with a total of *14* V overvoltage. this test is conducted for Topology B with circuit inductance of *75mH*. The controller's fault detection threshold is set at *10A*. During the switching process, the voltage across the capacitor rises to *67* V, allowing the circuit's surge to be absorbed by the snubber capacitor. Once fully charged, the capacitor's current decreases to zero and block the current, with a peak current of *14A* observed during the switching event.

In Fig. 9b, the capacitor starts with an initial charge of *−20* V (for Topology D). During the fault detection period, the surge is redirected into the capacitor, causing the initial reverse energy to discharge quickly, influencing the absorption process. Compared to Test 1, this results in a *12* V reduction ($V_{s1\text{-max}}$=*54* V) in the peak voltage of the main switch and an *11* V decrease ($V_{c\text{-max}}$=*56* V) in the overvoltage across the capacitor. However, in contrast to Test 1, the oscillation of the interrupted current is significantly increased. Additionally, the capacitor faces a maximum surge current of *27.5A*. In this test, overvoltage is mitigated, but the circuit currents experience oscillation and a surge.

By changing the system inductance to *2.06mH* and setting V_c=*0* V, as

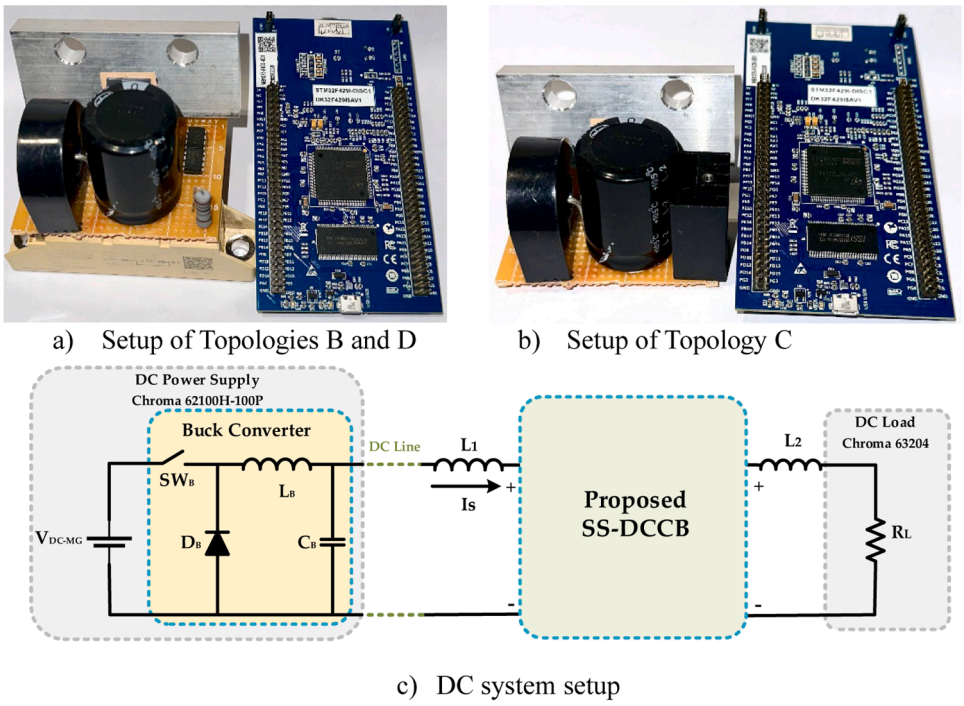


Fig. 8. Practical setup of the proposed models.

Table 1
The tests parameters.

Parameter	Acronym	Value	Unit
Input DC Voltage	$V_{DC\text{-}MG}$	48	V
Snubber Capacitor	C	470	μF
Microprocessor	ARM Microcontroller	STM32F407VG	-
Main Switch	S_1 (MOSFET)	IRFP4227	-
Bypass Thyristor	S2 (Topologies B&D)	SKKT27B12E	-
Bypass IGBT	S_2(Topology C)	FGH40N60UFD	-
Gate Driver	-	A341H	-
Load Resistance	R_{load}	9.6	Ω
MOV	MOV	EMC12080	-
Gate Resistance	RgTr	20	Ω
Current Transformer	CT	LEM 100P	-

Table 2
A summarize of the tests.

	L1	L2	C	Vc
Test 1	47.5 mH	27.5 mH	470 μF	0
Test 2	47.5 mH	27.5mH	470 μF	−20V
Test 3	1.03 mH	1.03 mH	470 μF	0
Test 4	75 μH	12 μH	470 μF	+28V
Test 5	75 μH	12 μH	10 μF	0

shown in Fig. 9c, the system response becomes relatively quicker, with the voltage across S_1 and the capacitor measuring *55* V and *56* V, respectively. However, some oscillation still exists in the circuit current.

In Test 4 (Fig. 9d), the system is tested with $a + 28$ V applied to the capacitor. As shown, there is no overvoltage across the main switch ($V_{s1\text{-max}} = 48$ V), with limited oscillations in the circuit currents and a quick interruption. In Test 5, as illustrated in Fig. 9e, the system inductance is set to $87\mu H$, and the capacitor is replaced with a $10\mu F$ capacitor, while $V_c = 0$ V. As seen, the switching speed is in the microsecond range, and a *58* V instantaneous surge is observed across the main switch. Additionally, no current oscillation is observed in this test.

In summary, it can be concluded that the circuit inductance directly influences the rise time (tr), switching speed, and current oscillations, emphasizing the importance of optimal design. Comparisons between the tests highlight the balance between complexity, control mechanisms, and surge mitigation effectiveness. The choice of configuration ultimately depends on the specific application requirements, with factors such as complexity, operational reliability, and surge handling efficiency being crucial in the design of SS-DCCBs. The findings from these tests provide valuable insights for optimizing circuit designs to ensure effective energy dissipation and circuit protection in various electrical applications.

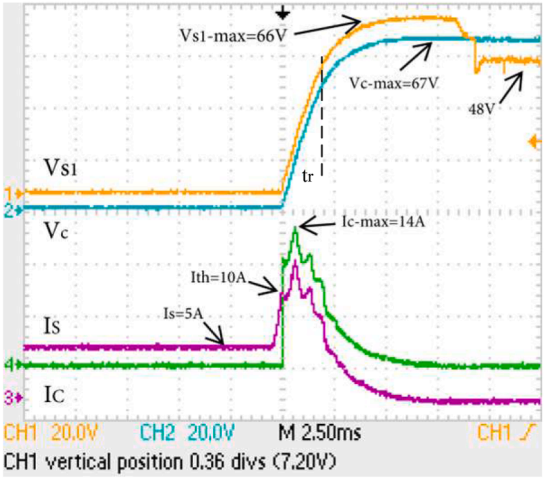
5. Discussion

Four unique configurations of SS-DCCB's are examined and evaluated for their ability to efficiently absorb the surge generated during fault detection and short circuits across the load. The analysis covers circuit performance, complexity, and the effectiveness of surge absorption. Table 2 provides a thorough comparison of the experiments conducted. As demonstrated through a series of tests, optimal design and selecting the appropriate component values can enhance SS-DCCB performance in terms of overvoltage suppression and current oscillation reduction.

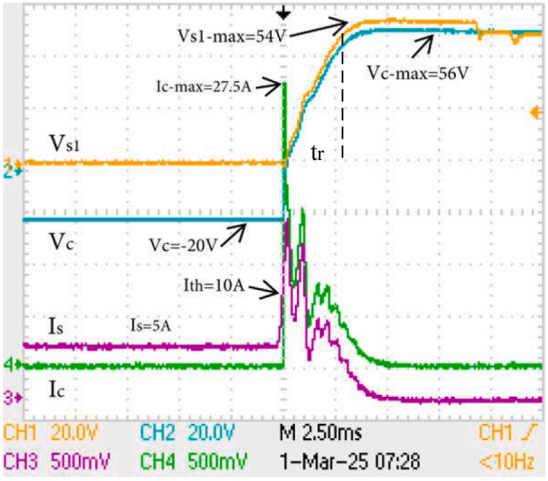
The first topology employs a MOV-based suppression technique, resulting in low switching effectiveness and a high level of degradability. This topology requires only one active and one passive component, but it exhibits a high switching overvoltage level and relatively low control system complexity. This test is performed with two different circuit inductances to elucidate the influence of circuit inductance on switching speed.

The second topology utilizes a TriCap based suppression topology based on CBT. It demonstrates high switching effectiveness and low degradability, making it the most effective among the presented topologies. However, it requires two active and one passive component, resulting in a moderate level of control system complexity.

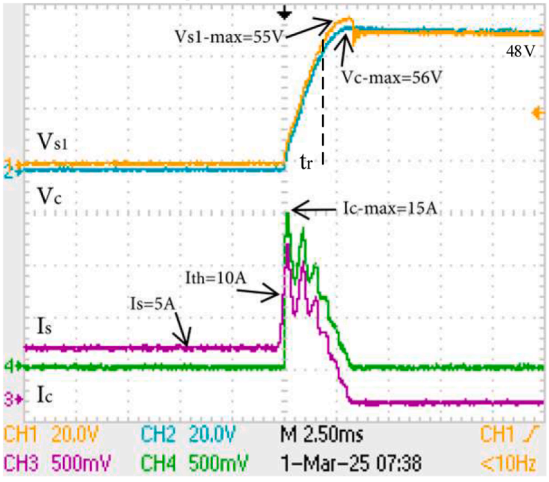
The third topology also employs a Cap-IGBT based suppression technique resulting in high switching effectiveness and low degradability, similar to the second topology. However, it requires two active and one passive component, leading to a higher level of control system complexity compared to the second topology.



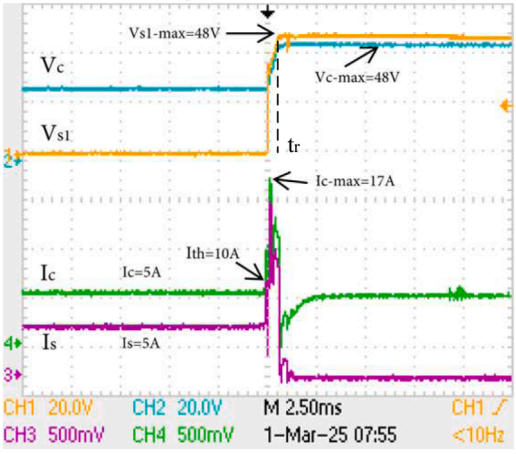
a) Test 1: L_{eq}=75mH, V_c=0V, C=470μF



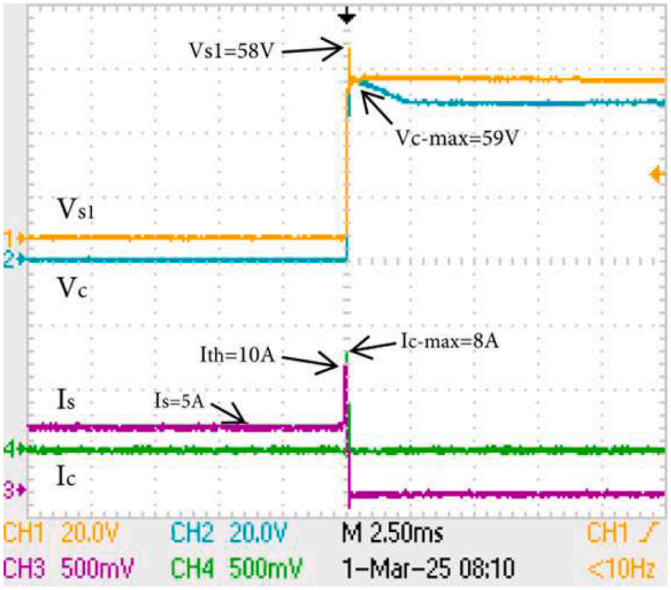
b) Test 2: L_{eq}=75mH, V_c=-20V, C=470μF



c) Test 3: L_{eq}=2.06mH, V_c=0V, C=470μF



d) Test 4: L_{eq}=87μH, V_c=+28V, C=470μF



e) Test 5: L_{eq}=87μH, V_c=0V, C=10μF

Fig. 9. Experimental Results: fault detection operation for Topologies B, C, and D.

The fourth proposed circuit structure utilizes a TriCap based suppression topology similar to the second topology but with a different circuit scheme. It exhibits medium switching effectiveness and low degradability, requiring two active and one passive component, resulting in a moderate level of control system complexity.

In addition to testing circuits with similar inductance across all four topologies, examinations were conducted on topologies one and two with varying circuit inductances (1.7mH and 75.5mH) to scrutinize the influence of inductance on switching speed. As concluded, circuit inductance has a direct impact on DCCB switching speed. Decreasing circuit inductance significantly enhances switching transitions. This observation holds true as a fundamental principle in DC circuit breakers, especially when the surge suppressor is positioned as a series component in the circuit. Across all tested topologies, the surge is rerouted through a series subcircuit.

Table 2 demonstrates that the second topology employing the CBT emerges as the most advantageous, presenting an optimal balance of superior switching performance, minimal degradation, and manageable complexity in the control system. Moreover, considering the drawbacks linked to MOVs during prolonged usage and the limited overvoltage capacity of capacitors, capacitors emerge as a viable alternative for surge suppression in DCCB applications. The switching effectiveness rate in the proposed model is satisfactory, as its switching overvoltage is lower than that of the MOV-based model. From a cost perspective, regardless of high efficiency (*99.78 %*) and cost-effectiveness of MOV-based SS-DCCB, upon long-term assessment and considering the high degradability rate of MOV, Topology B emerges as the more efficient option (Table 3).

6. Conclusion

In conclusion, this study investigated and evaluated four distinct configurations of SS-DCCBs to assess their efficacy in absorbing transient surges during fault detection and short circuits across the load. Through practical tests and analysis of circuit formulations and design principles, the study compares the performance and effectiveness of surge absorption techniques. The experiments highlight the advantages and drawbacks of different topologies, considering factors such as circuit complexity, switching effectiveness, and control system requirements. The results indicate that the proposed CBT emerges as the most effective among the tested topologies, offering high switching effectiveness, low degradability, and moderate control system complexity. This finding suggests that capacitors could serve as a viable alternative for surge suppression in DCCBs, particularly in mitigating the weaknesses associated with MOVs over the long term. The article also elucidates that the value of circuit inductance significantly impacts switching speed, with lower circuit inductance resulting in faster circuit switching. The comprehensive comparison presented underscores the importance of selecting the appropriate DCCB topology based on specific criteria such as switching effectiveness, degradability, and control system complexity. Overall, the study provides valuable insights into the design and selection of DCCBs for future network architectures, contributing to the advancement of DC microgrid protection technologies.

CRediT authorship contribution statement

Mehdi Moradian: Writing – original draft, Validation, Software, Methodology, Investigation, Formal analysis. **Tek Tjing Lie:** Supervision, Investigation, Conceptualization. **Kosala Gunawardane:** Supervision.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Mehdi Moradian reports financial support was provided by Auckland University of Technology. Mehdi Moradian reports a relationship with Auckland University of Technology that includes: funding grants and travel reimbursement. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Table 3
Comprehensive comparison of the experiments.

Parameter	Topology A	Topology B	Topology C	Topology D
DCCB Type	SS-DCCB	SS-DCCB	SS-DCCB	SS-DCCB
Suppression Subcircuit	MOV-Based	TriCap Based	Cap-IGBT Based	TriCap Based
Surge Mitigation Technique	Voltage Dependent	Current Block	Current Block	Current Block
Switching Effectiveness	Low	High	High	High
Degradability	High	Low	Low	Low
Active Components	1	2	2	2
Passive Components	1	1	1	1
Switching Overvoltage Level	High	Low	Low	Medium
SS-DCCB Efficiency	99.78 %	99.30 %	99.24 %	99.30 %
Cost Perspective	Low	Medium	Medium	High
Control system commands	2 × SW	2 × S1	2 × S1	2 × S1
		1 × S2	2 × S2	1 × S2
Control System Complexity	Low	Medium	High	Medium
Overall Assessment	Good	Best	Good	Good

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Data availability

No data was used for the research described in the article.

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