Two Resonant Topologies for Isolated Bi-Directional DC-DC Conversion

By

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Statement of Originality

‘I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for qualification of any other degree or diploma of a university or other institution of higher learning, except where due acknowledgement is made in the acknowledgements.’

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Abstract

A bidirectional dual active bridge is a structure comprising two full bridges which enables power to be transferred between two dc levels via an intermediate ac link. This thesis introduces two types of bi-directional dc-dc resonant converters, referred to as the LCL and the CLC, whose names relate to the resonant network connected between their dual active bridges. These converters provide high efficiency conversion over a wide range of dc supply voltages and for a wide power range. By virtue of their network's resonant operation the magnitudes of the reactive components of the bridge currents are reduced. As a result of the reduced currents lower rated switching devices may be used, and the conduction losses in the bridges are significantly smaller than those of conventional converters. Although the conceptual nature of the LCL and CLC converters is the same, they have slightly different operating characteristics as a result of the realisation of their tee networks. This thesis provides a comprehensive analysis and comparison of these two converters, each of which has different merits. In comparison with a conventional converter, which, aside from the isolation transformer, only has an inductor connected between the bridges, additional components are required in the resonant network of the LCL and CLC converters. It will be shown that the extra expenditure on the resonant network is repaid many times in the life of the converter.

After each converter is modelled, its currents and its power throughput are calculated by the summation of harmonic components calculated in the frequency domain. Theoretical calculations are then used to derive the power throughput, the current harmonic content and the switching status as a function of modulation. Circuit waveforms are calculated and then verified through simulations. The theory is validated with experimental results. Comparisons of the key metrics are made between the proposed resonant converters and a conventional converter for standard designs operating under fixed operating conditions. Finally, comparisons are made, on a cost basis, between optimised converters operating under varying operating conditions. The results show the advantage of the proposed converters.

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Abbreviations

ac	alternating current
BDC	bi-directional dc-dc converter
CCM	continuous conduction mode
CDAB	conventional dual active bridge
CLC	referring to a T network of a capacitor, inductor and a capacitor
CLL	referring to a network of a series capacitor and inductor and a shunt inductor
CSV	comma separated variables
DAB	dual active bridge
dc	direct current
ESL	equivalent series inductance
ESR	equivalent series resistance
FEM	finite element method
FFT	fast Fourier transform
FPGA	field programmable gate array
GaN	gallium nitride
IBDC	isolated bidirectional dc-dc converter
IC	integrated circuit
JFET	junction field effect transistor
LCL	referring to a T network of an inductor, capacitor and an inductor
LCLCL	referring to a network comprising a series inductor and capacitor, shunt inductor and a series capacitor and inductor
LLCL	referring to a network comprising a shunt inductor, series inductor and capacitor, shunt inductor
MOSFET	metal oxide substrate field effect transistor
NPT	non-punch-through
PE	power efficiency
PT	punch-through
PWM	pulse width modulation
rms	root mean square
Si	silicon
SiC	silicon carbide
SPS	single phase shift
THD	total harmonic distortion

TVS	transient voltage suppression (diode)
ZCS	zero current switching
ZVS	zero voltage switching

Symbols

α_1, α_2	phase shift between the legs 1,2 of Bridge 1 and 3,4 of Bridge 2 (rads)
ϕ	phase lead of Bridge 1 with respect to Bridge 2 (rads)
φ	phase lead index of Bridge 1
A..H	indices marking switching points
B	flux density
Capcost	the cost of the capacitor ($), where applicable
dcr	dc voltage conversion ratio
E_{off}	switching energy loss for transistor turning off (J)
Ein	the electrical energy supplied from the grid (kW-hours)
E_{on}	switching energy loss for transistor turning on (Ω)
Fcost	the fixed cost ($)
HWcost	the hardware cost ($)
HSpc	the heat-sink cost proportionality constant ($/W)
i_1	current in to network (A)
$\bar{i}_1$	rms value of current in to network (A)
i_2	current from network (A)
$\bar{i}_2$	rms value of current from network (A)
i_{B2}	current into Bridge 2 (A)
$\bar{i}_{B2}$	rms value of current into bridge 2 (A)
i_{DC1}	dc supply current to Bridge 1 (A)
i_{DC2}	dc supply current from Bridge 2 (A)
$k_{1\ldots4}$	parameters defining network reactances relative to X_D
k_c	magnetic component cost proportionality constant
k_p	power loss proportionality constant
k_r	power loss reduction factor, for increase in linear dimensions

Lcost	the cost of the inductor ($), where applicable
m_1, m_2	amplitude modulation indices for bridges 1 and 2
m	common amplitude modulation, for $m_1 = m_2$
P_1	power input to Bridge 1 (W)
P_2	power output from Bridge 2 (W)
pc	power loss in core of magnetic component (W)
pt	total power loss in magnetic component (W)
pw	power loss in winding of magnetic component (W)
P_i	ideal power throughput of converter, for lossless process (W)
P_{con}	conduction power loss (W)
P_B	base power throughput (W)
PHS	the heatsink power dissipation (W)
P_{sw}	switching power loss (W)
R_{Goff}	source resistance of gate drive circuit for off signal (Ω)
R_{Gon}	source resistance of gate drive circuit for on signal (Ω)
R_{on}	resistance of a turned-on MOSFET (Ω)
R_p	primary referred resistance of transformer (Ω)
tics	represents the index of a series (in time/angle dimension)
t_r	transformer turns ratio n_1/n_2
TRcost	the cost of the transformer ($)
Unitcost	the cost of electrical energy ($/kW-hour)
v_1	voltage input to network from Bridge 1 (V)
$\overline{v}_1$	ac rms value of voltage input to network from Bridge 1 (V)
v_2	ac voltage output from network to transformer (V)
$\overline{v}_2$	ac rms value of voltage output from network to transformer (V)
v_{B2}	ac voltage output from Bridge 2 (V)
$\overline{v}_{B2}$	ac rms value of voltage output from Bridge 2 (V)

V_{DC1}	dc supply voltage to Bridge 1 (V)
V_{DC2}	dc supply voltage to Bridge 2 (V)
V_{Drv}	output voltage of switch driver (V)
X_D	design reactance of resonant network (Ω)

1 Introduction

1.1 Background

The world's rapidly expanding population and increasing levels of consumerism have given rise to significant environmental issues that must be confronted. Firstly, there is a great reliance on fossil fuels to provide energy, of which a large part is consumed by transportation systems. While shale oil recovery by the hydraulic fracturing process has provided a temporary increase in production, it is only extending the point in time at which demand exceeds supply [1, 2]. The second, and interrelated, major problem is that of environmental damage in general, and specifically that of air pollution. Aside from the contentious issue of global warming, there is a requirement for a reduction in the burning of hydrocarbons to achieve adequate air quality. The basis for a solution to both problems is in the sustainable use of resources, and considerable effort is being expended investigating forms of renewable, or green, energy [2-4]. Two of the more promising alternative energy sources are from wind and solar farms. These allow for distributed and localised generation, which offers the advantages of reduced distribution costs and improved network security. However, the supply of energy from these sources is variable in nature, due to the dependency on the weather conditions, and results in grid planning and stability issues. Furthermore, the problems caused by these source variations are exacerbated by the wide variations in electrical energy demand, even on an hourly basis within modern societies. Electric vehicles (EVs) are a part of the solution to the energy problem.

In comparison with vehicles powered by internal combustion engines, EVs produce fewer harmful air pollutants and have higher levels of energy efficiency. In addition, EVs can improve the stability of the grid through the use of Vehicle-to-Grid (V2G) systems [5-7]. The battery in a V2G system can be charged by off-peak power from the grid, or, when the EV is not in use, the battery can be used as an energy source to provide grid support. Through the support of multiple batteries the stability, regulation and reliability of the grid can be improved. As a consequence, the increased use of V2G systems makes it possible to generate a greater proportion of electricity from renewable energy sources without compromising the quality of the grid [5].

To implement a V2G system, an isolated DC-DC converter that can provide bi-directional power transfer to and from the vehicle by either wired or wireless means is required. The same converter may be used in other bi-directional power transfer applications, such as the distributed generation (DG) system shown in Figure 1.1, which shows how a number of green energy sources may be integrated into a household electrical system. In this system the DC-DC converter is required to provide isolation for safety reasons, as the wiring of the batteries used in the system is accessible.

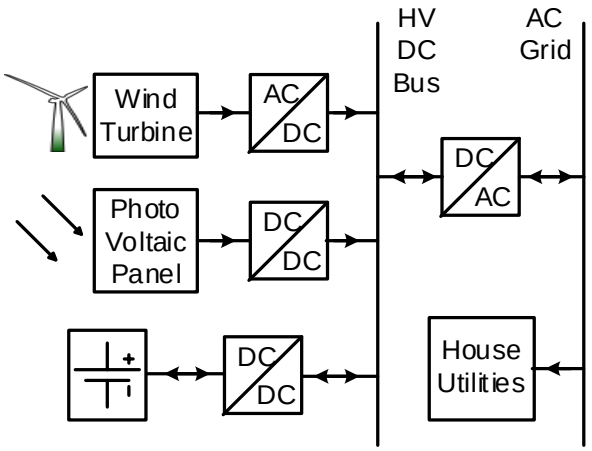


Figure 1.1: A Distributed Generation System

This thesis presents a novel bi-directional isolated DC-DC converter which may be used in the V2G or DG applications discussed above. It has hardware that is similar to that of a conventional dual active bridge converter (CDAB), except that the latter's inductor is replaced with a resonant network to reduce the converter's conduction losses. The converter's operation and performance is thoroughly investigated, both theoretically and experimentally. The performance analysis is mindful of practical aspects of the converter's design, including the voltage and current ratings required for the components, as well as running and capital costs. Through this consideration of costs, issues related to the sizing of components and circuit efficiency are accounted for, tying together the economic and engineering aspects of the proposed converter topology. It is the opinion of the author that this thesis will satisfy readers from both industrial and academic perspectives.

To allow the benefits of the proposed resonant DAB converters to be evaluated, it is necessary to have a knowledge of CDAB types. To this end a review of the CDAB is undertaken in Section 1.2.

1.2 A Review of the Conventional DAB Converter

At present, one of the most popular isolated bidirectional DC-DC (IBDC) converter topologies for medium power energy conversion is the conventional dual active bridge (CDAB) converter, whose topology is shown in Figure 1.2.

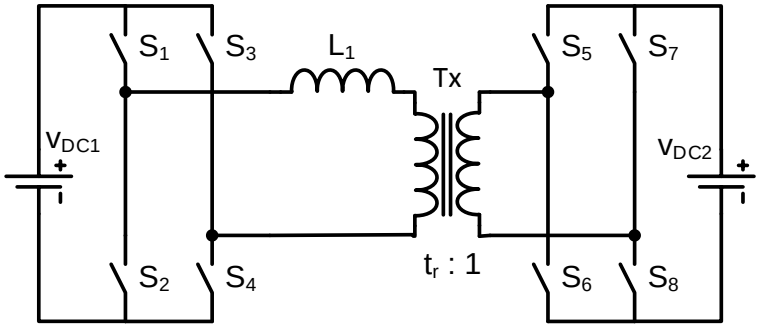


Figure 1.2: Conventional DAB Converter

This converter has many attractive qualities, including galvanic isolation, and the ability to accommodate a range of DC voltages through selection of an appropriate transformer turns ratio.

1.2.1 Control of CDAB

Originally, control of the CDAB was implemented through single phase shift (SPS) modulation, in which the legs of each bridge are operated in anti-phase with each other in order to generate bipolar square waves. This technique allows the power throughput to be controlled through simply varying the phase shift between the primary and secondary bridge waveforms and, for the system of Figure 1.2, the power throughput P (W) from V_{DC1} to V_{DC2} is given by [8]:

$$P = \frac{t_r V_{DC1} V_{DC2}}{X_L} \phi \left(1 - \frac{|\phi|}{\pi}\right) \quad (1)$$

Where: X_L is the reactance of inductor L_1 at the fundamental frequency (Ω)

ϕ is the phase lead of Bridge 1 relative to Bridge 2 (rad.)

t_r is the transformer's primary to secondary turns ratio

It is usual to have modulation angles in the 0° to 90° range. Although the same power control occurs for angles from 180° to 90°, this range is avoided as it results in higher currents and, thus, higher conduction losses [9].

In addition to being easy to control, the CDAB requires only a small number of power components, as apparent from Figure 1.2. Commonly, this component count is reduced further by integrating L_1 into Tx as the latter's leakage inductance.

Since the manner of switching affects the CDAB's performance, the zero voltage switching (ZVS) range of the CDAB is discussed in the next section.

1.2.2 ZVS Limits of CDAB

An accurate analysis of the topology of Figure 1.2 for an integrated magnetic component, which has the leakage reactance split symmetrically and a magnetising inductance added, requires the circuit shown in Figure 1.3.

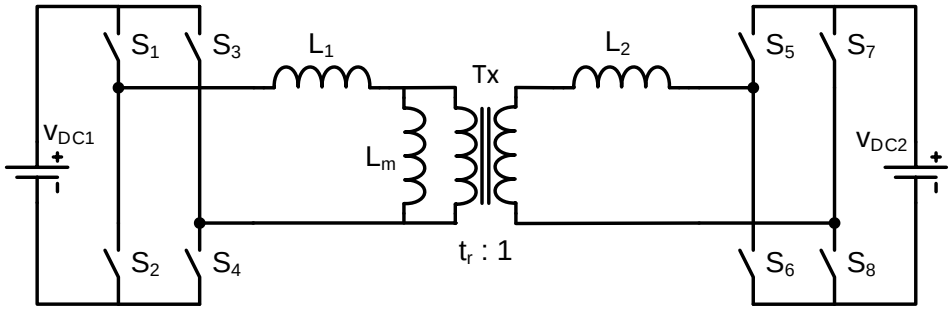


Figure 1.3: CDAB with magnetising reactance

With reference to (1), the primary referred values of L_1 and L_2 are equal to half the total leakage inductance, and the value of the magnetising inductance L_m is k_m times greater:

$$X_L = 2\pi f_s(L_1 + {t_r}^2 L_2)$$
$$L_m = k_m(L_1 + {t_r}^2 L_2) \quad (2)$$

The transfer characteristics and the ZVS limits of this converter are shown in Figure 1.4 [10] for unit values of V_{DC1}, V_{DC2} and X_L, for a range of dc transfer ratios (dcr), as defined by (3).

$$dcr = t_r \frac{V_{DC2}}{V_{DC1}} \quad (3)$$

The input bridge ZVS limits, within which soft-switching ideally occurs, were calculated by finding, for a large number of dcr values, the boundary case of the phase shift at which the transformer's primary current is zero at the switching points. Similarly, the output bridge ZVS limits are based on the secondary current. In a practical system

there is the added requirement to have adequate stored energy to provide the necessary commutation [8].

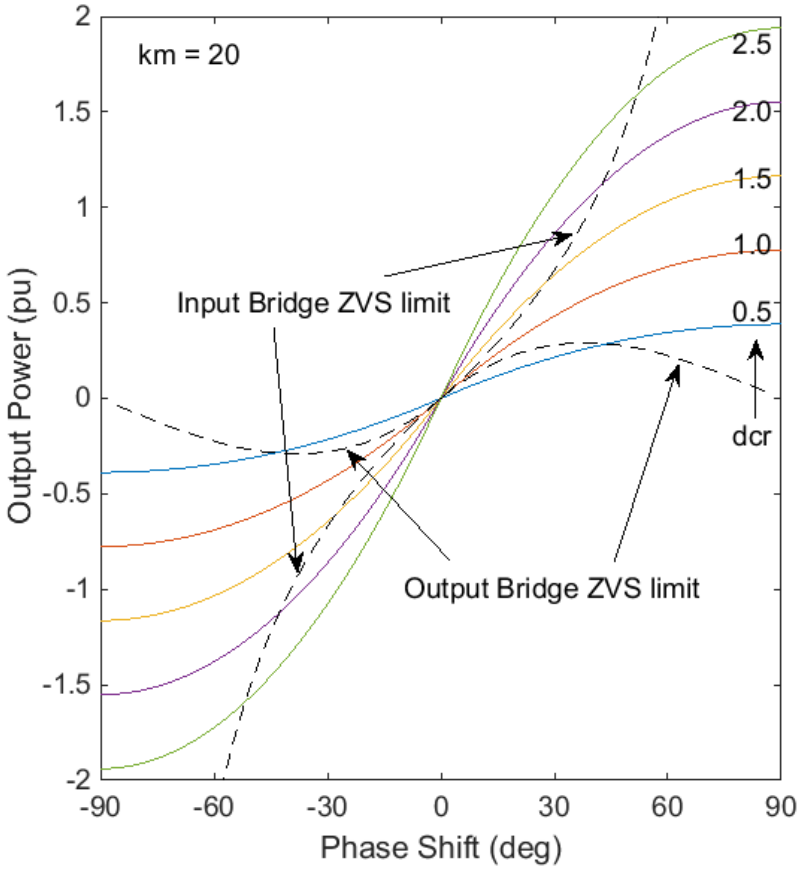


Figure 1.4: Transfer characteristic for km = 20

These characteristics were derived for a k_m value of 20. For this value, the magnetising current is virtually insignificant, so that the converter behaviour is essentially the same as that of Figure 1.2.

The dcr values are used to represent the relative voltage matching between the two bridges, with a unity value indicating a matched system. It can be seen that, for non-unity values of dcr, one, or both, bridges lose ZVS at small phase-shift values. Large dcr values make it harder for the input bridge to obtain ZVS, and smaller values make it harder for the output bridge. It is clear that the range of operating voltages is severely restricted if ZVS is to be maintained. For an application such as a battery interface to a dc voltage bus, a battery voltage span of 2 to 1 might correspond to a dcr range of 0.75 to 1.5. In this case ZVS could, in general, only be achieved at high power levels.

For larger values of phase shift the power output increases at a diminishing rate, even though the current is increasing steadily, and the current's square, and therefore

conduction losses, are increasing rapidly. It is for this reason that operation at large modulation angles is usually avoided.

Figure 1.5 again shows the converter's characteristics, this time for $k_m = 3$.

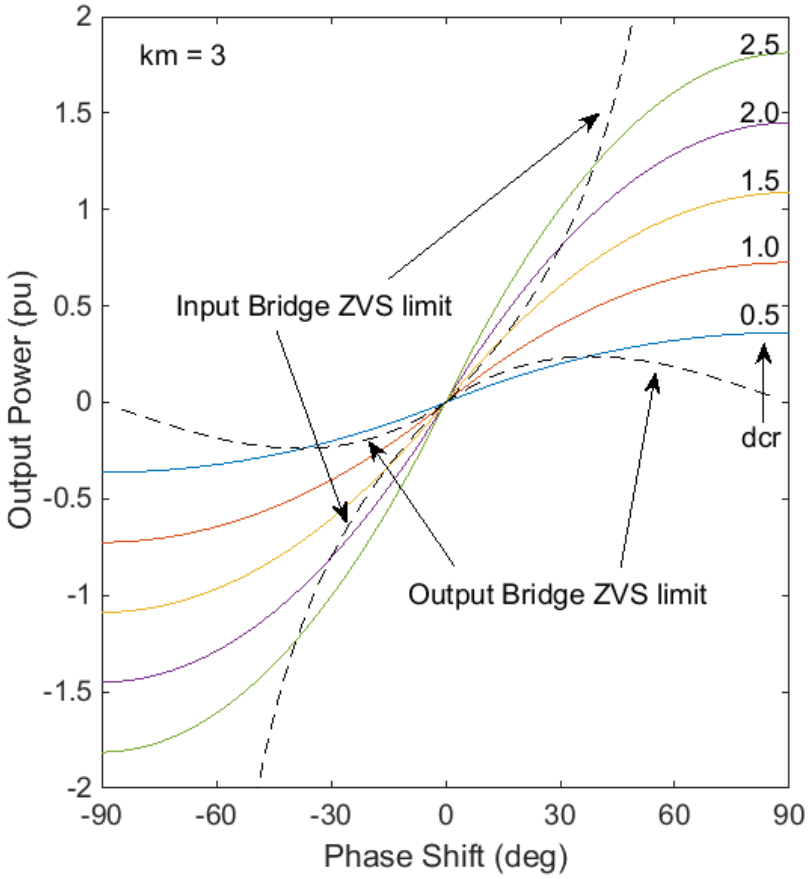


Figure 1.5: Transfer characteristic for km = 3

For this system, with a more easily realised transformer design, the magnetising currents will be significant and there will be a small decrease in the output power. More importantly, the increased, lagging, currents result in a wider range of dc supply voltage values for which ZVS is achieved. The penalty for the increased ZVS range is the increased conduction losses. There will be an increase in efficiency at lower power outputs, as a result of ZVS now being achieved, and a decrease in efficiencies at higher power outputs, as a result of the increased conduction losses.

From the foregoing, it is apparent that the CDAB topology suffers from poor power efficiency at both high and low power levels. The CDAB has its best performance in systems that don't have a large maximum modulation angle, suggesting that it should be designed with a relatively small X_L value to achieve this. However, operation of such systems at phase angles small enough to achieve the minimum power throughput is

limited by the resolution of the controller and the effect of the dead-band on the transfer characteristic [11], and will result in relatively low power efficiencies for non-unity dcr values. For the selection of the magnetising reactance, the compromise to be met is between switching losses, bought about by the loss of ZVS at low power levels, particularly for unbalanced bridge voltages, and conduction losses bought about by large reactive currents. The use of a large magnetising reactance will also require a larger transformer.

This section has undertaken a detailed look at the deficiencies of the CDAB converter, whose performance, as the incumbent converter, needs to be surpassed by its replacement if the latter is to be adopted. Section 2.2 provides a chronological review of the various attempts that have been made to improve the CDAB converter's performance. While it has been improved by these efforts, some of the fundamental problems highlighted in Section 1.2 remain. This thesis proposes two resonant DAB IBDCs, each of which addresses the major deficiency of the CDAB converter, namely its low power efficiency which results from its large reactive currents and power flow, particularly for wide variations in either the dc voltage levels or the power throughput.

1.3 Research Objectives

The fundamental objective is to decide if the proposed resonant converter topology is better than that of a conventional DAB converter. In order to establish this, a comparison will initially be made between the converters of each specific performance parameter, such as the full-power power efficiency. As there are a number of parameters, "better" would depend on the weighting one placed on each attribute, and would necessarily be subjective. Then, as a means of removing some of the subjectivity, a comparison will be made of the total cost of each of the optimised converters over its projected lifetime, being the summation of the hardware and the energy costs. This will establish, on a cost basis, the ranking of the CLC, LCL and CDAB converters.

In order to make the above comparisons, the characteristics of each of the resonant converters first needs to be determined. The most important performance metric is the magnitude of the power efficiency as a function of the power throughput and the dc supply voltages. This requires knowing the power throughput as a function of the modulation and the losses, which in turn depend on the switching status and on the hardware parameters. Also of interest is the performance sensitivity, as the resonant network is a

tuned inductor-capacitor network. Finally, the size and cost are impacted by the components used, especially the magnetic components. For this reason the magnitudes of the currents and the volt-second products of the latter are of interest.

The next section outlines the methodology used for the research.

1.4 Research Methodology

For each converter a model of the converter will be made, from which the voltage and current phasors will be calculated in the frequency domain for an ideal, or lossless, variant. The power throughput will be calculated by the summation of the real components of the current-voltage products, and the summation of the individual frequency components will provide the voltage and current waveforms in the time domain. Switching, conduction and magnetic losses will then be appended to the results from the ideal system. Simulation of the system in PLECS, and experimental results, will be used to validate the theoretical results.

1.5 Thesis Organisation

Chapter 1 provides a brief background of the requirements for an IBDC and a review of the characteristics of a CDAB converter, highlighting the deficiencies which need to be addressed.

Chapter 2 is a literature review which backgrounds the developments in isolated dc-dc converters.

Chapter 3 contains the theoretical circuit analysis for the LCL DAB converter, using a lossless circuit. Many of the calculations are performed in the frequency domain using numeric techniques, on account of the difficulty of obtaining an analytical solution for the resonant circuit's equations. The initial frequency domain modelling provides the equations for the currents, voltages and power which will subsequently be used for characterising the converter. Then, the converter's waveforms are generated from the time domain summation of the odd-harmonic phasor components generated in the frequency domain. This, multiple component, analysis provides a better accuracy than that of the commonly used fundamental harmonic analysis (FHA).

Chapter 4 follows the same procedure as that of Chapter 3 for the CLC DAB converter.

In Chapter 5 the theoretical performance of the LCL and CLC converters is compared with the results from laboratory testing, to access the validity of the modelling. Before the comparisons can be made, the theoretical analyses need to be aligned with the actual circuitry used in the prototype converters which would ultimately be tested. This is achieved by using the parameter values, which are hardware dependent, taken from the prototypes. Also, since the initial converter models used in Chapters 3 and 4 were lossless, the conduction, switching, magnetising and resistive losses need to be allowed for in the theoretical calculations. Following the theoretical analyses, comparisons are then made with the results from converter testing at different power and voltage levels.

In Chapter 6 comparisons are made between the CDAB and the resonant DAB converters in their standard form under fixed operating conditions. Then optimisations of the LCL and CLC converters are initially performed to improve their power efficiency, by using all three control angles. These involve the power efficiency at various power levels, the value of the ac link current, the value of the dc ripple current and the size of the magnetic components. Finally, comparisons are made of the total lifetime cost of the CDAB and the resonant converters when they are operated within a specified set of varying conditions.

Chapter 7 draws conclusions from the work done and makes recommendations for future work.

2 Literature Review of DAB Bi-Directional DC-DC Converter

2.1 Introduction

A predecessor of the conventional dual active bridge (CDAB) converter, the pulse width modulation (PWM) converter, was popular in the 1980s. It used a hard-switched bridge to drive a transformer whose rectified output was connected to the load through a filter comprising a series inductor and shunt capacitor, which provided energy storage and therefore continuity of the output current. Although the transformer had a modest VA rating, it could have been smaller if it were operated at a higher frequency. However, the switching frequency of this converter was limited by the switching losses which were significant because there was hard switching of the diagonal transistor pairs. The CDAB converter had its origins in the early 1990s [8-10, 12, 13]. With the availability of large, high voltage IGBTs which were faster than other switches available at the time, there was a requirement for multi-kW dc-dc power supplies which were smaller and cheaper, necessitating operation at higher switching frequencies. This, in turn, required a reduction in the switching losses. By the relocation of the PWM converter's inductor to become the leakage inductance of the transformer, the inductive energy was used to commutate the voltage of the switching device and its snubber capacitance in a soft-switching [9, 14] manner, reducing device stresses and switching losses. Instead of degrading the system's performance, the circuit parasitic elements, namely the transformer leakage inductance and the switch output capacitances, are put to use. The CDAB converter retains the advantage of being an isolated converter which has switching devices with defined voltage stresses and equal power losses, but obtains a higher power density, as a result of the higher switching frequency made possible with soft-switching. As a result of the addition of the second bridge, it also has bidirectional capability, both in buck and boost modes. The CDAB is defined by the simple topology of Figure 1.2. There is extensive literature on this, and other DAB converters, which will be examined in the following sections.

2.2 CDAB Converter Control

The converter's dynamic control aspects, which have been investigated in papers [15-21], are beyond the scope of this thesis. This section will focus on steady state control aspects, particularly on the range of power and the power efficiency.

Originally, control of the CDAB converter was by single phase shift (SPS) modulation, also known as conventional phase modulation (CPM), which is easily implemented but not very flexible. There have been many papers proposing improvements to the modulation of the DAB converter, albeit with an associated increase in complexity. A representative selection of these will be reported in chronological order:

In [22] the so called "extended phase shift" (EPS) modulation was used to extend the zero voltage switching (ZVS) range, in which the bridge having the relatively higher dc voltage was amplitude modulated to provide a third voltage level of 0 V for a portion of the cycle. By clamping the voltage of this bridge the current crossing in the other bridge could be shifted forward [9]. The value of the amplitude modulation used in the bridge with the larger effective dc voltage was simply calculated to result in balanced bridge ac voltages. This efficiency improvement resulting from the reduction in the switching losses is most significant for large dcr values.

Poor power efficiency at high modulation levels in a conventional DAB converter are a result of the large reactive power flows and associated large rms currents which cause excessive conduction losses. In [23] dual phase shift (DPS) modulation, in which the bridges have equal amplitude modulations as well as the phase shift between them, is used with the intention of reducing these reactive flows, thereby increasing the efficiency. It is suggested that the PWM may also be used to facilitate a soft start. Some of the power formulae are incorrect - the corrections are included in [24].

In [25] EPS is again used by the authors, this time with the intention of reducing the overall converter losses by the use of modulations derived from an algorithm which used the voltage conversion ratio and the power level as inputs. The efficiency improvement depends on the dcr value, with best results of up to 10% reported.

In [17], a three angle modulation system which could generate the so called "trapezoidal modulation" (TZM), "triangle modulation" (TRM) and a variant of TRM was used, mainly with the objective of improving response times. The TRM variant was only applicable in systems in which the dc voltage ratio was close to unity, and for this

reason would have limited application. There were no efficiency figures supplied, nor results on other parameters which may have been affected.

For a DAB converter with SPS, steep increases in current occur as the inter-bridge phase shift approaches $\pi/2$. The authors of [15] suggested that values greater than 0.35π should be avoided, to achieve a better compromise between conduction and switching loss minimisation. Large modulation values result in large reactive currents and power flow, and therefore larger conduction losses, whereas small values will result in a smaller ZVS range and greater switching losses. Other complications are the variation in the dc voltage ratio and the difficulty of providing control with very small phase shifts [26]. There was no power efficiency data presented.

A detailed loss analysis of a DAB converter providing an interface between a high voltage dc bus and a nominally 12 V battery in an automotive application is made in [27]. The results show the compromise which needs to be made between conduction and switching losses. Relatively small conduction losses are achieved as a result of using multiple parallel MOSFETs. Although power efficiencies of up to 96% were reported, there was a significant difference between the theoretical and the experimental values at low power levels, suggesting that there is a power loss mechanism which has not been accounted for.

In another example of DPS, the two modulation angles were calculated by algorithms for three separate cases in [28]. An optimisation of minimum rms current, minimum peak current and minimum reactive power could be selected. The authors decided that the minimisation of the peak current was appropriate, both as the best compromise and for ease of practical implementation. Maximum power efficiencies of up to 90% were obtained in simulations at maximum power output, and slightly less in the experimental results. When compared to SPS modulation, the efficiency improvements were only significant at low power levels.

The authors of [22] used EPS again in [29], this time calculating the two modulation angles using an algorithm, in order to provide converter control with ZVS in the whole operating range. Although the maximum power efficiencies obtained experimentally were less than 90%, they were noticeably better than those obtained with SPS modulation, particularly at the low power levels.

A composite modulation scheme was employed in [30], transitioning from dual PWM for small inter-bridge phase shifts through to single PWM which varied linearly to a maximum for a phase shift of $\pi/2$ at full power. This provided significant improvements in low-load efficiency without a loss in the full power capacity. For a dc conversion ratio range of 2:1, the efficiency varied from 77% at 3% load through to approximately 90% at full load, a large improvement over SPS.

In [31] the authors used a three angle modulation system, namely two independent bridge amplitude modulations and the phase shift between the bridges, to optimise the converter design on the basis of minimal conduction loss. Again the converter interfaces between a high voltage dc bus and a nominally 12 V battery in an automotive application, so the results of this work may not extend beyond this application. Numeric techniques were used to search for the best operating points. It was found that TCM was optimal at low power levels, up to the maximum power available under TCM, but beyond that it was best to use maximum modulation of one bridge and then both (c.f. SPS) at high power levels. The fundamental problem, of large currents and large reactive power flows, remains at high modulation levels.

A similar investigation to that in [31] was undertaken by the same authors in [32], this time to optimise the overall power efficiency. There was a significant improvement over the SPS performance, particularly at the low power levels. Best power efficiencies of up to 95% were obtained, although it dropped off steeply at low powers.

Another study of DPS modulation in [33] intended to show that the added degree of freedom enabled the same power transmission to be made with smaller currents. Power efficiency data was not provided.

Another study of the benefits of EPS is documented in [34]. It is concluded that it is easy to implement and for any given level of the transmitted power it has reduced reactive power flow and smaller rms currents than would have occurred with SPS modulation. Best efficiencies of approximately 90% are obtained experimentally, although these would probably be lower if the switching frequency were higher than 10 kHz.

In [35] the authors optimise the DPS modulation values for maximum power efficiency. Peak efficiencies of over 90% are obtained, again a significant improvement over SPS modulation used in the conventional DAB converter. The switching frequency

was 10 kHz again, so that the switching losses are under-represented in comparison with some other converters presented in the literature.

2.2.1 Effect of Dead-band/dead-time

A practical switching leg requires a dead-band between the transistor conduction states to ensure that there is no cross current conduction. This section examines how dead-time is implemented and the effect that it has on the control of the converter and its power throughput.

An adaptive switching controller is presented in [36]. When turning on a switch in a leg, the turn-on is delayed until the opposing anti-parallel diode is sensed to be conducting. Although extra hardware is required, the dead-time delay which is used is the minimum possible, and corrects for component and operating variations.

In [37] the authors show the effect of the dead-band on the phase shift and the power. It is recommended for system robustness that operation near boundary conditions should be avoided. Changes of inductor current polarity in the dead-band will cause voltage oscillations which generate added electromagnetic interference.

The dead-time is incorporated into the power flow calculation in [38] to provide an accurate relationship between the phase shift and the power throughput. The errors which exist for the conventional model are particularly significant for very small phase shifts. Reactive power flows resulting from bridge voltage imbalance are quantified.

In [39] the optimisation of the efficiency includes an allowance for the dead-time is in the control system. The concept is proven on a prototype system which had a switching frequency of 1 MHz, at which small time errors are significant.

In [40] the effect of the dead-time on the harmonic content of the converter is investigated. The error between the correctly switched waveform and the actual waveform is analysed as a tool to choose the dead-band width for a certain maximum distortion.

To avoid a conservatively large dead-time, with the attendant problems of pole ringing and loss, or partial loss, of zero voltage switching, [41] presents another controller using an adaptive dead-time. Unlike that of [36] above, the dead-time is not decided on a cycle by cycle basis but is slowly ramped down from its maximum value each time it was

previously proven to be adequately large. A small improvement in efficiency is achieved, along with the reduced noise noted above.

The effects of dead-time are shown in [11] to include phase drift and the modification of the power transfer characteristic. Phase drift refers to the occurrence of a dead zone in which changes in phase shift have only a small effect on the power transmission. It is also shown that the power transfer characteristic doesn't, in general, pass through the origin, and is dependent on the dc voltage ratio.

2.3 DAB Converter Hardware

Although most of the proposed improvements to the DAB converter have related to its control, there are also some discussions of different hardware possibilities:

2.3.1 Transformer

In [42] an adaptive inductance was controlled by a bias current so that the inductance had a smaller value at high modulation levels. This provides a better compromise between the inductive energy necessary to provide soft-switching at low modulation levels, and the large reactive power which flows at high modulation levels. Using this technique, full output power requires a smaller phase shift, with reduced circulating energy. There was no mention of the magnetising losses in the inductor which may have been introduced as a result of the control of the inductance by the use of saturation of its magnetic material. However, a peak power efficiency of over 97% was achieved in a 1 kW prototype converter switching at 50 kHz. The efficiency gain was approximately 5% at 10% of maximum power and 1.5% at full power.

In broad terms a similar approach was used in [43], except that the system used a specially designed transformer which had a second, lower leakage inductance value which was switched in at high power levels. Further performance optimisation was by the use of a variable switching frequency. The effect of the dc conversion ratio on the ratio of the peak inductor current to the dc input current was examined. It was concluded that a smaller link reactance was desirable to minimise, for a particular power output, the inductor current and therefore conduction losses. This, again, highlights the compromise to be made between switching and conduction losses, as mentioned before in the reference to paper [15]. The power efficiency of a 6 kW prototype was measured at various power

levels and dcr values. A maximum efficiency improvement of over 10% was achieved at 1 kW, with power efficiencies of up to 97% obtained.

An optimisation technique for the design of the transformer was presented in [44], in which the combined core and winding losses were minimised for a transformer realising its leakage reactance by winding separation. A comparison was made of the effectiveness of a combination of particle swarm optimisation with differential evolution and hand designs. The 5 kHz transformer designed for a 200 W prototype converter had losses of approximately 6.7% for the optimised design and 9% for the hand design.

In [45] three different transformer constructions were evaluated for use in a converter with low and high voltage connections. One case was a barrel construction and there were two planar transformers, one using PCB tracks as conductors and the other using Litz wire and copper foil. The lowest losses occurred in the planar transformer, with the1 kW 25 kHz prototype converter achieving a full load efficiency of 93%.

A comparison in a 100 kHz 2.2 kW converter application of nano-crystalline and ferrite cores was made in [46]. Even though the 3C90 ferrite core provided the best efficiency under normal conditions, it was concluded that the nano-crystalline core had the better performance because of its high thermal conductivity which simplified the thermal design.

In [47] the transformer design for a 3 kHz 6.7 kVA solid-state-transformer with natural cooling is studied with regard to the choice of core materials and the layout of the windings to obtain the required leakage inductance, a relatively high magnetising inductance and the required high voltage isolation. A finite element method (FEM) analysis established that the most cost effective design was a coax transformer with an amorphous alloy core.

2.3.2 Semiconductors

The anti-parallel diode is an important part of a dc-dc converter. In the case of hard switching its reverse recovery process can place a considerable burden on the opposing transistor which is switching on. Its conduction losses can also be significant, particularly when used in association with IGBTs, which can’t conduct in their third quadrant. A comparison is made in [48] between silicon (Si) diodes and the new silicon carbide (SiC) diodes. The latter were found to significantly reduce the switching losses, particularly at elevated temperatures. However, their larger bandgap resulted in an increased conduction

loss. In [49] two SiC diodes were connected in a series and parallel manner with each of the MOSFETs used in the converter, to the effectively replace the MOSFET's intrinsic diode, which has very poor dynamic characteristics, with a high performance diode.

Si IGBT and SiC JFET devices were compared [50] in a high power back to back converter used as a replacement for a low frequency transformer. The SiC-based system had a higher efficiency, because of its fast switching and therefore small switching losses, even though it operated at a higher frequency. It also used far fewer devices, because of their higher voltage ratings. Similar discussions are made in [51], with predictions of SiC MOSFETs offering big reductions in conduction and switching losses. Low weight and high power densities are achieved in each system.

In [52] a study is made of another dc-dc converter, from 5 kV to 700 V at 25 kW. The high voltage side again uses switches blocks made from a cascade connection of series SiC JFETs controlled by a MOSFET. The JFET switches have a negligible switching loss.

SiC MOSFETs with a co-packed diode are used in [53]. The high voltage rated SiC MOSFET has a smaller R_{DS} when switched on than its Si counterpart, along with lower leakage at elevated temperatures and lower thermal resistance. In another study, of a 350 V 3.5 kW DAB converter [54], it was also concluded that the SiC devices offered better performance, although, surprisingly, the converter only had a switching frequency of 20 kHz.

A comparison was made in [55] between silicon and gallium nitride (GaN) MOSFETs used in a low power, low voltage, high frequency step down DAB converter. The conclusion was that the GaN devices had superior performance on the inverter side where lower switching losses were offered and comparable performance to the Si devices on the rectifier side where conduction losses were dominant. GaN devices are evolving rapidly, so these comparisons are already dated.

In [56] a gate drive shaping network is used to provide an orderly turn-on of an IGBT, in the interests of reduced turn-on losses.

Two dynamic loss characteristics of IGBTs are described in [57]. It is shown that the turn-off losses depend not only on the IGBT's voltage and current at the point at which the transistor is turned off, but also on the path that the current took prior to turn-off. A similar phenomenon occurs with the conduction losses, where the voltage drop is

modulated by the history of the current. This effect is most significant at higher switching frequencies, and is also dependent on the IGBT's construction – punch-through (PT) and non-punch-through (NPT) devices are investigated.

An investigation along similar lines in [58] shows how the IGBT's stored charge lags behind its current, causing large turn-off losses when the current tail overlaps the re-applied voltage. It is shown that switching losses may be significantly reduced if ZVS turn-on were used and if the current waveform were shaped to allow carrier recombination to occur before the voltage is reapplied to a switch which has been turned off, to minimise the tail current.

2.3.3 Three Phase DAB Converter

The three phase configuration [10] is usually reserved for higher power levels. Its main advantage is its significantly smaller dc ripple current, enabling more flexibility in the choice of capacitors. It also has slightly smaller transistor currents, on a per transistor basis, and there is slightly more hardware required. A three phase transformer, if used, will have a somewhat smaller area product than that of three individual transformers, although the latter are easier to manufacture with matched inductances.

2.4 Current-Fed DAB Converters

Various current-fed converters have been reported in the literature [59-61]. Although this topology copes well with a wide dc voltage range, a large dc inductor is required and this topology is best suited to low voltage use because of the high voltage stresses incurred. Also, to be truly bidirectional, such a converter would need to have a symmetrical topology.

2.5 Resonant Converter Alternatives

The DAB converter is classified [62] as a quasi/pseudo resonant converter of the resonant-transition type – at switch turn-off a resonant transition occurs, and at turn-on that switch closes under ZVS conditions, which are ideally lossless. Turn-on losses were seen to be the drawback of the hard-switched PWM converter, which otherwise would have excelled because of its minimal conduction losses. The motivation for using resonant conversion is to achieve ZVS or ZCS to reduce the switching losses. For ZVS

the parasitic elements may be incorporated into the conversion process, rather than working against it.

For resonant conversion the resonant waveform occupies the whole cycle, in contrast to the switching transitions in the quasi resonant conversion, and therefore has a far smaller resonant frequency. A summary of the main resonant converter topologies will be reported in chronological order:

A constant output current resonant converter was presented in [63]. Although the converter analysed is unidirectional, its operating principle doesn't preclude the addition of another bridge to convert it to a bidirectional converter. This converter employed an LCL tee network which acted as an immittance converter [64], converting an ac voltage source to an ac current source for fixed frequency operation at the resonant frequency. A fundamental harmonic analysis is used to derive the converter's voltage gain. It has minimal conduction losses because there is no circulating power, as a consequence of the alignment of the bridge voltage and current waveforms. Its high output resistance makes it easy to parallel units, which may be advantageous for battery charging.

In [65] a fundamental harmonic analysis was made of a 200 W DAB series resonant converter (DBSRC) which had bidirectional power transfer which was phase shift controlled at a fixed frequency of 100 kHz. Its resonant network comprises a series inductor and capacitor. The converter operated with all switches in either ZVS or ZCS over the full power range, and had an efficiency of 95% at full load and 77% at 10% load. Switching at 10% above the resonant frequency was used to ensure the lagging currents necessary for ZVS operation.

A CLL variant of a DBSRC, in which a shunt inductor had been added to the series LC network, was analysed in [66]. It also used phase shift control at a fixed frequency, and achieved ZVS in all switches for the full load range, up to 1 kW. This was made possible by the shunt inductor, which provided the necessary additional lagging current. A disadvantage of this added current is the increased conduction losses which will result. The shunt inductor changes the converters gain-frequency characteristic so that a smaller range of the switching frequency is needed for regulation from light-load to full-load. It also has the advantage that voltage gains greater than unity may be obtained. The shunt may be implemented at no cost by the use of the mutual inductance of the transformer. No efficiency information was provided for this system.

Another analysis of a dc converter using an LCL tee network was made in [67], this time controlled with an asymmetric duty cycle, rather than with clamped mode. This converter had the potential for ZVS operation if designed correctly. As with the previous LCL tee converter, the addition of a second bridge would enable bidirectional operation. However, the use of an asymmetric waveform meant that a coupling capacitor was required between the bridge and the transformer to prevent dc being applied to the latter. From a control point of view, fast changes in the duty cycle would pose a problem for the same reason.

In [68] a comparison of the DBSRC and DAB converters was made, considering the DAB converter as a subset of the DBSRC in which an added capacitance is used. The comparison was made for fixed frequency operation with phase shift control, with the converter characteristics being calculated for progressive increases in this capacitance, as the DBSRC transitioned towards a DAB converter. It was demonstrated that, for the same power level, increases in capacitance resulted in a larger ZVS range, a smaller current, a smaller inductance and a smaller transformer. The only advantages of using the DBSRC operated in this manner was its smaller current harmonic distortion, as expected of a resonant converter, and smaller device turn-off losses as a result of the alignment of the voltage and current.

The authors of [69] presented a bidirectional DAB using an asymmetric CLLC resonant circuit to interface between 400 V and 48 V dc buses. Switching frequency variation was used for control. They concluded that, for lowest switching losses, it was best to operate the primary inverter with ZVS and the secondary synchronous rectifier with ZCS. For forward operation this avoided the CV^2 losses at high voltages and avoided the forward recovery problems of diodes abruptly commutating large currents when the opposing transistor turns off, as would be the case for ZVS. It is unclear how the converter, with an asymmetrical CLLC network, would work in the reverse direction. The authors claimed peak efficiencies of over 96% for forward operation of the 500 W converter. Reverse efficiency figures weren't provided.

In [70] an optimisation was used to calculate the three modulation angles which would minimise the current in a DBSRC operating at a fixed frequency. A fundamental mode analysis (FMA) was used to calculate the expected values, and a 1 kW prototype converter switching at 100 kHz was used for verification. Although, as a result of the minimal current, ZVS was lost for some operating conditions, the switching losses were

tolerable and there was a significant improvement in power efficiency, compared to SPS, for a range of dc voltage ratios. A peak power efficiency of 98.3% was achieved at a power output of 500 W.

The converter of [71] had a resonant network structure similar to that of the CLL shunt inductor variant of the DBSRC, except that the LCLCL tee network was symmetrical. The 5 kW converter interfaced two 380 V dc buses, and was controlled by a switching frequency which was lower than the resonant frequency to ensure soft commutation of the output rectifiers. ZVS of the inverter switches was achieved as a result of the added lagging current caused by the shunt inductance. Network design ensured that the voltage gain was greater than one for all conditions, to prevent a reversal in the frequency control characteristic. Power efficiencies between 91% and 98% were achieved in the 10% to 100% power range.

Another symmetrical network, this time of a pi LLCL configuration, was used in [72]. Again, frequency control was used with the switching frequency less than the resonant frequency. A modified control system was used to provide sufficient voltage gain while operating over a wide range of the dc voltage ratio. It selected a smaller gate drive width in the bridge running at the relatively lower voltage, after which the frequency was adjusted to provide the desired output voltage. The bridge legs operated in a mixture of ZVS and ZCS, maintaining a reasonable compromise between switching and conduction losses. The 1 kW prototype had a maximum power efficiency of approximately 96% when operating between a 400 V dc bus and a battery having a voltage range of 75 V to 130 V. This resonant converter has a power efficiency which is approximately 5% greater than a CDAB converter over most of the power range and for varying dc link voltages.

2.6 Summary

Various bidirectional dc-dc converters have been reviewed. Their prototypes had a wide range of environments in which they were designed to operate, both in terms of their maximum power throughput and their interface voltages and the range of these voltages.

The hardware platform of the conventional DAB, comprising the two bridges with the inductor between them, had a variety of control systems applied to it, to provide improved performance over SPS modulation.

It seems that a common theme in most cases is the compromise that has to be made between the switching and the conduction losses. Soft switching usually requires an adequacy of circulating energy and therefore a limited current minimum.

There were also hardware variations, notably in the resonant versions, which had added inductors and capacitors. Although not necessarily the case, it would be anticipated that the extra hardware would increase the size and cost of such a system. Whether this were worthwhile or not would depend on other performance factors, such as the power efficiency, the size of the dc ripple currents and the power density.

The power efficiency performance of these converters varied significantly, both in value at maximum output and the range of values for other power levels. To obtain a good comparison would necessitate specifying the operating conditions in which the converter were to work; the best converter for one environment may not be the best in a different environment.

When making comparisons, another complicating factor is the range of conditions internal to the converters, such as the selection of their switching frequency, the type and choice of semiconductor switches, and the characteristics of the magnetic components used. It would be reasonable to say that better performance may be obtained by operation at lower switching frequencies or by using larger or more expensive components. Cost almost always affects performance, and will usually be a major determinant in the selection of a product. For this reason it is desirable to quantify the costs of the converters.

There are two dc-dc converter topologies proposed. They have almost zero circulating current and power, and therefore minimal conduction losses. Each consists of two full-bridge dc-dc converters with an ac link composed of a transformer and a T-type network. Although the two topologies are conceptually the same, and have many similar performance characteristics, they are also quite distinct in other respects, notably their hardware implementation. Most of the analysis for the resonant converters will be made in the frequency domain, on account of the complexity of a time domain analysis for a second order system. This contrasts with the CDAB converter, in which a single inductive element is used for energy storage, for which a time domain analysis is easily made. The next chapter presents the LCL DAB converter, which has a T-type network comprising L-C-L components.

3 The LCL DAB Resonant Converter

3.1 Introduction

In this Chapter a DAB converter with a resonant LCL network connected between the bridges is described. This topology, known as an LCL resonant DAB, is modelled and analysed in order to develop the essential equations governing its operation and characterising its performance. The analysis is initially based on a circuit comprising ideal components in which there are no losses. Later, in Chapter 5, a complete model will be used in which hardware dependencies are included to allow for power losses.

3.2 The LCL Resonant DAB Topology

The topology of the LCL resonant DAB converter is shown in Figure 3.1. It consists of two full-bridge converters, each of which operates at a fixed switching-frequency f_s, to convert its dc supply into a two level pulse-width-modulated (PWM) voltage source output. The bridges are coupled by a resonant network comprising L_1, C_1, L_2 and a high frequency transformer, Tx. The transformer provides the required galvanic isolation, and is shown here having a magnetising reactance but no leakage reactance. In practice the transformer may be designed to have a specific leakage inductance which integrates L_2 into it, rather than implementing L_2 with a separate inductor.

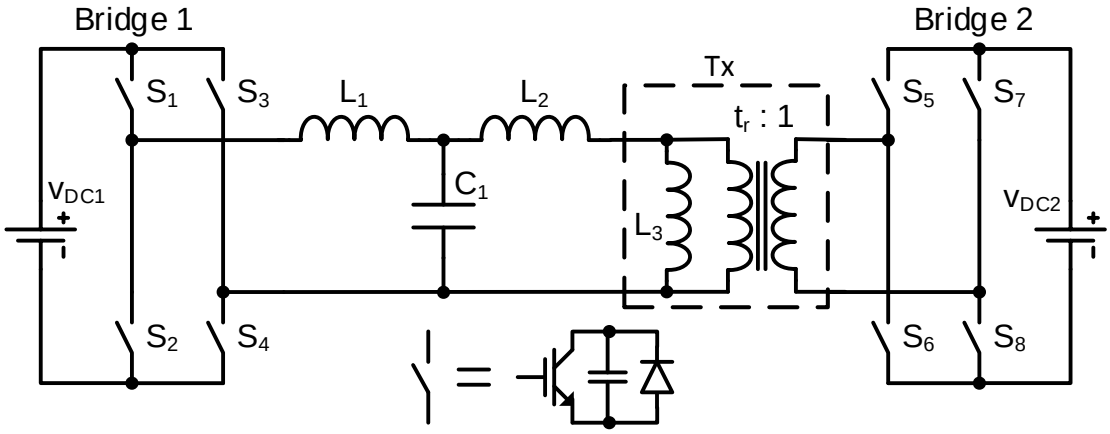


Figure 3.1: Topology of the LCL converter

If voltages V_{DC1} and V_{DC2} are dissimilar, the LCL network should be connected to the high voltage bridge; in theory it makes no difference, but it is usually more practical

to use high voltage low current components than low voltage high current components, on account of their smaller physical size.

The magnitude and direction of the power flow is controlled by varying the bridge duty cycles and the phase shift between the bridge voltages. The control of the switches is as follows: switches S_1 and S_2 of Bridge 1 are operated in anti-phase at f_s with a duty cycle of 50% to generate the voltage v_{S2} as shown in Figure 3.2. Switches S_3 and S_4 are operated in the same way, except that the switches in this leg lag those in the first leg by a displacement of α_1. The voltage v_1 driving the network in Figure 3.3 is equal to the difference between v_{S2} and v_{S4}. This control signal sequence is known as clamped-mode operation or, alternately, phase-shift PWM [73]. Thus α_1 modulates the duty cycle of v_1 in the range of 0 to 50% as α_1 changes from 0 to π radians. For $\alpha_1 = \pi$ the voltage signal is a bipolar square wave, i.e. it has only two voltage values, equal and opposite.

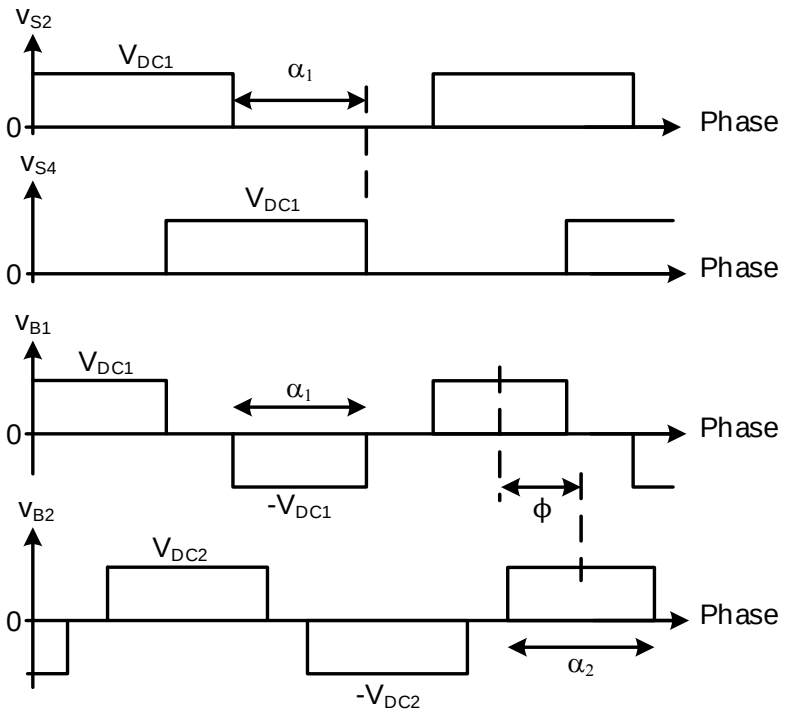


Figure 3.2: Generation of the bridge voltages

Switches S_5 to S_8 of Bridge 2 are controlled in a similar manner to those of Bridge 1 except that the phase-modulation is α_2, producing a voltage v_2 which lags that of Bridge 1 by a phase shift ϕ. This phase shift is measured between the centres of v_1 and v_2, rather than their edges, as in general α_1 and α_2 are different. In a typical system the network

voltages will have similar values, so that the required transformer turns ratio t_r will be the same as the ratio V_{DC1}/V_{DC2} of the nominal DC voltages at the input and output.

3.3 Mathematical Analysis of Operation

3.3.1 Circuit Model

Using the equivalent circuit of Figure 3.3, the converter shown in Figure 3.1 may be analysed. Transformer Tx is modelled as an ideal transformer combined with an inductor L_3, which represents the magnetizing inductance, and resistor R_3 which models the magnetising losses. For typical core permeabilities L_3 is relatively large, so that its main effect is to cause a small variation in the Bridge 2 current; it has no effect on the network voltages or currents, and will be ignored for now. Network resistances R_1 and R_2 model the losses of the inductors and the transformer. Typically the Q of a combined resistor-inductor will be greater than 100, so that the impedance differs from the inductive reactance by less than 0.005%. For this reason these resistors will be ignored for the calculation of the circuit currents which will subsequently be used to calculate the switching, conduction and resistive losses.

Before making a complete analysis, the fundamental response, which will be dominant, will be examined in the next section.

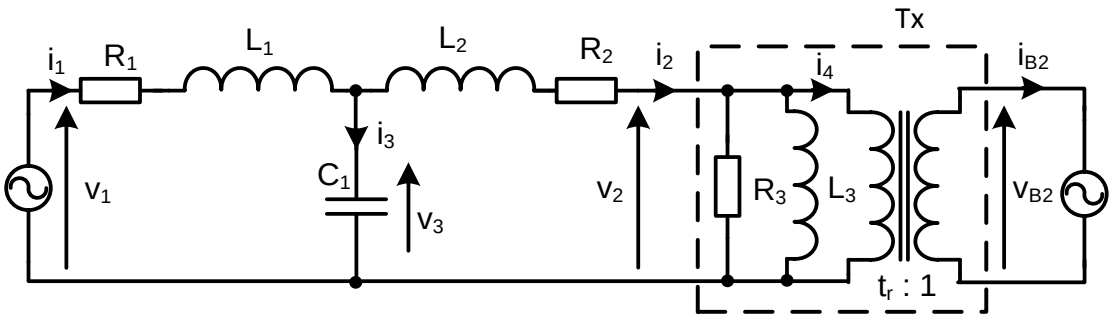


Figure 3.3: Circuit for analysis of LCL converter

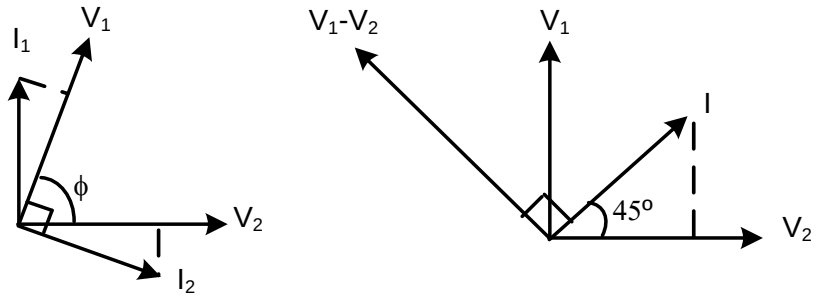
3.3.2 Operation at the Fundamental Frequency

Firstly, consider the circuit operation at the fundamental or switching frequency, the first harmonic of f_s, at which the amplitudes of v_1 and v_2, and therefore the power transfer, is largest. At this frequency the magnitudes of the reactances of L_1, C_1 and L_2 are equal, as given by (4).

$$L_1C_1 = L_2C_1 = \frac{1}{(\omega_s)^2} = \frac{1}{(2\pi f_s)^2} \quad (4)$$

By application of superposition, in which C_1 forms a parallel resonator of infinite reactance with each of L_1 and L_2 in turn, the voltage at the junction of L_1 and L_2 is equal to the vector sum of v_1 and v_2. Thereby, the voltage across L_1 is v_2 and the voltage across L_2 is v_1, so that I_1 is proportional to V_2, and I_2 is proportional to V_1, where I_1, I_2, V_1 and V_2 are the phasors corresponding to i_1, i_2, v_1 and v_2. Thus, each end of the network behaves as a current source whose value is dependent on the voltage on the opposite side.

Figure 3.4(a) shows the phasors of the fundamental frequency components for the case when V_1 leads V_2 by ϕ. Since I_1 leads V_2 by 90°, and V_1 leads I_2 by 90°, maximum forward power transfer, from source v_1 to source v_2, occurs for ϕ equal to 90°, for which phasors I_2 and V_2, and I_1 and V_1 align. In a similar way, for ϕ = -90°, when V_1 lags V_2, maximum reverse power transfer occurs and the bridge and network voltage and current pairs are in inverse phase.



(a) (b)

Figure 3.4: LCL phasors at the fundamental frequency.
(a) LCL converter (b) Conventional converter

In a CDAB converter running at full power with a phase shift of 90° and equal bridge voltages, as shown in Figure 3.4(b), there is a 45° angle between each of the voltage and current pairs, so that the transferred power is equal to the $V_1I / \sqrt{2} = V_2I / \sqrt{2}$. The bridge reactive power is greater than the transferred power by a factor of $\sqrt{2}$. It is because of the resonant converter's voltage and current phase alignment that, for a given power rating, it has full power bridge currents which are smaller than those of the CDAB converter by a factor of approximately $\sqrt{2}$.

It will be shown in the next section that the fundamental components are dominant in the power calculation, as expected in a resonant system, so that the conclusions of the fundamental analysis remain valid.

3.3.3 Power Calculation for LCL DAB

A Fourier decomposition of the ac rectangular signals v_1 and v_2 yields odd harmonics of the switching frequency, with diminishing amplitudes. To calculate the power throughput it is necessary to use a frequency domain analysis in which the components at each frequency are calculated and then summed. Voltage sources v_1 and v_2 in the model of Figure 3.3 can be derived from their Fourier series expansions of the bridge output voltage waveforms as:

$$v_1 = \frac{4V_{DC1}}{\pi} \sum_{n=1,3\ldots}^{\infty} \frac{1}{n} cos(n\omega_s t + n\phi)\, sin\frac{n\alpha_1}{2} \tag{5}$$

$$v_2 = \frac{4t_r V_{DC2}}{\pi} \sum_{n=1,3\ldots}^{\infty} \frac{1}{n} \cos(n\omega_s t)\, \sin\frac{n\alpha_2}{2} \tag{6}$$

A specific frequency component of v_1, the n^{th} harmonic, has a phasor V_1 whose RMS representation is given by:

$$V_1(n\omega_s) = \frac{4V_{DC1}}{n\pi\sqrt{2}} \sin\frac{n\alpha_1}{2} (\cos n\phi + j \sin n\phi) \tag{7}$$

Similarly, v_2 is represented by a phasor V_2 as given by:

$$V_2(n\omega_s) = \frac{4t_r V_{DC2}}{n\pi\sqrt{2}} sin\frac{n\alpha_2}{2} \tag{8}$$

Before calculation of the currents, the component values need to be considered. Since the actual values of components L_1, C_1, L_2 and L_3 may stray from their nominal values, they will be specified in terms of their ideal reactance at the switching frequency, the design reactance X_D:

$$X_{L1} = \omega_s L_1 = k_1 X_D \tag{9}$$

$$X_{L2} = \omega_s L_2 = k_2 X_D$$

$$X_{C1} = \frac{1}{\omega_s C_1} = k_3 X_D$$

$$X_{L3} = \omega_s L_3 = k_4 X_D$$

Each leg of the network ideally has the same reactance, X_D, so parameters k_1 to k_3 will ideally equal one. Parameter k_4, which determines the relative value of the magnetizing reactance and might typically have a value of approximately 10, doesn't have an effect on the Tee type network current calculations. It will be used later, when the Bridge 2 current is calculated.

For given circuit parameters, and for any particular harmonic, the current phasors, I_1 and I_2, calculated from (7) to (9) are given by:

$$I_1(n\omega_s) = \frac{j((n^2 k_2 - k_3)V_1 + k_3 V_2)}{nX_D(k_1 k_3 + k_2 k_3 - n^2 k_1 k_2)} \quad (10)$$

$$I_2(n\omega_s) = \frac{-j((n^2 k_1 - k_3)V_2 + k_3 V_1)}{nX_D(k_1 k_3 + k_2 k_3 - n^2 k_1 k_2)} \quad (11)$$

The ideal (lossless) power transfer is calculated by evaluating the real part of the product of V_1 and I_1 (or V_2 and I_2) after substitution of (7) and (8) into (10) and (11), ignoring products of dissimilar frequency components, and is given by:

$$P_i = \sum \mathrm{Re}(V_1 I_1) = P_B \sum_{n=1,3\ldots} \frac{\sin\left(\frac{n\alpha_1}{2}\right)\sin\left(\frac{n\alpha_2}{2}\right)\sin n\phi}{n^3\left(k_1 + k_2 - n^2\frac{k_1 k_2}{k_3}\right)} \quad (12)$$

Where:

$$P_B = \frac{8 t_r V_{DC1} V_{DC2}}{\pi^2 X_D}$$

In this equation the magnitude of the power flowing from V_{DC1} to V_{DC2} can be controlled by modulating the magnitudes of v_1 and v_2 with α_1 and α_2, and the direction controlled by setting ϕ to either +90°, for positive P_i values, or -90° for negative P_i values.

In this form P_B will have its normalised value of $8/\pi^2 \approx 0.8106$ for $X_D = 1\ \Omega$ and equal weighted DC supply voltages V_{DC1} and $t_r V_{DC2}$, as required for balanced network voltages v_1 and v_2, equaling 1 V.

The summation term on the right of (12) defines the effects of modulation and of variation in component values. For ideal values of L_1, C_1 and L_2, the value of the denominator increases rapidly for higher harmonics, having values of 1, 189, 2875 and 16121 at f_s, $3f_s$, $5f_s$ and $7f_s$ respectively. This shows that the fundamental is the only significant component, as expected, in view of the tuned nature of the network. At maximum modulation the summation is equal to 1.005, so that the normalized full power output is 0.8146 W; approximately 0.5% of the power is in the harmonic frequency components.

Since the power relationship given in (12) is a summation rather than an analytic expression, its power variation as a function of modulation and its sensitivity to component variations will be investigated by numeric methods. A MATLAB program was used to evaluate (12) for Monte Carlo variations of parameters k_1 to k_3 in the range 0.9 to 1.1 to represent ± 10% variations in L_1, C_1 and L_2 from their ideal values. For the purpose of these tests the phase-shift ϕ was set to 90° and equal bridge modulation values were used. Figure 3.5 shows the resulting minimum and maximum values of the normalised power.

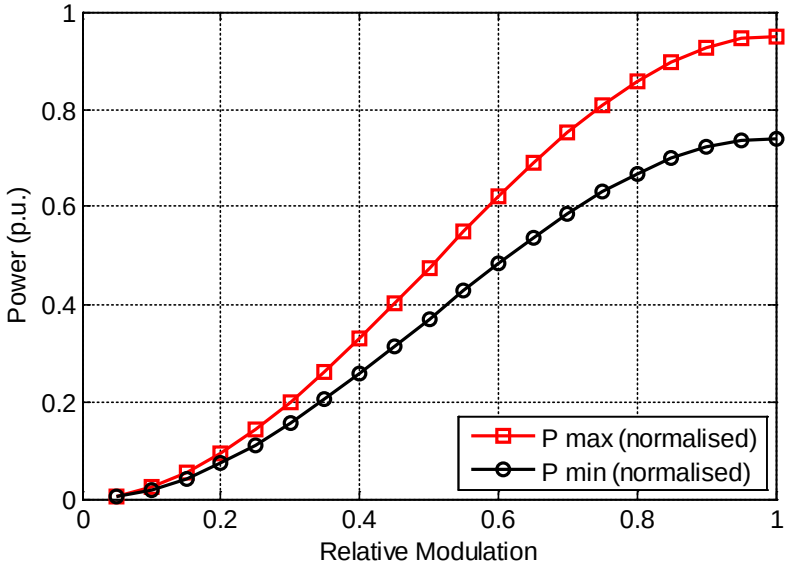


Figure 3.5: LCL power range for component variations

At maximum modulation the power value variation is approximately -9% to +17%, showing that the converter is not unusually sensitive to component variations. For a given power an imbalance in V_{DC1} and V_{DC2} affects the harmonic content of the bridge currents.

The relative harmonic content of the currents has an influence on the magnetizing and resistive losses in the magnetic components; higher frequencies cause a resistance increase by the eddy current loss mechanism, and increase the core losses in the magnetic components. Figure 3.6 shows the total harmonic distortion (THD) of the network input and output currents for varying modulation levels. The THD was calculated by (13), where i_f is the current fundamental value and i_{rms} is the total rms value. These results were obtained for a tuned system having matched bridge dc voltages and equal modulation values m_1 and m_2. It can be seen that there is a minimum at a relative modulation of 2/3,

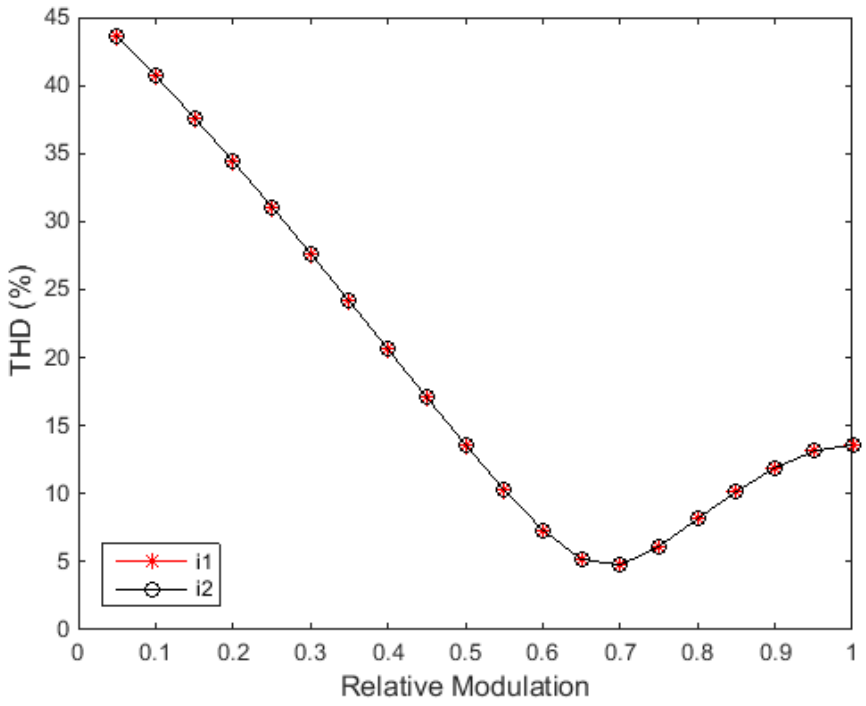


Figure 3.6: LCL percentage THD in currents i_1 and i_2

at which there is no 3rd harmonic because there is a Fourier series null. At 10% of full scale power transfer, the smallest level expected, which occurs with 20% modulation, the distortion level is approximately 35%, at which the value of the current fundamental is 94% of the total current.

$$THD\ (\%) = 100\sqrt{1 - \left(\frac{i_f}{i_{rms}}\right)^2} \qquad (13)$$

Of interest is the variation of the harmonic composition of the power and currents with modulation, as shown in Table 3.1. This normalised data was obtained for a system with matched supply voltages and components, $\phi = 90°$ and $m_1 = m_2$. Practically all the power is in the fundamental, particularly so for higher modulation levels. There is a very small additive contribution of power from the 3rd harmonic, and an even smaller subtractive contribution from the 5th harmonic. Higher harmonics are insignificant. The same trends apply to the currents; although i_1 only is shown here, i_2 is identical and i_4, the current remaining after the magnetising current has been subtracted, is very similar.

Mod^n	Power			i_1		
	Frequency			Frequency		
	f_1	$3f_1$	$5f_1$	f_1	$3f_1$	$5f_1$
0.1	0.0198	0.0009	-0.0001	0.1408	0.0094	0.0023
0.2	0.0774	0.0028	-0.0003	0.2782	0.0152	0.0024
0.3	0.1671	0.0042	-0.0001	0.4087	0.0155	0.0008
0.4	0.2800	0.0039	-0.0000	0.5292	0.0112	0.0000
0.5	0.4053	0.0021	-0.0001	0.6366	0.0052	0.0006
0.6	0.5305	0.0004	-0.0003	0.7284	0.0009	0.0010
0.7	0.6435	0.0001	-0.0001	0.8022	0.0002	0.0004
0.8	0.7332	0.0015	-0.0000	0.8563	0.0027	0.0000
0.9	0.7907	0.0034	-0.0001	0.8892	0.0059	0.0004
1	0.8106	0.0043	-0.0003	0.9003	0.0073	0.0008

Table 3.1: LCL power and i_1 harmonic content

3.3.4 Calculation of the RMS Quantities for LCL Converter

For the calculation of the resistive and magnetising losses, the rms current and voltage values are required. Their calculation is shown in the following sections.

RMS Current

The currents into and out of the T-type network in Figure 3.3, i_1 and i_2 respectively, are given by (10) and (11). Their rms magnitudes may be calculated from a frequency domain summation of their individual components.

$$\bar{i}_1 = \frac{4}{\pi X_D \sqrt{2}} \sqrt{\sum_{n=1,3\ldots} \left(\frac{(N_1)^2 + (N_2)^2}{D^2} \right)} \tag{14}$$

Where: $D = n^2(k_1k_3 + k_2k_3 - k_1k_2n^2)$

$N_1 = (\mathrm{k_3} - \mathrm{k_2 n^2}) V_{\mathrm{DC1}} \sin\frac{n\alpha_1}{2} \sin n\phi$

$N_2 = \mathrm{k_3} t_r V_{DC2} \sin\frac{n\alpha_2}{2} - (\mathrm{k_3} - \mathrm{k_2 n^2}) V_{DC1} \sin\frac{n\alpha_1}{2} \cos n\phi$

and,

$$\bar{i}_2 = \frac{4}{\pi X_D \sqrt{2}} \sqrt{\sum_{n=1,3\ldots} \left(\frac{(N_3)^2 + (N_4)^2}{D^2} \right)} \tag{15}$$

Where: $N_3 = \mathrm{k_3} V_{DC1} \, sin\frac{n\alpha_1}{2} \, sin\, n\phi$

$N_4 = (\mathrm{k_3} - \mathrm{k_1 n^2}) t_r V_{DC2} \, sin\frac{n\alpha_2}{2} - \mathrm{k_3} V_{DC1} \, sin\frac{n\alpha_1}{2} \, cos\, n\phi$

Current i_4, as shown in Figure 3.3, and its transformed value i_{B2} are given by:

$$\mathrm{i_4} = \mathrm{i_2} - \mathrm{i_{L3}} = \mathrm{i_2} + \frac{\mathrm{j} v_2}{\mathrm{k_4 X_D}} \tag{16}$$

$$\mathrm{i_{B2}} = t_r \mathrm{i_4} \tag{17}$$

Their rms values are:

$$\bar{i}_4 = \frac{4}{\pi X_D \sqrt{2}} \sqrt{\sum_{n=1,3\ldots} \left(\frac{(N_3)^2 + (N_5)^2}{D^2} \right)} \tag{18}$$

$$\bar{i}_{B2} = t_r \bar{I}_4 \tag{19}$$

Where: $N_5 = \mathrm{N_4} + (D / \mathrm{k_4}) t_r V_{DC2} \sin\frac{n\alpha_2}{2}$

RMS Voltage

For ease of use, it is convenient to use bridge relative-modulation indices φ, m_1 and m_2 instead of the modulation angles ϕ, α_1 and α_2:

$$\varphi = \phi/\pi \tag{20}$$

$$m_1 = \alpha_1/\pi$$

$$m_2 = \alpha_2/\pi$$

Although the rms magnitudes of the network voltages v_1 and v_2 may be calculated in the frequency domain by taking the rms sum of their respective components, they are easily calculated in the time domain:

$$\overline{V}_1 = V_{DC1}\sqrt{m_1}$$

$$\overline{V}_2 = t_r V_{DC2}\sqrt{m_2} \tag{21}$$

For the LCL converter, the standard modulation used to control the converter will comprise a fixed ϕ of $\pm 90°$ and equal bridge modulations m_1 and m_2. The per-unit values of the rms voltage, rms current and power are plotted in Figure 3.7, for variations in the modulation. The voltage and current variations approximate to square root and sine functions respectively, whereas the power has the expected sine squared function of modulation.

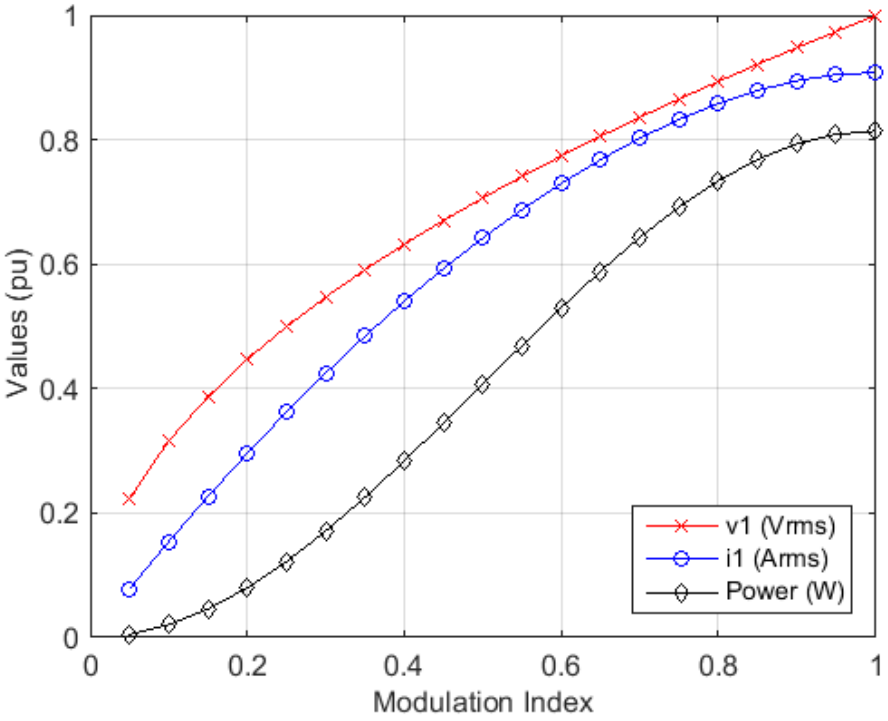


Figure 3.7: Voltage, current and power trends in LCL DAB converter

3.3.5 Switching Points and ZVS Range of LCL Converter

The switching points of the transistors are needed for the switching and conduction power loss calculations. The switching energy loss of a leg is determined by the magnitude and polarity of the leg current at the switching instant. A bridge leg has zero voltage switching (ZVS) status if its switches turn on at a negative current value, that is, their anti-parallel diodes conduct prior to their transistors. The switching points also define the conduction band for each transistor, in which the calculation of the conduction losses takes place.

The switching instances of the four switches S_2 to S_8 at the bottom of each leg are shown in Table 3.2 and Figure 3.8. Their complementary switches at the top of each leg, S_1 to S_7 respectively, have identical waveforms, albeit displaced by half a cycle. Switches S_1 and S_2 in Bridge 1, and S_5 and S_6 in Bridge 2, are in the leading legs, as shown in Figure 3.2.

Switch	On	Off
S_2	C	A
S_4	D	B
S_6	G	E
S_8	H	F

Table 3.2: Switching points of the bridge legs

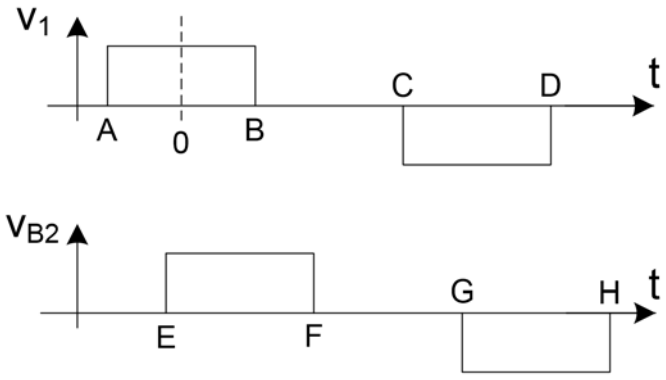


Figure 3.8: Bridge voltage switching points

Using these, and referring to Figure 3.2, the angles for the switching instances are shown in the following equations, for which the modulations have been defined in (20). As a numeric calculation will make use of these, they have been converted to indices, where one cycle, 2π radians, is represented by ‘tics’ points:

$$
\begin{aligned}
\mathrm{A} &= -\frac{\mathrm{tics}}{2\pi}\left(\frac{m_1\pi}{2}\right) = -\frac{\mathrm{tics}}{4}(m_1) \\
\mathrm{B} &= \frac{\mathrm{tics}}{2\pi}\left(\frac{m_1\pi}{2}\right) = \frac{\mathrm{tics}}{4}(m_1) \\
\mathrm{C} &= \frac{\mathrm{tics}}{2\pi}\left(\pi - \frac{m_1\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2 - m_1) \\
\mathrm{D} &= \frac{\mathrm{tics}}{2\pi}\left(\pi + \frac{m_1\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2 + m_1) \\
\mathrm{E} &= \frac{\mathrm{tics}}{2\pi}\left(\varphi\pi - \frac{m_2\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2\varphi - m_2) \\
\mathrm{F} &= \frac{\mathrm{tics}}{2\pi}\left(\varphi\pi + \frac{m_2\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2\varphi + m_2) \\
\mathrm{G} &= \frac{\mathrm{tics}}{2\pi}\left(\pi + \varphi\pi - \frac{m_2\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2\varphi + 2 - m_2) \\
\mathrm{H} &= \frac{\mathrm{tics}}{2\pi}\left(\pi + \varphi\pi + \frac{m_2\pi}{2}\right) = \frac{\mathrm{tics}}{4}(2\varphi + 2 + m_2)
\end{aligned}
\tag{22}
$$

To ensure that the indices have positive values, as φ may be negative, negative values need to be wrapped by one period.

Switching Modes and ZVS Range of LCL Converter

To get a broad impression of the switching characteristics of the legs their ZVS range will be determined. For a symmetric control of the leg switching, the two transistors in a leg have the same switching status, namely either ZVS or zero current switching (ZCS), according to the current polarity at the switching instant. Accordingly, the ZVS status of each of the four bridge legs may be determined by evaluating the switching current of a transistor in each of those legs.

For a *dcr* value of 1 and a φ value of 0.5 there are two possible switching modes. For most modulation values the converter operates in Mode A, as illustrated in Figure 3.9, which shows the Bridge 1 current i_1 and voltage v_1 for m_1 and m_2 values of 0.7. The waveforms for Bridge 2 are similar, except that they are lagging a quarter of a cycle. Each of the switching regions at t_1 to t_4 includes a narrow dead-band and therefore comprises two actions, namely the switching off of a leg transistor and then the switching on of the

complementary device. Switches S_1 and S_4 are on prior to t_1, followed by S_1 and S_3 up to t_2, S_2 and S_3 up to t_3 and S_2 and S_4 up to t_4, after which the sequence repeats. In this mode of operation, at t_1 S_4 is switched off and S_3's diode commutates the positive i_1 current from S_4. S_3 receives gate drive at the end of the dead-band, and turns on with a ZVS transition when the current changes direction at the next crossing, at which point S_3's diode turns off naturally. At t_2 S_1's gate is turned off and its diode, which has been carrying the negative current since S_1's natural commutation with ZCS, is forced off when S_2 turns on at the end of the dead-band. The transition at t_3, at which S_3 turns off and S_4 turns on, is similar to the leg 2 transition at t_1. The transition at t_4, at which S_2 turns off and S_1 turns on, is similar to the leg 1 transition at t_2.

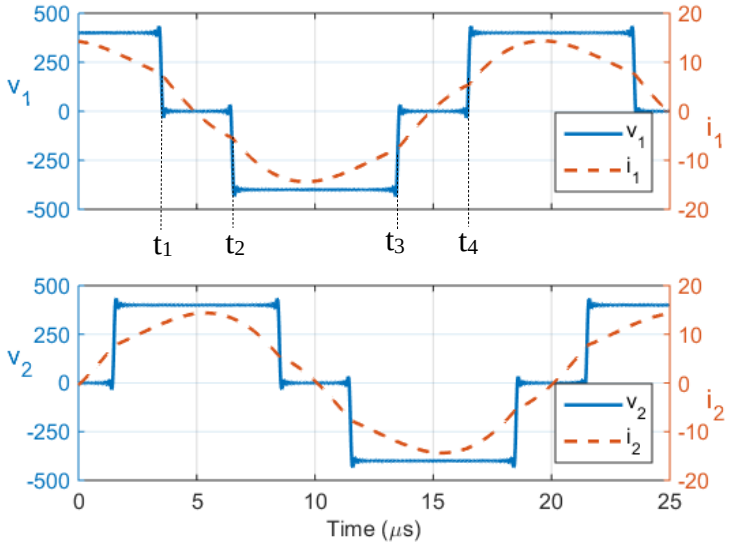


Figure 3.9: Bridge 1 switching of LCL converter for m = 0.7

Operation in Mode B occurs for m_1 and m_2 values greater than 0.92, as illustrated in Figure 3.10 for maximum modulation. In this mode all bridge legs switch with ZVS.

Since the bridge currents, which are dominated by their fundamental components, are in alignment with the bridge voltages, the LCL converter is almost unaffected by changes in the dcr. Changes in component values, the amplitude modulation level and the dcr value mainly affect the magnitudes of the currents. This is in contrast to a CDAB converter, for which the ZVS boundaries are very dependent on the dcr value, as shown in Figure 1.4. A MATLAB program, *lcl_zvs_rng* in Appendix A, was used for the tests in which the bridge modulations m_1 and m_2 were equal and Bridge 1 led Bridge 2 by 90°. Figure 3.11 shows the minimum, or worst-case, switching current values which occur in each leg for a variation in the dc voltage conversion ratio (dcr) from 0.7 to 1.4 and for ±

10% Monte-Carlo component variations. The current directions are chosen so that a positive current value indicates ZVS, that is, the transistor's diode has a forward current at the switching instant.

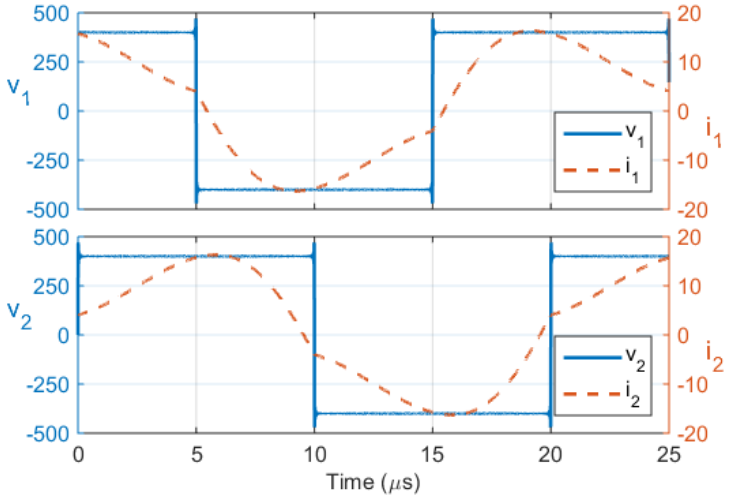


Figure 3.10: Bridge 1 switching of LCL converter for m = 1

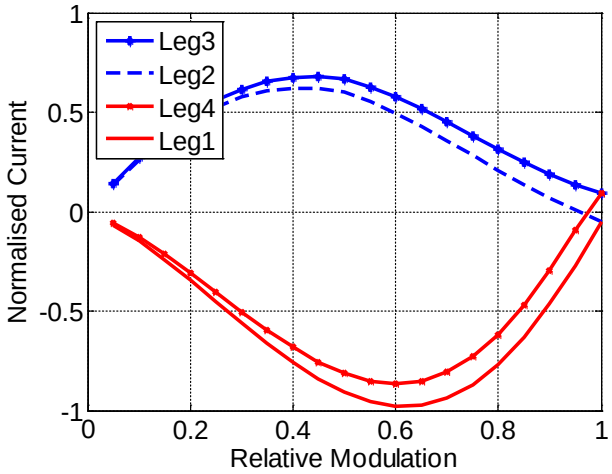


Figure 3.11: LCL minimum leg currents at the switching points

From Figure 3.11 it is apparent that, for most modulation values, the leading leg of the lagging bridge (Leg 3, switches S_5 and S_6) and the lagging leg of the leading bridge (Leg 2, switches S_3 and S_4) have ZVS for most modulation values, while the other two legs don't have ZVS. Similar results are obtained for reverse operation.

The ZVS characteristics and switching information will be made use of in the calculation of the switching and conduction losses in Chapter 5.

Power Flow of LCL Converter

Figure 3.12 shows the instantaneous power flow of the 4 kW converter at maximum throughput. The negative area in the plot, corresponding to the reverse power flow, is a very small fraction of the forward power. In contrast, Figure 3.13 shows the instantaneous power flow of a 4 kW CDAB running at maximum power; the reactive power is significant, and the instantaneous power has a larger peak value. A reduction in the reactive power component has many benefits; there are smaller peak and rms currents in the bridge transistors, smaller rms currents in the transformer ac link and smaller rms currents in the dc link capacitors.

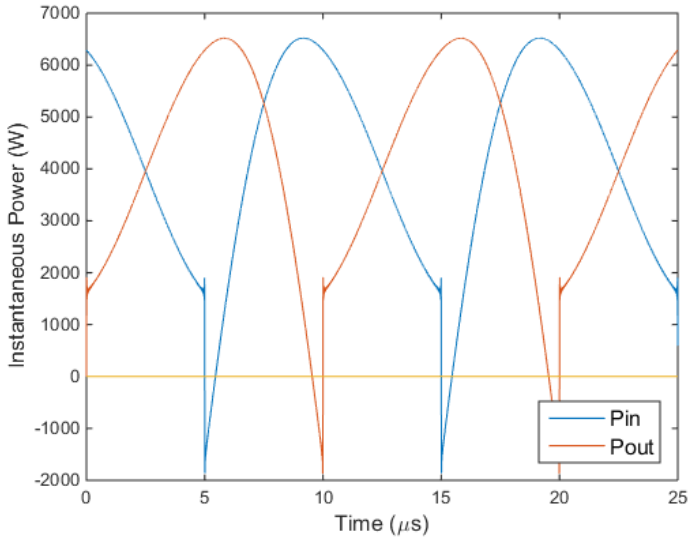


Figure 3.12: Power flow of LCL converter for 100% modulation

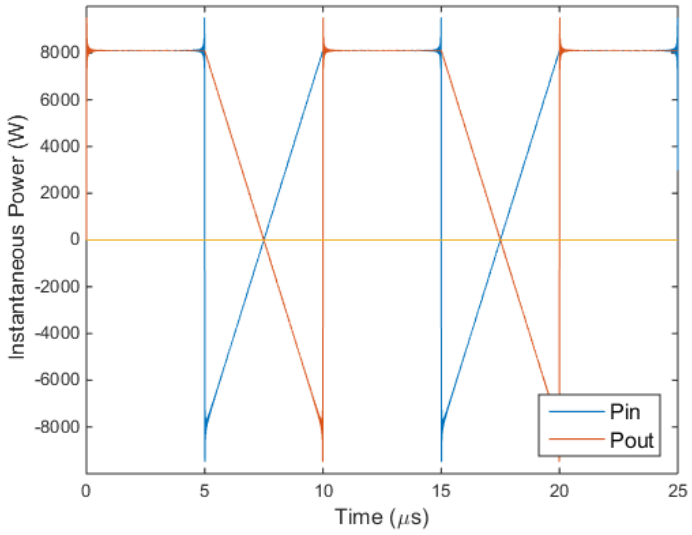


Figure 3.13: Power flow of CDAB for 100% modulation

3.4 Theoretical Performance of Lossless LCL Converter

Previous sections have shown how the power, voltage and current frequency components may be calculated for a lossless system. As an analytic approach was not possible, numeric techniques were used to perform all calculations, using equations (9) to (12) and (22). A MATLAB program, *lcl_dab_2igbt* in Appendix A, was used to perform the following operations, in order. Firstly, the circuit voltage and current phasors were calculated, based on the circuit of Figure 3.3, ignoring R_1, R_2 and R_3. From the frequency domain phasors, all time domain voltages and currents are calculated, with each cycle being divided into 'tics' points. This calculation is performed by the summation of the individual frequency components, corrected for the varying phasor sweep rates, as illustrated in the following example:

$$i_1(t) = \sum_{n=1,3\ldots} I_{1nMag}\, cos(I_{1nPh} + n\omega_s t) \tag{23}$$

Where:

I_{1nMag} is the magnitude of the nth harmonic component of phasor I_1

I_{1nPh} is the phase of the nth harmonic component of phasor I_1

The lossless, or ideal power P_i is then calculated; a negative value indicates a reverse power transfer. After the switching indices have been calculated, from (22), the transistor currents are calculated, each in a half cycle conduction band. The dc, rms, ac rms, minimum and maximum dc currents for each bridge are derived from the transistor currents.

A prototype was designed to provide a maximum power throughput of 4 kW when running from equal dc link voltages of 400 V. For this power, with a transformer nominal turns ratio t_r equal to 1, it is calculated, from (12), that the design reactance X_D is required to be 32.5 Ω. Choosing a design reactance of 31.83 Ω at the chosen switching frequency of 50 kHz will enable the capacitor C_1 to take a standard nominal value of 100 nF, and will also provide a slightly higher output power. Using this design, the converter's theoretical performance was examined using the MATLAB program, in which the maximum value of n, the harmonic number, was set to 99, so that 50 frequency components are used.

Plots of the bridge voltage and current waveforms, for $m_1 = m_2 = 1$ and $\phi = 90°$ are shown in Figure 3.14, for which there is a forward power throughput of 4 kW.

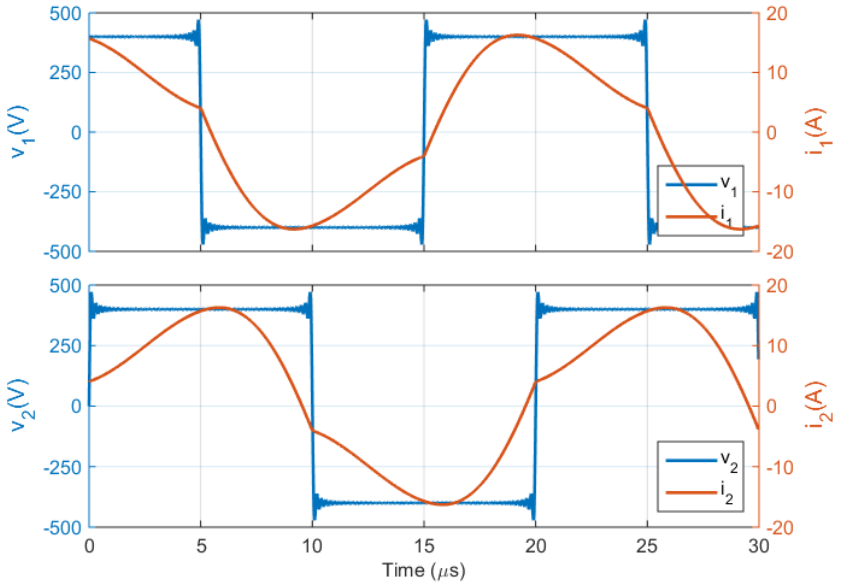


Figure 3.14: LCL bridge voltages and currents at 100% forward modulation

The bridge currents are approximately sinusoidal and in phase with their respective voltages. This indicates that the reactive power transfer between the bridges and the LCL resonant network is close to zero, and therefore that the bridge currents have minimal values. It may be noticed that the bridge voltage signals show slight ringing at their transitions, as per Gibb's phenomenon [74], as a result of the limited number of frequency components used in the calculation process.

Reverse operation at maximum modulation yields similar results, as shown in Figure 3.15, except that the bridge currents are in anti-phase with their respective voltages:

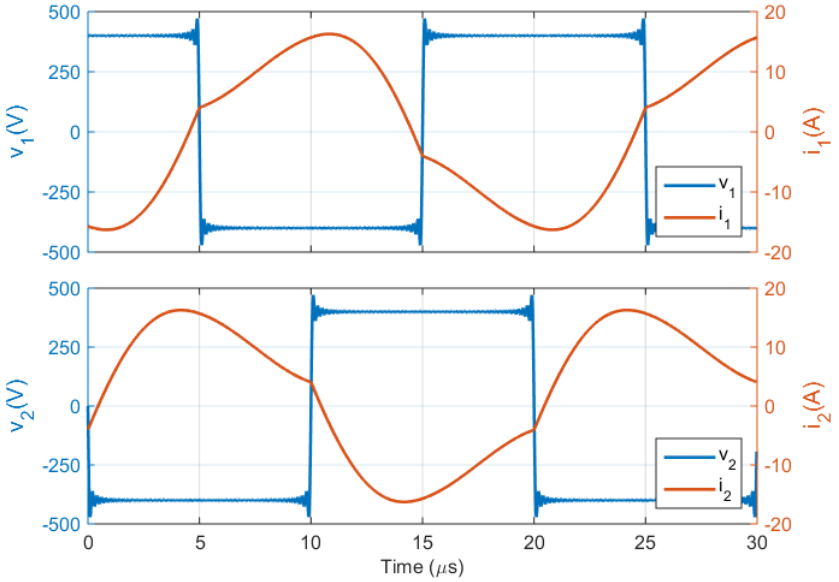


Figure 3.15: LCL bridge voltages and currents at 100% reverse modulation

Figure 3.16 show the results for 70% forward modulation. The current waveforms strongly resemble sinusoids – the modulation is close to the value of 2/3 which results in a null in the 3rd harmonic of the bridge voltages. This was seen in the minimum at this point in the current total-harmonic-distortion (THD) plot of Figure 3.6.

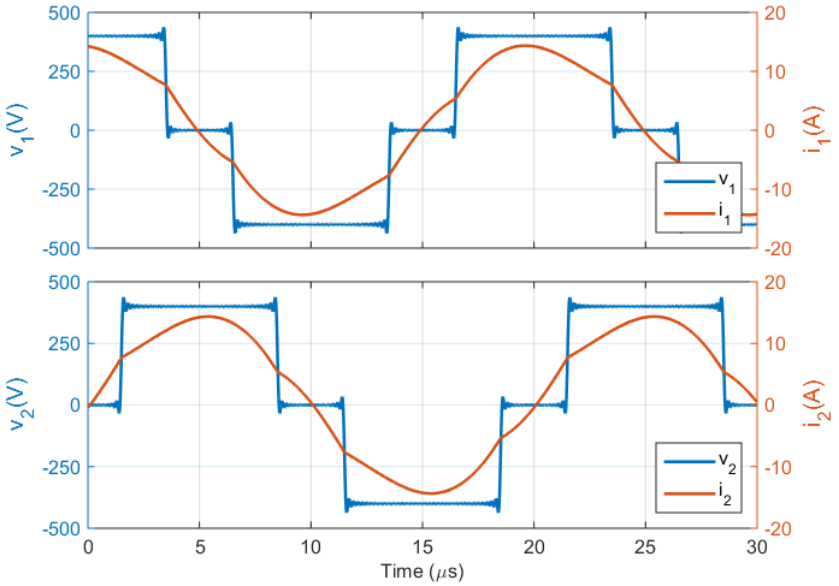


Figure 3.16: LCL bridge voltages and currents at 70% forward modulation

These theoretical waveforms, obtained from the frequency domain calculations using the first 50 harmonic components, are similar to those predicted by the fundamental analysis. The current waveforms consist of the dominant fundamental component which

is distorted by relatively small residual frequency components, namely the 3^{rd}, 5^{th} and higher harmonics.

The next Chapter will present the theory for the CLC DAB resonant converter. In terms of a fundamental frequency analysis, it is very similar to the LCL converter, but its hardware and performance are quite different.

4 The CLC DAB Resonant Converter

4.1 Introduction

In theory the T-type network for this converter comprises the dual of the LCL, a CLC, hence the name. These two networks are conceptually similar and behave in a similar manner; at the fundamental frequency, each of their T-type networks has reactances in each of its three legs which are equal to the design reactance X_D of the system.

In a practical implementation of the CLC network, the addition of L_1 in Figure 4.2 is required to prevent a capacitive connection between voltage sources v_1 and v_2, which have abruptly changing voltages.

The motivation for the use of the CLC topology is the reduced size of the inductive components; the network's central inductor may be implemented as the magnetising reactance of the transformer. Also, the capacitively coupled bridge connections block any dc bias, which may arise from control asymmetry, from being applied to the transformer.

4.2 The CLC Topology

The topology of the CLC resonant DAB converter is shown in Figure 4.1. There are two full-bridge converters, each of which operates at a fixed f_s, and outputs a two level pulse width modulated voltage source from its dc supply. The bridges are coupled with a resonant network comprising C_1, C_2 and transformer Tx, which also provides galvanic

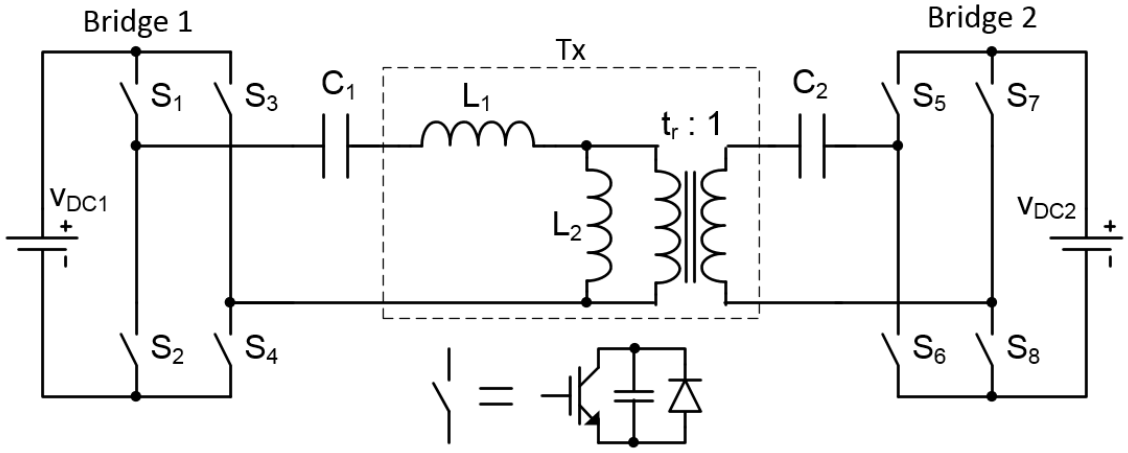


Figure 4.1: Topology of the CLC DAB converter

isolation. The transformer has leakage and mutual inductances L_1 and L_2 which are an integral part of the resonant network, and which are tuned to the fundamental of the switching frequency. An alternative implementation would use a transformer with minimal leakage reactance with the balance being placed in a separate series inductor L_1.

The bridge voltage waveforms are generated in the same manner as they were for the LCL converter, as per Figure 3.2. It can be seen that the opposite polarity of ϕ will apply in the phasor diagrams and the mathematics which follows, namely that a negative value of ϕ will result in a forward power throughput. The standard modulation used to control the converter will comprise a fixed ϕ of $\pm 90°$ and equal bridge modulations m_1 and m_2.

4.3 Mathematical Analysis

4.3.1 Circuit Model

The model of the circuit to be analysed is shown in Figure 4.2. Here C_2' is the reflected value of C_2, relocated to the left of the transformer. The network voltage source v_2 is derived from the bridge voltage v_{B2}, scaled by the transformer turns ratio. Copper losses in the transformer are modelled by resistors R_1 and R_2, and the magnetising losses by resistor R_3. For the analysis given in this section these will be ignored. This is justified by the very small influence the transformer losses exert on the circuit currents.

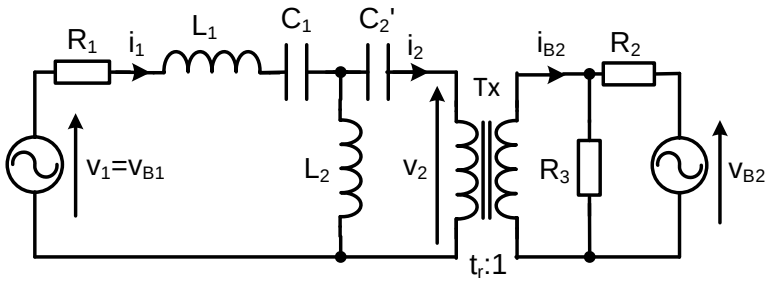


Figure 4.2: CLC circuit for analysis

4.3.2 Operation at the Fundamental Frequency

Firstly, consider the circuit operation at the fundamental frequency, at which the power throughput is largest. At this frequency the reactances of each leg of the T-type network are equal:

$$X_{C_1} - X_{L_1} = X_{C_1}\text{net} = X_{L_2} = X_{C_2}{}' = t_r{}^2 X_{C_2} \qquad (24)$$

$$(L_1 + L_2)C_1 = \frac{L_2 C_2}{{t_r}^2} = \frac{1}{\omega_s^2} = \frac{1}{(2\pi f_s)^2}$$

By the application of superposition, in which L_2 forms a parallel resonator of infinite reactance with each of the other legs in turn, the voltage across L_2 has is equal to the vector sum of v_1 and v_2. As a result, the voltage across the leg C_1L_1, which behaves as a capacitor with a net capacitance of C_1net, is v_2 and the voltage across C_2' is v_1. Thus, each end of the network behaves as a current source whose value is dependent on the voltage on the opposite side. In Figure 4.3 it can be seen that when the converter is operated in the forward direction with ϕ equal to -90° the currents and voltages align so that there is no reactive power, thereby minimizing the bridge currents, as shown previously for the LCL converter. The same applies for ϕ equal to 90°, for power transfer in the reverse direction. The strategy for control of the converter is to use PWM of the bridge voltages with equal values of α_1 and α_2 to control the magnitude of the power flow, as was done for the LCL converter. The phase shift ϕ between the bridges will be fixed at -90° or 90°, for forward and reverse operation respectively.

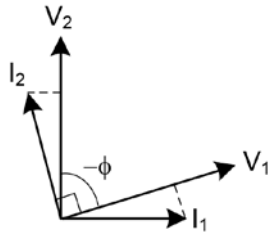


Figure 4.3: CLC fundamental network phasors

It will be shown in the next section that the fundamental components are dominant in the power calculation, as expected in a resonant system, so that the conclusions of the fundamental analysis presented here remain valid.

4.3.3 Power Calculation for CLC Converter

The network voltages generated by the two full-bridge converters are the Fourier series expansions given previously in equations (5) and (6). Their phasors, equations (7) and (8), are also as given for the LCL converter.

Four parameters will be used to make allowance for any component variations from their ideal values:

$$\begin{aligned} X_{L1} &= \omega_s L_1 = k_1 X_D \\ X_{C1} &= \frac{1}{\omega_s C_1} = k_2 X_D \\ X_{L2} &= \omega_s L_2 = k_3 X_D \\ X_{C2} &= \frac{1}{\omega_s C_2} = \frac{k_4 X_D}{{t_r}^2} \end{aligned} \tag{25}$$

At f_s the reactance of each leg of the T-type network is ideally equal to the design reactance, X_D, which is a major determinant in the converter's required power throughput. For a given value of X_D and f_s, the desired values of L_2 and C_2 are therefore known; parameters k_3 and k_4 will ideally equal 1.

The selection of components L_1 and C_1 is less straightforward: Since the difference between the values of X_{C1} and X_{L1} is X_D, there is a degree of freedom in the choice of L_1. There are several factors influencing the choice of L_1's value, some of which will be discussed later in this section; the value of k_1 will usually be in the range 0.6 to 1. After L_1's value has been determined by k_1, it follows that the value of parameter k_2 will ideally equal 1+ k_1, in order to obtain a net leg reactance equal to X_D.

For these parameters, and for any particular harmonic, the corresponding i_1 and i_2 current phasors, I_1 and I_2, are given by:

$$I_1(n\omega_s) = \frac{j(n^3 k_3(V_1 - V_2) - n k_4 V_1)}{X_D(n^2(k_1 k_4 + k_2 k_3 + k_3 k_4) - k_2 k_4 - n^4 k_1 k_3)} \tag{26}$$

$$I_2(n\omega_s) = \frac{j\left(n k_2 V_2 - n^3(k_1 V_2 + k_3(V_2 - V_1))\right)}{X_D(n^2(k_1 k_4 + k_2 k_3 + k_3 k_4) - k_2 k_4 - n^4 k_1 k_3)} \tag{27}$$

The ideal, or lossless power transfer P_i is calculated by evaluating the real part of the product of V_1 and I_1 (or V_2 and I_2) after substitution of (7), (8) and (25) into (26) and (27), extracting products of similar frequency components, and is given by:

$$\begin{aligned} P_i &= \sum \mathrm{Re}(V_1 I_1)\, P_i \\ &= P_B \sum_{n=1,3\ldots} \frac{n k_3 \sin\left(\frac{n\alpha_1}{2}\right) \sin\left(\frac{n\alpha_2}{2}\right) \sin(-n\phi)}{(n^2(k_1 k_4 + k_2 k_3 + k_3 k_4) - k_2 k_4 - n^4 k_1 k_3)} \end{aligned} \tag{28}$$

Where:

$$P_B = \frac{8 t_r V_{DC1} V_{DC2}}{\pi^2 X_D}$$

In (28) the magnitude of the power flowing from V_{DC1} to V_{DC2} can be controlled by varying α_1 and α_2, which modulate the magnitudes of v_1 and v_2, and the direction controlled by setting ϕ to either -90°, for positive values of P_i, or +90° for negative values of P_i.

In this form the constant P_B will have a normalised value of $8/\pi^2 \approx 0.8106$ for equal weighted dc supply voltages V_{DC1} and $t_r V_{DC2}$ of 1 V, and for an X_D value of 1 Ω. For equal bridge modulations α_1 and α_2, the summation term in (28) is approximately a sine squared function of modulation whose only significant harmonic component is the third harmonic, the magnitude of which depends on the value of parameter k_1. Figure 4.4 shows the current variations with modulation for a converter operated with ϕ = 90° and equal bridge modulations.

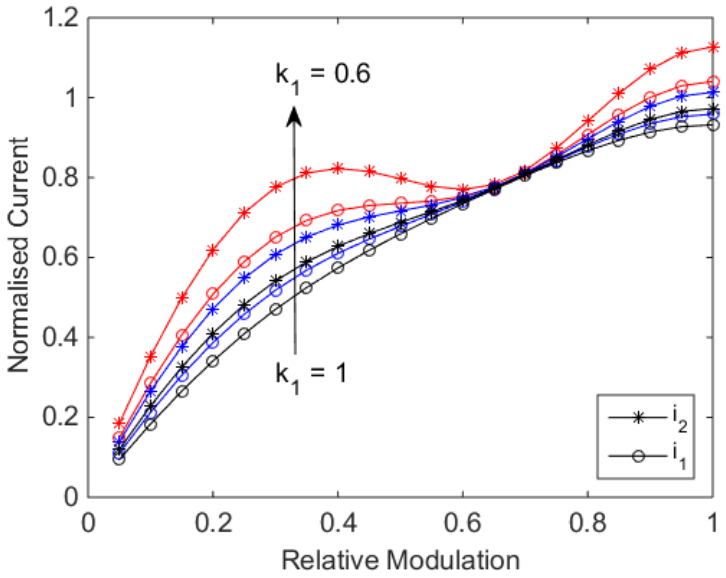


Figure 4.4: Effect of relative L_1 value

It can be seen that small values of k_1 result in an increase in the bridge currents, as the 3rd harmonic component is accentuated. This effect is greatest for relative modulations of 1/3, for which the contribution from the 3rd harmonic component is largest. Conversely, it can be seen that the 3rd harmonic has no effect at a relative modulation of 2/3, for which there is a Fourier series null. Series resonance causes a pole in the denominator of (26) -

(28) at $k_1 = 17/64$, placing a lower limit on the value of k_1, the value of the series inductor L_1 relative to the design reactance X_D.

Figure 4.5 shows the total harmonic distortion of the network input and output currents for varying modulation levels, for k_1 values from 0.6 to 1. The THD was calculated by (13). These results were obtained for a tuned system having matched bridge dc voltages and equal modulation values m_1 and m_2. The THD has a minimum at a relative modulation of 2/3, as for the LCL converter. The distortion level is higher than that of the LCL converter, as expected, because of the capacitive coupling of the high frequency components by C_1 and C_2. It is notable that a 50% THD occurs when the value of the current fundamental is 87% of the total current. The THD is larger for smaller values of k_1, because of the accentuated 3rd harmonic, as previously explained. The THD is also larger for i_2 than for i_1, because of the additional current flow through L_2. At high frequencies L_1 acts as though it is connected between the two sources, whereas L_2 is effectively driven by v_2. This mechanism also explains why the THD of the CLC DAB converter is greater than that of the LCL DAB converter.

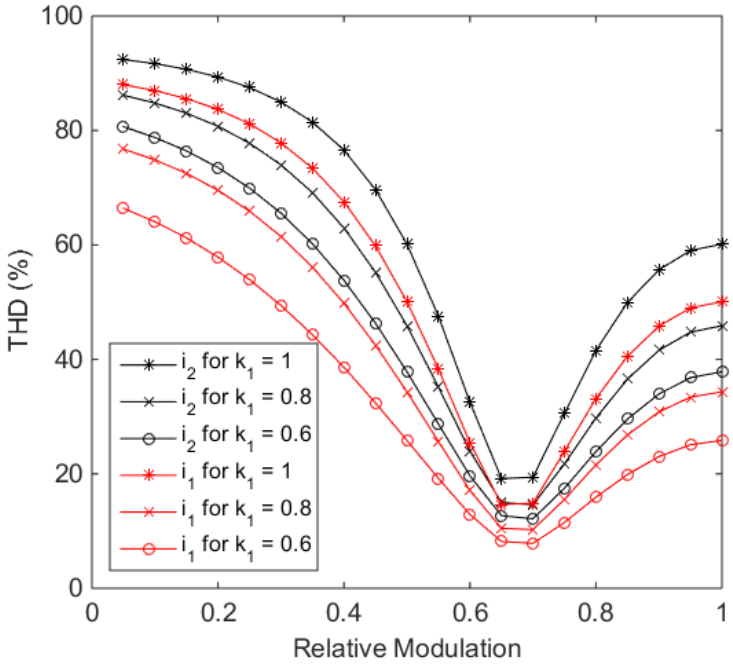


Figure 4.5: CLC percentage THD in currents i_1 and i_2

The variation of the harmonic composition of the power and currents with modulation is shown in Table 4.1. This normalised data was obtained for a system with matched supply voltages and components, $k_1 = 0.8$, $\phi = -90°$ and $m_1 = m_2$. Although most of the power transfer occurs at the fundamental frequency, particularly at higher

modulation levels, there is a larger harmonic content than for the LCL converter. There is a small addition of power by the 3rd harmonic, and a smaller subtraction by the 5th harmonic. Higher harmonics are generally not significant. The 3rd harmonic dominates in the currents. It is relatively more significant at low modulation levels, particularly in i_2. If the data in Table 4.1 were generated for a k_1 value of 0.6, there would be a relatively higher harmonic content; conversely, for a k_1 value of 1, the harmonic content would reduce. The balance to be struck in the selection of the value of k_1 is between the larger currents and THD which occur for small values, and the size, and therefore cost of L_1 for larger values of k_1.

Mod^n	Power			i_1			i_2		
	Frequency			Frequency			Frequency		
	f_1	$3f_1$	$5f_1$	f_1	$3f_1$	$5f_1$	f_1	$3f_1$	$5f_1$
0.1	0.020	0.015	-0.005	0.141	0.061	0.007	0.141	0.106	0.012
0.2	0.077	0.047	-0.010	0.278	0.100	0.008	0.278	0.178	0.013
0.3	0.167	0.069	-0.005	0.409	0.106	0.003	0.409	0.193	0.005
0.4	0.280	0.064	-0.000	0.529	0.080	0.000	0.529	0.150	0.000
0.5	0.405	0.036	-0.005	0.637	0.038	0.002	0.637	0.074	0.004
0.6	0.531	0.007	-0.010	0.728	0.007	0.004	0.728	0.013	0.008
0.7	0.644	0.002	-0.005	0.802	0.002	0.002	0.802	0.003	0.004
0.8	0.733	0.025	-0.000	0.856	0.020	0.000	0.856	0.039	0.000
0.9	0.791	0.056	-0.005	0.889	0.044	0.002	0.889	0.085	0.003
1	0.811	0.071	-0.010	0.900	0.054	0.003	0.900	0.105	0.006

Table 4.1: CLC power, i_1 and i_2 harmonic content

Figure 4.6 shows the converter's normalized power range when operated with equal bridge modulations, $k_1 = 0.6$ and with $\phi = -90°$. To gauge the power sensitivity of the converter, (28) was evaluated for Monte-Carlo variations of ±10% in the value of each of the four reactive elements. From this it can be seen that the converter's power is insensitive to component variations. The 3rd harmonic component of the currents causes the local rise in the power curve at a relative modulation of 1/3, but its effect is relatively small compared to the current variations seen in Figure 4.4.

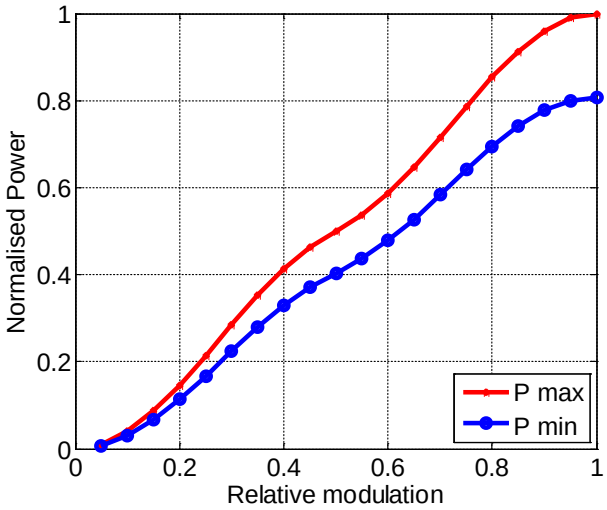


Figure 4.6: CLC power sensitivity to component variations

4.3.4 Calculation of the RMS Quantities for CLC Converter

RMS Current

The rms magnitudes of the currents into and out of the T-type network in Figure 4.2, i_1 and i_2 respectively, are calculated from a frequency domain summation of their individual components. Their RMS values are given in (29) and (30).

$$\bar{i}_1 = \frac{4}{\pi X_D \sqrt{2}} \sqrt{\sum_{n=1,3\ldots} \left(\frac{(N_6)^2 + (N_7)^2}{{D_2}^2} \right)} \tag{29}$$

Where: $D_2 = n^2(k_1k_4 + k_2k_3 + k_3k_4) - k_2k_4 - k_1k_3n^4$

$N_6 = n^2k_3t_rV_{DC2} \sin\frac{n\alpha_2}{2} sin\, n\phi$

$N_7 = (n^2k_3 - k_4)V_{DC1} \sin\frac{n\alpha_1}{2} - n^2k_3t_rV_{DC2}\, sin\frac{n\alpha_2}{2} \cos n\phi$

$$\bar{i}_2 = \frac{4}{\pi X_D \sqrt{2}} \sqrt{\sum_{n=1,3\ldots} \left(\frac{(N_8)^2 + (N_9)^2}{{D_2}^2} \right)} \tag{30}$$

Where: $N_8 = (n^2k_3 + n^2k_1 - k_2)t_rV_{DC2} \sin\frac{n\alpha_2}{2} sin\, n\phi$

$N_9 = n^2k_3V_{DC1}\, sin\frac{n\alpha_1}{2} + (k_2 - n^2k_1 - n^2k_3)t_rV_{DC2}\, sin\frac{n\alpha_2}{2} cos\, n\phi$

The bridge 2 rms current, $\bar{i}_{B2}$, is a scaled version of $\bar{i}_2$:

$$\bar{i}_{B2} = t_r \bar{i}_2 \tag{31}$$

RMS Voltage

Equation (21) also applies to the CLC converter.

4.3.5 ZVS Range of CLC Converter

The switching points previously calculated in (22) also apply to the CLC converter. MATLAB program, *clc_zvs_rng* in Appendix A, was used to find the ZVS range of the converter for equal bridge modulations m_1 and m_2, a k_1 value of 0.6 and Bridge 2 leading Bridge 1 by 90°. Figure 4.7 shows the minimum or worst-case switching current values which occur in each leg for a variation in dcr from 0.7 to 1.4 and for ± 10% Monte-Carlo component variations. For the chosen current directions a positive current value indicates ZVS.

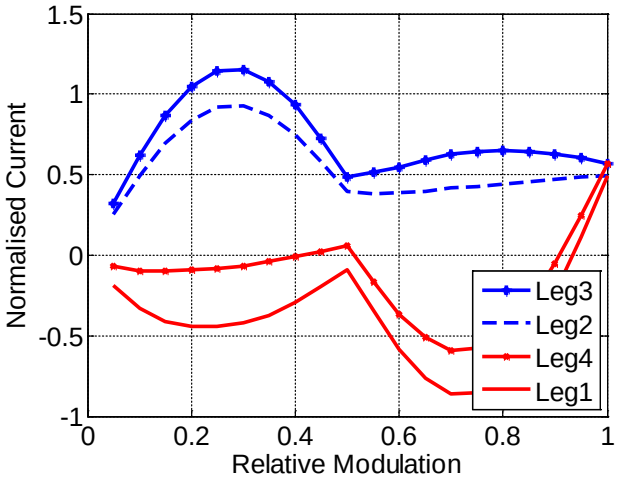


Figure 4.7: CLC minimum leg currents at the switching points

From the figure it can be seen that, for most modulation values, the leading leg of the leading bridge (Leg 3, switches S_5 and S_6) and the lagging leg of the lagging bridge (Leg 2, switches S_3 and S_4) have ZVS for all modulation values, while the other two legs don't, in general, have ZVS. Similar results are obtained for reverse operation. In Chapter 5 the ZVS status, along with the switching currents, will be used to calculate the switching losses of the transistors in the converter's legs.

4.4 Theoretical Performance of Lossless CLC Converter

A MATLAB program, *clc_dab_2igbt* in Appendix A, in conjunction with (22) to (28), was used to analyse a prototype converter which was designed to provide a maximum power throughput of 4 kW when running from equal dc link voltages of 400 V. For this power, it is calculated, from (28), that the design reactance, X_D, is required to be 32.5 Ω, and the transformer's nominal turns ratio, t_r, will equal 1. As with the LCL converter, the value of the design reactance was chosen, for practical reasons, to be 31.83 Ω at the chosen switching frequency of 50 kHz. The value of k_1 chosen was 1. Using this design, the converter's theoretical performance was examined using the MATLAB program, in which the maximum value of n, the harmonic number, was set to 99, so that 50 frequency components were used.

Plots of the bridge voltage and current waveforms, for $m_1 = m_2 = 1$ and forward operation with $\phi = -90°$ are shown in Figure 4.8. The dominance of the fundamental component, and its in-phase alignment, can be seen.

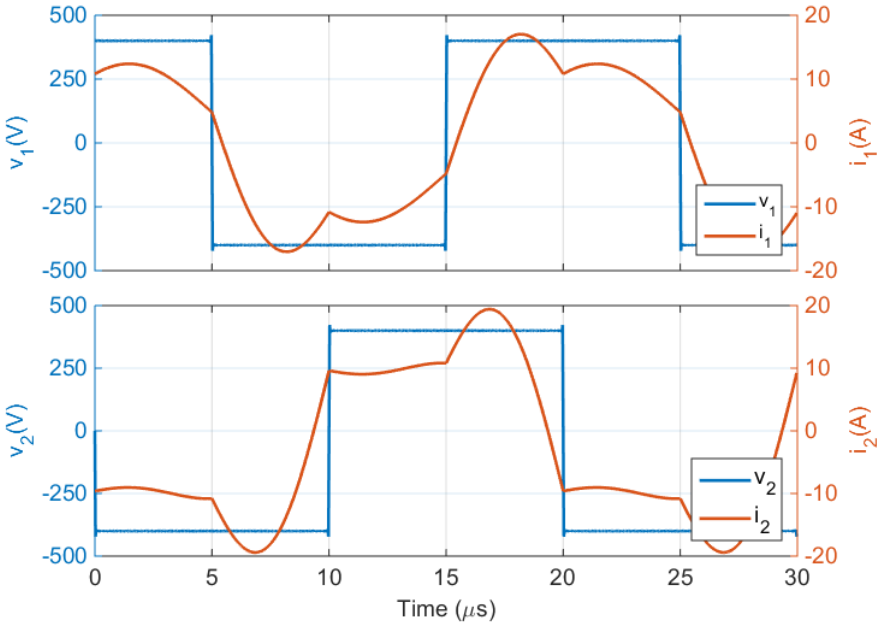


Figure 4.8: CLC bridge voltages and currents at 100% forward modulation

Reverse operation, with $\phi = 90°$, at maximum modulation yields similar results, as shown in Figure 4.9, except that the bridge currents are in anti-phase with their respective voltages:

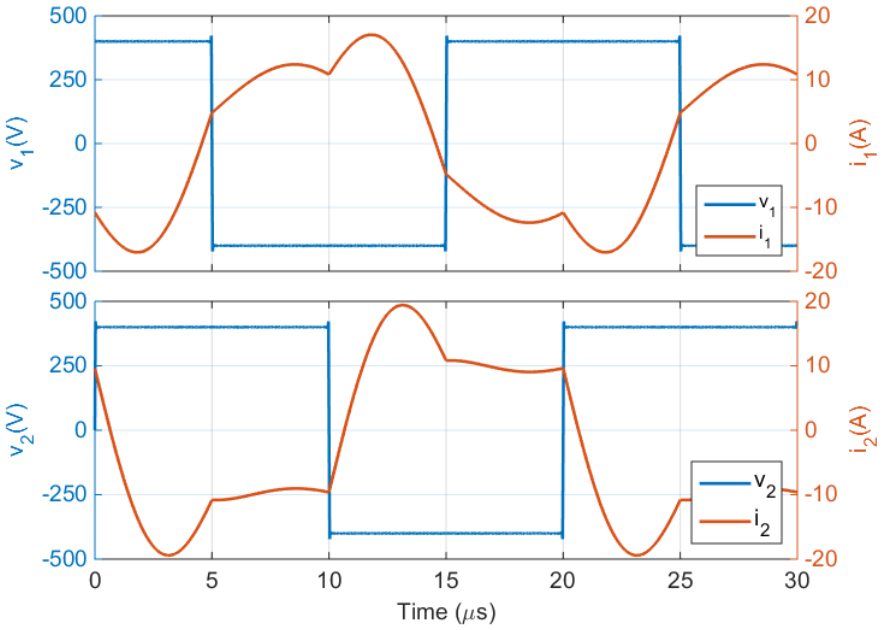


Figure 4.9: CLC bridge voltages and currents at 100% reverse modulation

Figure 4.10 shows the results for 70% forward modulation. The current waveforms strongly resemble sinusoids; the modulation is close to the value of 2/3 which results in a null in the 3rd harmonic of the bridge voltages. This also shows in the graph of Figure 4.5.

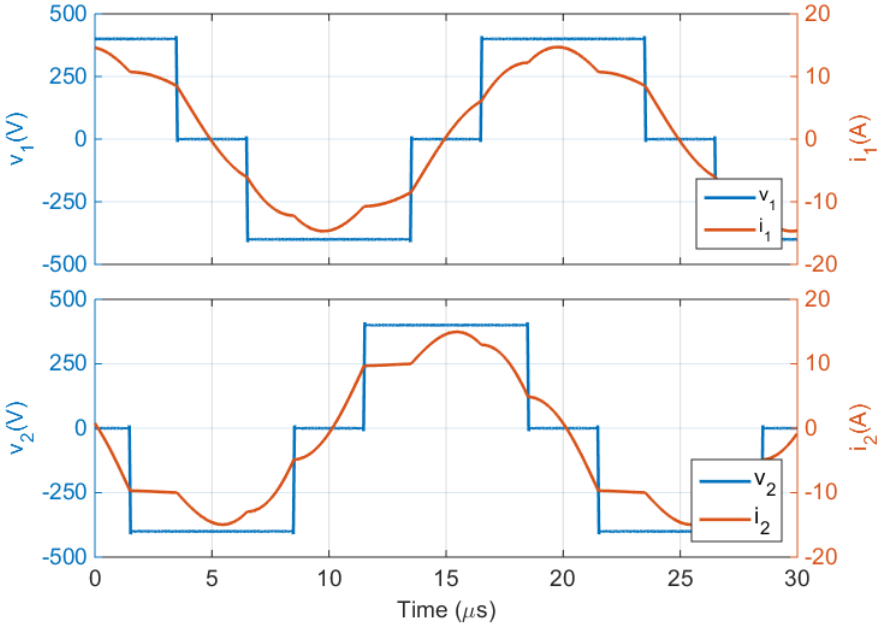


Figure 4.10: CLC bridge voltages and currents at 70% forward modulation

Power Flow of CLC Converter

Figure 4.11 shows the instantaneous power flow of the 4 kW converter at maximum throughput. As with the LCL converter, the negative area in the plot, corresponding to the reverse power flow, is a very small fraction of the forward power.

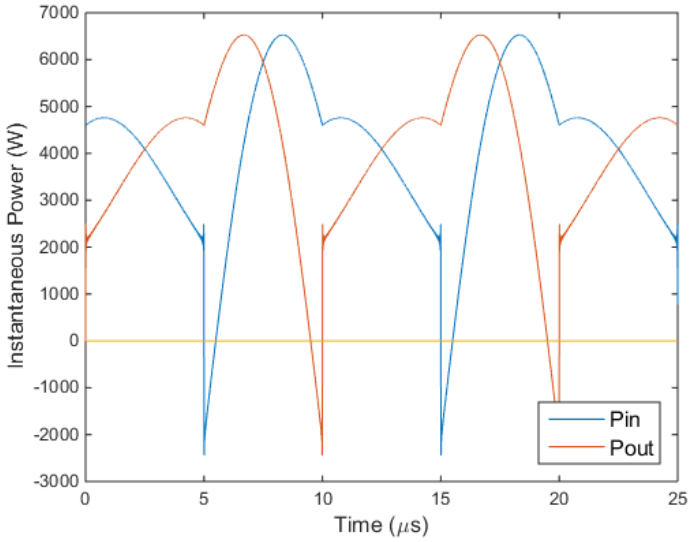


Figure 4.11: Power flow of CLC converter for 100% modulation

This concludes the theoretical treatment of the LCL and CLC DAB converters. In the next chapter the theory will be validated by experimental results.

5 Converter Performance and its Validation

5.1 Introduction

In Chapters 3 and 4 the operation and performance of ideal LCL and CLC converters was investigated. In this chapter models of the proposed converters implemented using non-ideal components are analysed, before being verified experimentally. This takes into account the voltage and current stresses placed upon circuit components, as well as the power losses, which are hardware dependent, and shows the viability of practical implementations of the proposed topologies.

Initially the LCL converter is investigated. Two different versions were laboratory tested. The first is an LCL converter with a maximum power throughput of 2.5 kW that operates from 380 V and 50 V dc power supplies, and with Bridges 1 and 2 implemented using IGBTs and MOSFETs respectively [75]. The second, a 4 kW converter, used IGBTs in both bridges and operated from 400 V dc power supplies. This is the unit for which the ideal analysis was conducted, in Section 3.4, and which will be analysed further in the following section.

5.2 LCL Prototype Converter

5.2.1 LCL Prototype Circuit

The LCL prototype circuit is shown in the circuit of Figure 5.1. It differs from the original topology of Figure 3.1 only in the addition of two capacitors, C_2 and C_3. Although these are not theoretically necessary, they prevent transformer saturation in the advent of a dc component occurring as a result of asymmetry in the open-loop control. They have a negligible reactance at the switching frequency.

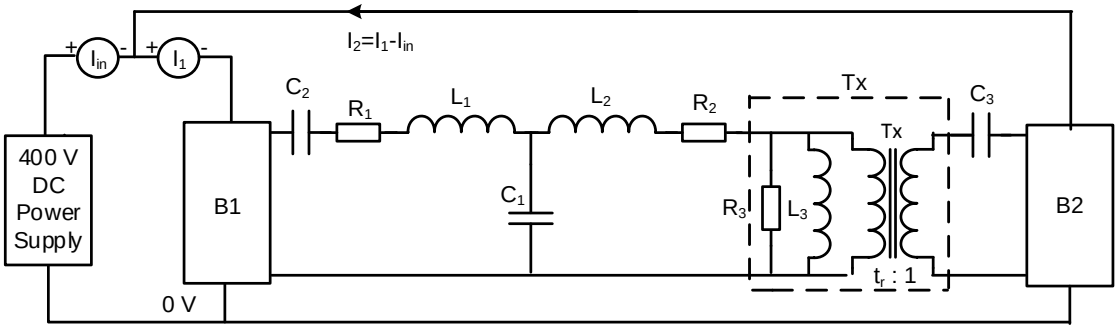


Figure 5.1: LCL DAB converter test hardware

No attempt was made to isolate the two bridges. This would have required significantly more hardware and the additional complexity was not considered necessary to prove the operation of the prototype converter.

As the converter has been designed for $V_{DC1} = V_{DC2} = 400$ V it is convenient to link the two supply rails. This has three advantages: Firstly, the power supply only has to supply the losses, so the average current required is small; a small capacitor can provide for the ripple currents. Secondly, it is possible to accurately measure the power losses with this experimental configuration, even with modest equipment, as the input current, and therefore the relative power loss is provided directly. For example, for a converter power efficiency of 90%, a 10% error in the relative power loss measurement results in a 1% error in the calculated value of the measured efficiency. Lastly, with a common supply voltage the need for an accurate measurement of two voltages is avoided, for the same reason that was mentioned above. An error in the measurement results only in an error in the power level, not the measured efficiency at that power level.

5.2.2 Switches

STGWA19NC60 IGBTs, from ST Microelectronics, were chosen for the switching transistors. They have low switching energy losses, an adequate voltage rating of 600 V, a conservative current rating of 31 A and an inbuilt ultra-fast soft-recovery diode. The selection of this device involved the trade-off between a smaller and lower rated device, which would have higher conduction losses, but would be faster and therefore have smaller switching losses, and a larger and slower device with smaller conduction losses but higher switching losses.

5.2.3 Drivers

Figure 5.2 shows one of the four circuits which uses a Silicon Labs Si8235 dual isolated driver integrated circuit (IC) to drive two of the eight transistors in the power bridges, in this case leg 1, transistor switches Q_1 and Q_2. A Schottky diode in parallel with one of the resistors in the drive circuit was used to obtain an R_{Goff} that was significantly smaller than R_{Gon}. This is necessary to lessen the effect of cross-current conduction between the switch-off and switch-on processes. For a leg switching with ZCS, a small gate source resistance in the off state is also necessary to prevent a device which is off from being turned on by the dv/dt effect of the opposing device turning on.

The IC has a 13 V dc power supply VD, and uses a boot-strapped power supply for the upper driver to provide for the positive gate drive, with respect to GNDA, to the top-side transistor.

The driver's inputs were driven by a microcontroller which used a state machine to implement equal amplitude modulations with the phase shift between the bridges set at either 90° or -90°. A fixed dead-band of 350 ns was used to prevent cross-current conduction.

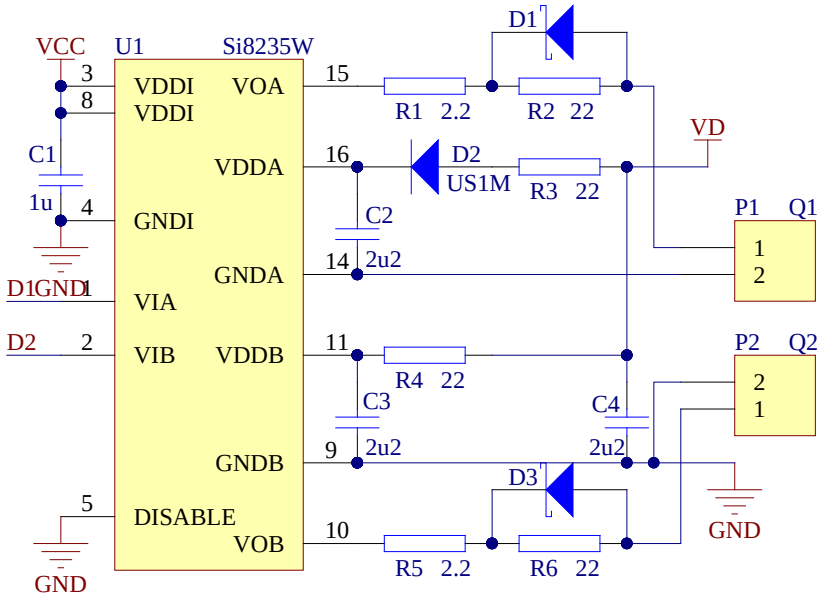


Figure 5.2: Drive circuitry for Leg 1 of LCL DAB

5.2.4 LCL Circuit Parameters

The measured values of the ac resistances are given in Table 5.1 where R_1 is the resistance of L_1 and R_2 is the resistance of L_2. The primary-referred transformer resistance, R_p, will be added to R_2 for the purpose of the loss calculations.

f (kHz)	50	150	250
R_1 (mΩ)	29.7	92.3	218
R_2 (mΩ)	27.7	91.9	225
R_p (mΩ)	43.6	56.2	68.4

Table 5.1: LCL inductor and transformer ac resistances

A summary of the circuit's hardware is shown in Table 5.2. The values of the reactive components actually used determines the parameters k_1 to k_4, which will be used in the calculations of the theoretical results.

X_D = 31.83 Ω; fs = 50 kHz; maximum power output = 4 kW		
Parameter	Ideal Value	Actual Value
V_{DC1}	400 V	400 V
V_{DC2}	400 V	400 V
Switches, Bridge 1, 2	ST Microelectronics STGWA19N60HD IGBT	
Inductors L_1, L_2: Dual E65/32/27 core set, 3C90 material		
L_1	101.3 µH	102 µH, k_1 = 1.007
L_2	101.3 µH	99 + 2 µH, k_2 = 0.997
C_1	100 nF	97.9 nF, polypropylene k_3 = 1.021
C_2	∞, dc removal	8 µF polypropylene
C_3	∞, dc removal	8 µF polypropylene
Transformer: Dual E65/32/27 core set, 3C90 material		
Turns-ratio tr	1	1.085
L_3	∞ (magnetizing inductance)	2.3 mH, k_4 = 22.7
L_p	0 (primary-referred leakage inductance)	2 µH

Table 5.2: LCL DAB converter system parameters

5.3 Converter Power Losses

Previously, the waveforms and magnitudes of the circuit currents have been defined by equations which were based on a lossless circuit model. This is a reasonable assumption if the losses are relatively small, in which case the voltage drops in the network resistors and the bridge switches are small relative to the source values.

However, to obtain an accurate power model of the system, allowance needs to be made for the power losses. The major power loss contributors are the switching and conduction losses of the bridge transistors, and the magnetising and resistive losses of the magnetic components.

The switching device model shown in Figure 3.1 is that of an ideal switch with conduction and switching losses added subsequently. Conduction losses arise from the product of the voltage-drop across and the current through a semiconductor switching device. The voltage-current relationship will usually be non-linear and therefore calculated by the integration, numerically, of the voltage-current product.

Although switching losses have numerous contributing components, three main forms exist: The first is the average value of the large, but narrow power spikes which

occur as a result of the voltage and current crossover which occur when a switching device changes state. The second is due to two energy components associated with the reverse recovery of the diode opposing the transistor being switched, in the event that the diode is carrying current prior to the switching process; as well as the diode's current burden on the transistor, the diode also requires its own turn off energy. Lastly, a loss arises because of the energy stored in the switching leg output capacitances.

Resistive losses are of the form I^2R and arise in conductors such as the wire in a wound magnetic component and the equivalent series resistance (ESR) in capacitors. The resistance has a linear voltage-current relationship, but may be a function of frequency, due to eddy current losses.

With magnetic components core losses are also incurred. Core losses comprise three main components: hysteretic losses, classical eddy current losses and excess eddy current losses.

There are also a variety of smaller losses which will be ignored. These include the control and driver circuitry and the ESR losses in capacitors.

The next sections detail the theoretical calculation of the losses in the semiconductor devices, in particular the switching and conduction power losses, which will make up the bulk of the power losses.

5.3.1 Switching Power Loss Calculation

The bridge transistor/diode switch combinations switch with either ZVS or ZCS, depending on the leg current polarity. For a device that switches with ZVS the switch-on energy loss, E_{on}, will be taken to be zero. For a device that switches with ZCS the switch-off energy loss, E_{off}, will be taken to be zero. The switching losses depend on the leg current at the switching point and the transistor's switching characteristic. The calculation process differs, depending on how the information is supplied. For the IGBTs used the turn-on and turn-off energy data was supplied directly in data sheet form, and include the output capacitance shown in the model of Figure 3.1. For the MOSFETs used the semiconductor parameters were supplied, so that the losses may be calculated from these and the driver information.

For the STGWA19NC60 IGBTs which were used in the two prototypes in this thesis, the switching energy loss data shown in Figure 5.3 and Figure 5.4 was taken from the manufacturer's data sheet [http://www.st.com/web/en/home.html]. This data was curve

fitted using the MATLAB program *STGWA19N60_swg_loss_data*, which was used to obtain three term polynomials for both E_{on} and E_{off} as a function of current at 125 °C and their temperature corrections for the calculation of the loss energies at other temperatures. The supplied data is specified for a collector to emitter voltage, V_{CE}, of 390 V; in using this data the energy losses were assumed to be proportional to V_{CE}. This data was merged to provide three dimensional switching losses in the MATLAB program *STGWA19N60_swg_loss*, which has voltage, current and temperature inputs and returns E_{on} and E_{off}. The MATLAB program is included in Appendix A.

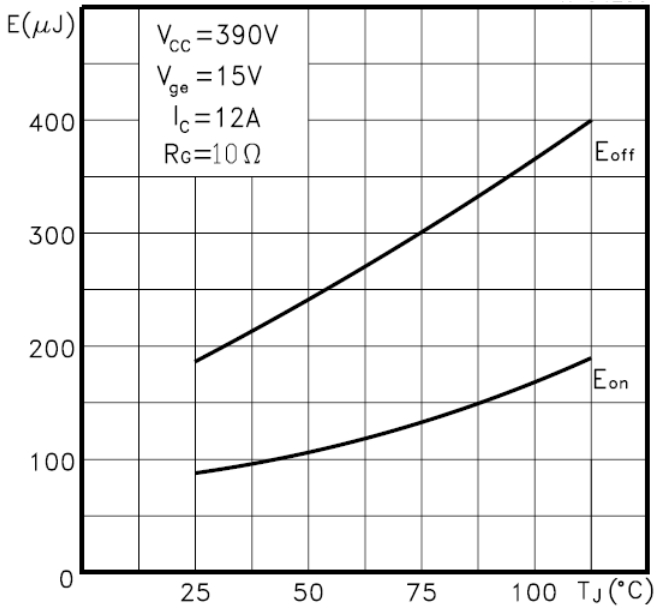


Figure 5.3: STGWA19N60 switching loss versus temperature

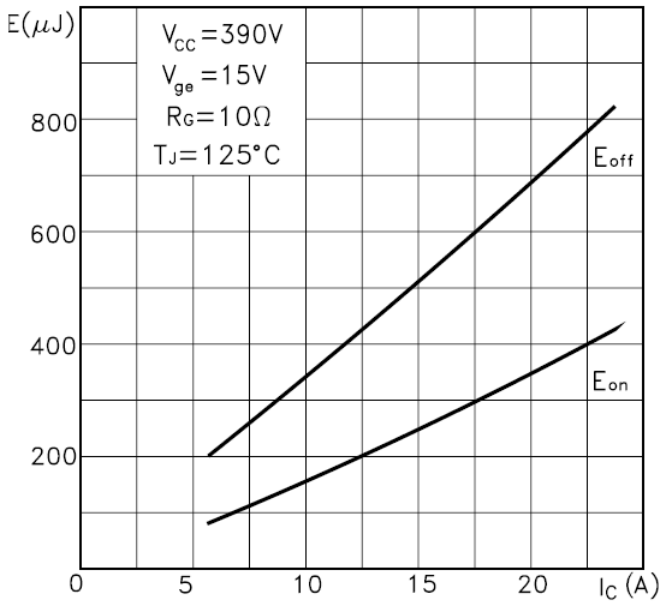


Figure 5.4: STGWA19N60 switching loss versus current

In practice, the switching losses of an IGBT will be slightly greater than that predicted theoretically. The turn-off loss of an IGBT has a dynamic component which depends on the history of the device's current, as well as its value prior to turn-off [57, 58]; this arises because of the stored charge which is an integral of the current. This can give rise to an excess loss which can be significant when there is a large amount of stored charge. If there isn't adequate time for this stored charge to recombine under zero voltage conditions, the IGBT will exhibit a tail current as this charge is removed by the voltage impressed across the device after it has, ideally, turned off. This will give rise to small amount of cross-conduction loss, particularly when non-ideal gate drive signals are used.

Although IGBTs were used in both bridges of the 4 kW prototype converters used in this thesis, the loss calculations for a bridge employing MOSFETs will also be given, as these devices were used in the alternative converters. MOSFETs were also used in one bridge of the 2.5 kW converter in [75]. For MOSFETs the energy loss calculations are given by [76]:

$$E_{onM} = V_{DD} I_L \frac{t_{ri} + t_{fu}}{2} + Q_{rr} V_{DD} \tag{32}$$

$$E_{offM} = V_{DD} I_L \frac{t_{ru} + t_{fi}}{2} \tag{33}$$

$$E_{onD} = V_{DD} \frac{Q_{rr}}{4} \tag{34}$$

Where:

E_{onM} is the MOSFET switch-on energy, which includes the reverse recovery burden caused by the opposing diode (J)

E_{offM} is the MOSFET switch-off energy (J)

E_{onD} is the diode reverse recovery energy occuring when the opposing MOSFET turns on (J)

V_{DD} is the dc rail voltage (V)

I_L is the load current (A)

Q_{rr} is the diode reverse recovery stored charge (C)

t_{ri} is the rise time of the current (s)

t_{fu} is the fall time of the voltage (s)

t_{ru} is the rise time of the voltage (s)

t_{fi} is the fall time of the current (s)

In the use of (32) to (34) it was assumed that the current rise time t_{ri} and the fall time t_{fi} were proportional to the drain current I_D.

The voltage fall and rise times t_{fu} and t_{ru} are determined by the Miller capacitance [77] and the drive currents:

$$t_{fu} = \frac{V_{DD} C_{GD}}{I_{Gon}} = \frac{Q_{GD}}{I_{Gon}} \tag{35}$$

$$t_{ru} = \frac{V_{DD} C_{GD}}{I_{Goff}} = \frac{Q_{GD}}{I_{Goff}} \tag{36}$$

In (35) and (36), if the gate-drain capacitance C_{GD} is used rather than the gate-drain charge Q_{GD}, it should be an averaged value at V_{DD} and $V_{DD}/2$. The gate charge and discharge currents are:

$$I_{Gon} = \frac{(V_{Drv} - V_{GP})}{R_{Gon}} \tag{37}$$

$$I_{Goff} = \frac{V_{GP}}{R_{Goff}} \tag{38}$$

In (37) and (38) the median drain current value is used in determining the gate plateau voltage V_{GP} which is used. The gate drive resistances R_{Gon} and R_{Goff} which are used should include the corresponding in-circuit resistances and the estimated source and sink voltage drops of the driver IC based on its source and sink characteristics and its active output voltage V_{Drv}.

5.3.2 Conduction Power Loss Calculation

The conduction losses of each switch are calculated by the integration of the product of its voltage and current between the switch-on and switch-off points, which will span half a cycle. For positive voltages and currents, namely 1st quadrant operation, the transistor characteristic is used.

In the 3rd quadrant the diode characteristic is used for IGBTs, and the transistor resistance characteristic is used for MOSFETs. If the MOSFET reverse voltage is large enough to forward bias its diode, as will usually be the case for a high voltage MOSFET, then the current will need to be partitioned between the MOSFET's transistor and its diode to obtain the reverse voltage drop. In the case of MOSFETs, it is also possible for external diodes, with an improved switching speed, to be used. For the calculations used in [75] it was assumed that the diode did not conduct, as the MOSFET drain to source resistance was sufficiently small that the diode's forward voltage didn't reach the threshold.

Two MATLAB programs were developed to model the voltage drops of the IGBTs that were used, one for each of the transistor and diode characteristics, *STGWA19N60_vt* and *STGWA19N60_vd*, in Appendix A. Each program calculates the voltage drop as a function of current and temperature. Linear interpolation is used between known temperature values. The data was obtained, in the MATLAB program *STGWA19N60_v_data*, Appendix A, from curve fitting the maximum values supplied in the manufacturer's data sheet, shown in Figure 5.5 and Figure 5.6.

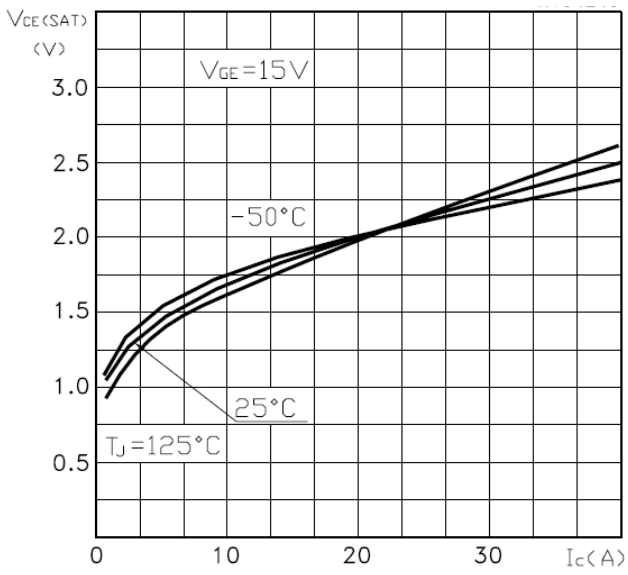


Figure 5.5: STGWA19N60 transistor voltage drop

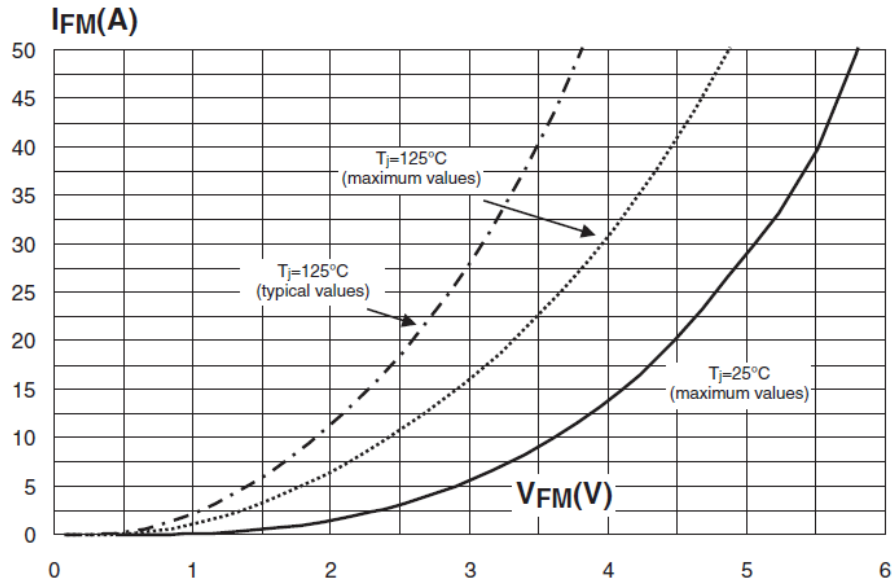


Figure 5.6: STGWA19N60 integrated diode voltage drop

5.3.3 Magnetising Losses

The inductors and the transformer used dual E65 core sets. For the short durations involved in the testing of the converter, it was assumed that the core temperature would be close to room temperature, which was taken to be 20°C. As a first approximation, a sinusoidal flux waveform was assumed for the inductors, which were designed to operate at a maximum flux density of 125 mT. Under these conditions the inductors have a core loss density, from the Ferroxcube calculator for 3C90 material, of 150 mW/cm^3. As the transformer is driven with a square wave signal, its flux will be approximately triangular. For a maximum flux density of 135 mT, the transformer's core loss density is 133 mW/cm^3. Each dual core set has a total volume of 158 cm^3, so that the total magnetising loss for the three components at maximum modulation is 67 W.

It was initially intended to model this loss using the shunt resistor R_3 in Figure 3.3, which would have a value of 2800 Ω to correspond to the losses at maximum modulation. This assumes that the magnetising loss varies, at smaller modulations, as the square of the flux density. A more accurate loss model, for example the modified Steinmetz equation (MSE) [78, 79], could be used, but may not be necessary for a small magnetic loss contribution. A reasonable approximation for the losses, using the Steinmetz equation is, in the case of Ferroxcube 3C90 core material [http://www.ferroxcube.com]:

$$P_V = kB^{2.8}f^{1.46} \tag{39}$$

Where:

P_V is the power loss volume density (mW/cm^3)

k is a proportionality constant

B is the flux density (mT)

f is the frequency of the sinusoidal flux waveform (Hz)

From this, the power loss is proportional to the flux density, and therefore voltage, raised to the power of 2.8. Based on this, the power loss is proportional to the modulation raised to the power of 1.4, rather than to modulation directly, as would be the case for a square law core loss relationship. For this reason, a fixed resistor doesn't model the loss accurately and the expression (39) will be used for the loss calculations.

5.4 Theoretical Power Efficiency Calculation

The effect of the resistive losses in R_1 and R_2, in Figure 3.3, is for each of these to take its power from the opposite source. This occurs since they have a voltage which is in phase with the source they are connected to, so that an effective decrease in this voltage decreases the current on the opposite side of the network, as stated in section 3.3.2. Conduction losses in the bridges act in the same way, as they are effectively a voltage drop in series with that source. The switching losses of the bridge transistors, which act as shunt elements, will be taken directly from their sources. The association of the magnetising losses of the transformer and inductors depends on how they are modelled. For L_1, L_2 and Tx in the LCL converter implemented as discrete components, L_2's loss will come from Bridge 1, while those of the other two will come from Bridge 2. Based on this, the power equations are:

$$P_1 = P_i + P_{R2} + P_{con2} + P_{sw1} + P_{magL2} \tag{40}$$

$$P_2 = P_i - P_{R1} - P_{con1} - P_{sw2} - P_{magL1} - P_{magTx} \tag{41}$$

$$P_{loss} = P_{R1} + P_{R2} + P_{con1} + P_{con2} + P_{sw1} + P_{sw2} + P_{mag} \tag{42}$$

$$PE = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} = 1 - \frac{P_{loss}}{P_{in}} \tag{43}$$

Where:

P_i is the (lossless) power throughput calculated by (12) (W)

P_1 is the power supplied by source 1 (W)

P_2 is the power delivered to source 2 (W)

P_{R1} and P_{R2} are the resistive power losses of R_1 and R_2 in Figure 3.3 (W)

P_{con1} and P_{con2} are the conduction power losses of the bridge transistors (W)

P_{sw1} and P_{sw2} are the switching power losses of the bridge transistors (W)

P_{mag} is the magnetising power loss of the transformer and inductors (W)

P_{loss} is the total power loss of the converter (W)

PE is the power efficiency of the converter

P_{in} and P_{out} are the converter's input and output powers (W)

5.5 Calculated Power Efficiency of LCL Prototype

The MATLAB program *lcl_loss_2igbt*, in Appendix A, was used to calculate the losses of this converter. Using the transistor current waveforms which have been calculated, and the switching indices, the conduction and switching losses of each bridge are then calculated. For the purpose of these calculations, the transistor junction temperatures were assumed to be 75°C; the actual junction temperatures were estimated, based on the power and the thermal resistances, be close to this at full power. After correcting the ideal power for the losses which have occurred the final values of P_1 and P_2 are obtained from (40) and (41). Finally, the volt-second products of the magnetising voltages are calculated; these specifications are needed for the design of the magnetic components.

Table 5.3 and Table 5.4 show summaries of the power losses at 10 modulation levels, for forward and reverse power transfer respectively. Switching, conduction, resistive and magnetising losses, as well as the bridge currents and the overall efficiency are included. The forward and reverse magnitudes of the currents, output power and efficiency are almost identical, showing that the converter's operation is symmetrical. Maximum efficiencies of approximately 95% are obtained.

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	11.7	21.2	27.8	31.2	31.6	29.7	25.7	19.9	13.4	21.6
Pcon1 (W)	4.6	10.7	16.8	22.2	26.9	30.7	33.8	36.3	38.2	39.0
Ptot1 (W)	16.3	32.0	44.6	53.4	58.5	60.4	59.5	56.2	51.6	60.6
Psw2 (W)	12.3	22.3	29.1	32.4	32.8	30.8	26.9	21.3	19.7	29.6
Pcon2 (W)	5.0	13.0	22.6	32.7	42.9	52.3	60.7	67.5	72.3	74.2
Ptot2 (W)	17.3	35.3	51.6	65.2	75.6	83.2	87.5	88.8	92.0	103.8
Pmag (W)	2.1	6.0	11.0	16.9	23.7	31.1	39.2	47.9	57.2	67.0
Pr (W)	0.7	1.8	3.4	5.2	7.0	8.8	10.6	12.1	13.3	14.0
Loss (W)	41.0	82.6	119.8	150.6	174.7	192.7	204.7	210.9	217.4	245.7
P1 (W)	128	466	973	1594	2268	2939	3551	4045	4366	4492
P2 (W)	92	391	863	1453	2103	2755	3354	3840	4152	4246
Efficiency	0.717	0.839	0.886	0.912	0.927	0.938	0.945	0.949	0.951	0.945
I_1 (Arms)	2.0	3.9	5.7	7.2	8.6	9.8	10.7	11.5	12.0	12.1
I_{B2} (Arms)	2.1	4.0	5.8	7.3	8.6	9.8	10.8	11.5	12.0	12.2

Table 5.3: Summary of LCL calculated efficiency with forward modulation

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	11.7	21.2	27.8	31.2	31.6	29.7	25.7	19.9	13.4	21.6
Pcon1 (W)	4.9	12.8	22.4	32.6	42.8	52.3	60.6	67.1	71.6	73.3
Ptot1 (W)	16.6	34.1	50.2	63.8	74.4	82.0	86.2	87.0	84.9	94.9
Psw2 (W)	12.3	22.3	29.1	32.4	32.8	30.8	26.9	21.3	19.7	29.6
Pcon2 (W)	4.7	10.9	16.9	22.3	26.9	30.7	33.9	36.6	38.9	39.7
Ptot2 (W)	17.0	33.1	46.0	54.7	59.7	61.6	60.8	57.9	58.5	69.4
Pmag (W)	2.1	6.0	11.0	16.9	23.7	31.1	39.2	47.9	57.2	67.0
Pr (W)	0.7	1.8	3.4	5.2	7.0	8.8	10.6	12.1	13.3	14.0
Loss (W)	41.0	82.5	119.7	150.6	174.6	192.7	204.7	210.9	217.3	245.4
P1 (W)	-92	-391	-863	-1453	-2102	-2753	-3352	-3837	-4153	-4249
P2 (W)	-129	-467	-973	-1593	-2266	-2937	-3549	-4042	-4367	-4494
Efficiency	0.718	0.839	0.886	0.912	0.927	0.938	0.945	0.949	0.951	0.945
I_1 (Arms)	2.0	3.9	5.7	7.2	8.6	9.8	10.7	11.5	12.0	12.1
I_{B2} (Arms)	2.1	4.0	5.8	7.3	8.6	9.8	10.8	11.5	12.0	12.2

Table 5.4: Summary of LCL calculated efficiency with reverse modulation

The conduction losses, as expected, are the largest component of the losses, hence the motivation to minimise them by the use of the resonant network. For these bridges, implemented using IGBTs, the inverting bridge has smaller conduction losses than the rectifying bridge. This occurs because the IGBT has a relatively small forward voltage drop compared to that of its lightly doped ultrafast soft recovery diode.

The switching losses in the bridges are independent of the direction of power transfer. They depend on the currents at the switching points, as shown in Figure 3.11, which shows that two legs have maximum values at a modulation index of 0.4, and the other two legs have maximum values at a modulation index of 0.6, so that the switching losses are a maximum in this range. The abrupt increase in the switching losses as the modulation index changes from 0.9 to 1 occurs because leg 1 gains ZVS at this point. Attaining ZVS status would be considered to be desirable in a bridge implemented with MOSFETs, to mitigate the losses occurring as the MOSFET which is switching on discharges the energy stored in its output capacitance. For the IGBTs used in the prototype converter, the switch-off energy losses are approximately double the switch-on energy losses; for this reason the leg switching losses are smaller when the leg has ZCS, rather than ZVS, status.

For forward power transfer the magnitudes of the four main power loss contributors are shown in Figure 5.7.

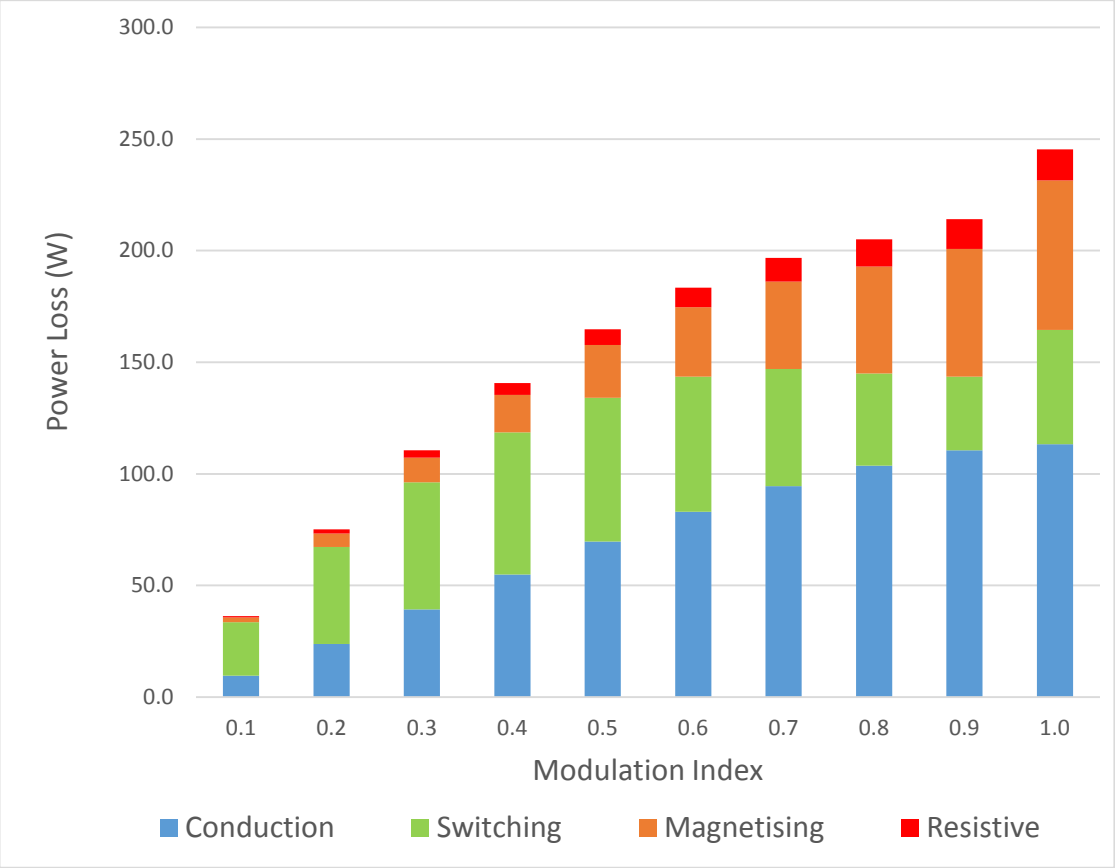


Figure 5.7: LCL IGBT converter calculated power loss components

With the exception of the switching losses, all power loss components increase progressively with increases in modulation. At maximum power throughput the core losses of the magnetic components and their resistive losses are 67 W and 14 W respectively. Their sum of 81 W makes up 33% of the total losses. There is room for improvement in the design of the magnetic components.

The power loss values in reverse operation are almost identical to those shown in Figure 5.7 for forward operation. Figure 5.8 shows the converter's power efficiency and power as a function of modulation for forward operation. The efficiency is over 85% for output powers greater than 10% of the maximum.

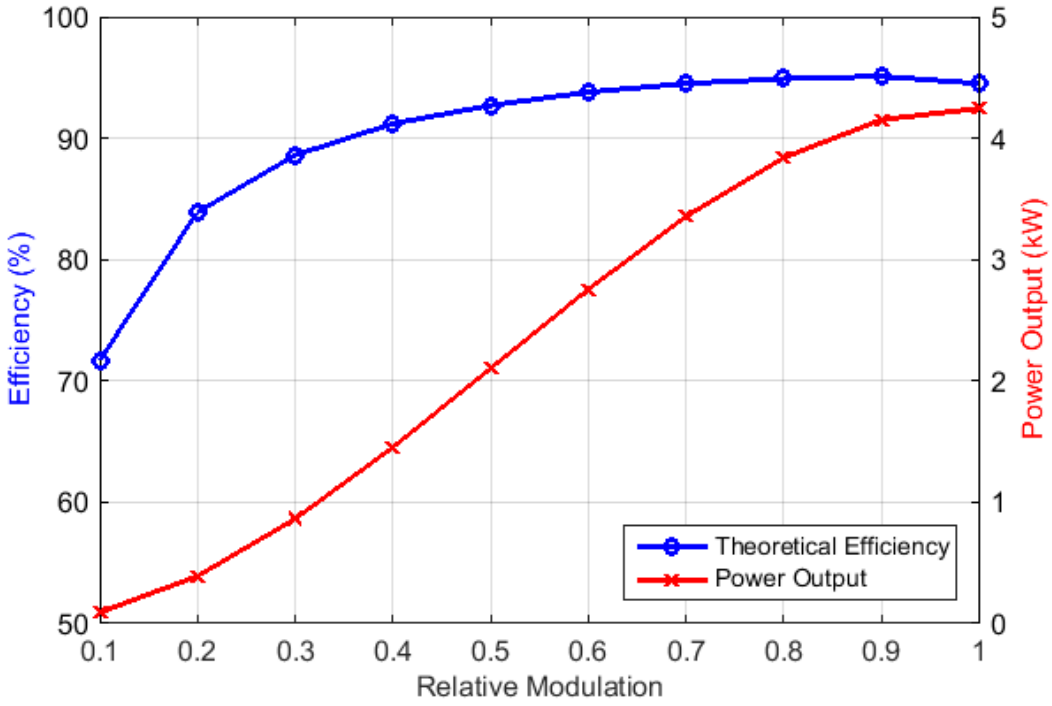


Figure 5.8: LCL Converter calculated power efficiency and power output

Variation in dc link voltage

Thus far the results presented are for a converter operating with matched loads, that is, for a dc conversion ratio (dcr) of unity. To find how the calculated power efficiency (PE_calc) of the LCL DAB converter is affected by changes in the dcr, tests were conducted with two values of V_{DC1} for 4 different modulations, forward and reverse, so that a dcr range of 1.4 to 0.7 was achieved. The calculated results are recorded in Table 5.5, in which the calculated efficiency PE_{400} for $V_{DC1} = V_{DC2} = 400$ V at the same power output, from Figure 5.8, is included for the purpose of comparison. It can be seen that the most obvious change is that the power efficiency is about 1% bigger at low power levels,

and slightly smaller at maximum output. At low power levels the switching losses are reduced as a result of the lower dc link voltage, and at maximum modulation the magnetizing losses are greater than those at the same power output with reduced modulation and full dc link voltage. The main effect of a reduced dc voltage is the reduced maximum power output.

	Forward Modulation, dcr = 1.4				Forward Modulation, dcr = 0.7			
	0.2	0.4	0.7	1.0	0.2	0.4	0.7	1.0
V_{DC1}	310	310	310	310	400	400	400	400
I_{DC1}	1.16	3.98	8.87	11.2	0.77	2.61	5.81	6.84
I_{1rms}	3.85	7.15	10.72	12.09	2.71	4.77	6.93	7.91
V_{DC2}	400	400	400	400	258	258	258	258
I_{DC2}	0.75	2.80	6.47	8.18	0.977	3.62	8.37	10.60
I_{2rms}	3.29	5.76	8.35	9.54	3.86	7.16	10.73	12.10
PE_calc	0.830	0.907	0.940	0.940	0.819	0.895	0.930	0.928
@Pout	299	1119	2587	3271	252	935	2159	2734
PE_{400}	0.820	0.900	0.935	0.944	0.806	0.890	0.928	0.938

Table 5.5: Effect of dcr variation on the LCL converter calculated efficiency

LCL Converter with MOSFETs in the bridges

The 4 kW converter that has been used for the theoretical calculations has IGBTs in both bridges, and both bridges have a high dc link voltage. While it is clearly better to use MOSFETs for bridge operation at low voltages, because of the reduced conduction losses, it isn't obvious how the LCL converter will perform when MOSFETs are used in high voltage bridges.

Figure 5.5 and Figure 5.6 show that, for the IGBTs used, the transistor's forward voltage is approximately 1.7 V at a median current value of 10 A, and the diode's forward voltage is up to 3 V at this current. If sizeable MOSFETs, with a low on-resistance value, were used instead of the IGBTs the conduction losses of the converter could be reduced, with a commensurate improvement in power efficiency. However, this does not allow for the poor switching characteristic of MOSFET intrinsic body diodes, as evidenced by high reverse recovery times, high stored charge and slow forward recovery. For non-ZVS operation, when hard switching is taking place in a leg, a slow diode incurs a large additional switching energy loss because of the diode's burden on its opposing transistor as the latter turns on. A second problem, which occurs in a leg switching with ZVS, is that there may be a large reverse voltage spike across the MOSFET about to be turned

on, at the start of the dead-band, as a result of the MOSFET diode's slow forward recovery and, therefore, high initial forward voltage drop as it commutates the current.

A solution which has been used [49] is the addition of two external diodes, as shown in Figure 5.9. Diode D_2 isolates the MOSFET's body diode, and D_3 acts as the new anti-parallel diode. This solution has the disadvantage of added hardware costs, and the extra space required on the heat-sink for these diodes. There is also the added conduction losses of the two diodes, which negates, to some degree, the justification for using the MOSFETs, namely, to minimise the conduction losses, particularly in the 3rd quadrant.

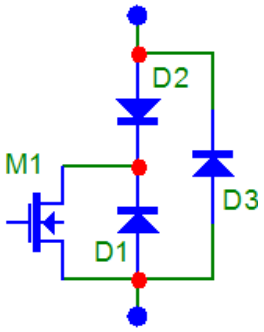


Figure 5.9: Isolation of a MOSFET's intrinsic diode

A converter which is identical to that analysed in the last section, but having IXFH26N60 MOSFETs instead of IGBTs in the bridges, was analysed with the intention of establishing its relative performance. The MOSFET characteristics are:

Symbol	Description	Value
t_{ri}	Current rise time	32ns for 13 A
t_{fi}	Current fall time	16 ns for 13 A
Q_{rr}	Reverse recovery stored charge	1 μC for 10 A
R_{on}	On-state resistance	0.35 Ω at 75°C
Q_{GD}	Gate-Drain stored charge at plateau	80 nC
t_{fu}	Voltage fall time	320 ns
t_{ru}	Voltage rise time	80 ns

Table 5.6: IXFH26N60 parameters

These MOSFETs, which provide a reasonable compromise between conduction and switching losses, had their losses calculated using the equations (32) to (38). Parameters t_{fu} and t_{ru} were calculated from (35) and (36), based on gate currents I_{Gon} and I_{Goff} of 250 mA and 1000 mA respectively.

The MATLAB program *lcl_loss_2fet*, Appendix A, was used to calculate the losses of this converter. Table 5.7 and Table 5.8 show summaries of the power losses, the efficiency and the bridge current values at 10 modulation levels, for forward and reverse power transfer respectively. Again, as expected of a converter having equal dc rail voltages, the converter's operation is symmetrical and maximum efficiencies of approximately 95% are obtained.

The loss contributions in the converter with the MOSFETs differ significantly from that of the converter using IGBTs. There are greater conduction losses in the inverting bridge, since the MOSFET has a 1st quadrant voltage drop determined by its R_{on} alone, whereas the body diode takes a large portion of the current in 3rd quadrant operation, resulting in a smaller voltage drop. This is the opposite of the result obtained with IGBTs in the bridges.

The switching losses are a maximum for modulation indices in the middle range, as they were for the converter using IGBTs, but their magnitude is considerably greater. This converter has, with this form of modulation and for typical operation, two legs switching with ZVS and two legs switching with ZCS. The losses attributed to the body diodes is significant when operating without ZVS. For this reason, it would appear that this converter will provide better power efficiency with high voltage bridges if the bridges are implemented with IGBTs.

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	19.8	42.6	64.5	81.7	91.6	92.1	79.4	51.4	9.5	14.9
Pcon1 (W)	2.5	9.1	19.5	33.1	48.6	64.6	79.5	91.8	99.9	102.9
Ptot1 (W)	22.3	51.7	84.0	114.8	140.2	156.7	158.9	143.1	109.4	117.8
Psw2 (W)	15.8	36.0	56.5	73.3	83.4	84.2	71.1	41.9	13.9	21.1
Pcon2 (W)	2.4	6.7	10.7	13.7	15.7	17.0	17.9	18.9	19.8	20.2
Ptot2 (W)	18.2	42.7	67.2	87.0	99.1	101.2	89.0	60.7	33.7	41.3
Pmag (W)	2.1	6.0	11.0	16.9	23.7	31.1	39.2	47.9	57.2	67.0
Pr (W)	0.7	1.8	3.4	5.2	7.0	8.8	10.6	12.1	13.3	14.0
Loss (W)	43.4	102.2	165.6	223.9	269.9	297.8	297.8	263.9	213.6	240.1
P1 (W)	134	481	998	1625	2300	2966	3562	4028	4310	4431
P2 (W)	91	379	832	1401	2030	2668	3264	3764	4096	4191
Efficiency	0.676	0.788	0.834	0.862	0.883	0.900	0.916	0.934	0.950	0.946
I_1 (Arms)	2.0	3.9	5.7	7.2	8.6	9.8	10.7	11.5	12.0	12.1
I_{B2} (Arms)	2.1	4.0	5.8	7.3	8.6	9.8	10.8	11.5	12.0	12.2

Table 5.7: LCL converter calculated forward performance with MOSFETs

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	19.8	42.6	64.5	81.7	91.6	92.1	79.4	51.4	9.5	14.9
Pcon1 (W)	2.3	6.4	10.4	13.5	15.6	16.9	17.8	18.6	19.4	19.8
Ptot1 (W)	22.1	49.0	74.9	95.2	107.2	109.1	97.2	70.0	28.9	34.7
Psw2 (W)	15.8	36.0	56.5	73.3	83.4	84.2	71.1	41.9	13.9	21.1
Pcon2 (W)	2.7	9.5	20.2	33.8	49.1	64.9	79.8	92.2	100.7	103.9
Ptot2 (W)	18.5	45.6	76.7	107.1	132.5	149.1	150.9	134.1	114.6	125.1
Pmag (W)	2.1	6.0	11.0	16.9	23.7	31.1	39.2	47.9	57.2	67.0
Pr (W)	0.7	1.8	3.4	5.2	7.0	8.8	10.6	12.1	13.3	14.0
Loss (W)	43.4	102.4	165.9	224.4	270.3	298.1	298.0	264.1	214.0	240.7
P1 (W)	-86	-371	-823	-1391	-2019	-2657	-3252	-3750	-4095	-4192
P2 (W)	-130	-474	-989	-1615	-2290	-2955	-3550	-4014	-4309	-4432
Efficiency	0.665	0.784	0.832	0.861	0.882	0.899	0.916	0.934	0.950	0.946
I_1 (Arms)	2.0	3.9	5.7	7.2	8.6	9.8	10.7	11.5	12.0	12.1
I_{B2} (Arms)	2.1	4.0	5.8	7.3	8.6	9.8	10.8	11.5	12.0	12.2

Table 5.8: LCL converter calculated reverse performance with MOSFETs

Figure 5.10 shows the magnitudes of the four main power loss contributors for forward power transfer. At full power output the losses are the same as those in the converter with IGBTs, as in Figure 5.7, but the losses are a lot greater in the middle range.

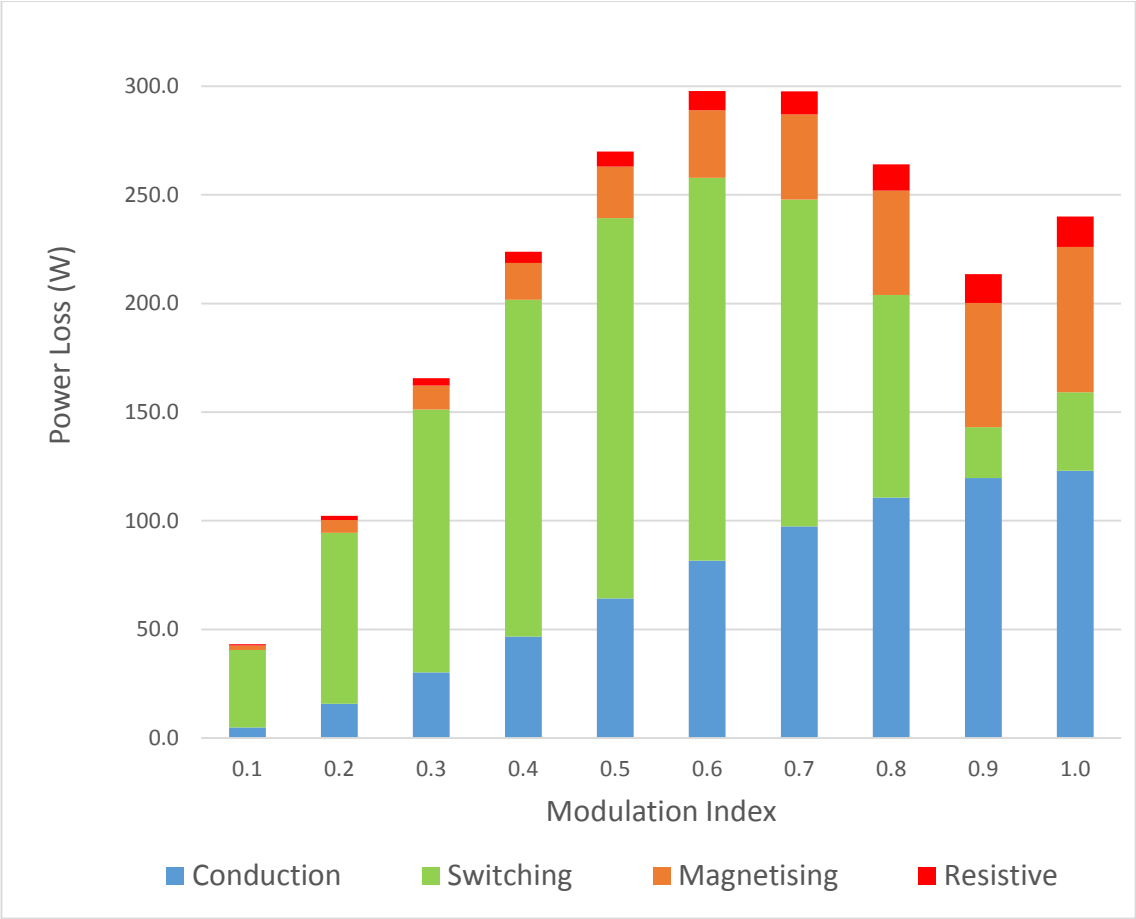


Figure 5.10: LCL MOSFET converter calculated power loss components

For a DAB converter with similar dc voltages the losses for forward and reverse operation will be similar. However, when the dc voltage levels differ, so may the losses. As an example of a converter with mixed voltages, the 2.5 kW converter in [75], used IGBTs in Bridge 1, which had a dc link voltage of 380 V, and MOSFETs in Bridge 2, which had a dc link voltage of 50 V. For reverse operation the losses are significantly larger than for forward operation. For reverse operation the IGBTs in Bridge 1 operate in rectifier mode, and have a significant diode voltage drop, as evidenced by an increased value of the full power Bridge 1 conduction losses P_{con1}, from 39 W to 73 W, and the associated increase in i_{B2}. For forward operation, Bridge 1 operates as an inverter, and the Bridge 2 MOSFETs act as synchronous rectifiers with somewhat smaller voltage drops.

The calculated performance for the 4 kW prototype LCL converter has been completed. It may now be compared with the experimentally obtained results.

5.6 Experimental Results of LCL Converter

5.6.1 Test Procedure

Figure 5.11 shows the prototype LCL converter of Figure 5.1 connected to the test instruments and power supplies. Tektronix DMM4040 6.5 digit bench meters measured the very small voltages across Kelvin connected resistors connected in series with each supply, to provide the supply current measurement; the sensing resistors had been previously calibrated using the Tektronix meters. A Tektronix MSO4104B four channel digital oscilloscope was used for the capture of the waveforms. Each bridge voltage was measured using Tektronix P5205A 100 MHz isolated voltage probes and the currents were read with Tektronix TCP0150 20 MHz clamp-on type Hall-effect current probes. Each set of measurements was conducted quickly, to avoid significant changes in the operating temperature of the magnetic components; they remained at the ambient temperature of approximately 20°C, which was the temperature used for their loss calculations. This allowed measurements to be conducted in a timely manner, without having to wait for thermal settling to occur.

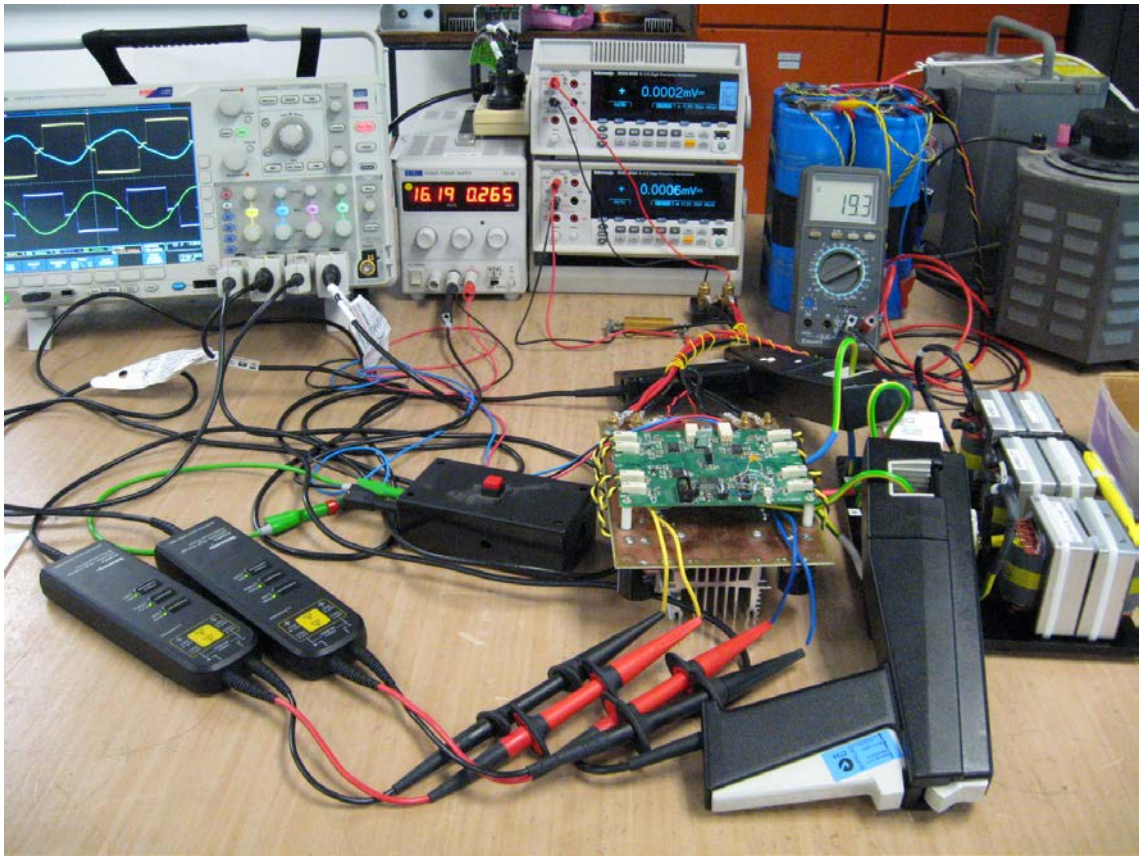


Figure 5.11: LCL DAB converter test setup

5.6.2 LCL Converter Results

This converter was tested over the range of amplitude modulations, with m_1 equal to m_2, for forward and reverse power transfer. For these modulations, measurements were made of the converter's input and output dc currents, I_{DC1} and I_{DC2}, and the rms values of the bridge currents, i_{B1} and i_{B2}. The active widths of the bridge ac voltages, W_1 and W_2, were also recorded; these are the time intervals in each half cycle for which the voltage is non-zero. The input and output powers, P_1 and P_2 for forward operation, were easily calculated from the products of the common dc link voltage, which was fixed at 400 V, and the dc current values. These results are shown in Table 5.9 and Table 5.10.

Mod^n. m	I_{DC1} (A)	I_{DC2} (A)	i_{B1} (A rms)	i_{B2} (A rms)	W_1 (μs)	W_2 (μs)	P_1 (W)	P_2 (W)	Power Efficiency
0.1	0.26	0.19	2.48	2.25	0.64	1.28	103	74	0.722
0.2	1.08	0.91	4.47	3.34	1.64	2.32	433	365	0.844
0.3	2.31	2.04	6.16	4.93	2.68	3.36	922	814	0.883
0.4	3.81	3.46	7.66	6.43	3.6	4.36	1525	1383	0.907
0.5	5.45	5.02	8.95	7.79	4.64	5.4	2179	2009	0.922
0.6	7.04	6.57	10.00	8.99	5.64	6.36	2817	2629	0.933
0.7	8.50	8.02	10.90	10.10	6.64	7.36	3401	3209	0.944
0.8	9.69	9.23	11.60	11.00	7.7	8.28	3877	3693	0.953
0.9	10.39	9.97	12.00	11.60	8.7	9.2	4156	3988	0.960
1	10.70	10.28	12.10	11.90	10	9.92	4280	4114	0.961

Table 5.9: Results for forward operation of LCL DAB converter

Mod^n. m	i_{DC1} (A)	i_{DC2} (A)	i_{B1} (A rms)	i_{B2} (A rms)	W_1 (μs)	W_2 (μs)	P_1 (W)	P_2 (W)	Power Efficiency
0.1	-0.20	-0.27	1.49	2.56	1.32	0.68	-80	-110	0.728
0.2	-0.93	-1.10	3.18	4.56	2.36	1.64	-370	-438	0.846
0.3	-2.07	-2.34	4.87	6.35	3.32	2.68	-826	-935	0.883
0.4	-3.50	-3.86	6.35	7.82	4.32	3.68	-1400	-1542	0.908
0.5	-5.04	-5.48	7.72	9.12	5.36	4.68	-2017	-2191	0.921
0.6	-6.62	-7.09	8.96	10.20	6.36	5.56	-2648	-2835	0.934
0.7	-8.08	-8.56	10.00	11.10	7.36	6.6	-3231	-3423	0.944
0.8	-9.25	-9.71	10.80	11.70	8.36	7.72	-3702	-3886	0.953
0.9	-10.04	-10.46	11.40	12.10	9.4	8.64	-4016	-4185	0.960
1	-10.29	-10.71	11.70	12.20	10	9.96	-4116	-4285	0.961

Table 5.10: Results for reverse operation of LCL DAB converter

Although the theoretical and measured results generally have a close agreement, there are some discrepancies which occur as a result of aspects which weren't accounted for in the theory.

The values of the measured bridge rms currents shown in Table 5.9 and Table 5.10 don't match those predicted by the theory, shown in Table 5.3 and Table 5.4, especially for smaller modulations. There are two, opposing, mechanisms which cause the current values to differ. Firstly, the theoretical values were based on calculations which didn't include any power losses. Under these conditions, the values of i_{B1} and i_{B2} should be equal for a matched network; this is borne out, almost exactly, in the data of Table 5.3 and Table 5.4. In practice the network power losses have to be supplied from additional current taken from the relevant bridge, causing an increase in the bridge currents. The second factor, which hasn't been allowed for in the theory, is the dead-band width. A smaller width of the bridge voltage active region results in smaller measured current and power values than that predicted theoretically for that value of modulation; this applies to both the ac and dc links. This effect is greatest for small modulations, in which, as a result of the dead-bands, one bridge voltage has a smaller active region and the other has a larger active region; the net effect is a reduction in power, which varies as the square of the voltage.

The active width of a bridge voltage is dependent on the ZVS status of that bridge's legs. For converter forward operation, W_1 is in agreement with the width of the Bridge 1 voltage that would result from the expected ZVS status of this bridge. The status is given by Figure 3.11, which shows that leg 1 doesn't have ZVS and leg 2 does, for all modulation levels except at 100 %. For this reason the leading edge of the bridge voltage switches from zero at the end of the dead-band, and the lagging edge returns to zero at the start of the dead-band. For this reason the bridge voltage active width is approximately 350 ns smaller than the product of m_1 and 10 μs. Active width W_2 is approximately 0.35 μs greater than the product of m_2 and 10 μs, for similar reasons. At 100 % modulation all legs obtain ZVS and so the active widths are equal to 10 μs, so that switching takes place at the start of the dead-band. The values obtained for reverse operation are also in agreement with the theory.

Figure 5.12 through to Figure 5.15 show the measured bridge voltage and current waveforms for forward and reverse operation at modulations of 100 % and 70 %. There

is good agreement between these and the theoretical waveforms of Figure 3.14 through to Figure 3.16.

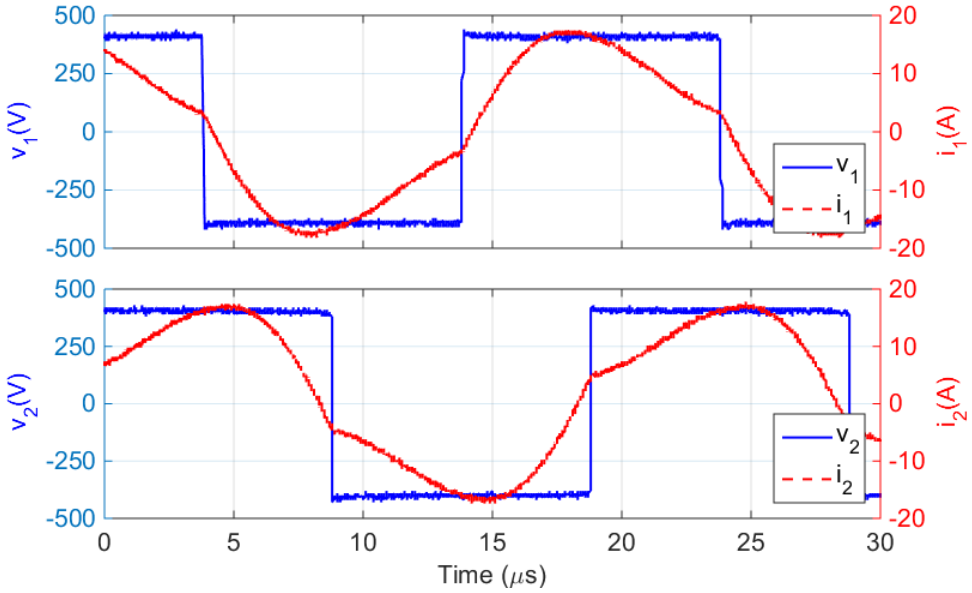


Figure 5.12: LCL bridge waveforms for 100% forward operation

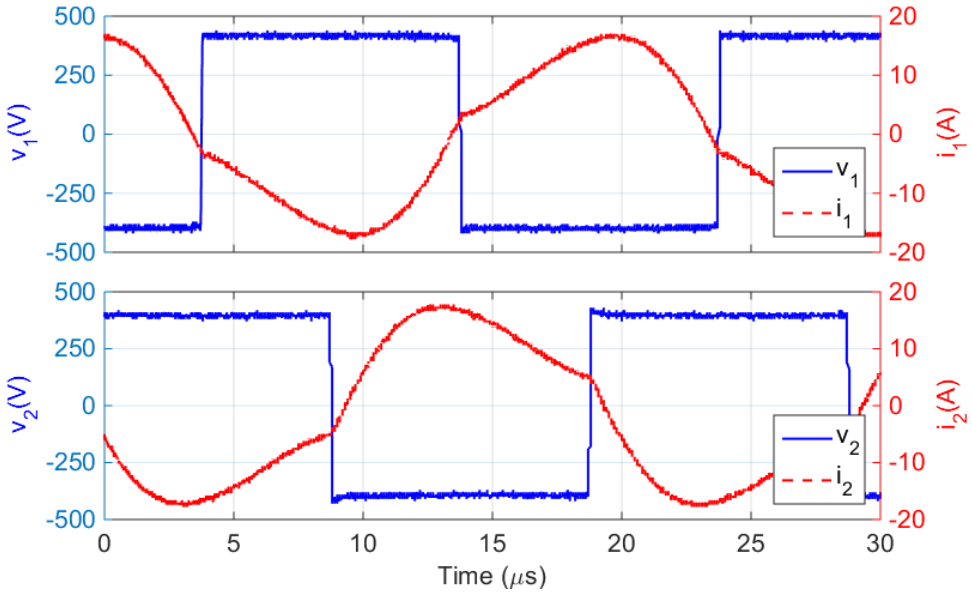


Figure 5.13: LCL bridge waveforms for 100% reverse operation

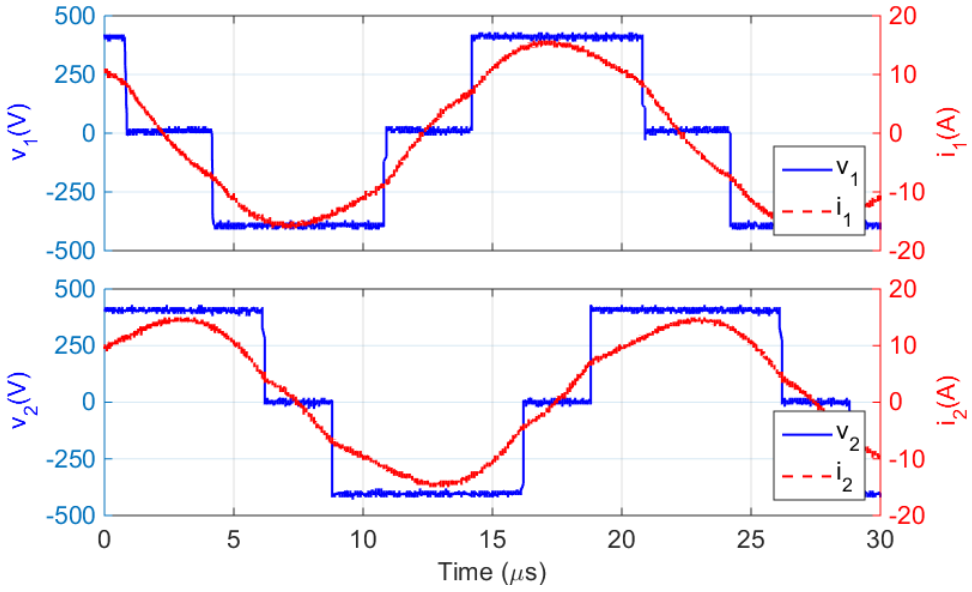


Figure 5.14: LCL bridge waveforms for 70% forward operation

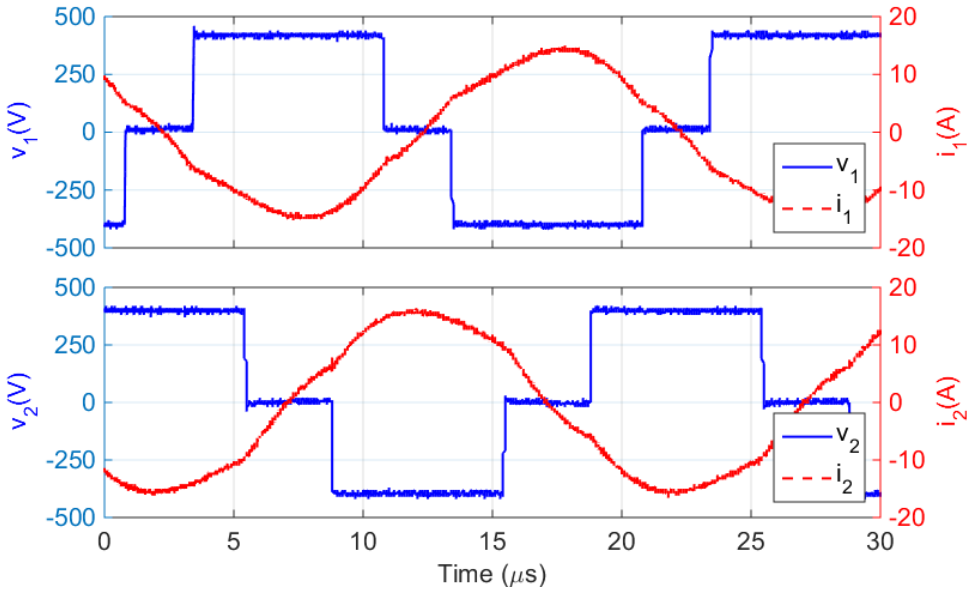


Figure 5.15: LCL bridge waveforms for 70% reverse operation

Table 5.11 provides a comparison of the theoretical and measured efficiency ratios, for forward and reverse converter operation. Again, there is a good agreement between the values. At the lowest modulation, m = 0.1, the power efficiency is greater than 70% at a power output of 80 W, approximately 2% of full power. At the highest modulations the experimental efficiency values are slightly higher than those predicted by the theory. This may be explained by the magnetic components heating slightly in the course of making the measurements, and therefore having slightly smaller core power losses; the core loss calculations were based on a temperature of 20°C, which is a worst case value.

Modn.	Forward Efficiency		Reverse Efficiency	
	Calculated	Measured	Calculated	Measured
0.1	0.717	0.722	0.718	0.728
0.2	0.839	0.844	0.839	0.846
0.3	0.886	0.883	0.886	0.883
0.4	0.912	0.907	0.912	0.908
0.5	0.927	0.922	0.927	0.921
0.6	0.938	0.933	0.938	0.934
0.7	0.945	0.944	0.945	0.944
0.8	0.949	0.953	0.949	0.953
0.9	0.951	0.960	0.951	0.960
1	0.945	0.961	0.945	0.961

Table 5.11: Power efficiency summary for LCL DAB converter

Another possible error contribution is that the values used for the transistor conduction characteristics were maximum rather than typical values, so that the calculated losses may be overstated.

The theoretical and measured efficiencies are shown in Figure 5.16 and Figure 5.17. Good efficiencies are maintained over a wide power range. The measured efficiencies at 10%, 20% and 100% of maximum power are 84%, 88% and 96%; this compares favourably with representative [28] CDAB efficiencies of 55%, 72% and 88% at the respective powers.

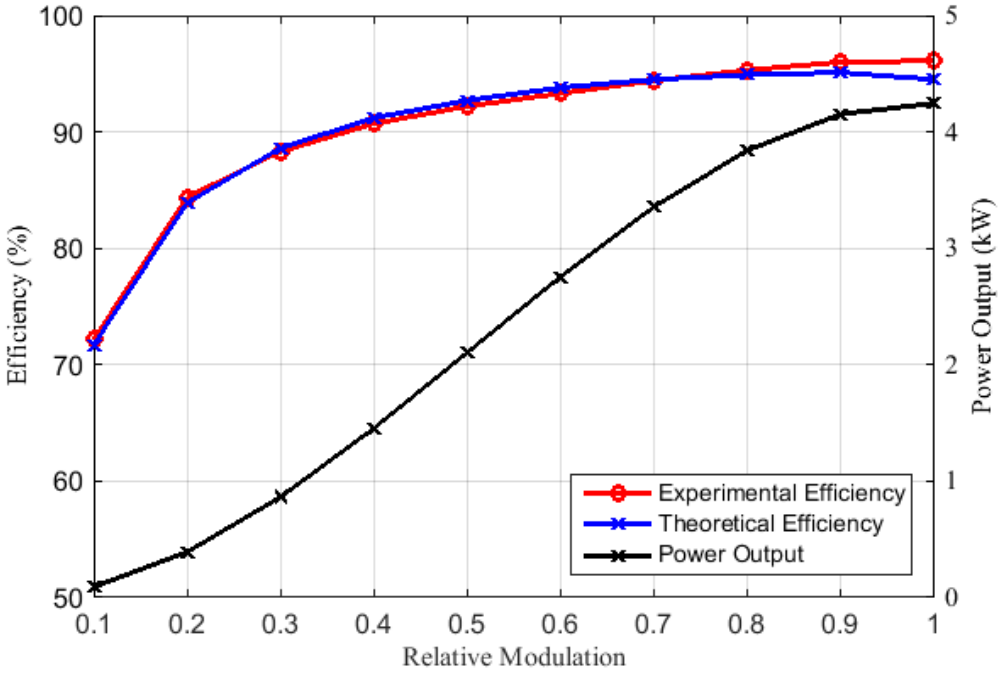


Figure 5.16: Forward power efficiencies of LCL DAB converter

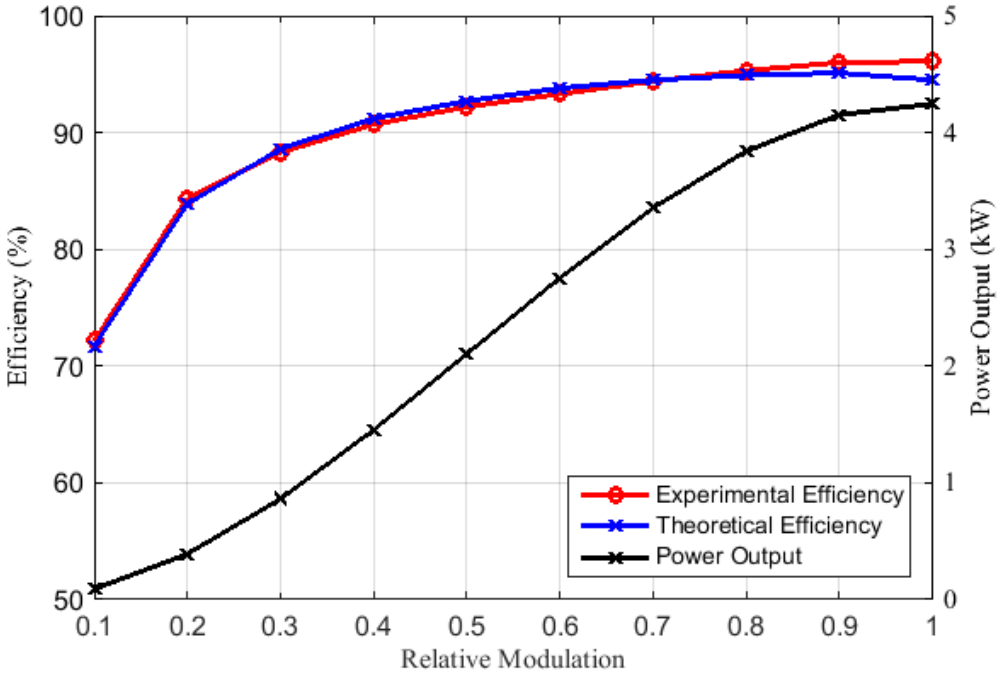


Figure 5.17: Reverse power efficiencies of LCL DAB converter

The results presented to this point have verified the LCL converter's operation for matched bridge dc voltages. The next section will examine the converter's performance for non-unity dcr values.

Variation in dc link voltage

Table 5.12 shows the measured results PE_expt of the power efficiency variation with dcr, for a dcr range of 1.4 to 0.7. For comparison, the calculated results PE_calc, which were recorded in Table 5.5, are also shown. Both the power input and output values are slightly smaller than those calculated, because of the loss of active bridge voltage in the dead-band. While the measured efficiencies are generally close to those predicted by the theory, they are slightly higher at the large modulations because of the conduction losses, which are overstated at the reduced bridge dc voltages. At low modulations the effect of the dead-band, which isn't accounted for in the theoretical model, will have an influence.

	Forward Modulation, dcr = 1.4				Forward Modulation, dcr = 0.7			
	0.2	0.4	0.7	1.0	0.2	0.4	0.7	1.0
V_{DC1}	310	310	310	310	400	400	400	400
I_{DC1}	1.07	3.79	8.47	10.7	0.710	2.49	5.55	7.02
I_{1rms}	4.32	7.50	10.8	11.9	2.98	5.06	7.03	7.83
V_{DC2}	400	400	400	400	258	258	258	258
I_{DC2}	0.694	2.66	6.15	7.87	0.941	3.50	8.06	10.3
I_{B2rms}	2.65	4.95	7.60	8.93	3.01	6.28	9.92	11.6
PE_expt	0.836	0.906	0.937	0.949	0.855	0.907	0.937	0.946
@Pout	278	1064	2460	3148	242	903	2079	2657
PE_calc	0.830	0.907	0.940	0.940	0.819	0.895	0.930	0.928

Table 5.12: Measured effect of dcr variation on the LCL converter efficiency

Measured Magnetising Losses

For the purpose of comparison with the theoretical values which were used, the magnetising losses of each magnetic component were measured by driving it from a single bridge with modulation m_1 ranging from 0.1 to 1, capturing the voltage and current waveforms. As an example, the transformer's waveforms are shown below for a modulation of 100%:

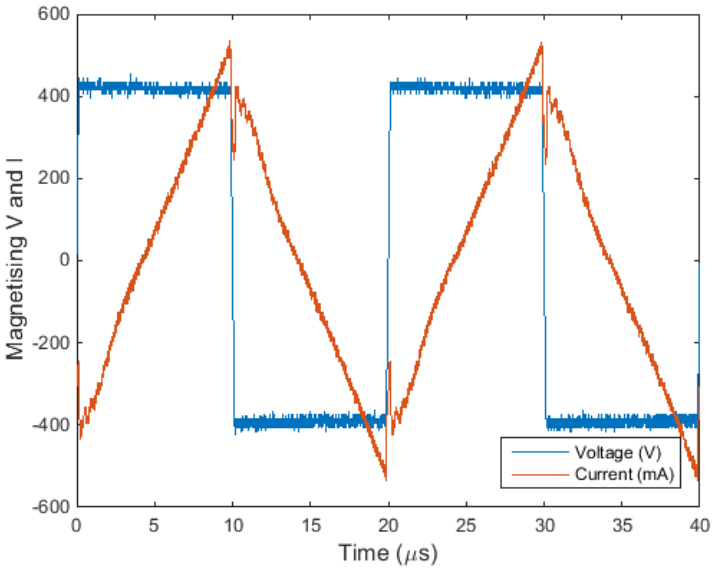


Figure 5.18: Magnetising voltage and current for LCL converter transformer

After loading the CSV file into MATLAB, the loss was calculated numerically from the V-I product over one cycle. The losses, which are shown in Figure 5.19, have a maximum of approximately 24 W for the inductor and 22 W for the transformer. The relationship between the core power losses and the modulation isn't straightforward. The inductor's measured core power loss, neglecting the deviation at modulation index values

of 0.2 and 0.3, is almost directly proportional to the modulation. The transformer's loss is approximately proportional to the modulation raised to the power of 1.4. Although neither is in agreement with the theory, a Steinmetz model should prove to be adequate at high modulation values and the error in the losses will not be significant at the smaller modulations.

There is the possibility of significant errors in the measurement process described. A skew between the voltage and current values will result in a variation in the power loss calculated from their product; such a skew will occur if there are dissimilar phase delays in the voltage and current channels, or their sensors. A test conducted found that a one sample shift, corresponding to 4 ns, caused a 20% error. A related effect, of finite measurement bandwidths, also contributes to these errors, particularly for narrow voltage waveform pulse widths which have a relatively large high frequency content.

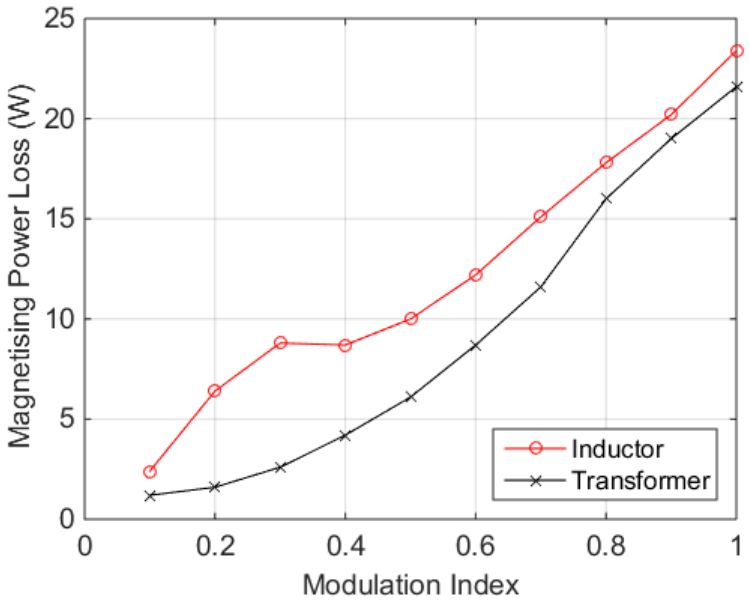


Figure 5.19: Magnetising power losses for LCL DAB converter

In this section it has been shown that the measured performance of the LCL converter closely matches that which was predicted in Section 5.5; this includes the voltage and current waveforms and values, and the power throughput and losses. In the next section the CLC converter is investigated both through calculated results and through experimental measurements.

5.7 CLC Prototype Converter

5.7.1 Introduction

Two CLC DAB resonant converters were laboratory tested. The first [80] was a CLC converter with a maximum power throughput of 4 kW, running from two 400 V dc power supplies, with IGBTs in both bridges. Its inductor was integrated into its transformer, as the latter's leakage reactance.

The second, the 4 kW converter covered in this thesis, used IGBTs in both bridges, had 400 V dc for both power supply rails and had its inductor implemented as a discrete unit. It was analysed, with an ideal circuit, in Section 4.4.

5.7.2 CLC Prototype Circuit and Test Hardware

This is shown in Figure 5.20. As with the LCL converter, no effort was taken to isolate the two bridges of the prototype; the advantages of using a common power supply were outlined in Section 5.2.1 on the LCL DAB converter.

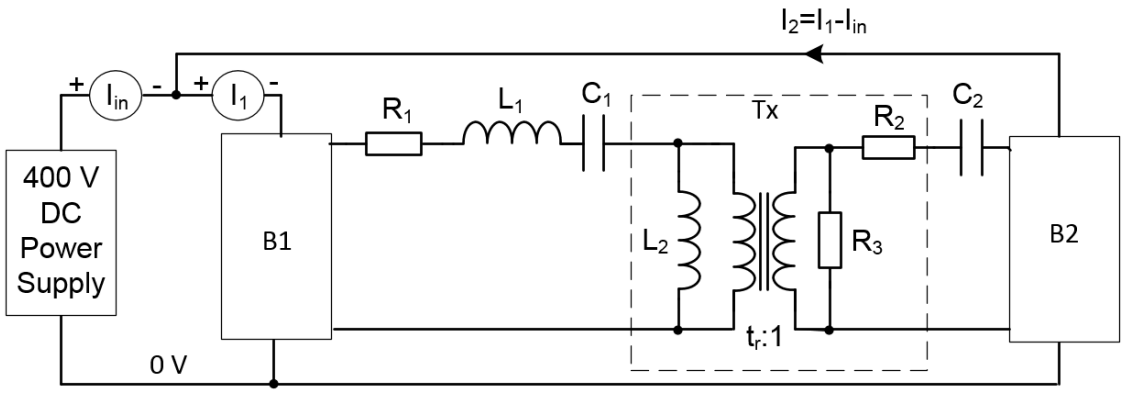


Figure 5.20: CLC DAB converter test configuration

As well as their resonant function, capacitors C_1 and C_2 prevent the occurrence of a magnetic dc bias, and therefore transformer core saturation; no special precautions are required to guard against bridge imbalance occurring during open loop testing.

STGWA19N60 IGBTs were used to implement both bridges of the converter. Their driver circuitry used a 16 V power supply and capacitively coupled outputs, so that it provided voltage levels of +12 V when 'on' and -4 V when 'off'. A dead-band of 350 ns was used.

A picture of the converter's resonant circuit components is shown in Figure 5.21.

Inductor L_1 was implemented as a discrete unit and L_2 as the magnetising reactance of the transformer. Inductor L_1 used an E65 core set with 3C90 material. It was designed to operate at a maximum flux density of 137 mT, so for a core volume of 79 cm^3 its core loss, assuming a sinusoidally varying flux, is 15 W. The transformer used a dual E65 core set, and was designed for a maximum flux density of 125 mT, so that for the assumed triangular flux variation the core loss is 23 W. The value of R_3 which would give the combined core power loss of 38 W at maximum modulation is 4.2 kΩ. However, as this was previously found in the LCL converter magnetising loss measurements to be a poor model, R_3 will be ignored, and the core power loss will be calculated assuming a proportionality to modulation raised to the power of 1.4.

Figure 5.21: CLC DAB converter resonant hardware

5.7.3 CLC Circuit Parameters

A summary of the parameters of this system is shown in Table 5.13. The values of the reactive components used in the test circuit determines the parameters k_1 to k_4, which were previously used for the calculations of the theoretical results shown in Chapter 4. These were based on X_D = 31.83 Ω and f_s = 50 kHz, with k_1 chosen to be 1.

X_D = 31.83 Ω; fs = 50 kHz; maximum power output = 4.3 kW		
Parameter	Ideal Value	Actual Value
V_{DC1}	400 V	400 V
V_{DC2}	400 V	400 V
Inductor L_1: E65/32/27 core set, 3C90 material		
L_1	101.3 μH	99.6 + 1μH, 133 mΩ k_1 = 0.993
C_1	50 nF	48.8 nF, k_2 = 2.049
C_2	100 nF	103.6 nF, k_4 = 0.965
R_1	0	0.133 Ω
R_2	0	0.126 Ω
Transformer: E65/32/27 core set, 3C90 material		
Turns-ratio tr	1	1.01
L_2	101.3 μH (mutual inductance)	101 μH, k_3 = 0.997
L_{prim}	0 (primary-referred leakage inductance)	1 μH, 126 mΩ
Switches, Bridge 1, 2	ST Microelectronics STGWA19N60HD IGBT	

Table 5.13: CLC converter system parameters

5.8 Calculated Power Efficiency of CLC Prototype

Using a similar process to that of the LCL converter in Section 5.4, the MATLAB program *clc_loss_2igbt*, Appendix A, was used to calculate the converter power losses. Table 5.14 and Table 5.15 summarise the power losses at 10 modulation levels, for forward and reverse power transfer respectively.

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	15.0	26.1	30.8	28.5	21.2	25.6	26.6	23.2	16.1	23.1
Pcon1 (W)	5.3	11.3	16.1	19.9	24.2	28.7	32.4	35.4	37.7	38.8
Ptot1 (W)	20.3	37.4	46.9	48.4	45.4	54.3	58.9	58.5	53.8	61.9
Psw2 (W)	19.7	33.9	39.8	37.3	29.7	30.2	31.0	28.8	39.6	58.9
Pcon2 (W)	7.2	17.2	27.0	35.2	42.1	49.1	57.4	66.6	74.6	77.7
Ptot2 (W)	26.9	51.1	66.8	72.5	71.8	79.2	88.4	95.4	114.2	136.7
Pmag (W)	1.2	3.4	6.2	9.6	13.4	17.7	22.3	27.2	32.4	38.0
Pr (W)	1.9	6.4	11.3	15.7	19.3	23.0	27.3	32.3	36.7	38.6
Loss (W)	50.3	98.3	131.2	146.2	150.0	174.1	196.9	213.4	237.2	275.2
P_1 (W)	170	596	1172	1767	2264	2773	3372	3940	4348	4508
P_2 (W)	120	498	1041	1621	2114	2599	3175	3727	4111	4233
Efficiency	0.704	0.835	0.888	0.917	0.934	0.937	0.942	0.946	0.945	0.939
I_1 (Arms)	2.4	4.5	6.1	7.4	8.4	9.3	10.2	11.0	11.7	11.9
I_{B2} (Arms)	3.0	5.4	7.1	8.2	8.9	9.5	10.3	11.3	12.2	12.5

Table 5.14: Summary of CLC calculated efficiency with forward modulation

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	15.0	26.1	30.8	28.5	21.2	25.6	26.6	23.2	16.1	23.1
Pcon1 (W)	5.8	14.5	23.6	32.2	40.4	48.7	57.1	64.7	70.3	72.6
Ptot1 (W)	20.8	40.6	54.4	60.7	61.6	74.3	83.7	87.9	86.4	95.7
Psw2 (W)	19.7	33.9	39.8	37.3	29.7	30.2	31.0	28.8	39.6	58.9
Pcon2 (W)	6.6	13.7	18.9	22.2	25.3	28.8	32.6	37.1	41.2	42.8
Ptot2 (W)	26.2	47.6	58.7	59.5	55.0	59.0	63.6	65.9	80.8	101.8
Pmag (W)	1.2	3.4	6.2	9.6	13.4	17.7	22.3	27.2	32.4	38.0
Pr (W)	1.9	6.4	11.3	15.7	19.3	23.0	27.3	32.3	36.7	38.6
Loss (W)	50.2	97.9	130.6	145.5	149.4	173.9	196.8	213.2	236.4	274.1
P_1 (W)	-123	-502	-1046	-1626	-2121	-2603	-3179	-3731	-4130	-4264
P_2 (W)	-173	-600	-1177	-1772	-2270	-2777	-3376	-3944	-4367	-4538
Efficiency	0.710	0.837	0.889	0.918	0.934	0.937	0.942	0.946	0.946	0.940
I_1 (Arms)	2.4	4.5	6.1	7.4	8.4	9.3	10.2	11.0	11.7	11.9
I_{B2} (Arms)	3.0	5.4	7.1	8.2	8.9	9.5	10.3	11.3	12.2	12.5

Table 5.15: Summary of CLC calculated efficiency with reverse modulation

Switching and conduction losses are recorded for each bridge, as well as the overall resistive and magnetising losses, the bridge currents and the overall efficiency.

From a comparison of the CLC losses in Table 5.14 and Table 5.15 with the LCL losses in Table 5.7 and Table 5.8, it is apparent that the CLC losses are slightly larger. This is due to the larger Bridge 2 switching losses, caused by the slightly higher Bridge 2

rms currents and also by the switching location. The Bridge 2 current at the switching point is seen in Figure 4.8 to be distant from the crossing, relative to the switching point for the comparable LCL waveform in Figure 3.14. A fundamental difference between the LCL and the CLC converters is the difference in the shape of their bridge current waveforms; the CLC converter waveforms have a higher harmonic content and therefore steeper sides. In the region of the current crossings, a small variation in the location of a switching point results in a large change in the value of the current and therefore the switching loss. Although it is common [63, 69-72, 81-83] for resonant systems to be analysed using a fundamental harmonic analysis (FMA), this approximation introduces significant errors, because of the aforementioned effect.

Figure 5.22 shows how the power losses are apportioned between the four major contributors.

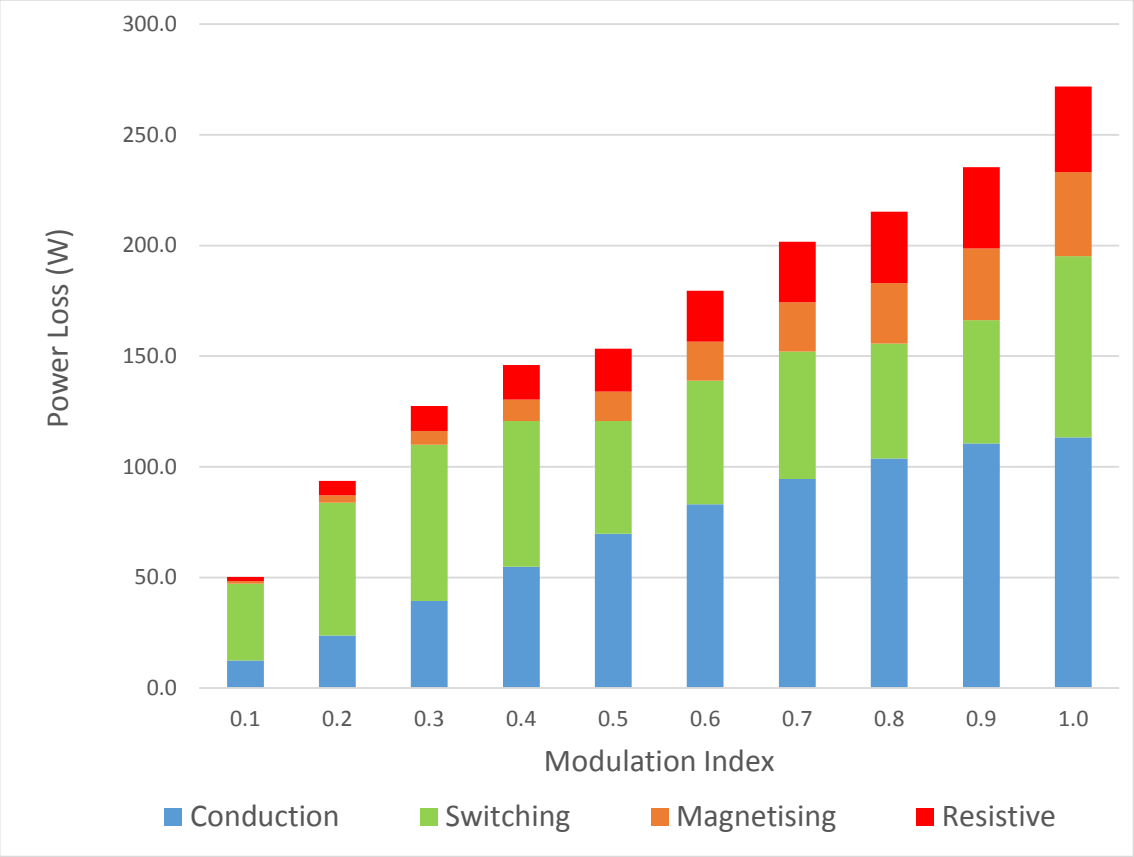


Figure 5.22: CLC IGBT converter calculated power loss components

As with the LCL converter, the losses increase with the modulation value, with the exception of the switching losses which have peaks at modulation indices of 0.3 and 0.7, as expected from the switching current peaks shown in Figure 4.7. The sum of the

magnetic component core and resistive losses is approximately the same in the CLC converter as the LCL converter, but the CLC converter has a greater contribution from resistive losses. This is reasonable, as it has two, rather than three, magnetic components, one of which uses a single core set. The CLC converter has fewer components, and in particular, smaller magnetic components.

Figure 5.23 shows the converter's calculated power efficiency and power as a function of modulation for forward operation. The power loss values in reverse operation are almost identical.

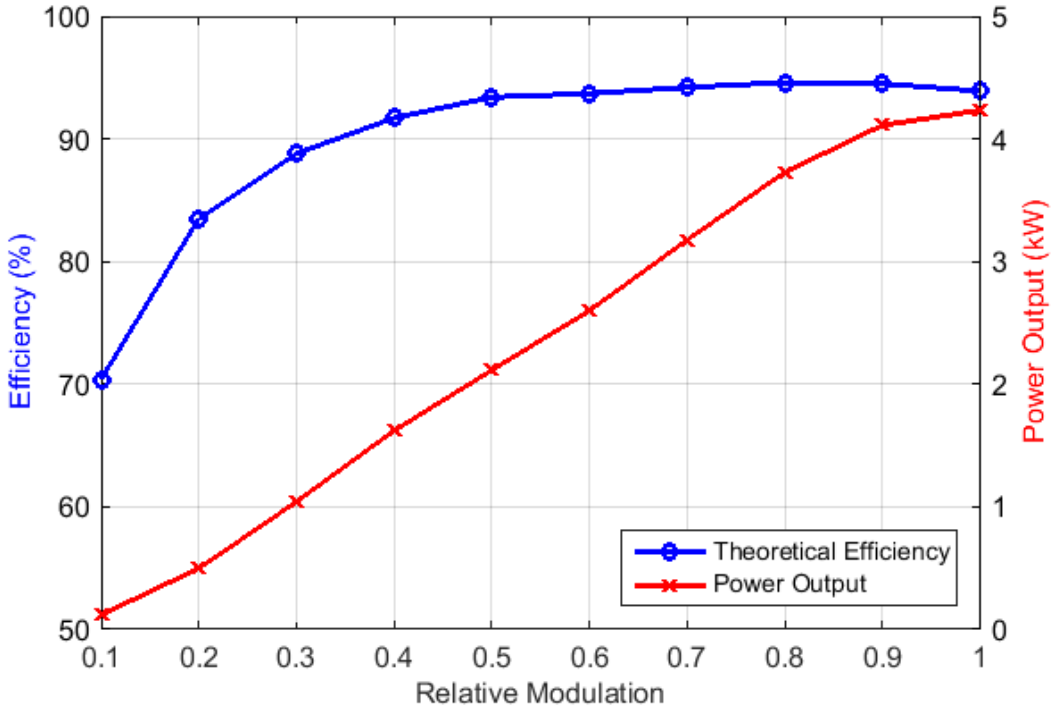


Figure 5.23: CLC converter calculated forward efficiency and power output

Variation in dc link voltage

To predict how the efficiency of the CLC DAB converter is affected by changes in the dcr, tests were conducted with two values of V_{DC1} for four different modulations, forward and reverse, so that a dcr range of 1.4 to 0.7 was achieved. The calculated values PE_calc of the power efficiency are recorded in Table 5.16, in which the previously measured efficiency PE_{400} for $V_{DC1} = V_{DC2} = 400$ V is included for ease of comparison.

	Forward Modulation, dcr = 1.4				Forward Modulation, dcr = 0.7			
	0.2	0.4	0.7	1.0	0.2	0.4	0.7	1.0
V_{DC1}	289	289	289	289	400	400	400	400
I_{DC1}	1.49	4.42	8.42	11.3	1.05	3.09	5.90	7.90
I_{1rms}	4.28	7.25	10.21	11.80	3.36	5.32	7.09	8.40
V_{DC2}	400	400	400	400	277	277	277	277
I_{DC2}	0.87	2.89	5.69	7.58	1.26	4.07	7.94	10.6
I_{2rms}	4.64	6.54	7.54	9.58	4.77	7.63	10.26	12.10
PE_calc	0.806	0.904	0.936	0.932	0.832	0.911	0.932	0.929
@P_{out}	348	1155	2277	3030	348	1127	2200	2937
PE_{400}	0.806	0.894	0.935	0.940	0.806	0.894	0.935	0.939

Table 5.16: Calculated effect of dcr variation on the CLC converter efficiency

The power efficiencies are in close agreement, with the exception of those for small modulations at a dcr of 0.7, which are up to 3% larger. This occurs as a result of the switching loss reduction for a smaller dc link voltage. From the results it is apparent that, for a particular modulation value, the main effect of a reduced dc voltage is the reduced maximum power output.

CLC Converter with MOSFETs in the bridges

The MATLAB program *clc_loss_2fet*, Appendix A, was used to calculate the losses of this converter. Table 5.17 and Table 5.18 show summaries of the power losses at 10 modulation levels, for forward and reverse power transfer respectively.

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	28.0	51.0	62.8	60.7	46.9	80.6	91.6	70.7	20.8	16.1
Pcon1 (W)	3.4	11.9	24.0	36.8	48.4	59.4	71.8	84.7	94.9	99.1
Ptot1 (W)	31.4	62.9	86.7	97.5	95.3	140.0	163.4	155.4	115.7	115.2
Psw2 (W)	14.1	26.3	31.8	29.5	22.4	50.0	61.2	33.8	29.7	45.8
Pcon2 (W)	4.2	9.9	12.8	13.3	14.1	15.9	17.7	20.0	22.1	23.0
Ptot2 (W)	18.3	36.2	44.6	42.8	36.5	65.9	79.0	53.7	51.9	68.7
Pmag (W)	1.2	3.4	6.2	9.6	13.4	17.7	22.3	27.2	32.4	38.0
Pr (W)	1.9	6.4	11.3	15.7	19.3	23.0	27.3	32.3	36.7	38.6
Loss (W)	52.8	108.8	148.9	165.6	164.6	246.5	292.0	268.6	236.7	260.6
P_1 (W)	180	614	1190	1778	2262	2795	3397	3941	4300	4446
P_2 (W)	127	505	1041	1612	2097	2548	3105	3673	4063	4186
Efficiency	0.707	0.823	0.875	0.907	0.927	0.912	0.914	0.932	0.945	0.941
I_1 (Arms)	2.4	4.5	6.1	7.4	8.4	9.3	10.2	11.0	11.7	11.9
I_{B2} (Arms)	3.0	5.4	7.1	8.2	8.9	9.5	10.3	11.3	12.2	12.5

Table 5.17: Summary of MOSFET CLC calculated forward performance

The profile of the losses shown in Figure 5.24 is quite different to that of Figure 5.22 for the IGBT bridges. The MOSFET version has slightly lower total losses at full output power, but has higher losses in the modulation index range of 0.3 and 0.7, where the switching losses peak. The conduction losses for the two different switching devices are very similar, which is purely coincidental, considering that they are generated by very different mechanisms. The magnetising and resistive losses are unaffected by the choice of switches.

Mod^n	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Psw1 (W)	28.0	51.0	62.8	60.7	46.9	80.6	91.6	70.7	20.8	16.1
Pcon1 (W)	2.9	7.0	9.6	10.9	13.0	15.6	17.3	18.3	19.3	19.7
Ptot1 (W)	30.9	58.0	72.3	71.6	59.9	96.2	108.9	89.0	40.0	35.8
Psw2 (W)	14.1	26.3	31.8	29.5	22.4	50.0	61.2	33.8	29.7	45.8
Pcon2 (W)	5.0	16.5	30.9	43.8	53.0	61.3	72.9	87.7	101.8	108.1
Ptot2 (W)	19.1	42.8	62.7	73.2	75.4	111.3	134.2	121.5	131.5	153.9
Pmag (W)	1.2	3.4	6.2	9.6	13.4	17.7	22.3	27.2	32.4	38.0
Pr (W)	1.9	6.4	11.3	15.7	19.3	23.0	27.3	32.3	36.7	38.6
Loss (W)	53.1	110.5	152.6	170.2	168.1	248.1	292.6	270.0	240.7	266.3
P_1 (W)	-111	-475	-1002	-1573	-2068	-2516	-3074	-3633	-4065	-4205
P_2 (W)	-164	-585	-1155	-1743	-2236	-2764	-3367	-3903	-4306	-4472
Efficiency	0.677	0.811	0.868	0.902	0.925	0.910	0.913	0.931	0.944	0.940
I_1 (Arms)	2.4	4.5	6.1	7.4	8.4	9.3	10.2	11.0	11.7	11.9
I_{B2} (Arms)	3.0	5.4	7.1	8.2	8.9	9.5	10.3	11.3	12.2	12.5

Table 5.18: Summary of MOSFET CLC calculated reverse performance

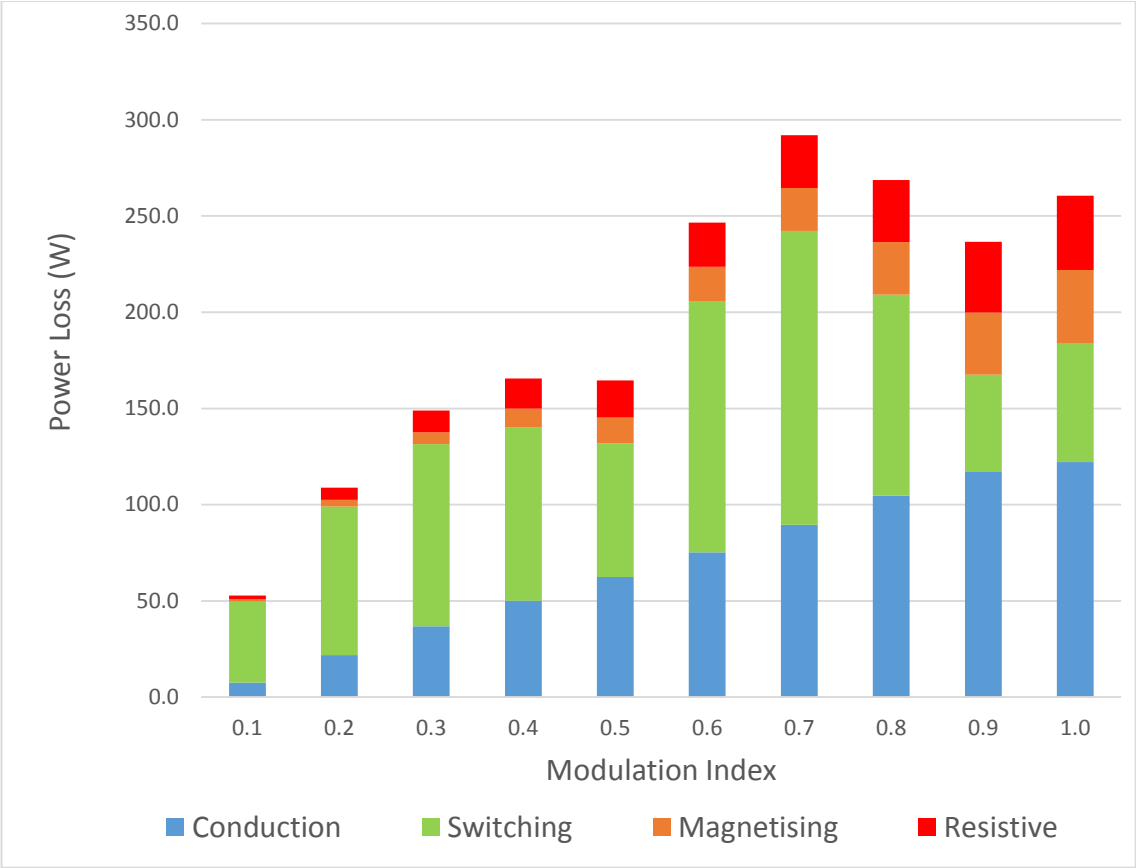


Figure 5.24: CLC MOSFET converter calculated power loss components

The results presented here will be validated by experimental results presented in the next section, which covers the testing of the CLC DAB converter.

5.9 Experimental Results for CLC Converter

5.9.1 CLC Converter Test Hardware and Results

The CLC converter prototype circuit of Figure 5.20 was tested following the same procedure that was used for the LCL converter in Sections 5.6.1 and 5.6.2. The results are shown in Table 5.19 and Table 5.20.

Mod^{n}. m	i_{DC1} (A)	i_{DC2} (A)	i_{B1} (A rms)	i_{B2} (A rms)	W_1 (μs)	W_2 (μs)	P_1 (W)	P_2 (W)	Power Efficiency
0.1	0.29	0.20	1.01	1.47	0.68	1.04	116	82	0.701
0.2	1.22	1.02	1.87	2.40	1.64	2.04	488	406	0.833
0.3	2.69	2.37	6.25	5.30	2.64	3.28	1075	950	0.884
0.4	4.14	3.80	7.85	6.50	3.64	4.32	1654	1518	0.918
0.5	5.33	5.00	8.86	7.70	4.64	5.32	2134	1998	0.936
0.6	6.61	6.20	9.68	9.86	5.64	6.32	2645	2480	0.937
0.7	8.04	7.58	10.40	9.62	6.64	7.32	3217	3032	0.943
0.8	9.35	8.88	11.10	10.50	7.60	8.36	3740	3552	0.950
0.9	10.19	9.75	11.40	11.30	8.60	9.00	4076	3902	0.957
1	10.59	10.1	11.70	11.80	10.0	10.0	4236	4050	0.956

Table 5.19: Results for forward operation of CLC DAB converter

Mod^{n}. m	i_{DC1} (A)	i_{DC2} (A)	i_{B1} (A rms)	i_{B2} (A rms)	W_1 (μs)	W_2 (μs)	P_1 (W)	P_2 (W)	Power Efficiency
0.1	-0.25	-0.35	1.20	1.46	1.32	0.68	-100	-139	0.721
0.2	-1.13	-1.34	2.20	2.00	2.32	1.64	-452	-538	0.840
0.3	-2.40	-2.70	5.20	2.70	3.32	2.68	-959	-1081	0.887
0.4	-3.81	-4.16	6.48	3.22	4.32	3.64	-1522	-1665	0.914
0.5	-5.01	-5.37	7.61	7.80	5.32	4.68	-2006	-2148	0.934
0.6	-6.17	-6.60	8.54	9.70	6.32	5.64	-2470	-2638	0.936
0.7	-7.57	-8.04	9.51	10.4	7.28	6.64	-3029	-3217	0.942
0.8	-8.87	-9.34	10.4	11.1	8.32	7.64	-3548	-3737	0.949
0.9	-9.85	-10.3	11.1	11.9	9.32	8.96	-3940	-4122	0.956
1	-10.29	-10.8	11.4	12.2	10.0	10.0	-4116	-4314	0.954

Table 5.20: Results for reverse operation of CLC DAB converter

At low modulations the values of the measured bridge rms currents are a little smaller than the predicted values given in Table 5.14 and Table 5.15, as a result of the dead-band reducing the active width of the bridge voltages. At high modulations the values of the measured bridge rms currents are a little larger than predicted by the theory because the power losses have to be supplied from additional current taken from the relevant bridge.

For converter forward operation, active width W_1 is in agreement with the Bridge 1 voltage that would result from the expected ZVS status of this bridge. The status is given by Figure 4.7, which shows that leg 1 doesn't have ZVS and leg 2 does, for all modulation levels except at 100 %. For this reason the leading edge of the bridge voltage switches from zero at the end of the dead-band, and the lagging edge returns to zero at the start of the dead-band. For this reason the bridge voltage active width is approximately 350 ns

smaller than the product of m_1 and 10 µs. Active width W_2 is approximately 0.35 µs greater than the product of m_2 and 10 µs, for similar reasons. At 100 % modulation all legs obtain ZVS and so the active widths are equal to 10 µs, so that switching takes place at the start of the dead-band. The values obtained for reverse operation are also in agreement with the theory.

Figure 5.25 through to Figure 5.28 show the measured bridge voltage and current waveforms for forward and reverse operation at modulations of 100% and 70%.

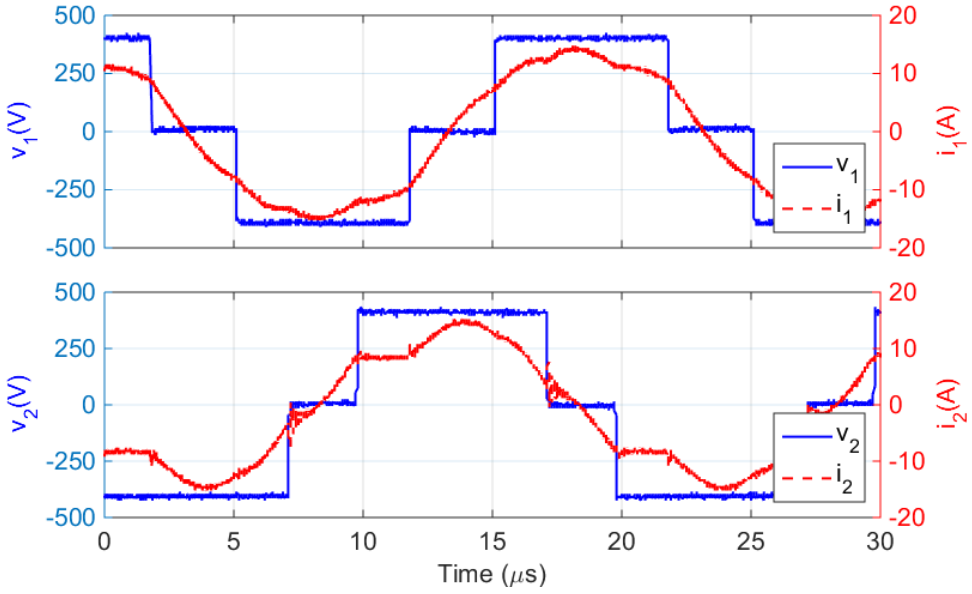


Figure 5.25: CLC bridge waveforms for 100% forward operation

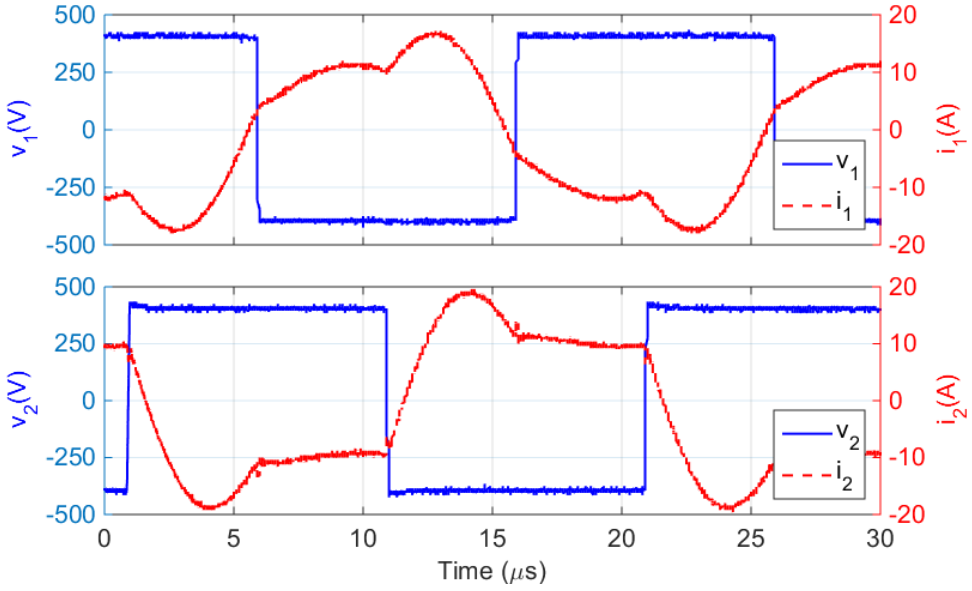


Figure 5.26: CLC bridge waveforms for 100% reverse operation

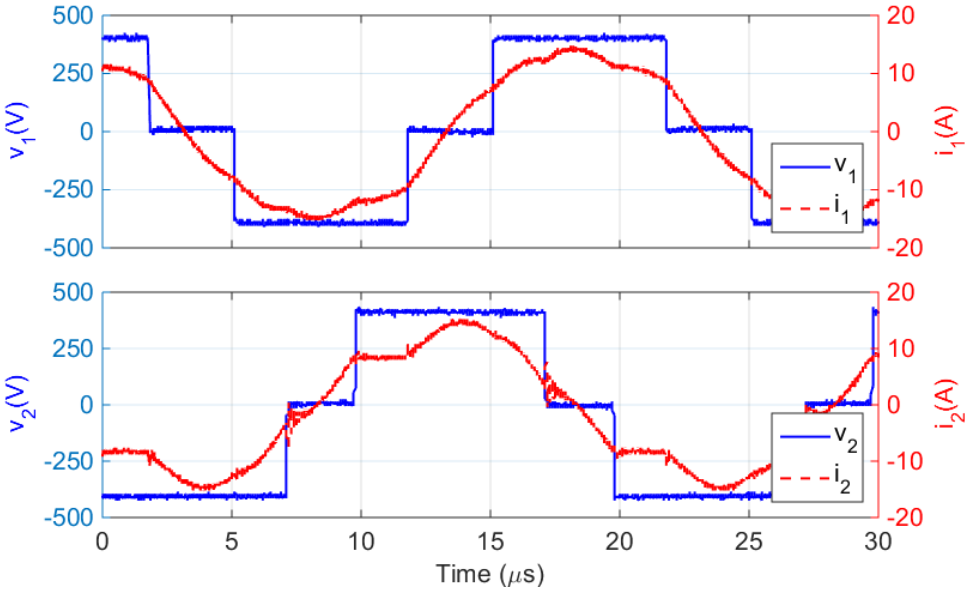


Figure 5.27: CLC bridge waveforms for 70% forward operation

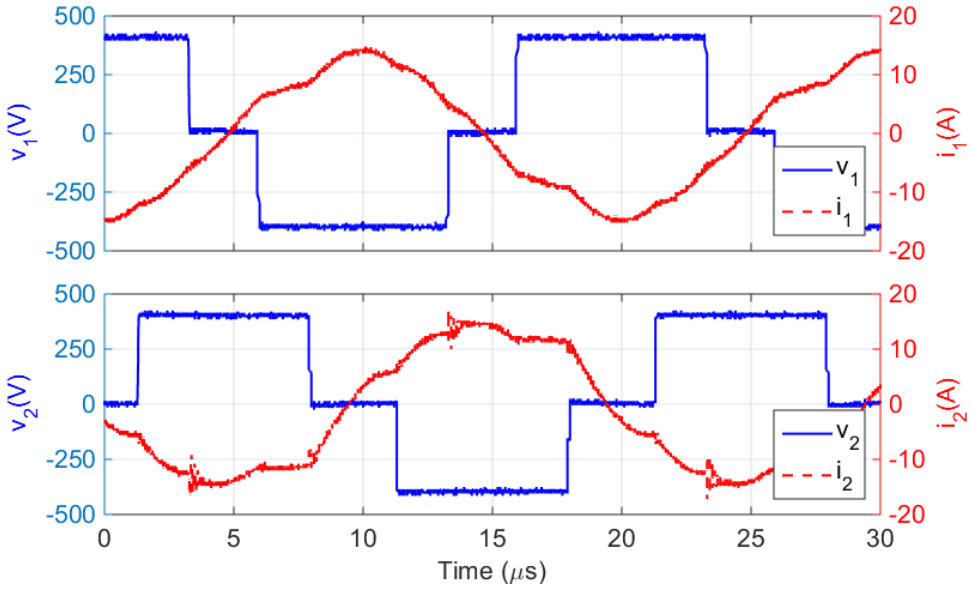


Figure 5.28: CLC bridge waveforms for 70% reverse operation

There is close agreement between these and the theoretical waveforms of Figure 4.8 through to Figure 4.10.

Table 5.21 provides a comparison of the theoretical and measured efficiency ratios, for forward and reverse converter operation.

Modn.	Forward Efficiency		Reverse Efficiency	
	Calculated	Measured	Calculated	Measured
0.1	0.704	0.701	0.710	0.721
0.2	0.835	0.833	0.837	0.840
0.3	0.888	0.884	0.889	0.887
0.4	0.917	0.918	0.918	0.914
0.5	0.934	0.936	0.934	0.934
0.6	0.937	0.937	0.937	0.936
0.7	0.942	0.943	0.942	0.942
0.8	0.946	0.950	0.946	0.949
0.9	0.945	0.957	0.946	0.956
1	0.939	0.956	0.940	0.954

Table 5.21: Power efficiencies of CLC DAB converter

Figure 5.29 and Figure 5.30 show comparisons of the measured and theoretical efficiencies of the CLC DAB converter, for forward and reverse operation respectively. Over most of the range there is close agreement between the theoretical and measured results, including the slight dips in the plots at a modulation index of 0.6. At the highest modulation levels the measured efficiencies are somewhat larger than the calculated efficiencies, as was the case for the LCL converter.

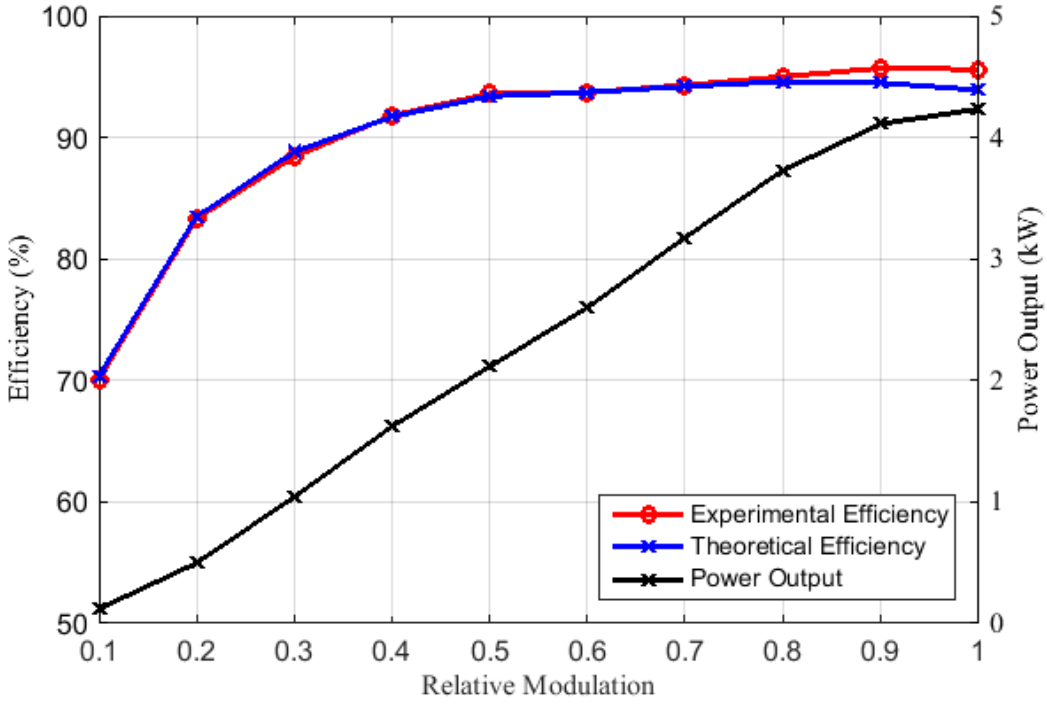


Figure 5.29: Forward power efficiencies of CLC converter

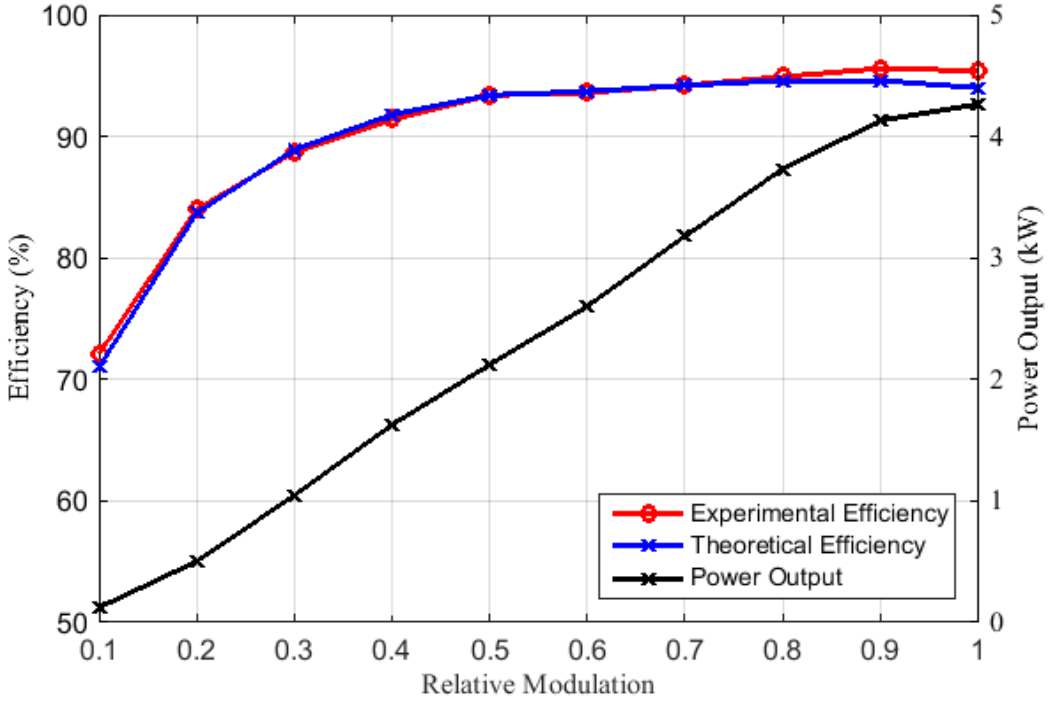


Figure 5.30: Reverse power efficiencies of CLC converter

For the range of power levels the efficiencies of the LCL and CLC converters are very similar.

Variation in dc link voltage

Table 5.22 shows the measured results of the efficiency variation with dcr, for a dcr range of 1.4 to 0.7, for comparison with the calculated results, PE_calc, which were recorded in Table 5.16. While the measured efficiencies are generally close to those predicted by the theory, they are slightly higher at the large modulations because of the

	Forward Modulation, dcr = 1.4				Forward Modulation, dcr = 0.7			
	0.2	0.4	0.7	1.0	0.2	0.4	0.7	1.0
V_{DC1}	289	289	289	289	400	400	400	400
I_{DC1}	1.16	3.93	8.00	10.6	0.94	2.88	5.60	7.42
I_{1rms}	4.28	7.25	10.21	11.80	3.36	5.32	7.09	8.40
V_{DC2}	400	400	400	400	277	277	277	277
I_{DC2}	0.69	2.59	5.41	7.24	1.15	3.83	7.62	10.23
I_{2rms}	4.64	6.54	7.54	9.58	4.77	7.63	10.26	12.10
PE_expt	0.824	0.913	0.937	0.946	0.847	0.919	0.942	0.955
@Pout	275	1036	2165	2896	318	1060	2110	2833
PE_calc	0.806	0.904	0.936	0.932	0.832	0.911	0.932	0.929

Table 5.22: Measured effect of dcr variation on the efficiency of CLC converter

conduction losses, which are overstated at the reduced bridge dc voltages. At low modulations the effect of the dead-band, which isn't accounted for in the theoretical model, will have an influence.

5.9.2 Summary

In this chapter it has been shown that the each of the LCL and CLC converters which were analysed and subsequently tested had very similar performance for forward and reverse operation, as expected for two bridges with the same devices running at the same voltages.

The experimental waveform shapes and values are very similar to those calculated, based on the theoretical analysis presented in Chapters 3 and 4. Further, the experimental work has proven the viability of the resonant converters proposed. When controlled with equal bridge modulations the power throughput is proportional to the square of the modulation index.

The LCL and CLC DAB resonant converters obtain high power efficiencies over a wide power range, and their operation is relatively insensitive to variations in the dc conversion ratio. For unity dcr the measured power efficiencies of the prototypes increased from a minimum of approximately 84% at 10% of maximum power output to a maximum of approximately 95% at maximum power output.

There is scope for hardware improvements. The resistive and magnetising losses in the magnetic components are a large portion of the overall losses, so their reduction would lead to a significant improvement in power efficiency. Integration of one of the inductors into the transformer, as a leakage reactance, should reduce the converter's size and cost.

From the loss analysis it is concluded that a low voltage, high current bridge is best implemented with MOSFETs, for which their low on resistance may be used to advantage to obtain low conduction losses, both in the 1st quadrant in the inverting bridge and in the 3rd quadrant in a rectifying bridge. In contrast, as was observed for the converters referred to in this thesis, a high voltage bridge is best implemented with IGBTs, for which their small switch-on energy losses are an advantage for leg operation with ZCS.

The LCL converter uses more components than the CLC converter and will therefore be larger and more expensive, but has a slightly better efficiency and has a current harmonic content which is lot smaller. This comparison, and comparisons with other converter types, is fraught with the significant dependence of the performance of the

converters on the particular hardware used in that converter's implementation. Nor is it obvious what the best hardware configuration is. In the case of the CLC converter there is also the degree of freedom in the choice of parameter k_1, which determines the relative reactance value of L_1. The next chapter will attempt to answer these questions.

6 Converter Comparisons and Optimisation

6.1 Introduction

In Chapters 3 to 5 the performance characteristics of the LCL and CLC converters were developed theoretically and validated through laboratory testing. This chapter compares the performances of these resonant converters with that of a CDAB converter operating under fixed conditions and, after optimisations have been performed, under varying conditions.

In the first comparison, in Section 6.2, some key conversion metrics will be calculated for the CDAB and the resonant converters under the same, fixed, operating conditions. For this comparison, the LCL and CLC converters will be operated with their standard form of modulation, comprising a fixed ϕ of $\pm 90°$ and equal bridge modulations m_1 and m_2, and the CDAB converter with SPS modulation. While this comparison is not complete, as it does not account for the wide range of hardware and operating environment variations, it does provide an easily assimilated view of the salient performance parameters.

For the resonant converters in their standard form, the modulation was chosen to minimise the conduction losses by keeping the bridge voltages and currents in phase with each other, thereby minimising the reactive current and power components. However, it is possible to obtain better power efficiency by using a more general modulation technique, taking full advantage of the three angles which may be controlled. While this is necessarily more complicated, in practice it is easily implemented by a field programmable gate array (FPGA) controller which holds pre-calculated modulation profiles in its memory. The map of these profiles may also accommodate other input variables, such as the dc link voltages, as well as the required magnitude and direction of the power transfer. With this in mind, Section 6.3 examines the performance obtained by the LCL and CLC converters for the case where their modulation is optimised to provide the highest power efficiency at each setting of power throughput, while operating under fixed conditions.

A database of these optimal modulation profiles, assembled from a range of operating conditions, will be used in Section 6.4 for the design of optimal converters that will operate within a specified set of conditions. After taking hardware variations into

account, this will enable a comprehensive comparison of the three converters to be made on a cost basis for converters designed to meet the same specification. By quantifying the comparison, the subjective aspects are removed.

The next section will compare the performances of non-optimised converters, converters in their standard form.

6.2 A Comparison of LCL, CLC and CDAB Converters

This comparison has been made between LCL, CLC and CDAB converters which have each been designed for a maximum power output of 4 kW when running from equal dc link voltages of 400 V. Each converter has a switching frequency of 50 kHz, and uses the same IGBT switches that were previously used in each bridge; this minimises the hardware variations between converters, enabling a better comparison. Switching and conduction power losses have been included in the calculations. The resistive and magnetising power losses of the magnetic components have not been included in the calculations, for two reasons: Firstly, these losses should be relatively small compared to the conduction and switching losses, and therefore don't have a large effect on the overall power efficiency. Secondly, the losses may take on a large range of values which are dependent on the size and cost of the magnetic components. The converter power efficiencies, PE, have been calculated at 20%, 50% and 100% of the maximum power output.

For the analysis the transformers were assumed to have symmetrically distributed integral leakage inductances, as shown in Appendix C, and the magnetising inductances of the LCL and CDAB converters were assumed to be large compared to the design reactance. In each case the transformer turns ratio t_r was set to 1, which would be expected to be optimal for a converter that behaves symmetrically and which has equal dc link voltages.

Two CDAB converters were analysed, with maximum modulation angles ϕ of 0.36π and 0.5π radians; the first limit is commonly used in practice, and the second limit is often used by academics [9, 30, 84]. Two CLC versions were analysed, in which the L_1 proportion of the design reactance, k_1, had values of 0.6 and 1; these values were selected, based on the discussion around Figure 4.4, as the expected extremities of the range of k_1.

Each converter uses its standard modulation; the CDAB uses SPS modulation, and the resonant converters use a fixed inter-bridge phase shift of 90° and equal values of PWM for each bridge. The value of the design reactance, X_D, was selected to obtain the required maximum output power at the maximum modulation; equations (1), (12) and (28) are used for the CDAB, LCL and CLC converters respectively, and the switching and conduction power losses were calculated as detailed in Section 5.3. The analysis results are shown in Table 6.1.

Converter type, design reactance and parameter	Power Output (W)	PE (%)	Results for maximum power			
			Peak Bridge Current (A)	AC Bridge Current (Arms)	DC Link Ripple Current (Arms)	[L_1] Trfmr Size (V.μs.Arms)
LCL X_D = 32.1 Ω	4000	0.966	16.1	11.3	4.9	[37k]+98k 135k
	2000	0.942				
	800	0.902				
CLC X_D = 33.2 Ω k_1 = 1	4000	0.963	16.4	11.2	4.5	123k
	2000	0.949				
	800	0.901				
CLC X_D = 34.8 Ω k_1 = 0.6	4000	0.953	19.3	11.7	5.1	116k
	2000	0.950				
	800	0.828				
CDAB X_D = 29.8 Ω φ_{max} = 0.5	4000	0.912	21.1	17.2	13.7	138k
	2000	0.951				
	800	0.960				
CDAB X_D = 27.7 Ω φ_{max} = 0.36	4000	0.930	16.4	14.2	9.7	114k
	2000	0.952				
	800	0.960				

Table 6.1: Converter comparison for standard modulation

For each of these converters, with equal dc link voltages, the values of the bridge AC currents are the same for each bridge. However, the average dc link currents into Bridge 1 and out of Bridge 2 differ as a result of the power losses, which are also reflected in the power efficiencies.

The size of the DC link ripple current, along with the source impedance, affect the size of the capacitor smoothing the dc link voltage. Its value shown in the table is the average of the values for each bridge; the Bridge 1 calculation is given by:

$$I_{ripl\_1} = \sqrt{I_{DC1\_ms} - {I_{DC1}}^2} \tag{44}$$

Where:

I_{ripl_1} is the rms value of the ac component of the Bridge 1 dc link current

I_{DC1_ms} is the mean squared value of the Bridge 1 dc link current

I_{DC1} is the average value of the Bridge 1 dc link current

From Table 6.1 it can be seen that the resonant converters have DC link ripple currents which are half that of the CDAB converters, and will therefore require smaller DC link capacitors.

The last column of the table shows the product of the component's rms current and its total volt-second product. As an example, L_1 in the LCL converter has a maximum rms current of 11.3 A and a maximum volt-second product of 3300 V.μs, resulting in a "Size" of 37290 V.μs.Arms. For this converter the transformer has equal primary and secondary currents of 11.3 Arms and primary and secondary volt-second products of 4664 V.μs and 4000 V.μs, so that its "Size" is the sum, which is equal to 97903 V.μs.Arms. For a power dissipation limited design the volume and cost of a magnetic component are approximately proportional to the calculated "Size" value, as shown in (64) in Appendix B.

From Table 6.1 it can be seen that the three resonant converters have better power efficiencies at full power than the CDAB converter for the stated conditions, with unity dcr. Also, it has been seen in Chapter 5 that for the LCL and CLC converters these power efficiencies aren't affected significantly by dcr variations; this is not the case for CDAB converters. A better full-power efficiency has the added advantage of a smaller heatsink requirement; for a PE value of 0.966, as for the LCL converter, the heatsink is only required to dissipate approximately 141 W, whereas 301 W must be dissipated for a converter having a PE of 0.93, as is the case for the better of the two CDAB converters.

The bridge and dc link ripple currents for the three resonant converters are significantly smaller than those of the CDAB converter. The peak currents are comparable, with the exception of the CDAB with the large maximum modulation angle. As with the previously mentioned heat dissipation, these stresses affect transistor selection and reliability.

Compared to the CDAB converter having a φ_{max} of 0.36, which has the better performance, the resonant converters have larger magnetic components; marginally larger in the case of the CLC converter, and approximately 40% larger in the case of the LCL converter. As well, the LCL converter has a capacitor, and the CLC converter has two capacitors. While these are low cost items compared to the magnetic components, they will add to the size.

In a choice between these converters, there are competing factors; the resonant converters offer better performance than the CDAB converter in every respect, but are larger and may have a larger cost. The CLC converter offers the best compromise between hardware cost and performance, although the LCL converter has marginally greater power efficiency, smaller currents and a reduced harmonic content. In choosing between the two CLC converters, with different k_1 values, there is compromise between the slightly smaller bridge and dc link currents for a large k_1, as stated in the discussion involving Figure 4.4, and the smaller transformer size for a small k_1. The variation in performance and size is very small, so a k_1 value at the top of the range would appear to be best.

The overall size of, for example, a CLC converter, may not be very different in practice from that of the CDAB converter, when the more onerous thermal conditions of the latter, requiring a significantly larger heatsink, are taken into account. Also, this analysis has not taken into account the resistive and magnetising losses of the transformer; for a given power level the LCL and CLC converters have smaller currents than a CDAB converter, and therefore smaller resistive losses. The size of the transformer also has a large effect on the overall converter size. For a CLC converter the magnetising reactance is equal to the design reactance, whereas the magnetising reactance in a CDAB converter would ideally be a lot larger than the design reactance, resulting in a larger transformer. In Section 6.4, a comprehensive analysis of the three converters will address these issues.

In the next section, the performance of the optimised LCL and CLC converters, without the constraints of the standard modulation, will be examined.

6.3 Optimised Operation at Fixed DC Link Voltages

The LCL and CLC converters to be optimised are identical to those of Section 6.2, and have the parameters shown in Table 6.1. As before, the values of X_D that were used were such that the required output power was achieved with maximum bridge

modulations m_1 and m_2, with a fixed φ. For smaller output powers, there is the freedom to change all three modulation angles in order to obtain the best power efficiency.

6.3.1 Theoretical Performance of Optimised LCL Converter

An initial optimisation of this converter, using MATLAB's *fmincon*, failed to reach optimal values of the three modulation angles which would minimise the power loss and therefore the power input, for a given required power output. This was due to the process pursuing a local minimum to its end point. For this reason an exhaustive search procedure was adopted instead. While this procedure is guaranteed to converge to a solution, it has the disadvantages that the solution is not exact, as the variables are discretised, and the process is slow.

Using an exhaustive search optimisation, program *lcl_modopt_p10* in Appendix A, the optimum modulation values were found to minimise the input power for a desired output power. The program uses three nested loops, one for each modulation angle. It uses index step sizes of 0.02 in the two outer loops, for φ and m_1, while the inner loop successively adjusts m_2 until the output power has converged within a 1% tolerance band of the desired output power. By linear extrapolation the final values of the input and output powers and the currents are obtained with good accuracy, negating the effects of discretised variables. For this converter, the performance was calculated for output powers in 10% steps of the maximum power output as shown in Table 6.2:

P_{in} (W)	460	877	1286	1694	2101	2506	2910	3310	3706	4108
P_{out} (W)	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	0.20	0.20	0.20	0.24	0.28	0.30	0.34	0.36	0.38	0.44
m_1	0.28	0.40	0.54	0.56	0.62	0.68	0.74	0.74	1.00	0.98
m_2	0.30	0.42	0.50	0.56	0.59	0.66	0.69	0.88	0.88	1.00
i_1 (A)	5.17	6.97	7.86	8.67	8.89	9.55	9.82	10.83	10.93	11.47
i_2 (A)	4.92	6.67	8.35	8.64	9.17	9.76	10.21	10.19	11.10	11.47
i_{b2} (A)	4.92	6.66	8.35	8.64	9.16	9.76	10.21	10.19	11.10	11.47
i_{c1} (A)	9.40	12.86	15.37	16.04	16.32	17.21	17.24	17.71	18.14	17.63
Vs_{L1} (V.μs)	1638	2167	2373	2432	2593	2872	3033	3303	3442	3413
Vs_{M1} (V.μs)	2758	3767	4533	4672	4783	5000	5015	5205	5341	5054
Vs_{M2} (V.μs)	1188	1688	2000	2250	2375	2625	2750	3500	3500	4000
PE	0.869	0.912	0.933	0.945	0.952	0.958	0.962	0.967	0.971	0.974

Table 6.2: LCL converter results for optimal modulation

Where:

PE is the power efficiency

Vs_{L1} is the volt-second product of L_1 in Figure 3.3 (V.μs)

Vs_{M1} is the volt-second product of v_3 in Figure 3.3, for L_2 integrated into the transformer (V.μs)

Vs_{M2} is the volt-second product of v_{B2} in Figure 3.3, at the transformer secondary (V.μs)

As the previous forward power transfer data in Table 5.3 were calculated for ten amplitude modulation values, rather than for 10% steps of the output power, the non-optimised results are shown in this same format, for comparison, in Table 6.3. They were obtained from the same program by forcing m_1 to equal m_2.

P_{in} (W)	464	889	1303	1715	2124	2530	2935	3331	3728	4141
P_{out} (W)	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
m_1	0.21	0.30	0.38	0.44	0.50	0.56	0.63	0.72	0.81	1.00
m_2	0.21	0.30	0.38	0.44	0.50	0.56	0.63	0.72	0.81	1.00
i_1 (A)	3.82	5.33	6.31	7.28	8.11	8.85	9.56	10.00	10.61	11.32
i_2 (A)	3.82	5.33	6.31	7.28	8.11	8.85	9.56	10.00	10.61	11.32
i_{b2} (A)	3.82	5.33	6.31	7.28	8.11	8.85	9.56	10.00	10.61	11.32
i_{c1} (A)	5.47	7.61	8.97	10.33	11.50	12.53	13.53	14.14	15.01	16.04
Vs_{L1} (V.μs)	1556	1895	2048	2183	2355	2537	2715	2953	3138	3300
Vs_{M1} (V.μs)	1440	1996	2477	2840	3183	3502	3792	4160	4436	4664
Vs_{M2} (V.μs)	844	1188	1500	1750	2000	2250	2500	2875	3250	4000
PE	0.862	0.900	0.921	0.933	0.942	0.948	0.954	0.961	0.966	0.966

Table 6.3: LCL converter results for no optimisation

Comparing these two, the greatest improvement in power efficiency of approximately 1.2 percentage points occurs below the centre of the power range, with a smaller improvement at the ends. An improvement of 0.8 of a percentage point in the efficiency at maximum power output occurs with a very small change in the angles; the power output without losses, as given by (12), has reduced, but the power losses have reduced even more. The optimised converter has slightly greater rms currents and greater magnetising volt-second products, as shown in the last column. As a result of this the magnetic components will be larger and therefore more expensive.

As an illustration of the change in the power losses that have occurred in the optimisation process, the waveforms of the optimised converter for a power throughput of 2400 W are shown in Figure 6.1, and Table 6.4 shows the switching and conduction losses of each converter leg, where:

I_{sw} is the turn-on current for the transistors in the leg

E_{off} and E_{on} are the turn-off and turn-on switching energy losses for each transistor in the leg

P_{sw} is the switching power loss for that leg

P_{con} is the conduction power loss for that leg

P_{sum} is the sum of the switching and conduction power losses

Leg	I_{sw} (A)	E_{off} (μJ)	E_{on} (μJ)	P_{sw} (W)	P_{con} (W)	P_{sum} (W)
1	11.0	0	114	11.4	17.5	28.9
2	0.6	0	4.7	0.5	14.4	14.9
3	0.2	0	0.8	0.1	27.3	27.4
4	11.6	0	118	11.8	23.8	35.6
Total				23.8	83.0	106.8

Table 6.4: Leg losses for optimised LCL converter at P_{out} = 2400 W

For the smaller phase shift, with φ = 0.3, all legs switch off with zero loss in ZCS mode.

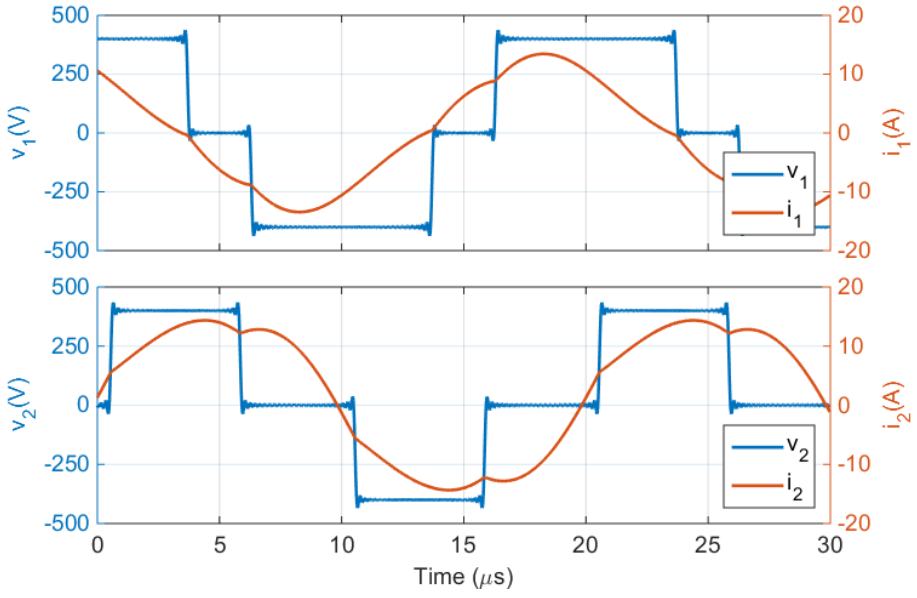


Figure 6.1: Waveforms for optimised LCL converter at P_{out} = 2400 W

The non-optimised converter's waveforms and loss results are shown in Table 6.5 and Figure 6.2.

Leg	I_{sw} (A)	E_{off} (µJ)	E_{on} (µJ)	P_{sw} (W)	P_{con} (W)	P_{sum} (W)
1	6.1	0	57	5.7	13.4	19.1
2	-9.3	226	0	22.6	13.5	36.1
3	-9.3	227	0	22.7	22.2	44.9
4	6.1	0	58	5.8	22.1	27.9
Total				56.8	71.2	128.0

Table 6.5: Leg losses for non-optimised LCL converter at P_{out} = 2400 W

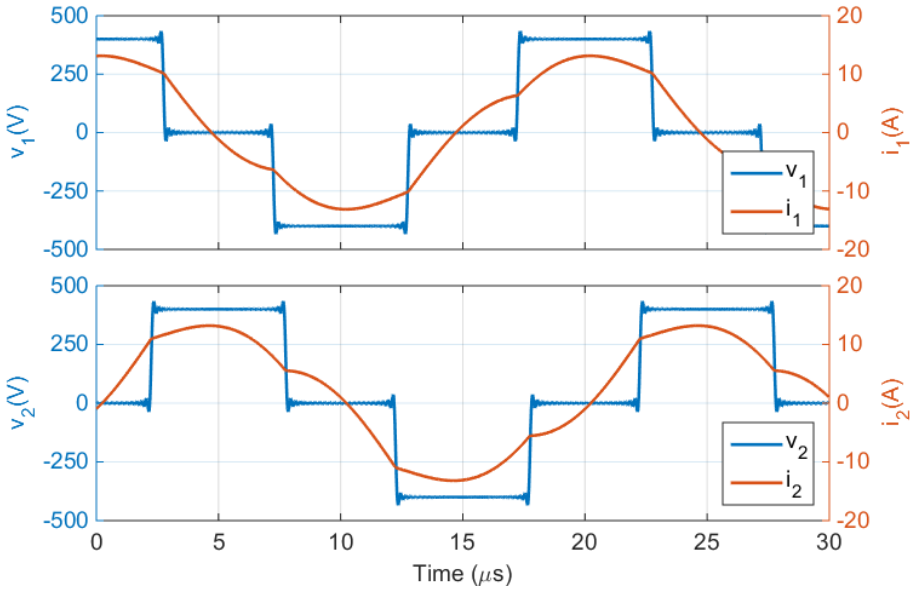


Figure 6.2: Waveforms for non-optimised LCL converter at P_{out} = 2400 W

In contrast to the optimised converter, the non-optimised converter switches with ZVS on two legs and has total losses of 128.0 W, 21.2 W more than the optimised converter. The overall effect of the optimising process is a switching power loss reduction from 56.8 W to 23.8 W, at the expense of a small increase in the conduction power losses from 71.2 W to 83.0 W.

For the IGBT switching devices used, the turn-off losses are approximately twice the turn-on losses under the same voltage and current conditions, hence the advantage of using ZCS rather than ZVS. For different devices, for example MOSFETs, the results would in general be different, and would depend on the characteristics of the devices used.

6.3.2 Theoretical Performance of Optimised CLC Converter

Using the same procedure that was used with the LCL converter, program *clc_modopt_p10*, in Appendix A, was used to calculate the optimum modulation values for the two CLC converters specified in Table 6.1. The results for the first converter, with $k_1 = 1$ and $X_D = 33.2\ \Omega$, are shown in Table 6.6, with Table 6.7 showing the non-optimised values for comparison.

P_{in} (W)	455	874	1287	1694	2095	2501	2905	3306	3703	4123
P_{out} (W)	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	-0.72	-0.66	-0.62	-0.76	-0.76	-0.70	-0.66	-0.64	-0.62	-0.54
m_1	0.26	0.34	0.38	0.56	1.00	0.68	0.72	0.74	0.90	0.96
m_2	0.27	0.31	0.39	0.59	0.53	0.69	0.75	1.00	1.00	1.00
i_1 (A)	4.54	5.13	6.29	8.71	8.47	9.51	9.96	10.81	10.82	11.16
i_{c2} (A)	4.46	5.53	6.14	8.35	11.07	9.45	9.76	10.02	10.72	11.15
Vs_{M1}	1952	2550	3121	2659	2464	3466	3951	4430	4560	5154
Vs_{M2}	1943	2627	3084	2538	3460	3443	3867	4055	4502	5144
PE	0.879	0.916	0.932	0.944	0.955	0.960	0.964	0.968	0.972	0.970

Table 6.6: CLC converter results for optimal modulation, $k_1 = 1$

P_{in} (W)	468	889	1300	1707	2108	2522	2930	3333	3734	4154
P_{out} (W)	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50
m_1	0.19	0.28	0.35	0.42	0.50	0.58	0.66	0.73	0.81	1.00
m_2	0.19	0.28	0.35	0.42	0.50	0.58	0.66	0.73	0.81	1.00
i_1 (A)	3.92	5.27	6.25	7.15	7.96	8.72	9.34	9.88	10.52	11.17
i_{c2} (A)	3.92	5.27	6.25	7.15	7.96	8.72	9.34	9.88	10.52	11.17
Vs_{M1} (V.μs)	2262	3090	3674	4103	4451	4731	4972	5169	5319	5470
Vs_{M2} (V.μs)	2262	3090	3674	4103	4451	4731	4972	5169	5319	5470
PE	0.855	0.900	0.923	0.937	0.949	0.952	0.956	0.960	0.964	0.963

Table 6.7: CLC converter results for no optimisation, $k_1 = 1$

Comparing these two, the best improvement in efficiency, of approximately 2.4 percentage points, occurs at the bottom of the power range, with a lessening improvement as the power increases. At the maximum power output there is 0.7 of a percentage point improvement. Also, while the related rms currents are approximately the same, the optimised system has significantly smaller magnetising voltage-second products, as shown in the last column. As a result of this the magnetic components will be smaller and, therefore, less expensive.

The optimised converter's waveforms and losses are shown in Figure 6.3 and Table 6.8, while those for the standard modulation are shown in Figure 6.4 and Table 6.9.

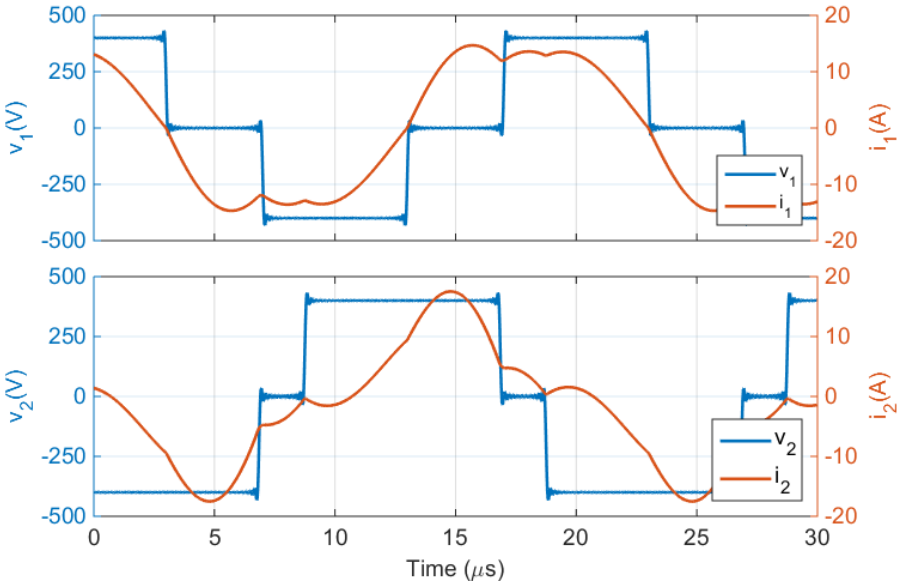


Figure 6.3: Optimised CLC converter at P_{out} = 2400 W

Leg	I_{Sw} (A)	E_{off} (µJ)	E_{on} (µJ)	P_{sw} (W)	P_{con} (W)	P_{sum} (W)
1	10.2	0	102	10.2	17.5	27.7
2	0.6	0	4	0.4	14.4	14.8
3	0.8	0	6	0.6	26.0	26.6
4	10.0	0	100	10.0	23.1	33.1
Total				21.2	81.0	102.2

Table 6.8: Leg losses for optimised CLC converter at P_{out} = 2400 W

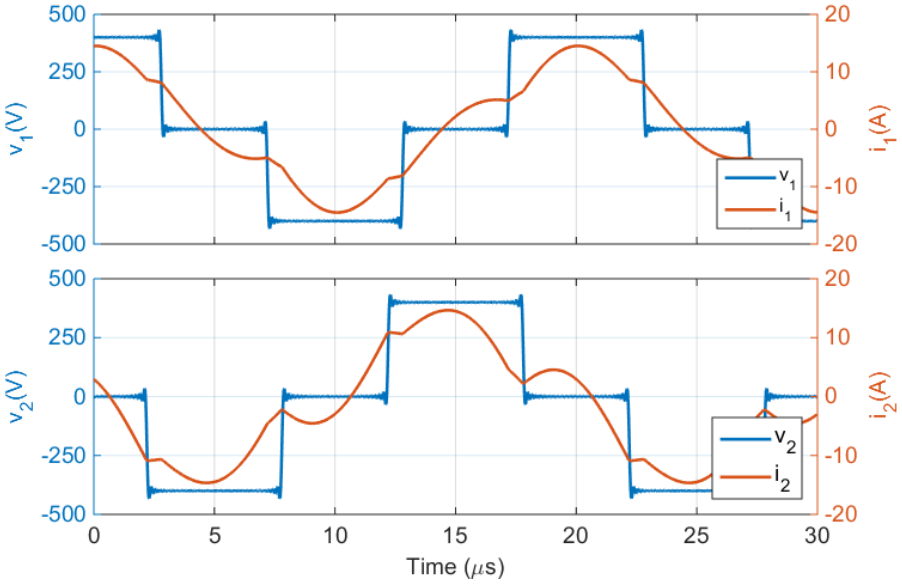


Figure 6.4: Non-optimised CLC converter at P_{out} = 2400 W

Leg	I_{Sw} (A)	E_{off} (μJ)	E_{on} (μJ)	P_{sw} (W)	P_{con} (W)	P_{sum} (W)
1	4.8	0	45	4.5	13.1	17.6
2	-8.6	210	0	21.0	13.1	34.1
3	-8.6	210	0	21.0	21.9	42.9
4	4.8	0	45	4.5	21.9	26.4
Total				51.0	70.0	121.0

Table 6.9: Leg losses for non-optimised CLC converter at P_{out} = 2400 W

As a result of the optimisation the switching losses have been reduced from 51.0 W to 21.2 W, while there has been a small increase in the conduction losses from 70.0 W to 81.0 W, an overall improvement of 18.8 W.

Table 6.10 and Table 6.11 show the effect of optimisation for the CLC converter having k_1 = 0.6, where there are the same trends as with k_1 = 1. The full power efficiency has been improved by 1%, as the power loss has been reduced from 197 W to 155 W.

P_{in}	455	869	1280	1690	2093	2494	2899	3299	3692	4155
P_{out}	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	-0.70	-0.66	-0.62	-0.58	-0.76	-0.70	-0.66	-0.64	-0.62	-0.54
m_1	0.28	0.34	0.38	0.42	0.88	0.72	0.76	0.92	1.00	0.96
m_2	0.26	0.32	0.38	0.44	0.56	0.69	0.78	0.81	1.00	1.00
i_1	4.36	5.06	5.97	7.12	9.20	9.27	9.69	9.99	10.59	11.35
i_{c2}	4.65	5.33	6.04	6.90	11.02	9.50	9.58	10.25	10.59	11.34
Vs_{M1}	1941	2414	2857	3346	2196	3015	3533	3695	4001	4615
Vs_{M2}	1959	2453	2871	3284	2939	3110	3480	3865	4001	4604
PE	0.878	0.920	0.937	0.946	0.956	0.962	0.966	0.970	0.975	0.963

Table 6.10: CLC converter results for optimal modulation, k_1 = 0.6

P_{in}	465	909	1320	1718	2106	2517	2931	3341	3746	4197
P_{out}	400	800	1200	1600	2000	2400	2800	3200	3600	4000
φ	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50
m_1	0.20	0.25	0.32	0.40	0.50	0.61	0.68	0.75	0.83	1.00
m_2	0.20	0.25	0.32	0.40	0.50	0.61	0.68	0.75	0.83	1.00
i_1	3.71	6.39	7.32	7.84	8.27	8.60	9.19	9.85	10.63	11.67
i_{c2}	3.71	6.39	7.32	7.84	8.27	8.60	9.19	9.85	10.63	11.67
Vs_{M1}	2342	2710	3256	3715	4124	4444	4613	4750	4864	4967
Vs_{M2}	2342	2710	3256	3715	4124	4444	4613	4750	4864	4967
PE	0.860	0.880	0.909	0.931	0.950	0.953	0.955	0.958	0.961	0.953

Table 6.11: CLC converter results for no optimisation, k_1 = 0.6

In summary, the effect of the optimisation process, making use of all three modulation angles, has been an improvement in the power efficiency by approximately 1%. This has been obtained by decreasing the switching power losses, by moving the leg switching mode to ZCS.

6.4 Converter Operation with Varying Conditions

In Section 6.2 the design of the converters was reasonably uncomplicated. For equal dc link voltages it was assumed that a transformer turns ratio of one would be optimal for a converter which behaves symmetrically. However, this assumption may not be correct; in the last section it was demonstrated how non-optimal performance in one area could be more than compensated for by the performance improvement in another area. The selection of converter parameters such as X_D, t_r, f and k_m is certainly not obvious for the operation of a converter with a range of dc link voltages, in an environment in which the converter is required to deliver varying amounts of power. Also, for a given set of these parameters, there is considerable freedom in the design of the magnetic components; a reduction in their losses may be achieved with an increase in their size, with a commensurate increase in cost. For these reasons, optimisation is a necessary part of the design process.

The optimisation of power efficiency, which is one of the most important performance metrics of a converter, necessarily conflicts with the converter's cost. In the absence of a cost constraint a converter's power efficiency can be made arbitrarily close to 100%; the converter would be very large and operate at a small switching frequency. To obtain an optimal design, or to evaluate how good a converter is, there must be a weighting of the relevant, and competing, performance metrics [84]. The choice of these weightings would depend on the converter's application, and is also rather subjective. As a means of removing this subjectivity, the approach which will be taken here is to optimise the converter's total cost in its design lifetime. This reduces the optimisation from a multivariable problem to a single variable problem which may be quantified, albeit with some assumptions in the choice of parameters. This optimisation establishes the converter parameters that result in the lowest overall lifetime cost, comprising the capital cost and the cost of the energy consumed, for the operation of the converter in a specified set of conditions. It is assumed, in this study, that there are no component failures in this converter lifetime. For these conditions, this optimisation enables the best design

parameters to be selected for a particular converter type, and also enables a comparison to be made between converters of different types. To this end, a separate cost analysis was conducted for each of three converters: the LCL and CLC resonant converters and the CDAB converter.

6.4.1 Operating Conditions and Assumptions

The application for the converter cost analysis is that of Figure 1.1, in which the isolated converter transfers power between a high voltage DC bus and a storage battery. For this application it was assumed that the dc links have zero source impedance and that the bridges were implemented with the same IGBTs that were previously used. All converter components were assumed to have their ideal values; manufacturing tolerances were not allowed for.

The most important conditions that need to be taken into account are the dc link voltages, the power level and direction, and the time for which the converter runs at each of these settings. It was assumed that the converter's lifetime was 10 years, and that it would transfer, on average, 20 kW-hours of energy for each day of this period. This corresponds to approximately 18000 hours of operation at its maximum power of 4 kW. For the intended use with electric vehicles, the assumed proportion of time spent at each operating condition is shown in Table 6.12. The duties of 10%, 5% and 85% correspond to time spent in grid support, recharging a low battery and fully charging the battery respectively. For forward power transfer energy is consumed from the high voltage bus, and therefore, ultimately, from the grid. This is offset by power transfer in the reverse direction.

A transistor operating temperature of 75°C has been used for all calculations.

V_{DC1} (V)	V_{DC2} (V)	Forward Power Output			Reverse Power Output		
		800 W	2 kW	4 kW	800 W	2 kW	4 kW
280	400	-	-	-	-	-	-
400	400	-	-	85%	-	-	10%
400	280	5%	-	-	-	-	-

Table 6.12: Relative hours of duty for each condition

6.4.2 Converter Costing

The total cost of operating the converter for its lifetime is the sum of the energy cost and the hardware cost:

$$Totcost = Ein * Unitcost + HWcost \quad (45)$$

Where:

Ein is the electrical energy supplied from the grid (kW-hours)

Unitcost is the cost of electrical energy ($/kW-hour)

HWcost is the hardware cost ($)

The energy cost has been assumed to be $0.29/kW-hour, as per Appendix D.

The hardware cost, which has been based on the manufacture of 1000 converters, has been separated into fixed and variable cost categories:

$$HWcost = Fcost + HSpc * PHS + TRcost + Lcost + Capcost \quad (46)$$

$$PHS = P_{con1} + P_{con2} + P_{sw1} + P_{sw2} \quad (47)$$

Where:

Fcost is the fixed cost ($)

HSpc is the heat-sink cost proportionality constant ($/W)

PHS is the heatsink power dissipation (W)

TRcost is the cost of the transformer ($)

Lcost is the cost of the inductor ($), where applicable

Capcost is the cost of the capacitor ($), where applicable

The fixed cost, which was calculated to be $150, includes the design and manufacturing costs and the cost of all hardware components, including the semiconductors, but does not include components of variable size. The fixed cost value is common to all systems, and therefore has no effect on the cost comparisons; it has only been defined for the sake of completeness.

Empirical observations were used to establish the proportionality constants for the costs of the variable size components:

The heat-sink and fan assembly were costed assuming a linear relationship between the cost and the power rating. From Appendix D the proportionality constant is \$0.10/W. If the heat-sink alone were costed, a scaling analysis would suggest that the cost would be proportional to $P^{1.5}$ for similar shapes; the dissipation is determined by the surface area, and therefore by the square of the lineal dimension, and the cost is determined by the volume, the cube of the lineal dimension. However, the cost of the associated fan increases less quickly than the power dissipation to be catered for. Hence the assumption that the overall cost has a direct proportionality with the power rating.

The cost of each magnetic component was assumed to be proportional to its volume, as given by (67) in Appendix B, in which the calculations are based on 3C90 core material. To determine the relationship for TRcost in (46), the characteristics of a known transformer were used as a reference. This transformer, which used a dual E65 core set made of 3C90 material, had a total power loss of 21 W at 50 kHz at its maximum magnetisation $I_w V_{sp}$ of 96000 V.μs.A and had a cost of \$41.4, as per Appendix D. To cater, in the optimisation, for an increase in the size and cost of the transformer, the loss reduction factor k_r described in Appendix B, was used. The reference transformer was selected for the base design, with $k_r = 1$, on the basis that it had the greatest power losses that would be acceptable from an efficiency point of view. A smaller transformer may also be inadequate from a thermal perspective. Larger, and more expensive, transformer options, with the corresponding magnetising and resistive power loss reductions, were accommodated by values of k_r less than 1. Based on the reference design, and making use of the relationship (67) in Appendix B, the transformer cost is given by:

$$TRcost = \left(\frac{I_w V_{sp}}{96000}\right)^{2.1} \left(\frac{f_s}{50000}\right)^{1.1} {k_r}^{-1.8} * 41.4$$
$$= 9.8 * 10^{-15} (I_w V_{sp})^{2.1} {f_s}^{1.1} {k_r}^{-1.8} \quad (48)$$

Where:

I_w is the maximum rms winding current (A)

V_{sp} is the maximum total volt-second product of the magnetic component's winding (V.μs)

k_r is the loss reduction factor

The reference transformer had a relative magnetising inductance of 16. In recognition of the increased size, and therefore cost, of a transformer having a larger value of the relative magnetising inductance, a factor k_{mc} is introduced to adjust the cost. This factor k_{mc} has values of 1, 0.95, 0.9, 0.85 and 0.8 for k_m values of 16, 8, 4, 2 and 1 respectively, so that the final expression for the transformer's cost is:

$$TRcost = 9.8 * 10^{-15}(I_w V_{sp})^{2.1} {f_s}^{1.1} {k_r}^{-1.8} k_{mc} \tag{49}$$

The values assigned to k_{mc} are both conservative and approximate, and would depend on how the leakage reactance is implemented in the transformer.

For the discrete inductor, which was only used in the LCL converter, the proportionality constant used in its costing calculation was based on the characteristics of the reference transformer above. From (61), if the inductor has a designed total power loss of 11 W at 50 kHz at its maximum magnetisation $I_w V_{sp}$ of 40000 V.μs.A, then its lineal size, relative to the reference transformer, is given by:

$$\frac{21}{11} = \left(\frac{96000}{40000}\right)^{1.17} {k_L}^{1.67} \tag{50}$$

from which,

$$k_L = 0.8$$

An inductor of this specification, with a lineal size which is 80% of that of the reference inductor, has a cost, from (67), which is given by:

$$\begin{aligned} Lcost &= \left(\frac{I_w V_{sp}}{40000}\right)^{2.1} \left(\frac{f_s}{50000}\right)^{1.1} {k_r}^{-1.8} * 41.4 * 0.8^3 \\ &= 3.1 * 10^{-14}(I_w V_{sp})^{2.1} {f_s}^{1.1} {k_r}^{-1.8} \end{aligned} \tag{51}$$

Costing of the capacitors, if used, makes use of the close correlation between the cost of a capacitor and its maximum stored energy, and is given by (76) in Appendix D.

6.4.3 Power Loss Calculations

From (61), and making use of the characteristics of the reference transformer defined in the last section, the total power loss of the transformer, comprising the sum of the magnetising and the resistive power losses, is given by:

$$P_{Tr} = 21\left(\frac{I_w V_{sp}}{100000}\right)^{1.17}\left(\frac{f_s}{50000}\right)^{0.61} k_r$$
$$P_{Tr} = 4.2 * 10^{-8}(I_w V_{sp})^{1.17} {f_s}^{0.61} k_r \quad (52)$$

The inductor's power loss, where applicable, is calculated:

$$P_L = 11\left(\frac{I_w V_{sp}}{40000}\right)^{1.17}\left(\frac{f_s}{50000}\right)^{0.61} k_r$$
$$= 6.2 * 10^{-8}(I_w V_{sp})^{1.17} {f_s}^{0.61} k_r \quad (53)$$

The power losses that have been calculated in (52) and (53) are the total of the magnetising and the resistive power losses at maximum loading. For the transformer, the resistive losses were assumed to be partitioned equally between the primary and secondary windings. For the 3C90 material assumed to be used, which has a power loss flux density exponent of 2.8, an optimally designed magnetic component has a resistive power loss that is 1.4 times greater than the magnetising power loss at maximum load. For smaller currents and smaller volt-second products the resistive and magnetising power losses reduce in accordance with their respective power laws. The relationships for the transformer are given in (54); those for the inductor are similar.

$$P_{Mt} = P_{Mag} + P_R$$
$$P_{Mag} = P_{Tr}\frac{1}{2.4}\left(\frac{V_s}{V_{sp}}\right)^{2.8} \quad (54)$$
$$P_R = P_{Tr}\frac{1.4}{2.4}\left(\frac{I_r}{I_w}\right)^2$$

Where:

P_{Mt} is the magnetic component's total power loss (W)

P_{Mag} is the magnetising power loss (W)

P_R is the resistive power loss (W)

V_s is the total volt-second product of the windings (V.s)

I_r is the rms winding current (A)

6.4.4 Analysis Procedure

The MATLAB programs lcl_cost_min, clc_cost_min and L_cost_min, in Appendix A, were used to optimise the cost of the LCL, CLC and CDAB converters, respectively.

Each program makes use of a pre-calculated set of data for that converter. This data includes the optimal modulation settings for a range of hardware configurations and operating conditions. Each of the parameter values has been discretised in a range which is expected to contain the optimal value for the stated operating conditions. As the choice of the size of the magnetic components and their characteristics is wide ranging, it was not practical to allow for these in the data set; these characteristics will be taken into account later.

In the case of the LCL converter, the hardware configurations are specified by the design reactance (X_D), the relative magnetising reactance (k_m), the effective transformer turns ratio (t_{rr}) and the switching frequency (f_s). The operating conditions are specified by the dc link voltages, the value of the transferred power and the direction of the power transfer. Pre-calculated data, collected by the program lcl_data, was used as it enables the cost optimisation program to run quickly, so that it may respond interactively to changes in its settings; collection of the pre-calculated data takes a considerable time. Although the same procedure is followed for each converter, there are minor variations in the hardware configurations for the converters. For example, for the CLC converter k_m =1 as the magnetising reactance is always equal to the design reactance, so the parameter k_m in the LCL converter is replaced with k_1.

For a particular hardware configuration, the procedure starts with a sweep through the required operating conditions to ascertain the maximum rms current and volt-second values for the magnetic components. For this phase of the procedure, the magnetising and resistive power losses of the magnetic components are ignored in the calculation of the circuit voltages, currents and powers. Following this, a second sweep is performed using magnetic components whose base design and characteristics make use of the maximum values previously calculated. Iterations of the value of the loss reduction factor k_r, which is effectively the fifth hardware parameter, are made to evaluate the effect of magnetic component size changes, from the base design, on the cost and on the power losses. During this operation the energy input is accumulated and the costs are calculated. For the calculation of the converter's power input, the power losses of the magnetic components are calculated and then added to the input power calculated in their absence.

It is necessary to perform the calculations in this order, as the characteristics of the magnetic components are initially unknown. An iteration of this process is not required, as the magnetic component losses are small compared to the total power, so that a good accuracy is obtained.

After the total cost in (45) is calculated for each hardware configuration, the systems are then ranked from the lowest cost, for the optimal design, through to the highest cost.

6.4.5 Cost Analysis Results

LCL Results

The LCL converter was implemented with one discrete inductor and a distributed inductance integrated into the transformer, as in Appendix C. For this converter, the ranges of the hardware parameters, which are shown in Table 6.13, have been chosen to be sufficiently wide to accommodate all anticipated solutions.

Parameter	Minimum	Maximum	Step Value	Number of Values
X_D (Ω)	14.0	77.8	Ratio of 1.1	18
k_m	2	16	Ratio of 2	4
t_{rr}	0.6	1.4	0.1	9
f_s (kHz)	12.5	100	Ratio of 2	4

Table 6.13: Hardware parameters for LCL converter

A modified transformer ratio, t_{rr}, has been used to isolate t_r from changes in k_m; t_{rr} would be expected to be 1 for equal bridge DC voltages.

The best nine configurations of the analysis results are shown in Table 6.14, where:

Eout is the energy output (kW.Hours)

Ein is the energy input (kW.Hours)

Ecost is the cost of the energy input ($)

HScost is the cost of the heatsink ($)

HWcost is the total hardware cost ($)

X_D (Ω)	27.27	24.79	27.27	27.27	24.79	30.00	30.00	27.27	36.30
k_m	16	16	8	16	16	16	8	8	16
t_{rr}	0.9	0.8	0.9	0.9	0.8	1.0	1.0	0.9	1.2
f (kHz)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
k_r	1.0	1.0	1.0	0.5	0.5	1.0	1.0	0.5	1.0
i_1 (A)	12.0	11.8	12.0	12.0	11.8	12.0	12.0	12.0	11.9
I_3 (A)	13.3	14.7	13.3	13.3	14.7	12.0	12.0	13.3	10.0
i_{B2} (A)	11.8	11.6	11.6	11.8	11.6	11.8	11.6	11.6	11.8
I_{C1} (A)	20.3	20.9	20.4	20.3	20.9	19.3	19.3	20.4	17.7
Vs_{L1} (V.μs)	1570	1401	1570	1570	1401	1725	1726	1570	2041
Vs_{M1} (V.μs)	2508	2330	2508	2508	2330	2631	2635	2508	2905
Vs_{M2} (V.μs)	1875	1875	1875	1875	1875	1875	1875	1875	1875
PHS (W)	139	149	141	127	137	146	149	129	147
Eff_{Avg}	0.966	0.965	0.965	0.969	0.968	0.964	0.964	0.968	0.964
Ein (kWHr)	63238	63255	63283	63033	63056	63358	63379	63079	63385
Ecost ($)	18339	18344	18352	18280	18286	18374	18380	18293	18382
Lcost ($)	9	7	9	32	25	11	11	32	16
TRcost ($)	28	29	27	99	101	26	25	93	24
HScost ($)	14	15	14	13	14	15	15	13	15
Capcost ($)	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7
HWcost ($)	204	204	203	296	292	205	204	291	207
Totcost ($)	18543	18548	18555	18576	18578	18579	18584	18584	18589

Table 6.14: Results for LCL converter running for 20000 hours

The table has three vertical zones: The top group is the hardware characteristics. This is followed by the maximum values required of the reactive components, comprising the rms currents and volt-second products. The last group shows the maximum heatsink power dissipation required, the average efficiency and energy input, the hardware costings and the total cost of the converter for its design lifetime. The second column shows the results for the optimum case, with the minimum total cost, with subsequent columns showing more expensive converter options.

There is a small range in total cost between the nine systems shown. The worst system has a total cost which is $46, or 0.25% more expensive than the total cost of the best system.

Eff_{Avg}, the average efficiency for the various energy transfers, is the ratio of the energy output to the energy input. For the optimal system the value is 96.6%.

There are three converter systems in the table have a reduction factor, k_r, value of 0.5, requiring magnetic components which are significantly bigger to achieve the

reduction in the power losses. Compared to systems with a k_r value of 1, these three systems have a significantly higher hardware cost, which is more than offset by the lower energy cost resulting from the decreased magnetic component losses and therefore slightly higher power efficiency.

It is notable that the value of t_{rr} in the optimal system is not 1, as speculated in Section 6.4, which is not intuitive. This shows the value of the optimisation. An example of this interesting, albeit unpredicted result is seen in the last column of Table 6.14. This system, which has a larger t_{rr} value of 1.2 and a relatively large X_D of 36.3 Ω, has a marginally smaller efficiency than that of the second best system. It achieves the required power output with this large system impedance by having an increased voltage from the transformer primary.

From the table, a switching frequency of 100 kHz provides the best results in each case. Optimal operation of this LCL converter at a high frequency is predictable, in that this converter, of the three considered in this thesis, has the largest magnetic component cost contribution. As this switching frequency is on the top border of the range of anticipated operating frequencies, it has not been proven to be an optimal solution. Therefore, data was gathered for operation at 200 kHz, and the optimisation performed for the extended frequency range. Although the resulting cost minimisation suggested that a switching frequency of 200 kHz was better, the costing was only marginally better than that obtained for operation at 100 kHz. Because the dead-bands occupy a relatively significant proportion of the switching cycle at 200 kHz, operation of the IGBTs at this frequency was considered to be impractical. For this reason, the data provided in Table 6.14 was considered to be the best valid data.

Table 6.15 shows the results for a shorter run of 2000 hours. The energy cost for this run time is approximately ten times greater than the total hardware cost. As expected, the value of k_r is 1 in all systems, as it is not economic to increase the magnetic component sizes, and therefore efficiency, for the small amount of energy consumed. Now that the energy cost is less significant compared to the hardware cost, the system of column two, in which k_m is 8, is more economic than that of column four, in which k_m is 16. This is a reversal of the results shown in columns two and four of Table 6.14.

X_D (Ω)	27.27	24.79	27.27	24.79	30.00	30.00	33.00	27.27	33.00
k_m	8	16	16	8	8	16	8	4	16
t_{rr}	0.9	0.8	0.9	0.8	1.0	1.0	1.1	0.9	1.1
f (kHz)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
k_r	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
i_1 (A)	12.0	11.8	12.0	11.7	12.0	12.0	12.0	11.9	12.0
I_3 (A)	13.3	14.7	13.3	14.5	12.0	12.0	10.9	13.3	10.9
i_{B2} (A)	11.6	11.6	11.8	11.5	11.6	11.8	11.6	11.6	11.8
I_{C1} (A)	20.4	20.9	20.3	20.2	19.3	19.3	18.4	20.3	18.4
Vs_{L1} (V.μs)	1570	1401	1570	1386	1726	1725	1883	1570	1883
Vs_{M1} (V.μs)	2508	2330	2508	2274	2635	2631	2768	2508	2764
Vs_{M2} (V.μs)	1875	1875	1875	1875	1875	1875	1875	1875	1875
PHS (W)	141	149	139	151	149	146	152	155	148
Eff_{Avg}	0.965	0.965	0.966	0.963	0.964	0.964	0.963	0.962	0.964
Ein (kWHr)	6328	6326	6324	6343	6338	6336	6343	6352	6340
Ecost ($)	1835	1834	1834	1839	1838	1837	1840	1842	1839
Lcost ($)	9	7	9	7	11	11	14	9	14
TRcost ($)	27	29	28	26	25	26	24	25	25
HScost ($)	14	15	14	15	15	15	15	15	15
Capcost ($)	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7
HWcost ($)	203	204	204	201	204	205	205	203	206
Totcost ($)	2038	2038	2038	2040	2042	2042	2045	2045	2045

Table 6.15: Results for LCL converter running for 2000 hours

CLC Results

The CLC converter that was used in the costing analysis had a model that used a transformer with integrated distributed inductance and capacitors on each side, so that a completely symmetrical topology is achieved, as in Appendix C. For this converter, the ranges of the hardware parameters are shown in Table 6.16.

The analysis results for 20000 hours of running are shown in Table 6.17. The cost range for the nine systems shown is approximately $33, even less than for the LCL converter. The distinction between the LCL and the CLC converters, and within one converter system, is almost at the margin of error, and there are the same efficiency-cost compromises at play.

Parameter	Minimum	Maximum	Step Value	Number of Values
X_D (Ω)	9.3	47.2	Ratio of 1.1	18
k_1	0.6	1.0	0.1	5
t_r	0.6	1.4	0.1	9
f_s (kHz)	12.5	100	Ratio of 2	4

Table 6.16: Hardware parameters for CLC converter

The hardware cost for the CLC converter is approximately $10 less than for the LCL converter, as expected because the latter has an extra magnetic component, the inductor L_1, and a slightly smaller transformer. The small cost of the extra capacitor used in the CLC converter doesn't change the outcome.

The favoured value of k_1, the leakage reactance's proportion of the design reactance, is between 0.8 and 1. For these values the size of third harmonic current and its contribution to the power is not very significant, as mentioned in the discussion following Figure 4.4.

X_D (Ω)	29.3	26.6	29.3	29.3	32.2	26.6	32.2	29.3	35.4
k_1	0.9	1.0	0.9	0.8	0.9	1.0	0.8	0.8	1.0
t_r	1.0	0.9	1.0	1.0	1.1	0.9	1.1	1.0	1.2
f (kHz)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
k_r	1.0	1.0	0.5	1.0	1.0	0.5	1.0	0.5	1.0
i_1 (A)	12.4	12.3	12.4	12.5	12.3	12.3	12.5	12.5	12.2
i_{B2} (A)	12.4	12.3	12.4	12.5	12.4	12.3	12.6	12.5	12.4
Vs_{M1} (V.μs)	2271	2138	2271	2200	2470	2138	2390	2200	2764
Vs_{M2} (V.μs)	2282	2586	2282	2212	2105	2586	2045	2212	2019
PHS (W)	142	140	134	142	146	131	144	133	145
Eff_{Avg}	0.966	0.965	0.967	0.965	0.965	0.967	0.964	0.967	0.964
Ein (kWHr)	63259	63279	63112	63315	63328	63127	63348	63172	63366
Ecost ($)	18345	18351	18303	18361	18365	18307	18371	18320	18376
TRcost ($)	23	25	82	23	24	87	23	78	26
HScost ($)	14	14	13	14	15	13	14	13	14
Capcost ($)	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
HWcost ($)	193	194	250	192	194	256	192	247	195
Totcost ($)	18538	18545	18553	18553	18559	18562	18563	18567	18571

Table 6.17: Results for CLC converter running for 20000 hours

Using a larger transformer, to reduce power losses, is shown to be marginally economic. As an example, there is a total cost difference of approximately $17 between the systems of columns three and seven of Table 6.17. Aside from the sizes of the transformers, these systems have the same hardware. The column seven system's losses have been reduced by 9 W, with the attendant $62 increase in hardware cost, which is partially compensated for by the slight efficiency increase and $44 reduction in the energy cost.

Operation at 100 kHz is favoured in all cases. As was the case for the LCL converter, an optimisation for an extended frequency range suggests that the optimum switching frequency is 200 kHz. Once again, there is a negligible cost improvement gained by using this frequency, so that the results of Table 6.17 remain valid and would be practical to use.

Table 6.18 shows the results for 2000 hours of running. As with the LCL converter operating for the shorter run time, the value of k_r is 1 in all cases, as the relatively greater hardware cost means that the increased transformer size can't be justified.

X_D (Ω)	29.3	29.3	26.6	32.2	32.2	35.4	29.3	35.4	32.2
k_1	0.9	0.8	1.0	0.8	0.9	0.9	1.0	1.0	1.0
t_r	1.0	1.0	0.9	1.1	1.1	1.2	1.0	1.2	1.1
f (kHz)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
k_r	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
i_1 (A)	12.4	12.5	12.3	12.5	12.3	12.3	12.3	12.2	12.3
i_{B2} (A)	12.4	12.5	12.3	12.6	12.4	12.5	12.3	12.4	12.3
Vs_{M1} (V.μs)	2271	2200	2138	2390	2470	2675	2342	2764	2551
Vs_{M2} (V.μs)	2282	2212	2586	2045	2105	1966	2342	2019	2158
PHS (W)	142	142	140	144	146	146	148	145	149
Eff_{Avg}	0.966	0.965	0.965	0.964	0.965	0.964	0.964	0.964	0.964
Ein (kWHr)	6326	6331	6328	6335	6333	6338	6338	6337	6340
Ecost ($)	1835	1836	1835	1837	1837	1838	1838	1838	1839
TRcost ($)	23	23	25	23	24	24	25	26	25
HScost ($)	14	14	14	14	15	15	15	14	15
Capcost ($)	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
HWcost ($)	193	192	194	192	194	194	195	195	195
Totcost ($)	2028	2028	2029	2029	2030	2032	2033	2033	2034

Table 6.18: Results for CLC converter running for 2000 hours

CDAB Results

For this converter, the ranges of the hardware parameters are shown in Table 6.19.

Parameter	Minimum	Maximum	Step Value	Number of Values
X_D (Ω)	9.3	47.2	Ratio of 1.1	18
k_m	2	16	0.1	4
t_r	0.6	1.4	0.1	9
f_s (kHz)	12.5	100	Ratio of 2	4

Table 6.19: Hardware parameters for CDAB converter

Table 6.20 shows the results of the cost analysis for the CDAB converter running for 20000 hours. These differ significantly from those of the resonant converters: The outstanding difference is that low switching frequency values are favoured, the opposite of the resonant converters. The range of best operation occurs for switching frequencies of 12.5 kHz and 25 kHz. As the former is on the bottom border of the range of anticipated operating frequencies, it may not be an optimal solution. For this reason, additional data was gathered at 6.25 kHz, and a cost optimisation performed including this data. The results of the optimisation were unchanged, suggesting that the converter's performance at 6.25 kHz was worse than at 12.5 kHz. This would be expected, since the small efficiency gain, and therefore energy cost reduction, does not match the increase in cost of the larger transformer, which comprises approximately 39% of the hardware cost for 25 kHz operation and 55% of the hardware cost for 12.5 kHz operation. For this reason the results of Table 6.20 are valid. Operation at 25 kHz, as in column two of the table, provides the lowest cost by the use of the smaller transformer size. This more than offsets the decreased power efficiency and therefore increased cost of the energy consumed.

There are larger conduction losses for the CDAB converter, as a result of the larger bridge currents. The switching losses are also bigger, not only because the currents are greater but also because of the location of the switching points at the extremities of the current waveform. The transformer losses are small compared to the switching and conduction losses and the transformer is already large because of its low frequency operation required to keep the switching losses down. It is therefore uneconomic to increase its size further, in order to reduce its losses. For this reason k_r is 1 in all cases.

The heatsink values follow directly from the lower power efficiency and increased power losses; the CDAB converter requires a heatsink dissipation that is almost twice that of the resonant converters.

X_D (Ω)	24.2	26.6	32.2	26.6	24.2	32.2	29.3	22.0	29.3
k_m	16	8	16	8	8	16	8	16	8
t_r	0.9	1.0	1.2	1.0	0.9	1.2	1.1	0.8	1.1
f (kHz)	25.0	12.5	12.5	25.0	12.5	25.0	12.5	12.5	25.0
k_r	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
i_1 (A)	15.3	14.6	13.3	14.7	15.5	13.3	13.9	16.4	14.0
i_{B2} (A)	13.7	14.6	16.1	14.6	13.8	16.1	15.5	12.9	15.5
Vs_{M1} (V.μs)	7680	15040	15040	7360	14400	7680	15040	14720	7840
Vs_{M2} (V.μs)	7500	15000	14000	7000	15000	7000	15000	15000	7500
PHS (W)	251	234	235	258	237	258	237	240	260
Eff_{Avg}	0.941	0.945	0.945	0.940	0.944	0.940	0.944	0.944	0.939
Ein (kWHr)	65079	64818	64832	65226	64872	65219	64864	64873	65272
Ecost ($)	18873	18797	18801	18915	18813	18913	18810	18813	18929
TRcost ($)	112	211	208	97	201	107	214	218	112
HScost ($)	25	23	24	26	24	26	24	24	26
HWcost ($)	287	384	381	272	375	283	387	392	288
Totcost ($)	19160	19181	19183	19188	19188	19196	19198	19205	19217

Table 6.20: Results for CDAB converter running for 20000 hours

For the short running period shown in Table 6.21, in which the hardware cost becomes relatively more important, the optimal operating frequency has increased from that seen in Table 6.20. Again, a loss reduction is not economic, so k_r remains at 1 in all cases.

X_D (Ω)	26.6	29.3	24.2	32.2	26.6	26.6	32.2	24.2	29.3
k_m	16	16	16	16	8	8	16	16	8
t_r	1.0	1.1	0.9	1.2	1.0	1.0	1.2	0.9	1.1
f (kHz)	50.0	50.0	50.0	50.0	25.0	50.0	25.0	25.0	50.0
k_r	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
i_1 (A)	14.6	13.9	15.4	13.4	14.7	14.8	13.3	15.3	14.1
i_{B2} (A)	14.6	15.4	13.8	16.3	14.6	14.8	16.1	13.7	15.7
Vs_{M1} (V.μs)	3520	3600	3600	3840	7360	3920	7680	7680	3920
Vs_{M2} (V.μs)	3500	3500	3750	3500	7000	3500	7000	7500	3750
PHS (W)	312	317	319	329	258	333	258	251	343
Eff_{Avg}	0.928	0.927	0.927	0.925	0.940	0.924	0.940	0.941	0.922
Ein (kWHr)	6616	6624	6621	6644	6523	6651	6522	6508	6669
Ecost ($)	1919	1921	1920	1927	1892	1929	1891	1887	1934
TRcost ($)	48	50	53	54	97	53	107	112	57
HScost ($)	31	32	32	33	26	33	26	25	34
HWcost ($)	229	231	235	237	272	236	283	287	241
Totcost ($)	2148	2152	2155	2164	2164	2165	2174	2174	2176

Table 6.21: Results for CDAB converter running for 2000 hours

6.4.6 Comparison of Cost-Optimised Converters

A summary of the salient parameters of the cost optimised converter results is shown in Table 6.22.

The conclusion which is drawn from running the converters for 20000 hours is that the LCL and CLC converters have almost identical total lifetime costs; hardware costs for the LCL converter are greater, but it has a marginally larger power efficiency than its CLC counterpart. The CDAB converter cost approximately 3% more than the resonant converters, which corresponds to the efficiency difference and therefore energy costs for a long run time. For the hardware costs, the LCL converter is predictably more expensive than the CLC converter, which is approximately 33% cheaper than the CDAB converter.

The same trends occur for operation of the converters for 2000 hours, a tenth of the expected converter usage. Even for this duration, the cost of the energy is approximately ten times greater than the hardware cost, so that the more efficient resonant converters have lower total costs. The CDAB has a greater hardware cost because of its lower efficiency and therefore larger heatsink, as well as a larger transformer because of the converter being restrained to operate at low switching frequencies as a consequence of the significant switching losses it would suffer if operated at higher frequencies. For the energy quantities involved, the small efficiency difference between the LCL and CLC

converters has a negligible effect on the energy cost, so that the cost difference between these converters is that of their hardware.

Run time	20000 hours			2000 hours		
	LCL	CLC	CDAB	LCL	CLC	CDAB
i_1 (A)	12.0	12.4	15.3	12.0	12.4	14.6
i_{B2} (A)	11.8	12.4	13.7	11.6	12.4	14.6
PHS (W)	139	142	251	141	142	312
HWcost ($)	204	193	287	203	193	229
Totcost ($)	18543	18538	19160	2038	2028	2148

Table 6.22: Salient parameters of cost optimised converters

Compared to the CDAB converter, the transistors in the resonant converters also have smaller currents and significantly smaller power dissipations, which cause lower stresses and therefore do not compromise their reliability.

The conclusion that the LCL and CLC resonant converters have a lower cost is predictable; as the cost of the energy consumed by the converter in its lifetime is significantly greater than the cost of the converter, the expense incurred in improving the efficiency of the converter is repaid many fold in energy savings over that period.

The resulting designs, that provide the optimal cost solution for a particular converter type, differ from what may be intuitively expected; an example of this would be non-unity transformer turns ratios being used in a system which has equal dc link voltages. This outcome is a consequence of the wide range of parameters in systems which provide comparable performance; in this case a change in the transformer turns ratio has been made, along with a different design reactance. The trade-off between hardware cost and efficiency is also clearly displayed. The optimising process is a useful design tool, aside from its use for providing comparisons between different converter types.

As the cost analysis was performed for bridges implemented with IGBTs, it may be suggested that the CDAB converter's performance is less than optimal with these devices. For full power operation of the CDAB converter all bridge legs switch with ZVS, so that the switching losses incurred are those for transistor turn-off, which, for IGBTs, are

higher than those for transistor turn-on. To ascertain if a CDAB converter implemented with MOSFET switches would have had a better performance, the losses of a CDAB converter having the parameters shown in Table 6.23 was analysed.

V_{DC1}, V_{DC2} (V)	400
X_D (Ω)	27.7
φ_{Max}	0.36
k_m	∞
MOSFETs	IXFH26N60

Table 6.23: CDAB Converter Parameters

These particular MOSFETs have been chosen for their good switching characteristics, which will enable good performance at high switching frequencies.

Table 6.24 shows the forward power transfer performance of this converter. It has been implemented with an ideal transformer, so that the only power losses considered are the conduction and switching losses.

f_s	25 kHz		50 kHz		100 kHz	
X_D (Ω)	27.2		27.3		26.9	
P_{out} (W)	800	4000	800	4000	800	4000
P_{Cond} (W)	7.2	215.5	7.3	217.7	7.3	224.2
P_{Sw} (W)	6.3	58.8	16.0	121.7	25.4	255.8
Eff	0.983	0.936	0.972	0.922	0.960	0.893

Table 6.24: CDAB converter performance with MOSFETs

From Table 6.24 it can be seen that, by comparison with Table 6.1, the MOSFET variant of the CDAB converter has a performance similar to the IGBT variant at 50 kHz. There is a slight improvement in power efficiency at low power levels, as a result of the reduced conduction losses of the MOSFET in these conditions, but there is a reduced power efficiency at full power. Operation at higher switching frequencies is not practical, because of the resulting low power efficiency which occurs as the switching losses

dominate, as shown for the 100 kHz results. Operation at 25 kHz yields marginally better power efficiencies, with values comparable to those obtained for IGBTs. Optimisation of the cost would result, as it did before with the IGBTs, in operation at a switching frequency of 25 kHz and therefore with a larger and more expensive transformer. The heatsink size is determined by the maximum dissipation which remains high. The MOSFETs are also more expensive. Appendix D records that the cost of eight IXFH26N60 MOSFETs is $103 (1000 unit price), compared with $20 for the STGWA19NC60 IGBTs. As well as the significant cost penalty of an additional $83, the MOSFETs are also likely to be less robust than the IGBTs.

The conclusion to be drawn from this is that the original cost analysis, which was made for a CDAB converter which had its bridges implemented with the STGWA19NC60 IGBTs, was realistic for this converter.

6.4.7 Conclusions

This chapter has analysed the performance of converters transferring power between 400 V sources. In Section 6.2 it was seen that the LCL and CLC converters had better full-power power efficiencies than the CDAB converter, but larger magnetic components, particularly for the LCL converter.

Section 6.3 showed that optimisation of the resonant converters, using three angle modulation, provided worthwhile improvements in the power efficiency as a result of reduced switching losses.

Section 6.4 optimised the lifetime total cost of each of the converters, as an objective means of ranking them given that there were potentially conflicting performance metrics. From this study the hardware cost was lowest for the CLC converter, 6% greater for the LCL converter and 49% greater for the CDAB converter. The energy/running cost, which is inversely proportional to the efficiency, was lowest for the LCL converter, marginally greater for the CLC converter and 3% greater for the CDAB converter. As the running cost is at least a hundred times greater than the hardware cost, it largely determined the total lifetime cost. The size of the converters was not investigated, but an important determining factor would be the heatsink power dissipation, which was lowest for the LCL converter, 2% greater for the CLC converter and 81% greater for the CDAB converter.

In previous chapters it has been shown that, for operation at this voltage level, IGBT switching devices had superior performance. Calculations performed for optimised CDAB converters using MOSFETs reached the same conclusion, justifying the converter comparisons.

Also of interest, was that the results of the optimisation process were not intuitive. This was evident in the selection of a transformer with a non-unity turns ratio and in the selection of the switching frequency, which was at the upper end of the range for the resonant converters and at the lower end for the CDAB converter. The use of oversized magnetic components, which would cost more but provide lower losses, and therefore lower running costs, could not be justified even for the longest runtime.

7 Conclusions and Future Work

7.1 Conclusions

This thesis has presented two resonant dc-dc converters suited for use in vehicle to grid or distributed generation applications. These converters are conceptually very similar, comprising a dual active bridge, an isolating transformer and a Tee network tuned to the switching frequency. The standard control is effected by equal modulation of the bridges at a constant switching frequency, with a fixed inter-bridge phase shift of ±90°, according to the direction of power transfer. For this modulation arrangement the fundamental bridge voltages and currents align, thereby minimising the bridge currents and the conduction power losses. With the converter controlled in this manner the power throughput has a sine squared relationship with bridge modulation, and power efficiencies of over 96% at maximum output are easily achieved. For converter control with three angle modulation, the optimum performance, with a power efficiency gain of approximately 1%, may be realised.

As well as a transformer with integral leakage inductance, the LCL converter requires one inductor and one capacitor, and the CLC converter requires two capacitors. The performance of these converters is tolerant of reasonably wide variations in component values. Also, for the CLC converter, which has ac coupled bridges by virtue of its capacitors, there is inherent prevention of dc current flow in its transformer; this removes a complication from the design of the control system.

For the intended application, with high voltage dc links, the preferred switching devices for best power efficiency are IGBTs. These are cheap and robust, and have switching characteristics which suit the resonant converter's usual switching mode, in which two legs have ZVS and two legs have ZCS. For operation of one bridge at low dc voltages MOSFETs would be the preferred devices, because of their low conduction losses, particularly in third quadrant operation. Operation with low dc voltages on both bridges would require physically large capacitors, which may not be practical. While most of the theoretical and experimental work has focused on power transfers of up to 4 kW between 400 V dc links, the converters are scalable, with the appropriate hardware, for higher power operation.

A comparison was made between the LCL and CLC resonant converters and the CDAB converter. This was made on the basis of converters optimised for lowest lifetime cost for the intended application. The LCL and CLC converters had almost identical lifetime costs, both for 20000 and 2000 hours of operation. For 20000 hours of operation the energy cost, and therefore the power efficiency, is dominant, so that the CDAB converter was over 3% more expensive. For 2000 hours of operation, for which the energy cost is approximately ten times greater than the hardware cost, the CDAB converter was approximately 6% more expensive, because of the greater hardware cost of its larger heatsink and transformer. From these results, it is seen that the CLC converter is the cheapest of these converters and would be selected in preference to the LCL converter as the latter is physically larger. It was seen in the optimisation of the CLC converter that values of k_1 close to unity were favoured, although there were a number of possible system configurations which would provide very similar performance.

The optimisation process was a useful tool in the process of converter design; some of the optimum system configurations were neither intuitive nor would they be easily derived without using this approach.

As well as being cost effective, when compared to the CDAB converter, the resonant converters have the advantage of smaller bridge ac and dc link ripple currents and smaller power losses, as a consequence of their higher power efficiency.

The overall conclusion which is drawn is that these resonant converters presently have significant advantages for their use in DC-DC conversion. There is also the potential to further improve their performance.

7.2 Contributions to Knowledge

The main contributions of this study are listed below:

- For the LCL and CLC converters, equations were derived expressing the power throughput and the various frequency domain currents as functions of the supply voltages and the three modulation angles. Using the phasors, a time domain summation yielded the signals which were required for the calculation of the conduction and switching losses and the magnetic component maximum volt-second products. This approach provides greater accuracy than one based on a fundamental approximation analysis.

- The “standard” design approach, in the absence of optimisation, for each converter was specified: For the supply voltages used, the design impedance was selected to provide the required power throughput at maximum modulation. The transformer turns ratio is selected to provide equal network AC voltages, and the reactive components chosen so that the reactances of each network leg are equal to the design impedance. In the case of the CLC converter, the reactance of the inductor in series with one of the capacitors should be approximately 90% of the design reactance, although the value isn’t critical. Finally, the reactances may be distributed to provide a symmetric network, and the series inductances integrated into the transformer if desired.
- Performance comparisons were made for resonant converter operation with different switching devices. IGBTs were shown to provide the best results for high voltage DC links, and MOSFETs for low voltage DC links.
- Optimisation of the converter performances under fixed operating conditions was demonstrated. By varying the inter-bridge phase shift from 90°, an improvement in power efficiency was achieved by reducing the switching losses using three angle modulation.
- Quantitative comparisons of key performance metrics were made, for fixed operating conditions, between the resonant converters and a CDAB converter, showing the advantages of the resonant converters.
- For the V2G target application, comparisons were made between the total lifetime costs of running LCL and CLC resonant converters and a CDAB converter. The CLC converter had the lowest cost, with the LCL marginally more expensive. Each converter was optimised using an exhaustive search process, which was also shown to be an effective tool for designing a converter for a specific set of operating conditions, based on minimising its cost.

The study has resulted in the publication of two IEEE transactions papers and two IEEE conference papers, as listed below:

1. R. P. Twiname, D. J. Thrimawithana, U. K. Madawala, C. A. Baguley, “*A New Resonant Bidirectional DC-DC Converter Topology*”, Power Electronics, IEEE Transactions on, 2014. **29**(9): p. 4733-4740.

2. R. P. Twiname, D. J. Thrimawithana, U. K. Madawala, C. A. Baguley, *"A Dual-Active Bridge Topology with a Tuned CLC Network"*, Power Electronics, IEEE Transactions on, 2015. **30**(12): p. 6543-6550.
3. R. P. Twiname, D. J. Thrimawithana, U. K. Madawala, C. A. Baguley, *"A Resonant Bi-directional DC-DC Converter"*, Industrial Technology (ICIT), IEEE International Conference on, 2014. p. 307-311.
4. R. P. Twiname, D. J. Thrimawithana, U. K. Madawala, C. A. Baguley, *"A Novel Dual Active Bridge Topology with a Tuned CLC Network"*, Industrial Technology (ICIT), IEEE International Conference on, 2014. p. 895-900

7.3 Suggestions for Future Work

As the trend to operate at higher switching frequencies continues, the effect of the dead-band becomes more significant and requires investigation. Also, it is likely that further advancement of FET technology will result in competitively priced FETs which will out-perform IGBTs at high voltage levels so that higher switching frequencies and speeds may be used. If this is the case, and for radio-frequency interference minimisation, it would be beneficial for these resonant converters to operate with ZVS for all switching devices. Converter operation could also be extended to include, for example, frequency control as well as three angle control.

For high power converters the three phase resonant converter shown in Appendix E appears to be very attractive because of its low switching power losses, as a result of the very low switching currents. Also, by virtue of its three phase operation, it has lower ripple currents and therefore dc capacitor requirements.

To determine the optimum modulation angles for the resonant converters, their power input was minimised for a particular power output. While the values of m_1 and m_2 thus obtained are optimal from a power efficiency point of view, they may not be the best angles for an overall optimisation. In the power equations (12) and (28) the values of m_1 and m_2 are interchangeable. Initial experiments with the values obtained from the optimiser suggest that in some instances it is possible to obtain, with m_1 and m_2 swapped, a power efficiency which is only marginally smaller but with a significant reduction in the required volt-second products of the magnetic components. This, in particular, requires further investigation.

An investigation of the effect of variations in the relative magnetising inductance k_m on the size of a transformer is possible future work. Empirical relationships, only, were used in this thesis for the quantification of this parameter's influence on the size. A complete analysis of this effect would be dependent on the transformer's shape and on the method of leakage inductance implementation, and would probably require an FEM approach.

Appendix A MATLAB Programs

In this thesis, a number of MATLAB programs are used for performing calculations. A summary of the functionality of the main programs follows:

lcl_dab_2igbt Script.

Function:	Calculate all voltages and currents of LCL DAB converter using IGBTs in the both bridges [and plot bridge voltage and current waveforms].
Inputs	V_{DC1}, V_{DC2}, X_D, t_r, φ, m_1, m_2, f, temp, k_1 to k_4, R_1, R_2.
Outputs	Input and output power, all voltage, current waveforms, bridge dc, rms and ac rms currents, transistor switching and conduction losses, magnetising losses and resistive losses.
Calls	STGWA19N60_swg_loss, STGWA19N60_vd, STGWA19N60_vt
Comments	Based on Figure 3.3 and equation (9). Losses are added to the results of a lossless circuit analysis.

lcl_loss_2igbt Function**.**

Function:	Calculate all losses in LCL DAB converter using IGBTs in the both bridges. Used for the assembly of the loss table.
Inputs	Parameters passed are φ, m_1, m_2. Parameters specified in function are V_{DC1}, V_{DC2}, X_D, t_r, f, temp, k_1 to k_4, R_1, R_2.
Returns	Column vector having 29 rows: modulation, all losses, input and output power, efficiency and bridge rms currents.
Calls	STGWA19N60_swg_loss, STGWA19N60_vd, STGWA19N60_vt
Comments	Based on Figure 3.3 and equation (9). Losses are added to the results of a lossless circuit analysis.

lcl_zvs_rng Script.

Function: Calculate the minimum currents in each leg of LCL DAB converter using IGBTs in the both bridges, for dcr and Monte Carlo component variations.

Outputs Plot of Leg currents versus modulation.

Calls lcl_iv12

lcl_loss_2fet Function**.**

Function: Calculate all losses in LCL DAB converter using MOSFETs in the both bridges. Used for the assembly of the loss table.

Inputs Parameters passed are φ, m_1, m_2. Parameters specified in function are V_{DC1}, V_{DC2}, X_D, t_r, f, k_1 to k_4, R_1, R_2 and MOSFET t_{fu}, t_{ru}, t_{ri}, t_{fi}, Q_{rr} and R_{on}.

Returns Column vector having 29 rows: modulation, all loss components, input and output power, efficiency and bridge rms currents.

Loads Matrix vc(2,630) from Thermal\Volts_D_R.mat. This was written by script v_r_d.m, and provides the voltage drop of a parallel diode-resistor combination, for 3rd quadrant operation.

Comments Based on Figure 3.3 and equation (9). Losses are added to the results of a lossless circuit analysis. Run v_r_d.m first with MOSFET temperature and R_{on} values entered.

STGWA19N60_swg_loss Function.

Function: Calculate switching losses of STGWA19N60 IGBT.

Inputs Parameters passed are the transistor's temperature, voltage and current.

Returns Switch-off and switch-on energy losses E_{off} and E_{on}.

Comments	Uses a 3 term polynomial. Data is fitted and calculated in STGWA19N60_swg_loss_data. Temperature interpolation.

STGWA19N60_vd Function.

Function:	Calculate the forward voltage of the diode in a STGWA19N60 IGBT.
Inputs	Parameters passed are the transistor's temperature and its current.
Returns	Diode forward voltage vd.
Comments	Uses a log function. Data is fitted and calculated in STGWA19N60_v_data. Temperature interpolation of value.

STGWA19N60_vt Function.

Comments	Similar to STGWA19N60_vd above, but calculates the voltage of the IGBT's transistor.

lcl_iv12 Function.

Function:	Calculate i_1, i_4, v_1 and v_2 in Figure 3.3 at specified location.
Inputs	Parameters passed are V_{DC1}, V_{DC2}, φ, m_1, m_2, X_D, k_1 to k_4, t_r and an index for the location.
Returns	i_1, i_4, v_1 and v_2.
Comments	Calculates the phasors, then sums the time domain components.

v_r_d Script.

Function:	Calculates and saves a voltage-current matrix for a parallel resistor and diode carrying a specified current.
Inputs	Current look-up index, one unit per 0.1A. Resistance, diode characteristic and temperature.
Outputs	Voltage.

Comments — Uses diode equations with temperature interpolation, apportioned currents.

clc_dab_2igbt — Script.
This has the same functionality as lcl_dab_2igbt, but is for a CLC DAB converter based on Figure 4.2 and equation (25).

clc_loss_2igbt — Function.
This has the same functionality as lcl_loss_2igbt, but is for a CLC DAB converter based on Figure 4.2 and equation (25).

clc_loss_2fet — Function.
This has the same functionality as lcl_loss_2fet, but is for a CLC DAB converter based on Figure 4.2 and equation (25).

clc_zvs_rng — Script.
This has the same functionality as lcl_zvs_rng. It calls clc_iv12.

lcl_modopt_p10 — Script.

Function: Find the optimal modulations for a LCL DAB converter for 10% steps in a specified power output.

Inputs — V_{DC1}, V_{DC2}, X_D, t_r, f, temp, k_4, R_1, R_2.

Outputs — Input and output power, modulations φ, m_1, and m_2, rms currents and volt.μs products.

Calls — lcl_d_2igbt (or other hardware, as required).

Comments — Can operate with reverse power. Assumes that the converter has a tuned network (k_1...k_3 = 1), so that only entry of the relative magnetising reactance (k_4) is required.

clc_modopt_p10 Script.

Function: Find the optimal modulations for a CLC DAB converter for 10% steps in a specified power output.

Inputs V_{DC1}, V_{DC2}, X_D, t_r, f, temp, k_1, R_1, R_2.

Outputs Input and output power, φ, m_1, and m_2, rms currents and volt.μs products.

Calls clc_d_2igbt (or other hardware, as required).

Comments Can operate with reverse power. Assumes that the converter has a tuned network, so that only entry of the value of L_1 relative to X_D (k_1) is required.

lcl_d_2igbt Function.

Function: Calculate the currents, voltages, powers and volt-second products of LCL converter having a transformer with distributed leakage inductance.

Inputs Parameters passed are V_{DC1}, V_{DC2}, φ, m_1, m_2, X_D, k_m, t_{rr} and f.

Returns p_1, p_2, $i_1$rms, $i_3$rms, i_{b2}rms, i_{c1}rms, vs_{l1}, vs_{m1} and vs_{m2}.

Comments Reactances are tuned. RMS ripple current calculations added at end, for manual use.

clc_d_2igbt Function.

Comments: For a CLC converter. Has the same functionality as lcl_d_2igbt above.

L_d_2igbt Function.

Comments: For a CDAB converter. Has the same functionality as lcl_d_2igbt above.

lcl_cost_min Script.

Function: Find the minimum total lifetime cost of operating a LCL DAB converter in a specified set of conditions.

Inputs The hardware specified by X_D, k_m, t_{rr}, f, k_r. Operating conditions specified by the runtime at each power level, the DC link voltages and forward and reverse. Costs include the unit cost of power and the hardware costs specified by a number of proportionality constants.

Outputs Optimum hardware parameters, volt-second products and rms current ratings required for magnetic components. Maximum heatsink dissipation. Average efficiency. Energy used. Running cost, cost of hardware and total cost.

Comments Pre-calculated optimised LCL data, gathered by lcl_data, is retrieved from the matrix LCL_June30.mat which is loaded into the workspace. Assumes that the converter has a lifetime of 10 years, uses IGBTs to implement both bridges. Runs for 20000 hours. Run profile is mainly forward at maximum power.

clc_cost_min Script.

Comments For a CLC DAB converter. Very similar to lcl_cost_min. The hardware is specified by k_1, rather than k_m.

L_cost_min Script.

Comments For a CDAB converter. Very similar to lcl_cost_min.

Appendix B Magnetic Component Power Losses and Costing

The power loss of the winding in a magnetic component is:

$$p_w = {I_w}^2 \frac{\rho L_t N^2}{A_w} \quad (55)$$

Where:

p_w = winding power loss (W)

I_w is the rms winding current (A)

ρ is the resistivity of the conductor (Ωm)

L_t is the average length of a turn (m)

N = number of turns

A_w = area of winding window (m^2)

The power loss of the core in a magnetic component is:

$$P_c = V_c k B^{\alpha} f^{\beta} = A_c L_c k (\frac{V_{sp}}{2NA_c})^{\alpha} f^{\beta} \quad (56)$$

Where:

V_c = core volume (m^3)

k is the Steinmetz constant

B is the peak flux density (Wb/m^2)

f is the frequency (Hz)

V_{sp} is the voltage-second product (Vs)

A_c is the core cross sectional area (m^2)

L_c is the core magnetic length (m)

The total power loss is:

$$p_t = p_w + p_c \quad (57)$$

Substituting (55) and (56) into (57), then differentiating with respect to N and then equating to 0 yields the value of N for minimal power loss. Substitution of this N value into (55) and (56) yields the relationship:

$$p_w = \mathrm{p_c}\frac{\alpha}{2} \tag{58}$$

From (55), (56) and (57) the minimum total power loss is:

$$p_{t\_min} = (I_w V_{sp})^{\left(\frac{2\alpha}{2+\alpha}\right)} A_w{}^{\left(\frac{-\alpha}{2+\alpha}\right)} \left(\frac{L_c}{A_c{}^{\alpha-1}}\right)^{\left(\frac{2}{2+\alpha}\right)} L_t{}^{\left(\frac{\alpha}{2+\alpha}\right)} \frac{(\alpha+2)\rho}{\alpha} \left(\frac{\alpha k f^{\beta}}{2^{\alpha+1}\rho}\right)^{\left(\frac{2}{2+\alpha}\right)} \tag{59}$$

For a core with a given geometric shape, the power loss will vary from a base value as all dimensions are scaled equally from their base values. If the linear dimensions are increased by a scale factor k_L, the expression (59) may be rewritten, with the introduction of a proportionality constant k_p, which takes the base value into account:

$$p_{t\_min} = k_p (I_w V_{sp})^{\left(\frac{2\alpha}{2+\alpha}\right)} k_L{}^{\frac{6-5\alpha}{2+\alpha}} f^{\frac{2\beta}{2+\alpha}} \tag{60}$$

The expression (60) shows how the loss of an optimally designed magnetic component is related to the power throughput, the component's size and the operating frequency. For Ferroxcube 3C90 core material, α is approximately equal to 2.8 and β is approximately equal to 1.46. For these exponents (60) may be rewritten:

$$p_{t\_min} = k_p (I_w V_{sp})^{1.17} k_L{}^{-1.67} f^{0.61} \tag{61}$$

The second term of (61) is dependent on the power throughput, which is related to the product of the component's rms current and its volt-second product. This is a more accurate gauge of the power rating of a high frequency magnetic component having a non-sinusoidal waveform than the VA product of its rms voltage and current.

The third term in (61) may be thought of as the loss reduction factor, k_r, which defines the power loss reduction that occurs as a result of an increase, in isolation, in the component's size:

$$\mathrm{k_r} = k_L{}^{-1.67} \tag{62}$$

As an example, for 3C90 core material, a lineal size increase by a factor of 2 will result in the total loss of the magnetic component changing by a factor k_r of $2^{-1.67}$, equating to 0.31; the volume needs to increase by a factor of 8 to achieve this loss reduction.

The fourth term of (61) shows how an increase in the operating frequency increases the power loss. As a consequence of the exponent being smaller than that in the Steinmetz equation, the power loss doesn't increase as quickly with frequency.

Again, for a given geometric shape and for a given maximum temperature rise, the power loss, or dissipation, of the magnetic component is proportional to its surface area, which is proportional to the square of the linear dimension:

$$p_{t\_min} = k_s {k_L}^2 \tag{63}$$

Where k_s is a proportionality constant.

Assuming that the power throughput is dissipation limited, from (61) and (63), it follows that:

$$I_w V_{sp} = \left(\frac{k_s}{k_p}\right)^{0.86} \frac{{k_L}^{3.14}}{f^{0.52}} \tag{64}$$

Where k_p is a proportionality constant.

The expression (64) indicates that, at a particular operating frequency, the power rating of the magnetic component is proportional to the linear dimension raised to the power of 3.14. For comparison, the classical relationship, which is based on a specified maximum winding current density and maximum core flux density, states that the power rating depends on the area product and therefore results in the rated power being proportional to the linear dimension raised to the power of 4. It may appear from the frequency term in the denominator of (64) that the power rating decreases as f increases; this is not the case, as there is an inherent f term embedded in the volt-second product.

As a first order approximation the cost of a magnetic component is proportional to its volume, the cube of the linear dimension. From (61), for a specified power loss:

$$const = k_p (I_w V_{sp})^{1.17} {k_L}^{-1.67} f^{0.61} \tag{65}$$

Taking the cube of k_L, the magnetic component's cost is:

$$Cost = k_c(I_w V_{sp})^{2.1} f^{1.1} \tag{66}$$

Where k_c is a proportionality constant.

Again, (66) is based on a magnetic component using 3C90 material. An increase in the operating frequency, with an attendant decrease in V_{sp}, results in a cost reduction, as expected, with an inverse frequency relationship. Incorporating the cube of k_L as well, from (62), provides the complete relationship:

$$Cost = k_c(I_w V_{sp})^{2.1} f^{1.1} {k_r}^{-1.8} \tag{67}$$

Appendix C Implementing Distributed Leakage Inductance in Transformers

LCL Converter

For a converter making use of the transformer's leakage inductance for the implementation of inductor L_2 in Figure 3.3, an accurate model, in which the leakage inductance is distributed, is shown in Figure C.1. In this circuit inductors L_2 and L_4 represent the primary-referred leakage inductance of transformer Tx and L_3 represents its magnetising inductance. The calculated values are for a tuned system.

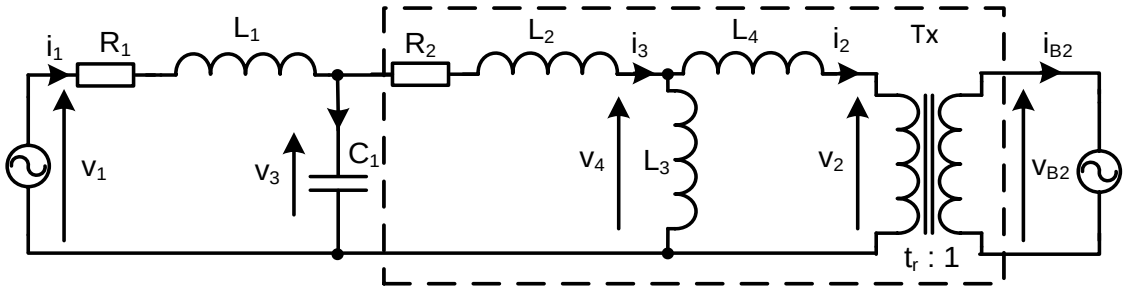


Figure C.1: Model of LCL converter with distributed transformer leakage inductance

The magnetising inductance is defined as:

$$\mathrm{L_3 = k_m(L_2 + L_4) = k_m * 2L_2} \tag{68}$$

A tuned network requires that the inductance to the left of C_1, L_1, is equal to the effective inductance to the right of C_1:

$$L_1 = \mathrm{L_2 + L_3//L_4 = L_2}\frac{1 + 4k_m}{1 + 2k_m} \tag{69}$$

Using Thevenin's theorem, the effective voltage driving the effective inductance is:

$$\mathrm{v_e} = \mathrm{t_r}v_{B2}\frac{L_3}{(L_3 + L_4)} = v_{B2}\frac{t_r}{1 + \frac{1}{2k_m}} = v_{B2}t_{rr} \tag{70}$$

In (70), t_{rr} is the effective transformer turns ratio, as a result of a finite k_m value.

The parameters used in the MATLAB program lcl_d_2igbt are:

$$\begin{aligned} \mathrm{X_{L1}} &= \omega_s \mathrm{L_1} = \mathrm{k_1 X_D} = X_D \\ \mathrm{X_{L2}} = \mathrm{X_{L4}} &= \omega_s \mathrm{L_2} = \frac{\mathrm{k_2 X_D}}{2} = \frac{1+2k_m}{1+4k_m} X_D \\ \mathrm{X_{C1}} &= \frac{1}{\omega_s \mathrm{C_1}} = \mathrm{k_3 X_D} = X_D \\ \mathrm{X_{L3}} &= \omega_s \mathrm{L_3} = \mathrm{k_4 X_D} = 2k_m \frac{1+2k_m}{1+4k_m} X_D \end{aligned} \tag{71}$$

CLC Converter

Inductor L_1 in Figure 4.2 is replaced with two, distributed, inductors, L_1 and L_3. The topology of the converter is:

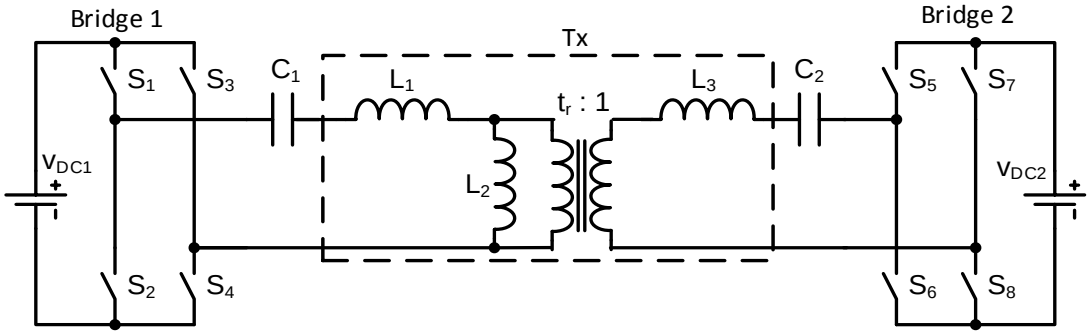


Figure C.2: Topology of CLC converter with distributed transformer leakage inductance

With L_3 and C_2 referred to the primary as L_3' and C_2', the model for analysis is:

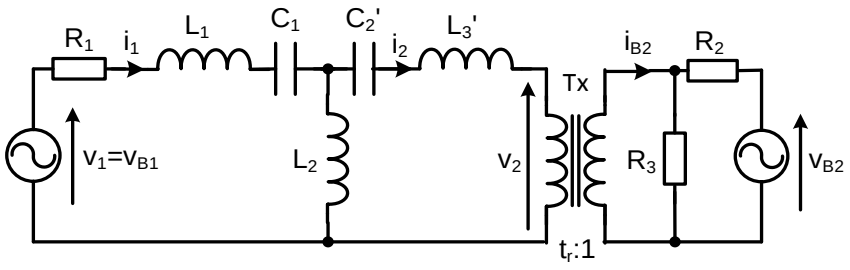


Figure C.3: Model of CLC converter with distributed transformer leakage inductance

For each of the three legs of the Tee network to have a reactance of X_D, the component values and the parameters used in the MATLAB program clc_d_2igbt are:

$$\begin{gathered} C_1 = C_2', \quad L_1 = L_3' \\ X_{L1} = \omega_s L_1 = \frac{k_1 X_D}{2} \\ X_{L2} = \omega_s L_2 = X_D \\ X_{C1} = \frac{1}{\omega_s C_1} = (1 + \frac{k_1}{2}) X_D \end{gathered} \tag{72}$$

Appendix D Costings in this Thesis

In this thesis the per-unit pricing was based on 1000 unit quantities and costs are given in New Zealand dollars at the time of writing.

Electrical Energy Cost

The retail cost of electricity is approximately $0.29 per unit (kW.hour) [http://www.mbie.govt.nz/info-services/sectors-industries/energy/energy-data-modelling/statistics/prices/electricity-prices/sales-based-residential-prices.pdf].

Heatsink and Fan Cost

The pricing is based on the characteristics of an OS509-140 heatsink made by Aavid Thermalloy [http://www.aavid.com/]. This heatsink is 140 mm long and has the cross-section shown in Figure D.1.

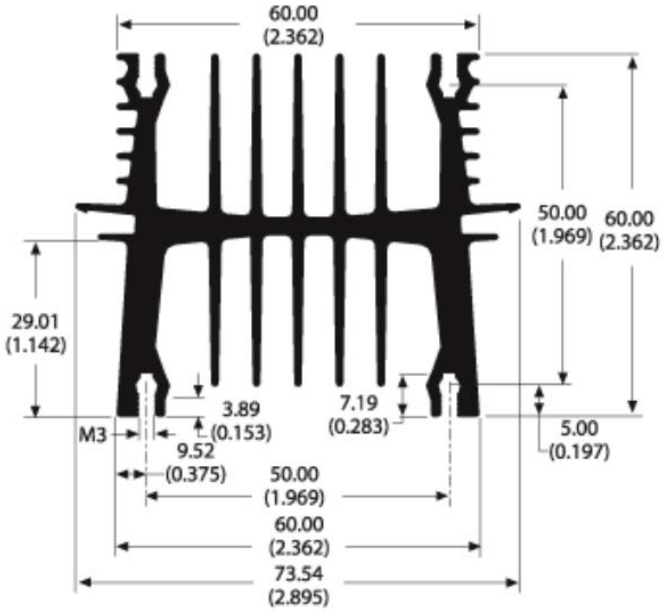


Figure D.1: Heatsink cross-section

Forced cooling tests conducted with a KDE1206 60 mm square fan running at rated voltage yielded a heatsink temperature rise of 35°C above ambient when dissipating 211 W. Extrapolating from this, and assuming a maximum ambient temperature of 33°C, at the maximum design temperature of 75°C the heatsink will dissipate 253 W. The heatsink cost is $17.74 and the fan cost is $7.5, a combined cost of $25.24 to dissipate 253 W, so

that the cost coefficient is approximately $0.10/W [http://nz.element14.com/fans-heat-sinks-hvac].

Capacitor Costing

The costs of a number of Cornell Dubilier 940 series polypropylene capacitors, with capacitances in the range 47 nF to 1 μF, were plotted against their maximum stored energy, as shown in Figure D.2 [http://nz.element14.com/film-capacitors].

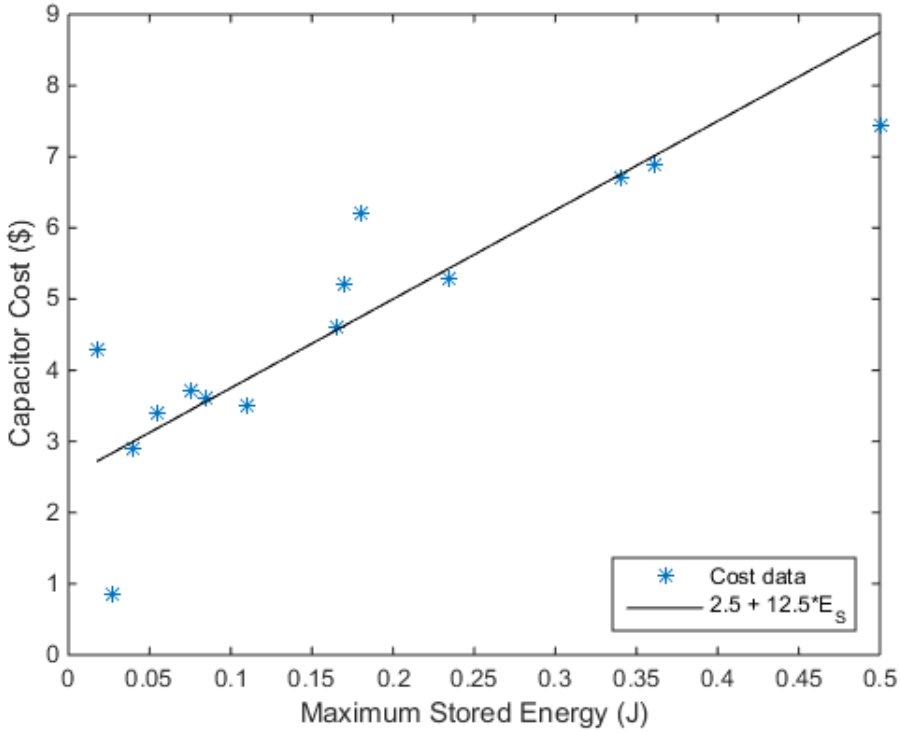


Figure D.2: Capacitor cost as a function of stored energy

A reasonable model for the capacitor's cost is given by (73):

$$Capcost = 2.5 + 12.5 * \mathrm{E}_S \tag{73}$$

$$E_S = 0.5 C {V_M}^2 \tag{74}$$

Where:

E_S is the maximum stored energy (J)

V_M is the maximum voltage (V)

C is the capacitance (F)

For a sinusoidal current waveform:

$$E_S = 0.5\left(\frac{1}{2\pi f X_c}\right)\left(\sqrt{2} i_c X_c\right)^2$$
$$E_S = \frac{0.5 X_c {i_c}^2}{\pi f} \quad (75)$$

From (73) and (75), the approximate cost is:

$$Capcost = 2.5 + \frac{2 X_c {i_c}^2}{f} \quad (76)$$

Where:

Xc is the reactance of the capacitor (Ω)

i_c is the capacitor's rms current (A)

Transformer Cost

The basis for the costings of the magnetic components was a dual E65 core set, comprising four cores, one bobbin and the copper wire. The prices of these were $3.60 per unit, $0.45 per unit and $34 per kilogram respectively [http://marquemagnetics.com/].

The windings were assumed to occupy 90% of the bobbin's winding window with a winding factor of 0.8, resulting in a copper volume of 76 cm^3 From the wire tables for 280/38 Litz wire, the 2.2 mm^2 wire has a mass of 1 kg per 97 cm^3, so that the winding mass is approximately 0.78 kg. [http://www.pack-feindraehte.de/en/products/litzwire/technische_daten.php?produkt_id=1&LC=EN].

The assembly cost has been assumed to be negligible compared to the material costs, so that the total cost of this magnetic component is $41.4.

Transistor Cost

The unit price of an STGWA19NC60 IGBT is $2.50, and the unit price of an IXFH26N60 MOSFET is $12.88 [http://nz.mouser.com/Semiconductors/Discrete-Semiconductors/_/N-awhng/].

Appendix E Three Phase Resonant DC-DC Converters

A three phase converter could be implemented by using three individual DAB converters, phase shifted 120° from each other, and sharing common dc links. The main advantage of this hardware intensive implementation would be the significantly reduced dc link ripple currents resulting from interleaved operation. Also, in theory, a smaller transformer is required, but this may not be practical.

An economic implementation of a three phase converter consists of two three-phase bridges, in which each bridge comprises three legs which are driven with phase displacements of 120° to each other, as in Figure E.1. This has line voltages which are the same as those of three individual DABs, each with bridge amplitude modulations of 2/3. Looking at the fundamental components for this system, the line currents are 60° ahead of the phase currents, which are, in these resonant converters, in phase with the line voltages. The phase voltages lag the line voltages by 30°, so that the line currents, which are the leg currents, lead the phase voltages by 90°, so that the switching points of the legs are at the zero crossings of the leg fundamental currents. For this reason, a three phase LCL resonant converter operating at full power has the significant advantage that the leg current at the switching point of each leg is approximately 10% of the leg current's peak value; there is a similar result for the CLC converter. As a consequence the switching losses in the three phase resonant converter will be small compared to the standard CDAB, which switches at approximately 80% of its peak current when operated at full power.

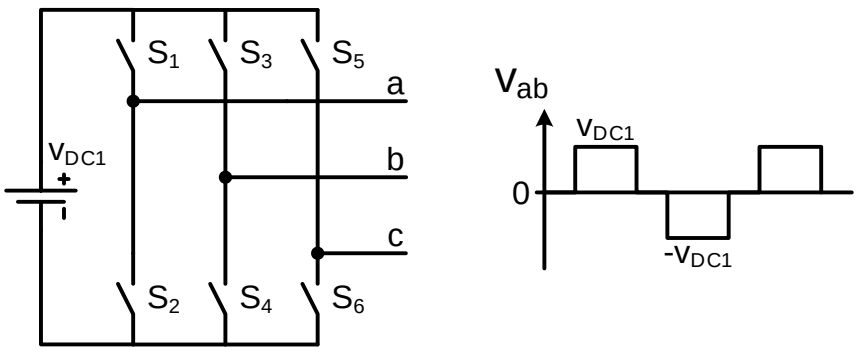


Figure E.1: Three phase bridge and its line voltage

For the LCL and CLC resonant converters, the disadvantage of using this three phase topology is that the amplitude modulation is fixed at 2/3. These converters would typically be controlled by varying the bridge amplitude modulation, with a fixed phase shift of either 90° or -90° between the bridges. If a three phase converter having the proposed resonant topology were implemented using the phase shift between bridges to control the power throughput, the advantage of the smaller conduction losses that these converters have is negated for all but maximum modulation values. As the bridge amplitude modulation is fixed at 2/3, an alternative control system is required for operation at reduced power levels. Control systems such as burst mode or frequency control may be attractive options.

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