Effect of Coupling Capacitance in Voltage Multiplier Design Optimization for RF Energy Harvesting

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***Abstract*—Electromagnetic energy harvesting has been identified as a free compliment resource to wireless sensor nodes, which essentially prolongs the operating lifespan of built-in batteries. Voltage multiplier is a critical component in energy harvesting circuits and it attracted plenty of efforts in studying how to optimize the design. However, little information was found on how to determine the necessary amount of coupling capacitance required in a voltage multiplier design. This paper aims to fill in this gap and provides an analysis on how coupling capacitance affects voltage and power outputs. Computer simulations affirm that as long as the coupling capacitance is beyond a certain value, .e.g., 10pF for Wi-Fi energy harvesting circuit operating at 2.45GHz, it has limited effect on voltage output and power output of a voltage multiplier.**

Keywords-energy harvesting, voltage multiplier, pumping capacitance, circuit design

I. INTRODUCTION

The recent flourish of wireless communications is accelerated by the advancement in complementary metal-oxide-semiconductor (CMOS) technology and digital signal processing (DSP) algorithms. Among those wireless systems, wireless sensor networks (WSNs) promise a ubiquitous wireless networking paradigm in the near future with an salient feature by integrating wireless communications, micro-electro-mechanical systems (MEMS) and DSP [1]. The rising concept of Internet of Things (IoTs) [2], which promotes pervasive wireless networking among all the entities in the universe, could be considered as an extension of WSNs. As we know, energy is always required for proper operations of transceivers and DSP units in sensor nodes, which is usually stored in the form of chemical batteries. However, replacing batteries become extremely difficult, if not impossible, because wireless sensor nodes are expected to be deployed in harsh or even hazardous environment. When the built-in batteries run out of power, those sensor nodes will become useless, and even pollutive given the fact that some batteries are not environmental friendly.

In order to solve such kind of bottleneck related to WSNs, one may rely on reducing the operating voltages of embedded systems to prolong the operating life of on board batteries of wireless sensor nodes. With the continuing scaling down of CMOS technology according to Moore's Law, creative radio transceivers and simple DSP units can now operate with supply power as low as hundreds of nano-watts [3]. Alternatively, one may adopt energy harvesting [4], as a complementary or replaceable energy source in the design of wireless sensor nodes. For example, several types of energy sources, such as solar energy (i.e., photovoltaic), electromechanical energy (i.e, piezoelectric), kinetic energy (e.g., wind, tide, vibrational movement), thermoelectric energy and electromagnetic energy [5] have been proposed. Among those available energy resources, ambient radio frequency electromagnetic energy has the least power density, around 1μW/cm^2. The idea of harvesting electromagnetic energy dated back in the late 19th century when Nikola Tesla described the concept of wireless power transfer, though it remains the most challenging type of energy to be harvested [6].

We could achieve electromagnetic energy harvesting through one of the following three methods: (i) near-field magnetic resonance and inductive coupling; (ii) far-field radio frequency (RF) / microwave rectenna conversion; and (iii) laser-based optical power transmission/reception, among which the last two methods are feasible for fairly long distance [7]. For example, radio frequency identification (RFID), which has been widely used in our daily life, essentially adopts electromagnetic energy harvesting using near-field radiation in high frequency (HF), 13.56MHz or using far-field radiation in ultra high frequency (UHF), 860MHz~920MHz. In brief, energy radiated from a RFID reader was harvested by a RFID tag, which rectifies the signal, converts it to useful DC power to drive the chip, and backscatters its transmitted data to the RFID reader. The reading range of purely passive RFID tags is dependent on the transmit power level of a RFID reader, and typically within 1 meter under the regulated radio radiation level [8].

Although the principle of electromagnetic energy harvesting is to convert RF signals to DC power, it is not a trivial task to design such an energy harvesting circuit. It usually consists of five components: (i) an antenna, (ii) an impedance matching network, (iii) a voltage multiplier, (iv) a voltage regulator and (v) a large capacitor or re-chargeable battery as energy reservoir. Antenna design and impedance matching have been well-explored in the literature, while little work was found on design of voltage multiplier for the purpose of energy harvesting, despite of plenty of work reported on

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voltage multiplier for high voltage generation in power electronics. In this paper, we focus on the design of voltage multiplier in microwave frequency.

Voltage multiplier consists of a number of peak-to-peak detectors and also known as charge pump (though some papers referred charge pump as a DC step-up converter). Historically, voltage multiplier was evolved from voltage doubler [9], which is made of two capacitors and two diodes. Schottky diodes are usually used due to their superior performance in terms of low forward voltage, low substrate loss, fast switching and excellent frequency response, all of which are important for an energy harvesting circuit. Nevertheless, diode-connected transistors in CMOS technology present the alternative with reduced integration cost [7]. Vita and Iannaccone provided the design criteria for the energy harvesting section of UHF and microwave passive RFID tags with 0.35μm CMOS technology [10] and they proposed a model for Dickson voltage multiplier using modified Bessel functions. In a separate effort, Curty et al. proposed a linear two-port model for Cockcroft-Walton voltage multiplier at 915MHz. Furthermore, a quadratic model in 0.18μm CMOS technology and a linear model in 0.35μm CMOS technology for Dickson voltage multiplier was developed in [11] and [12], respectively. They both validated their results at 860~910MHz frequency band. A more comprehensive work on RF energy harvesting was recently reported in [13], where the authors also focused an operating frequency at 915MHz. None of the aforementioned work discussed on how to select the coupling capacitance in a voltage multiplier design.

Popularity of wireless local area networks (WLANs) using Wi-Fi at 2.4GHz and 5.2GHz motivates us to investigate RF energy harvesting at higher frequency rather than those bands lower than 920MHz. A pioneer work studied an integrated energy harvesting circuit for digital TV (DTV), GSM 900MHz, GSM1800 and Wi-Fi 2.4GHz signals [14]. However, they did not bother an analytical model for voltage multiplier in 2.4GHz band. In this paper, we attempt to develop such an analytical model to help researchers and developers to select proper coupling capacitance in the design and implementation of RF energy harvesting circuits for Wi-Fi signals.

The rest of this paper is organized as follows. In Section II, we revisit the circuits for voltage multiplier, followed by our proposed analytical model on the selection of coupling capacitance in Section III. In Section IV, we discuss computer simulation results from Agilent ADS. Finally, Section V concludes our work.

II. MODIFIED DICKSON VOLTAGE MULTIPLIER

Voltage multiplier was originally designed to convert a low AC voltage to a higher DC voltage using multiple stages of voltage doubler, for which two conventional configurations are Villard Doubler circuit (see Fig. 1(a)) and Greinacher Doubler circuit (see Fig. 1(b)). Noteworthily, British physicists John Cockcroft and Ernest Walton invented Cockcroft-Walton voltage multiplier (see Fig. 1(c)) based on Greinacher Doubler and for which they won the Nobel Prize in 1951. Later, Dickson improved Cockcroft-Walton voltage multiplier by introducing clocking signals in the circuit, as shown in Fig. 1(d). However, the requirement of extra clocking signals prevents Cockcroft-Walton or Dickson voltage multiplier from being adopted in energy harvesting circuits. Fortunately, modified Dickson voltage multiplier (as shown in Fig. 1(e)) eliminates the requirement of clocking signals and it becomes extremely popular in the design of energy harvesting circuits.

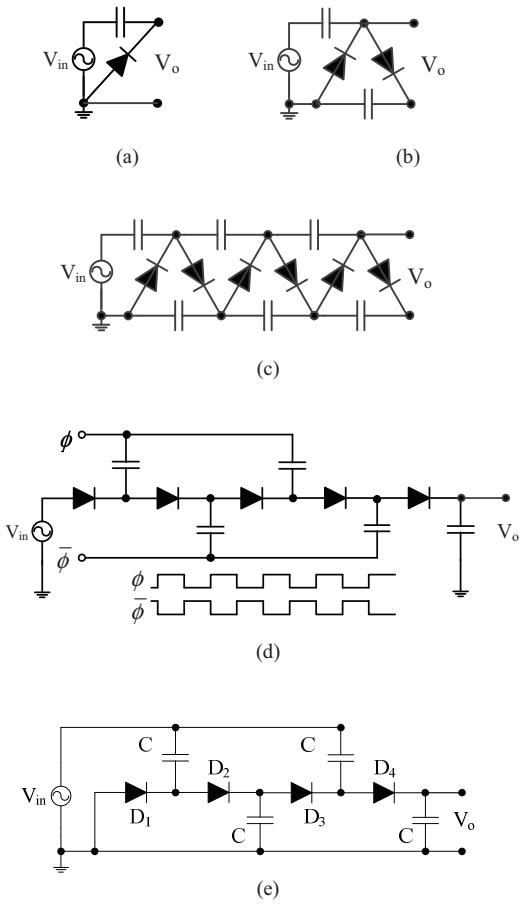

Fig. 1. Evolution of Voltage Multipliers: (a) Villard Voltage Doubler; (b) Greinacher Voltage Doubler; (c) Cockcroft-Walton Voltage Multiplier; (d) Dickson Voltage Multiplier; (e) Modified Dickson Voltage Multiplier.

A. Voltage and Power Output

For Dickson Voltage Multiplier shown in Fig. 1(d), Dickson provided an empirical formula for its peak voltage output [15].

$$V_o = V_{in} + N\left[\left(\frac{C}{C+C_S}\right)V_\phi - V_T\right] - V_T - \frac{NI_o}{(C+C_S)f} \qquad (1)$$

where V_{in} is the DC input voltage, N is the number of diodes, C is the clock coupling capacitance, C_S is the parasitic capacitance at each diode, $V_{\square}$ is the peak-to-peak voltage of clock signal, V_T is the diode threshold voltage, f is the clock frequency and I_{out} is output current. For Modified Dickson

Voltage Multiplier, V_{in} is zero (as no DC input is required) and $V_{□}$ is equal to $2V_{ac}$, where V_{ac} and f are the amplitude and the frequency of RF input signal, respectively. We assume sinusoidal voltage input and the following derivation can be extended to other types of input signals. Purely resistive load is assumed with R_L, thus we have

$$I_o = \frac{V_o}{R_L} \tag{2}$$

By substituting (2) into (1) we can have

$$V_o = \frac{2NfR_L CV_{ac} - (N+1) fR_L (C+C_S) V_T}{fR_L (C+C_S) + N} \tag{3}$$

and the power delivered to the load is

$$P_o = \frac{V_o^2}{R_L} \tag{4}$$

In order to have a positive DC output, the input signal must have an amplitude

$$V_{ac} \geq \frac{(N+1)(C+C_S)}{2NC} V_T \tag{5}$$

which provides us a good reference on the minimum input voltage. However, limited information could be found on how to select the values of coupling capacitance, C, although the optimal value of N can be found by simple iterations. In practice, the values of available capacitance range from several femtofarads (fF) to hundreds of microfarads (μF) and it is not a trivial task to obtain the optimum value, which motivates us to look for an analytical method to address this issue.

III. Selection of Coupling Capacitance

We attempt to derive an analytical model to look for the optimal value of coupling capacitance, which plays an important role in the design of voltage multiplier.

A. Power Output

From (3) and (4), we can see that P_o is a function of C, therefore, we look at the first order derivative

$$\frac{dP_o}{dC} = \frac{X(Y-Z)}{R_L [fR_L (C+C_S) + N]^3} \tag{6}$$

where $X=2[2NfR_LCV_{ac}-(N+1)fR_L(C+C_S)V_T]$, $Y=[2NfR_LV_{ac}-(N+1)fR_LV_T][fR_L(C+C_S)+N]$, $Z=[2NfR_LCV_{ac}-(N+1)fR_LC+C_S)V_T]fR_L$. By setting the first order derivative to zero, we can have

$$\begin{cases} (a).\ X=0 \Rightarrow C = \dfrac{C_S}{\dfrac{2NV_{ac}}{(N+1)V_T} - 1} \\ (b).\ Y=Z \Rightarrow V_{ac} = \dfrac{(N+1)V_T}{2(N+fR_LC_S)} \end{cases} \tag{7}$$

Conditions (a) and (b) in (7) are independent, therefore P_o will achieve its maxima when either condition is met. Let us denote the particular coupling capacitance at which P_o achieves its maxima as C_{opt}. For condition (a), we notice that C_{opt} will vary according to the input voltage V_{ac}. This imposes a challenging design problem—if the design objective is to maximum P_o at a wide range of power inputs, one needs to find a way to adapt the coupling capacitance accordingly to V_{ac}, which is certainly not an easy task. The second order derivative of (3) is not negative at all times, which indicates that maximum P_o may not be achievable.

$$\frac{d^2P_o}{dC^2} = (Y-Z)\frac{d}{dC}\left(\frac{X}{Q}\right) \tag{8}$$

where $X=2[2NfR_LCV_{ac}-(N+1)fR_L(C+C_S)V_T]$, $Y=[2NfR_LV_{ac}-(N+1)fR_LV_T][fR_L(C+C_S)+N]$, $Z=[2NfR_LCV_{ac}-(N+1)fR_LC+C_S)V_T]fR_L$, $Q=R_L[fR_L(C+C_S)+N]^3$.

For condition (b), it indicates that once V_{ac} is fixed at a particular value, denoted as $V_{ac,opt}$, P_o can achieve its maxima without dependence on C.

$$V_{ac,opt} = \frac{(N+1)V_T}{2(N+fR_LC_S)} \tag{9}$$

From (8), we can see that $V_{ac,opt}$ is a rather fixed values as when the voltage multiplier circuit is fixed, values of N, V_T, R_L, and C_S are determined values and f is the only variable. However, it is impractical to change f especially when the energy resource is also fixed.

B. Voltage Output

As discussed above, the maximum voltage output of a Modified Dickson Voltage Multiplier is given in (3). Let us take the first order derivative of (3), then

$$\frac{dV_o}{dC} = \frac{S-T}{[fR_L(C+C_S)+N]^2} \tag{10}$$

where $S=[2NfR_LV_{ac}-(N+1)fR_LV_T][fR_L(C+C_S)+N]$, $T=[2NfR_LCV_{ac}-(N+1)fR_L(C+C_S)V_T]fR_L$. By setting the first order derivative to zero, we can have

$$S = T \Rightarrow V_{ac} = \frac{(N+1)V_T}{2(N+fR_LC_S)} \tag{11}$$

which is identical to (8), indicating that the coupling capacitance does not affect the maximum voltage output that can be achieved by the voltage multiplier.

IV. Simulation Results

We use Agilent ADS software to validate the model and simulate a voltage multiplier made of two diodes and two coupling capacitors. Schottky diodes with model number HSMS-2862 from Avago Technologies [16] are used in the design, and Fig. 2 shows the schematic of the simulated voltage multiplier. We have included the effect of parasitic capacitances and inductances of package type SOT-23 by using the linear models provided in [17]. Input power is fixed at 0dBm, and then a sweep from -10dBm to 15dBm is performed. After preliminary simulations, load resistance is fixed at 350Ω in order to achieve maximum power delivery at the load. Coupling capacitance, C, is varied from 1pF to 2000pF. DC voltage, V_o and power efficiency

$$\eta = \frac{P_{out}}{P_{in}} \tag{12}$$

are two important performance metrics for the design of voltage multipliers. Furthermore, we also look at the input matching in terms of S_{11} (S-Parameters) to determine the return loss.

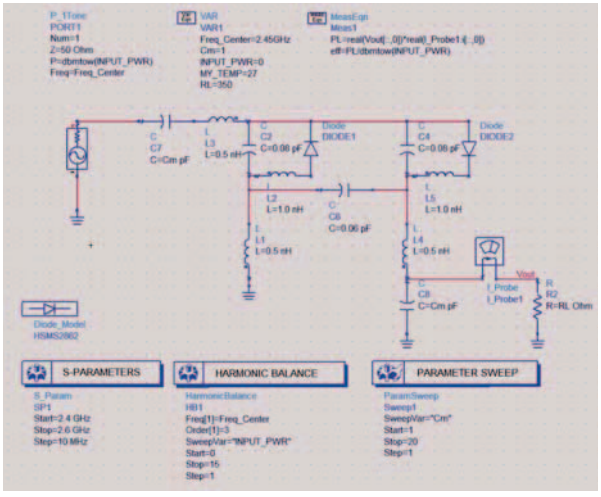

Fig. 2. Simulated Voltage Multiplier

As shown in Fig. 2, two simulation instances are used, harmonic balance and s-parameters to investigate the effect of different input power level and input matching, respectively. As our design focuses on harvesting Wi-Fi signals, the operating frequency of the input signal is set to 2.45GHz. For S-parameter simulation, it is varied from 2.4GHz to 2.6GHz. Room temperature at 27°C is used in the simulation.

At 0dBm input power, Fig. 3 shows that coupling capacitance has negligible effect on DC voltage output and power efficiency of voltage multiplier. In order to confirm this observation, we have refined the sweep range to [1pF 20pF]. When the value of C is small (<10pF), increasing C will improve the performance of a voltage multiplier. In addition, the value of C should be larger than the diode stray capacitance, C_S (about 0.08pF in the simulation), as we have noticed in (7). Once C is greater than 10pF, the performance gain due to increasing C is diminishing.

Fig. 4 presents the transient effect of coupling capacitance. We can see that when C is small, output voltage appears as biased AC voltage. The output voltage rises gradually as C increases, and the ripple voltage will become smaller. This is due to the longer time required to discharge a larger capacitor, which smooth out the output voltage. We further observed that the output voltage tends to saturate at the same value despite of different C values, as long as it is beyond certain critical value about 1.5pF.

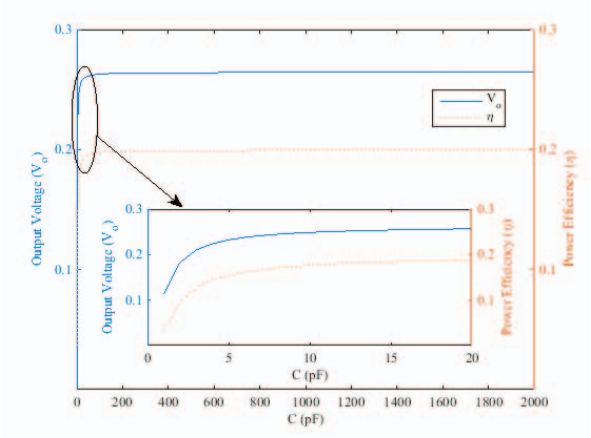

Fig. 3. Effect of Coupling Capacitance C=1~2000pF

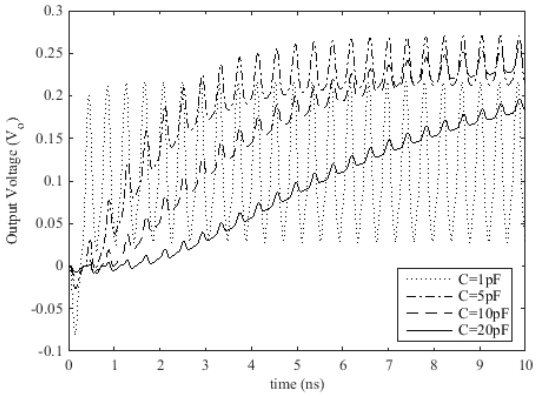

Fig. 4. Transient Effect of Coupling Capacitance C=1~20pF

As can be seen from Fig. 5, when the input power is increased, C affects the output voltages in a similar way—when C exceeds 10pF, its effect on output voltages starts to saturate. In fact, the effect of load resistance (R_L) will dominate. The larger the load resistance, the higher the output voltage. Fig. 6 reveals that it is important to increase C beyond the critical value (~10pF) in order to achieve good power efficiency. Furthermore, when input power increases beyond 15dBm, the effect of C tends to saturate.

Fig. 7 shows that *C* has limited effect on input matching, and the input impedance remains capacitive at a wide range of operating frequencies.

V. Conclusion

An analytical model on how to select the coupling capacitance in a voltage multiplier design is presented. Through computer simulations, we find that when the coupling capacitance is small, performance improvement can be achieved by increasing the coupling capacitance. Once it is beyond a certain value, 10pF for the case of Wi-Fi energy harvesting at 2.45GHz using Avago HSMS2862 Schottky diodes, its effect on the voltage and power outputs of a voltage multiplier is diminishing. As such, it is important to identify the critical value and make sure the coupling capacitance is larger than that particular value.

It is worthy highlighting that identical coupling capacitance is assumed at all stages of pumping devices in the analysis and computer simulation. If different coupling capacitance values are used, it would be interesting to study how that affects the performance of a voltage multiplier. Furthermore, it would be valuable to include parasitic effects of printed circuit boards and other factors. These have been left out for our future studies in this area.

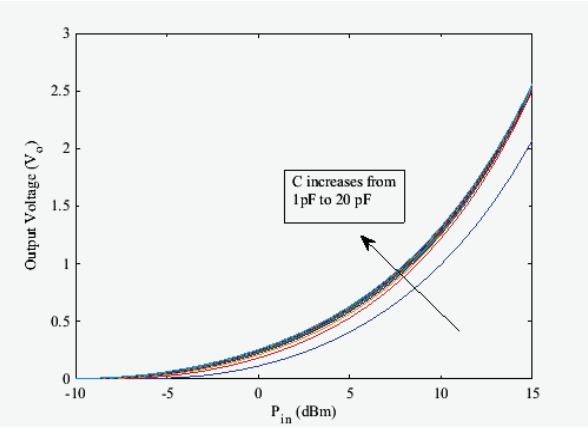

Fig. 5. Effect of Input Power and Coupling Capacitance on V_O

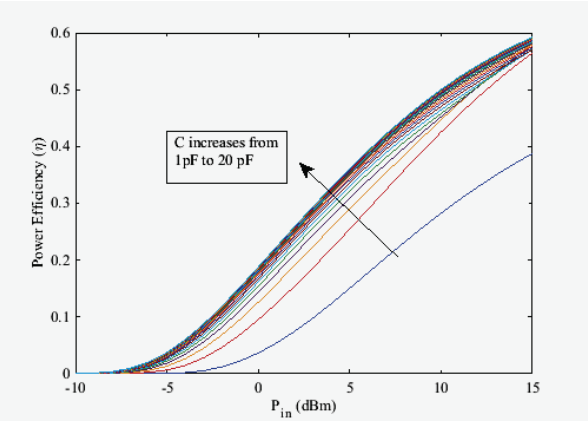

Fig. 6. Effect of Input Power and Coupling Capacitance on η

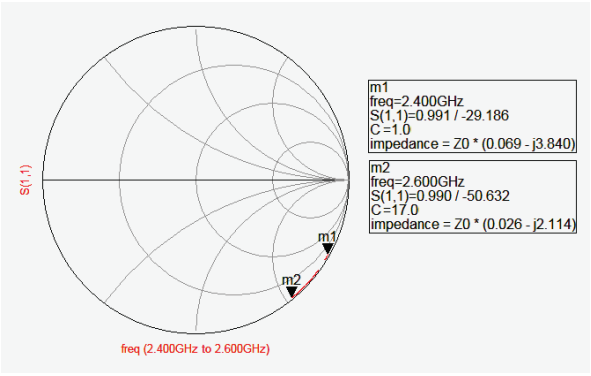

Fig. 7. Input Matching at Different Frequencies

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