CONTROL STRATEGIES AND STABILISATION TECHNIQUES FOR DC/DC CONVERTER

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By

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Dedication

This thesis is lovingly dedicated to my wife, **Grace Uwayo**, and our daughter, **Skylar Uwamungu Uhiriwe**. Your love, patience and constant encouragement have been my greatest source of strength throughout this journey. Every challenge became lighter because you were beside me, and every achievement became more meaningful because I could share it with you.

I also dedicate this work to my father and my mother. Your prayers, your sacrifices and your faith in me laid the foundation for everything I have achieved, and your encouragement still carries me every day. I am deeply grateful that you are here to share this moment with me.

To all of you, with my deepest love and gratitude.

Preface

This thesis presents the outcomes of my doctoral research conducted at Auckland University of Technology (AUT) in partial fulfilment of the requirements for the degree of Doctor of Philosophy. The research was undertaken within the School of Engineering, Computer and Mathematical Sciences as part of the Future Architecture of Networks (FAN) research programme. This research investigates advanced modelling, stabilization techniques, and robust control strategies for Dual Active Bridge (DAB) and Quad Active Bridge (QAB) converters operating in low-voltage DC microgrids.

The observer-based and learning-assisted control techniques are developed to enhance voltage regulation, disturbance rejection, transient performance, and system stability under challenging operating conditions. The contributions are supported by mathematical analysis, simulation, software-in-the-loop tests on the OPAL-RT OP5700 simulator, and open-loop tests of a laboratory DAB prototype.

Except where acknowledged, the work presented in this thesis is original and has not been submitted, either in whole or in part, for any other degree or qualification. It is hoped that the findings will contribute to the advancement of robust control strategies for future DC microgrids and renewable energy systems.

Abstract

This research investigates control strategies and stabilisation techniques for dual active bridge (DAB) and quad active bridge (QAB) converters in low-voltage DC (LVDC) microgrids supplying resistive loads, constant-power loads (CPLs) and pulsed-power loads (PPLs). These loads, the coupling between the ports of multiport converters and the nonlinear converter dynamics make fast and stable voltage regulation difficult. The thesis makes six contributions. First, a generalised harmonic model of the four-winding QAB transformer currents, including the dead time, agrees with a detailed switching simulation within 5.2% up to the 15th harmonic and supplies the coefficients of the control model; even harmonics appear only when the two half-cycles are unequal. Second, an adaptive super-twisting sliding mode controller (ASTSMC) with a nonlinear extended state observer and a feedforward decoupler is proposed for the QAB with CPLs, with a Lyapunov proof of practical finite-time stability and bounded adaptive gains. It settled a 48→60 V reference step in 1.14 ms, against 1.50 ms for an SMC with a nonlinear extended state observer and 6.00 ms for a decoupled PID, and gave the smallest dip after a load step (2.33%). Third, three known nonlinear controllers were customised for the QAB with PPLs; for a 100→200 W PPL step, the adaptive suboptimal second-order SMC limited the voltage change to 0.5/0.3 V, against up to 4.2 V for the others, at almost the same efficiency (90.72% against 90.78%). Fourth, for a resonant DAB with CPLs, a variable-gain SMC was derived that remains stable even when its base gain is below the worst disturbance, and it was combined with a physics-informed

neural network (PINN) that estimates the unknown disturbance current. The PINN estimate was correct on new runs (R^2 = 0.991), and after a 300→900 W CPL step the voltage drop fell from 6.2% without an estimator to 3.7%, close to an SMC with a linear extended state observer (3.1%) and better than a twisting second-order SMC. Fifth, a common test method applies the same tests, limits and tuning to all controllers of a chapter. Sixth, a laboratory DAB prototype with an OPAL-RT interface was built and tested in open loop. The controllers were evaluated in MATLAB/Simulink simulation and run on an OPAL-RT OP5700 simulator (software-in-the-loop); closed-loop tests on hardware remain future work.

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Attestation of Authorship

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for the qualification of any other degree or diploma of a university or other institution of higher learning.



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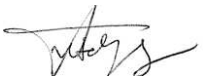
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4. A. Nduwamungu, R. Peykarporsan, T. T. Lie, I. Lestas, N. K. C. Nair, and R. Zamora, "Toward a Digital Twin Framework for Fault Detection and Zone Localisation in PV Microgrids Using a BiLSTM-Autoencoder," *IEEE Transactions on Industrial Informatics*, manuscript TII-26-10120. **Under review**.

Conference Papers

1. A. Nduwamungu, T. T. Lie, N. K. C. Nair, and I. Lestas, "Nonlinear Control-Oriented Modelling and Real-Time Simulation of a DAB Resonant Converter for Data Centre Applications," in *Proc. IEEE PES 17th Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Auckland, New Zealand, 2025, pp. 1–6, doi: 10.1109/APPEEC66370.2025.11382070. **Published**

2. A. Nduwamungu, T. T. Lie, I. Lestas, N.-K. C. Nair, and K. Gunawardane, "Decentralised Voltage Regulation and Accurate Current Sharing in a Parallel Buck Converters With Optimised Piecewise Linear Droop Control," in *Proc. 18th Int. Conf. on Probabilistic Methods Applied to Power Systems (PMAPS)*, Auckland, New Zealand, 2024, pp. 1–6, doi: 10.1109/PMAPS61648.2024.10667273. **Published**

3. A. Nduwamungu, T. T. Lie, I. Lestas, N.-K. C. Nair, and K. Gunawardane, "Analysis of Resistive and Constant Power Loads Effects on a Quad Active Bridge Converter for DC Grid Interconnections," in *Proc. IEEE Power & Energy Society General Meeting (PESGM)*, Austin, TX, USA, 2025, pp. 1–5, doi: 10.1109/PESGM52009.2025.11225318. **Published**.

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Nomenclature

Notation

Scalars are set in italic (v, L), vectors in bold lowercase ($\mathbf{x}$, $\mathbf{u}$) and matrices in bold uppercase ($\mathbf{A}$, $\mathbf{G}$). A dot denotes the time derivative, a hat an estimate ($\hat{\imath}$), a bar a value averaged over one switching period ($\bar{v}$) or a small-signal deviation, and an asterisk an operating point (v^*). Subscript i denotes the port number ($i = 1, \ldots, 4$); subscript ij denotes the link between ports i and j. Where a letter has a different meaning in one chapter, the chapter is given in brackets.

Abbreviations

ADRC	Active disturbance rejection control
ANN	Artificial neural network
ASSOSMC	Adaptive suboptimal second-order sliding mode control
ASTSMC	Adaptive super-twisting sliding mode control
CMPC–ISMC	Combined model predictive control with integral sliding mode control
CPL	Constant-power load
CPPRL	Constant-plus-proportional reaching law
CRRL	Constant-rate reaching law
DAB	Dual active bridge
DC MG	DC microgrid
DER	Distributed energy resource
DPS	Double phase shift
DSP	Digital signal processor
EMI	Electromagnetic interference
ESO	Extended state observer
EV	Electric vehicle
FFT	Fast Fourier transform
FHA	First (fundamental) harmonic approximation
FPGA	Field-programmable gate array
GHA	Generalised harmonic approximation
HFT	High-frequency transformer

HIL	Hardware-in-the-loop
IAE	Integral of the absolute error
IHOSMC	Integral higher-order sliding mode control
ISMC	Integral sliding mode control
LESO	Linear extended state observer
LMI	Linear matrix inequality
LVDC	Low-voltage direct current
MCU	Microcontroller unit
MIMO	Multiple-input multiple-output
MPC	Model predictive control
NLESO	Nonlinear extended state observer
PI / PID	Proportional–integral / proportional–integral–derivative
PINN	Physics-informed neural network
PINN–SMC	Variable-gain SMC with a PINN disturbance estimator
PPL	Pulsed-power load
PRRL	Power-rate reaching law
PWM	Pulse-width modulation
QAB	Quad active bridge
RES	Renewable energy source
RG	Research gap
RMS, RMSE	Root mean square; root-mean-square error
SIL	Software-in-the-loop
SMC	Sliding mode control
SMC–LESO	SMC with a linear extended state observer
SMC–NLESO	Sliding mode control with a nonlinear extended state observer
SPS	Single phase shift
SST	Solid-state transformer
STA	Super-twisting algorithm
STSMC	Super-twisting sliding mode control
THD	Total harmonic distortion
TPS	Triple phase shift
TSOSMC	Twisting second-order sliding mode control
VGSMC	Variable-gain sliding mode control
ZCS / ZVS	Zero-current / zero-voltage switching

Symbols: converters

Symbol	Description	Unit
V_i, v_{c_i}	DC voltage of port i; output-capacitor voltage of port i	V
V_{in}, V_0	Input and output voltage of the DAB (Ch. 5)	V

Symbol	Description	Unit
C_i, C_o	Output capacitance of port i; of the DAB (Ch. 5)	F
L_i	Leakage inductance of winding i (Y model)	H
L_{ij}	Link inductance between ports i and j (Δ model)	H
L_r, C_r, X	Resonant inductor and capacitor; net tank reactance (Ch. 4, 5)	H, F, Ω
n, n_{ij}	Transformer turns ratio; between ports i and j	–
f_{sw}, f_s	Switching frequency	Hz
T_c, T_s	Control (switching) period; sampling period	s
ω	Angular switching frequency, $2\pi f_{sw}$	rad/s
ϕ_i, φ_{ij}	Phase of bridge i; phase shift between bridges i and j	rad
d_{ij}	Phase-shift ratio, φ_{ij}/π	–
P_{ij}	Average power transferred from port i to port j	W
i_{L_i}, i_o	Average bridge current delivered to port i; to the DAB output (Ch. 5)	A
$i_{\mathrm{load},i}$	Load current of port i	A
$\bar{I}_i$, K	Current scale of port i (Ch. 3); largest DAB output current (Ch. 5)	A
P_{CPL}, P_i	Power of a constant-power load; of a pulsed-power load (Ch. 4)	W
R_{load}, R	Load resistance	Ω
$G_{\mathrm{inc},i}$	Incremental load conductance of port i	S
t_{dead}	Dead time	s
k	Harmonic order	–
M_k, c_k	Amplitude of harmonic k of a winding current: model; FFT	A
R_{eq}	Equivalent AC resistance of the rectifier and load (FHA)	Ω
η_{tot}	Total efficiency	%

Symbols: control and stability

Symbol	Description	Unit
$V_{i,\mathrm{ref}}$, V_{ref}	Voltage reference	V
e_i, e	Voltage tracking error	V
σ_i, S_i, s	Sliding variable (ASTSMC; SMC–NLESO; VGSMC)	V

Symbol	Description	Unit
A_i, B_{13}, B_{24}, D_i	Coefficients of the averaged port model (Ch. 3)	s^{-1}; $\mathrm{V\,s^{-1}\,rad^{-1}}$; F^{-1}
$\Phi_i(\cdot)$	Current-to-phase map of port i	rad
k_1, k_2	Proportional super-twisting gains of ports 3 and 4	$\mathrm{rad\,V}^{-1/2}$
k_3, k_4	Integral super-twisting gains of ports 3 and 4	rad/s
$\varrho_1, \ldots, \varrho_4$	Adaptation rates of the ASTSMC gains	–
ε_i, ϑ	Boundary-layer width	V
ν_i	Integral state of the super-twisting algorithm	rad
z_{1i}, z_{2i}	NLESO estimates of v_{c_i} and of the disturbance current	V, A
d_i	Total (lumped) disturbance current	A
Δ_i	Lumped uncertainty in the sliding dynamics	V/s
ε_0, γ_0, α, β	Base gains and growth rates of the VGSMC (Ch. 5)	V/s, s^{-1}, s^{-1}, $(\mathrm{V\,s})^{-1}$
ζ, λ_i	Integral gain of the sliding surface	s^{-1}
ω_o	Observer bandwidth	rad/s
$\mathbf{x}_i$, u_i	State vector and incremental phase-shift input of port i (MPC)	–, rad
$\mathbf{A}_i$, $\mathbf{B}_i$, $\mathbf{E}_i$	State, input and disturbance matrices (MPC, continuous time)	–
$\mathbf{A}_{id}$, $\mathbf{B}_{id}$, $\mathbf{E}_{id}$	The same matrices in discrete time	–
$\mathbf{Q}$, R, $\mathbf{\Pi}$	MPC state, input and terminal weights	–
$\mathbf{G}$, $\mathbf{H}$, $\mathbf{A}$	Coupling matrix, decoupler $\mathbf{H} = \mathbf{G}^{-1}$ (Ch. 4) and decoupler target $\mathbf{A}$ (Ch. 3)	–
$\mathcal{V}$, $\mathcal{W}$	Lyapunov functions	V^2, –
Z_{out}, T_m	Closed-loop output impedance; minor-loop gain (Ch. 5)	Ω, –
t_r, t_s	Rise (or fall) time; settling (recovery) time	s
OS, US	Overshoot; undershoot	%
J	Tuning score (Ch. 3)	mV s
Δu	Steady-state control activity	mdeg

Chapter 1

Introduction

1.1 Background and Motivation

Low-voltage direct current (LVDC) microgrids are a promising architecture for integrating distributed energy resources (DERs), particularly in systems that require high efficiency, flexibility and resilience [1]. As the share of renewable sources and energy storage grows, LVDC microgrids rely increasingly on high-frequency isolated bidirectional DC/DC converters to connect storage units, renewable generators and fast transient loads.

Among the available topologies, the Dual-Active-Bridge (DAB) converter and its multi-port extensions, such as the Quad-Active-Bridge (QAB) and Multiple-Input Multiple-Output (MIMO) configurations, have attracted significant research interest [2]. These converters provide galvanic isolation, bidirectional power transfer and soft switching over wide load and voltage ranges. Their modular design and multi-port power routing also make them attractive where compactness, scalability and high power density are required, such as data centres, electric vehicle (EV) charging, aerospace and naval power platforms, and resilient DC microgrids [3, 4].

Recent reviews have examined modulation and control strategies for DAB-based

converters, such as Single-Phase Shift (SPS), Double Phase Shift (DPS) and Triple Phase Shift (TPS). These studies report gains in efficiency, dynamic performance and control simplicity. Multi-port DAB variants have also extended these converters to the coordinated management of several sources and loads in LVDC networks.

Several challenges remain, however. The nonlinear behaviour of DAB and QAB converters, together with parameter variations, load disturbances and measurement uncertainty, can degrade control performance and reliability. Linear controllers often struggle to keep robustness and a fast transient response over a wide operating range. This motivates nonlinear and observer-based controllers, such as super-twisting sliding mode control (STSMC) with a disturbance observer. Tests on real-time simulators are also needed to show that such controllers can be executed in practice [5].

1.2 Significance and Challenges of DC/DC Converters

Tightly regulated downstream converters and point-of-load supplies in LVDC microgrids often behave as Constant-Power Loads (CPLs) within their control bandwidths. Such loads have a negative incremental impedance: when the bus voltage falls, they draw more current to keep their power constant. This can destabilise the source–load interaction and cause oscillations or voltage collapse if it is not mitigated [6, 7].

Many critical applications also contain Pulsed Power Loads (PPLs), such as radar transmitters, electromagnetic launchers, medical imaging systems and pulsed industrial actuators, which draw large bursts of current for short times. These bursts can cause deep bus-voltage dips and excite resonant modes of the distribution network. High-bandwidth control loops and fast energy buffers (e.g., supercapacitors or auxiliary converters) are therefore often used to decouple the PPL dynamics from the main DC bus [5].

Studies of microgrid and shipboard DC systems have shown that Model Predictive

Control (MPC) and other optimisation-based methods can coordinate the energy flow among sources, storage and dynamic loads. By predicting future states and adjusting the control action in real time, MPC can improve the stability margins and the energy use of systems with CPLs and PPLs. Impedance-based stability methods, including the Middlebrook criterion and impedance specification methods, assess stability through the ratio of the source output impedance to the load input impedance. Nyquist-based margins remain the main tool for checking source–load stability when DAB and QAB converters supply CPLs [5, 8].

Small-signal or linearised controllers often lack robustness under strongly nonlinear and time-varying conditions, especially when several active-bridge converters operate together with changing loads. CPLs worsen negative-impedance instability, while PPLs add fast disturbances that need a quick and adaptive response. Sliding Mode Control (SMC) and its higher-order variants, particularly STSMC, are attractive here because they are robust to parameter variations, unmodelled dynamics and external disturbances. Combined with observers, they can estimate states and disturbances that are not measured, which improves regulation.

Real-time simulation and hardware-in-the-loop (HIL) testing help to bridge the gap between control design and practical use, because they show whether a control algorithm can be executed under realistic conditions. This research therefore develops robust nonlinear controllers and observers for high-frequency isolated bidirectional DC/DC converters, compares them in simulation and checks them on a real-time simulator. The aim is to improve the stability, transient response and resilience of LVDC microgrids.

1.3 Problem Statement

This study investigates the control and stabilisation of DAB and QAB converters supplying resistive loads, CPLs and PPLs in LVDC microgrids. It examines how the

load type affects stability, bus-voltage dips and the transient response. It compares the adaptive super-twisting sliding mode control (ASTSMC), sliding mode control with a nonlinear extended state observer (SMC–NLESO), the adaptive suboptimal second-order sliding mode control (ASSOSMC), the integral higher-order sliding mode control (IHOSMC) and the combined model predictive control with integral sliding mode control (CMPC–ISMC), together with PID and PI controllers with decoupling, to find the best balance of robustness, performance and efficiency. It also assesses how the load type and the controller affect the total harmonic distortion (THD) and individual harmonics at the converter output. The controllers are run on the OPAL-RT OP5700 simulator (software-in-the-loop). Finally, for the resonant DAB converter, a physics-informed neural network (PINN) that estimates the unknown disturbance is combined with a variable-gain SMC and compared with (i) an SMC with a Linear Extended State Observer (SMC–LESO) and (ii) a Twisting Second-Order Sliding Mode Control (TSOSMC).

1.4 Research Objectives and Scope

This research addresses limitations in the control and stabilisation of DAB and QAB converters supplying resistive loads, CPLs and PPLs in LVDC microgrids. It combines averaged, harmonic and small-signal modelling with Lyapunov- and impedance-based stability analysis, and compares sliding-mode, predictive and learning-assisted controllers under common tests. The study is guided by the following objectives:

1. **Modelling and stability analysis:** develop averaged, harmonic and small-signal models of the QAB and DAB converters and assess the stability of the closed loops with Lyapunov and impedance (minor-loop) methods.

2. **Load impact assessment:** quantify how resistive loads, CPLs and PPLs affect

the bus-voltage dips, the recovery, the overshoot and the stability limits of the converters.

3. **Controller benchmarking:** compare known and new controllers under the same tests, limits and tuning effort: PID/PI with decoupling, SMC with an extended state observer (SMC–LESO and SMC–NLESO), the adaptive super-twisting SMC (ASTSMC), the adaptive suboptimal second-order SMC (ASSOSMC), the integral higher-order SMC (IHOSMC), the combined model predictive control with integral SMC (CMPC–ISMC), the twisting second-order SMC (TSOSMC) and the PINN–SMC.

4. **Learning-assisted control:** integrate a physics-informed neural network (PINN) that estimates the unknown disturbance with a sliding mode controller, and evaluate whether it improves disturbance rejection.

Types of test. The results of this thesis come from the four types of test defined below; the type behind each result is stated where the result is given and summarised in Table 6.1 of Chapter 6.

- *Simulation:* the controller and the converter model run in MATLAB/Simulink on a computer. Used in Chapters 3–5.
- *Software-in-the-loop (SIL):* the controller and the converter model run together on the OPAL-RT OP5700 simulator, in real time or slower. Used in Chapters 3–5.
- *Hardware-in-the-loop (HIL):* a real controller board controls a converter model that runs in real time. Not used in this thesis.
- *Hardware test:* a real converter. Used for the laboratory DAB prototype in open loop (Appendix A): the phase shift was sent from OPAL-RT, without feedback control.

Closed-loop tests of the controllers on hardware were outside the scope of this research because of time constraints.

1.5 Major Contributions of the Thesis

Table 1.1 lists the six contributions of the thesis, what each is based on, what is new in this thesis and the main evidence. Table 1.2 groups every method of the thesis into new work, improvements, adaptations of known methods, engineering work, and known methods used only for comparison.

Table 1.1: Contributions of the thesis.

	Contribution (Ch.)	**Based on (known)**	**New in this thesis**	**Main evidence**
C1	Harmonic model of the QAB transformer currents (3)	Generalised harmonic approximation; half-wave symmetry	Model of the four-winding QAB with dead time; even harmonics explained by unequal half-cycles; coefficients B_{13}, B_{24} for the controller	Odd harmonics within 5.2% of the switching simulation up to k = 15; even harmonics 0.018–0.023% (equal half-cycles), 0.30–0.97% (51 ns difference)
C2	ASTSMC for the QAB with CPLs (3)	Super-twisting algorithm; NLESO; decoupling	Adaptive gains that grow with the error; load-current estimate through the exact current-to-phase map; decoupler $\mathbf{G}^{-1}\mathbf{A}$; Lyapunov stability proof with bounded gains	Lowest tuning score (J = 77.6 against 130.9–525.9); settling 1.14 ms against 1.50–6.00 ms; load-step dip 2.33% against 2.61–4.06%; control signal moves four times less than with the SMC–NLESO
C3	Three nonlinear controllers customised for the QAB with PPLs (4)	Suboptimal second-order SMC; integral higher-order SMC; MPC with integral SMC	For the two coupled load ports: PPL as a disturbance term; one shared 2×2 decoupler; adaptive gain for the ASSOSMC; saturation instead of sign; gain bounds and a voltage guard for the IHOSMC	ASSOSMC: voltage change 0.5/0.3 V against 3.0/2.8 V (IHOSMC) and 3.5/4.2 V (CMPC–ISMC); efficiency 90.72% against 90.78% and 89.06%
C4	VGSMC and PINN disturbance estimator for the DAB with CPLs (5)	Variable-gain reaching laws; PINNs; disturbance estimation	(a) VGSMC: variable-gain reaching law with a boundary layer, derived step by step, stable even when the base gain is below the worst disturbance; (b) PINN that estimates the output disturbance, trained with data and the physics of the output node, with a filter, used inside the VGSMC	PINN estimate correct on new runs (R^2 = 0.991); dip after a CPL step 3.7% instead of 6.2% without an estimator; about as good as the SMC–LESO, better than the TSOSMC
C5	A fair test method (3–5)	Standard performance indices	Same tests, limits and tuning for all controllers of a chapter; indices defined and computed by script from saved data	Tables 3.2–3.6 and 5.3–5.10
C6	DAB prototype and OPAL-RT connection (App. A)	Standard H-bridge, gate-driver and sensor design	Test platform for a phase-shift-controlled DAB (engineering contribution)	Gate signals with dead time and power transfer measured at about 50 V

Table 1.2: Grouping of the methods of the thesis.

Group	Elements	Why
New work	C2: ASTSMC for the coupled QAB with CPLs	The adaptive gain rule, the load estimate through the exact current-to-phase map, its combination with the $\mathbf{G}^{-1}\mathbf{A}$ decoupler, and the stability proof are developed in this thesis.
	C4(b): PINN disturbance estimator inside the VGSMC	The estimator of the unknown output disturbance, trained with the physics of the output node, its filter and its use inside the SMC are developed in this thesis.
Improvement	C4(a): VGSMC reaching law	It builds on the known idea of reaching laws whose gains change with $\|s\|$; the law is derived step by step, its stability is proven, and it is applied to the resonant DAB.
Known methods, adapted	C1: harmonic model of the QAB	The harmonic method is known; its application to the four-winding QAB with dead time, the explanation of the even harmonics and the controller coefficients are adaptations.
	C3: ASSOSMC, IHOSMC and CMPC–ISMC	The three controllers are known; they are customised for the coupled ports 3 and 4 of the QAB with PPLs.
	C5: fair test method	The indices are standard; their common use for all controllers is the method contribution.
Engineering work	C6: DAB prototype and OPAL-RT connection	Standard power-electronics design that provides the test platform.
Known methods (comparison only)	PID with decoupling, SMC–NLESO (Ch. 3); PI with decoupling (Ch. 4); SMC–LESO, TSOSMC (Ch. 5)	Taken from the literature and tested under the same conditions; not claimed as contributions.

1.6 Thesis Structure

This thesis is organised into six chapters and one appendix.

- Chapter 1 introduces the research motivation, problem statement, objectives, types of test and the contributions of the thesis.

- Chapter 2 reviews the modelling and control techniques for DAB and QAB converters, including MPC, SMC and its variants, and combined strategies, and identifies the research gaps.
- Chapter 3 models the harmonics of the QAB converter and designs and compares controllers for its two load ports supplying CPLs, including the proposed ASTSMC (C1, C2).
- Chapter 4 compares three nonlinear controllers customised for the QAB converter supplying PPLs (C3).
- Chapter 5 derives the VGSMC and the PINN disturbance estimator for the resonant DAB converter and compares them with the SMC–LESO and the TSOSMC (C4).
- Chapter 6 summarises the key findings, the practical implementation considerations, the limitations and the directions for future research.
- Appendix A describes the laboratory DAB prototype and its connection to the OPAL-RT simulator (C6).

Chapter 2

Literature Review

This chapter reviews the background of the thesis. It covers DC/DC converter architectures with emphasis on DAB and QAB topologies, analyses how constant-power and pulsed-power loads affect stability and dynamics, and summarises classical and advanced control strategies together with stabilisation and disturbance-rejection methods. It ends with the research gaps that motivate the objectives and the tests of the following chapters.

2.1 Overview of DC/DC Converter Architectures

DC/DC converters play a key role in matching voltage levels, managing power and transferring energy efficiently within electronic systems. They allow different power sources to be combined, provide galvanic isolation and support compact, lightweight designs. They are essential in renewable energy systems, battery charging and power supplies tailored to specific applications. DC/DC converters can be classified as single-input single-output (SISO) [4], multiple-input multiple-output (MIMO) [5], single-input multiple-output (SIMO) [6] and multiple-input single-output (MISO) [7] converters, each with its own applications. Fig. 2.1 shows a microgrid (MG) composed of different

distributed energy resources (DERs), DC/DC and DC/AC converters and loads that are difficult to control with classical controllers. Many studies recommend hierarchical control to deal with the integration of DERs into MGs and the coordination of MGs in a cluster. DC/DC converter architectures include non-isolated PWM stages (buck,

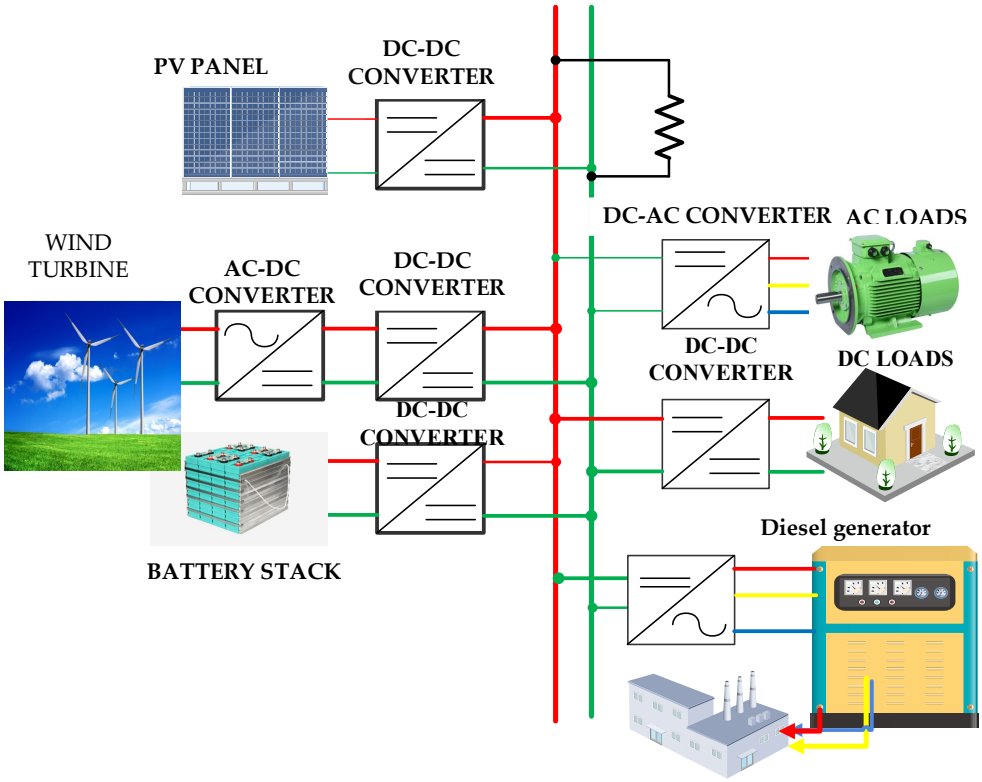


Figure 2.1: DC microgrid with DC/DC and DC/AC converters.

boost, buck-boost, SEPIC, Ćuk and Zeta, often interleaved for high current), switched-capacitor and hybrid converters for compact fixed-ratio conversion, and isolated PWM bridges (flyback, forward, push-pull, half-bridge and full-bridge) [8, 9]. They also include resonant converters, such as the LLC converter, with a series inductor L_r and capacitor C_r and the magnetising inductance L_m of the transformer, and the LCC converter, with one inductor, a series capacitor C_s and a parallel capacitor C_p. These reach high efficiency through soft switching. Current-fed and impedance-source variants are used where current limiting or a voltage boost is needed [10]. Within this family,

the DAB and QAB stand out because they combine isolation, bidirectional or multi-port power flow and simple phase-shift control of the power, which naturally supports wide soft-switching regions [11]. This gives high efficiency and power density and makes them good interconnection points in LVDC microgrids, where they can link storage, DERs and demanding loads without extra conversion stages. These properties allow modular, plug-and-play integration of several sources and buffers, tight bus-voltage regulation with low electromagnetic interference (EMI), and scalable energy routing between ports. They also raise research questions: managing the zero-voltage switching (ZVS) boundaries, coping with the negative incremental resistance of CPLs, and riding through fast PPLs, where advanced control adds clear value. In short, while the wider converter family covers many niches, the DAB and QAB offer the best combination of versatility, efficiency and system-level scalability [12]. The DAB and QAB are well suited to connecting DERs to the utility grid.

The choice of MG control topology depends on several factors, including the control layers, the communication topology and the type of load [13]. MG control schemes can be classified into four groups according to the type of controller, its location, its structure and the communication link: centralised, decentralised, distributed and hierarchical [14]. Hierarchical control uses several control levels, which makes the MG more flexible and efficient. It comprises primary, secondary and tertiary control, as shown in Fig. 2.2. Each task is performed at its own level, and the levels communicate to achieve the overall objectives. Challenges remain, however, particularly because DC MGs supply different loads, such as CPLs, resistive loads, mixed loads and PPLs, which strongly affect network stability [15].

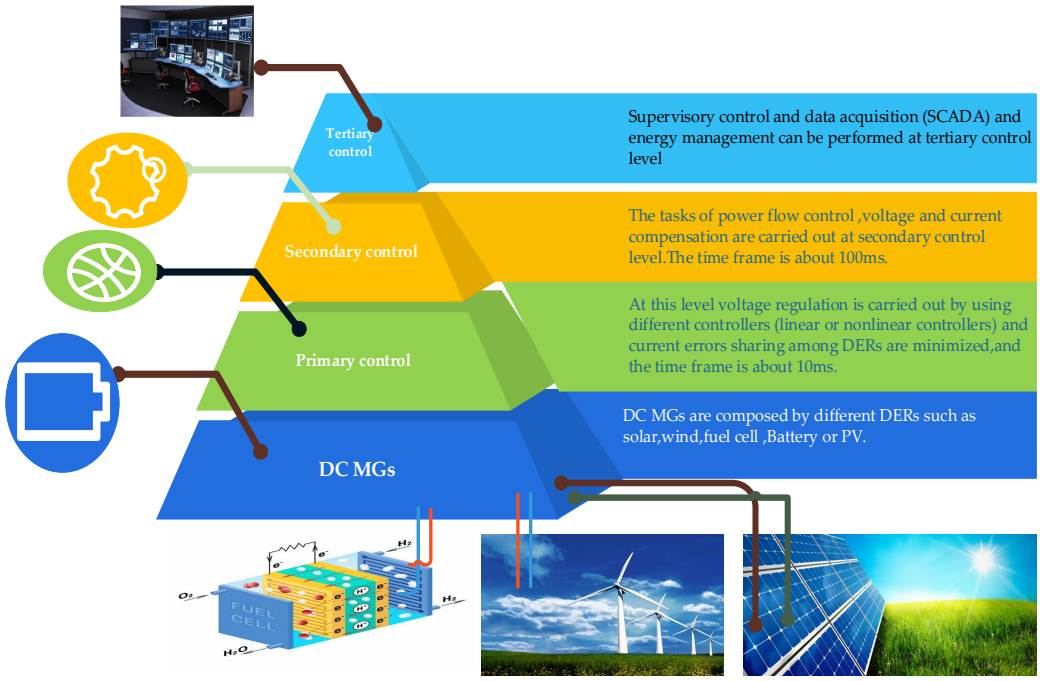


Figure 2.2: Hierarchical control of DC MGs.

2.1.1 DAB Converters and Resonant Topologies

Microgrids are small-scale power networks that supply energy to a specific group of users. They integrate distributed generation (DG) sources, such as microturbines, fuel cells, photovoltaic systems and wind turbines, with energy storage, demand management and supervisory control [16]. The DAB converter has a simple circuit structure with a single inductor and a high-frequency transformer (HFT). In high-power applications, however, a blocking capacitor is needed to prevent magnetic saturation, and its large capacitance increases the volume of the converter. Single phase shift (SPS) control is widely used but gives limited soft switching over a wide range of voltages and loads. Double phase shift (DPS), extended phase shift (EPS) and variable frequency (VF) control improve soft switching at the cost of a more complex controller [17].

In contrast, LLC and series resonant converters (SRC) can keep soft switching over a wider range of conditions by adjusting the switching frequency alone. Unlike the SRC, the LLC converter can also step the voltage up. During reverse power flow, however,

the LLC behaves like an SRC because of clamping effects. For bidirectional power flow, auxiliary inductors and capacitor-inductor-inductor-capacitor ($CLLC$) topologies have been proposed, although they increase the number of components [18]. Another challenge of LLC-based converters is synchronous rectification (SR), which is difficult to implement accurately in real time. Auxiliary circuits, such as current transformers and voltage detectors, or open-loop control are commonly used for this. Open-loop methods, however, restrict the operating range and cannot support boost mode under some conditions [19].

DAB converters can be divided into resonant and non-resonant types. Resonant DAB converters use a resonant circuit to achieve high-efficiency power conversion [20]. They often use frequency modulation and phase-shift control. Frequency modulation improves efficiency by adjusting the switching frequency through feedback; adaptive, segmented and continuous schemes have been proposed [21, 22]. Fig. 2.3 shows a grid-connected DAB with two inverters, an HFT and the utility grid. Non-resonant DAB

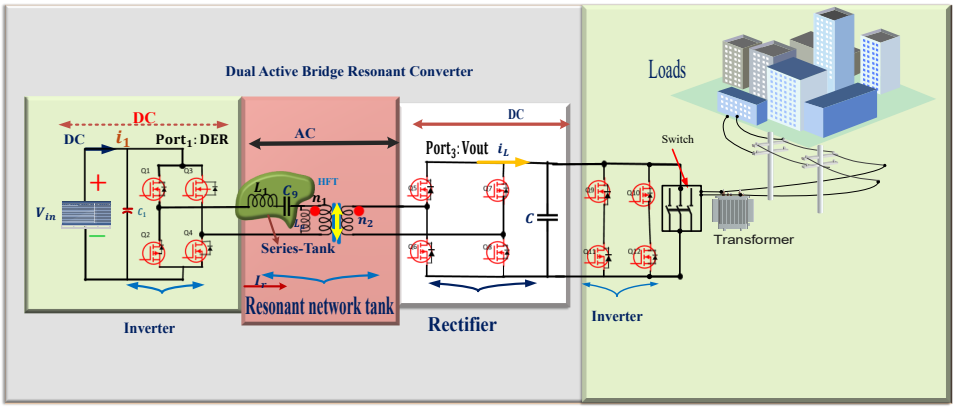


Figure 2.3: Grid-connected DAB converter interfacing PV.

converters do not depend on resonance tuning and give reliable performance, although resonant DABs can reach a higher efficiency under some conditions. Because of their simple structure and flexible frequency modulation, non-resonant DABs can operate over a wider frequency range [23]. DAB-based resonant converters (DAB-RCs), with a

series inductor and capacitor and a magnetising inductance (L_r, C_r, L_m), face stability and efficiency problems when they supply CPLs and resistive loads (R) in DC MGs (Fig. 2.4). These problems come mainly from the negative incremental impedance of CPLs, which causes nonlinear oscillations of voltage and current, reduces the damping of the system and degrades its performance [24, 25].

2.1.2 Time-Domain Modelling of DAB Converters

The DAB converter is one of the most widely studied isolated bidirectional topologies, and its modelling begins naturally in the time domain. Each active H-bridge generates a square-wave voltage, and the leakage inductance ensures energy transfer between ports. The power flow between ports of DAB is expressed by:

$$P = \frac{nV_1V_2}{\pi\omega L}\,\varphi\left(\pi - |\varphi|\right), \qquad -\frac{\pi}{2} \le \varphi \le \frac{\pi}{2} \tag{2.1}$$

where V_1 and V_2 are the bridge voltages referred to the same side of the HFT, n is the turns ratio, ω is the angular switching frequency, L is the inductance and φ is the phase shift. With the port capacitors and load resistances included, this gives a piecewise state-space model driven by binary switching functions. Such time-domain models are used to analyse the current waveforms and the zero-voltage and zero-current switching (ZVS/ZCS) boundaries, and to derive the averaged models used in control design [26].

2.1.3 Frequency-Domain Modelling of DAB Converters

Since both bridges produce square-wave voltages, which contain harmonics, frequency-domain analysis gives useful insight into the behaviour of the converter. The fundamental harmonic approximation (FHA) gives a compact power–phase relationship that shows the influence of the voltage levels, the leakage inductance and the switching frequency. The circulating current and the light-load efficiency, however, depend

strongly on the higher harmonics, which are captured by harmonic balance or harmonic state-space (HSS) models. These methods go beyond the FHA to quantify the RMS current and the distortion, and to study modulation schemes such as SPS, DPS and TPS [27].

2.1.4 Resonant DAB Converters

The resonant DAB (R-DAB) adds a resonant tank, usually a series inductor and capacitor (L_r–C_r), to the power path of the conventional DAB. This shapes the current into a sinusoid and widens the ZVS/ZCS region, which improves efficiency, especially at light and partial load. In the time domain, the resonant tank adds second-order dynamics:

$$L_r \frac{di_r}{dt} + v_c = v_1 - v_2, \quad C_r \frac{dv_c}{dt} = i_r \tag{2.2}$$

where i_r and v_c are the resonant current and the capacitor voltage. In the frequency domain, an impedance-based analysis gives a transfer function from the bridge voltages to the resonant current, which shows how the tank frequency and the quality factor affect the gain, soft switching and efficiency [28]. Applications of DAB converters include data-centre power supplies, fast bidirectional charging, PV-to-grid and energy storage interfaces, and PPL supplies. Fig. 2.4 shows a resonant DAB supplying a CPL, whose destabilising effect must be mitigated.

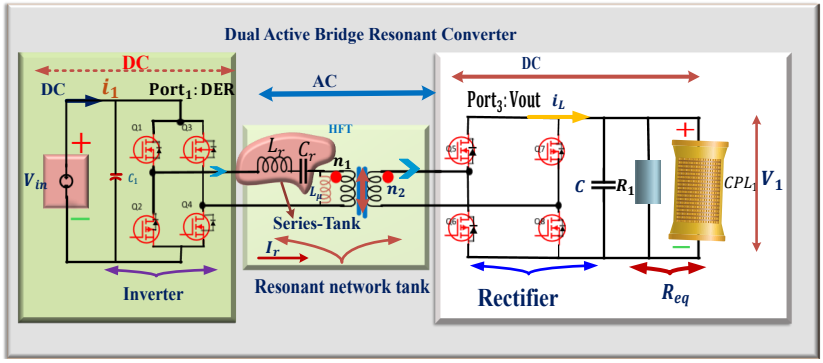


Figure 2.4: Resonant DAB converter supplying a CPL.

2.1.5 QAB Converters and Resonant Topologies

The QAB converter is a multi-port DC/DC converter designed to integrate different sources and loads in DC MGs, including renewable sources, energy storage (such as batteries, flywheels, thermal and chemical storage), CPLs, PPLs and mixed loads. It comprises four full bridges magnetically coupled through a high-frequency transformer, which provides galvanic isolation, phase-shift control of the power flow and bidirectional energy transfer. Zero-voltage and zero-current switching reduce its losses significantly [29], and it can remain stable under fluctuating renewable generation, variable demand and CPLs [30]. Fig. 4.1 shows a resonant QAB converter supplying PPLs: a four-port isolated DC/DC hub that routes bidirectional power through a multi-winding transformer and a resonant tank under phase-shift control. Fig. 3.1 shows the QAB supplying CPLs. The resonance reduces the circulating current and the device stress, which gives high efficiency and robust performance with CPLs and PPLs. The topology, its Y and Δ equivalent models and its power-flow equations are presented in detail in Section 3.2.

2.1.6 Time-Domain Modelling of QAB

The QAB extends the DAB principle to four ports: the square-wave voltages of several bridges act through the leakage paths (or an inductance matrix), which gives coupled equations of the form $L_{ij}\, di_{ij}/dt = v_i - v_j$ together with the port-capacitor dynamics. This state-space view is the basis for analysing the coupling between ports and the robustness to CPLs [31].

In the frequency domain, the operation of several bridges creates multiple interactions. Generalised FHA and harmonic balance or state-space methods predict the cross-coupled power flows and circulating currents and guide the design of decoupling controllers [32].

2.1.7 Resonant QAB Converters

Adding a resonant tank to each pair of ports (e.g., $L_{r,ij}$, $C_{r,ij}$) reduces the circulating current and widens the soft-switching range, and impedance-based or harmonic analyses map the cross-port power transfer and the efficiency regions of multi-source DC systems [33]. Since the DAB converter is a QAB converter with only two active ports, the DAB power-flow equations extend to the QAB [34]; the port-to-port power-flow and phase-shift expressions used in this thesis are derived in Section 3.2.

2.1.8 Impact of Constant Power Loads and Pulsed Power Loads

The load sets the electrical conditions of the converter and therefore affects its stability, its transient behaviour and its soft-switching (ZVS/ZCS) margins in DAB- and QAB-based LVDC systems [35]. In this thesis, the loads are grouped into three classes, resistive loads, CPLs and PPLs, because each has its own incremental impedance and disturbance profile. Resistive loads add damping and serve as a baseline. CPLs have a negative incremental resistance, which erodes the stability margins and deepens voltage dips. PPLs draw short, large bursts of power that can cause bus sags, excite resonances, raise the current stress and push the converter out of soft switching unless they are buffered or mitigated by the controller [36].

Impact of Constant Power Loads: DC MGs commonly use conventional converters such as buck, boost and non-inverting buck-boost converters. Some applications, however, need DC/DC converters with large step-up or step-down ratios, for which multi-level converters are essential. For control, the main challenge for DC/DC converters in DC MGs is the instability caused by CPLs [37]. CPLs are tightly regulated power-electronic loads whose I–V characteristic has a negative incremental impedance [38]. This negative incremental impedance reduces the stability margin of the interaction

between the feeder and the CPL and the damping of the system, and it often leads to instability.

As Fig. 2.5 shows, the incremental impedance of a CPL is always negative, even though its instantaneous impedance V/I is always positive. This can degrade the performance of the system and cause underdamped or unstable oscillations when a CPL is cascaded with a source converter: as the voltage falls, the current drawn by the load rises.

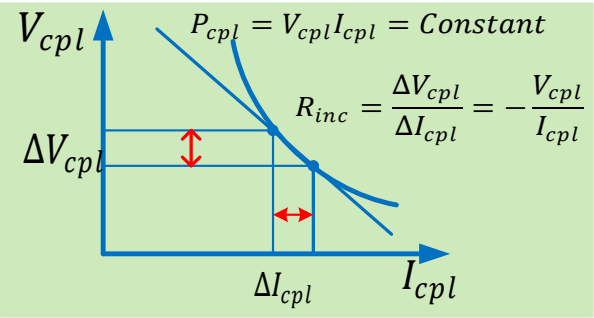


Figure 2.5: Negative incremental impedance.

Impact of Pulsed Power Loads (PPLs): PPLs are short, high-power events. MIL-STD-1399 defines them as lasting longer than one AC cycle and less than 10 s. They are usually modelled with rectangular or ramp shapes, and a power trajectory is used to describe the pulse energy. These features make them fundamentally different from small-signal disturbances and highly disruptive to DC networks [39]. In DC microgrids with DC/DC converter front ends, PPLs cause fast current steps that produce bus-voltage dips and spikes, excite network resonances and can remove the soft-switching margins. They are therefore treated as large-signal events, not small perturbations, in safety-critical platforms such as ships and aircraft [40].

The literature and the standards agree that, without fast buffering and high-bandwidth controllers, PPLs can force converters and resonant interfaces (e.g., DAB and QAB front ends) outside their intended operating region and degrade their efficiency and soft

switching. PPL-aware control combined with a hybrid energy storage system (HESS) stabilises the bus and keeps it within the naval and aviation power-quality limits [41]. Fig. 2.6 shows a shipboard DC microgrid that supplies continuous loads and pulsed power subsystems (PPLs, radar). The PPL branches are buffered by fast energy storage (supercapacitors within a HESS) and connected through DAB or QAB converters to keep the DC bus within the power-quality limits during pulses.

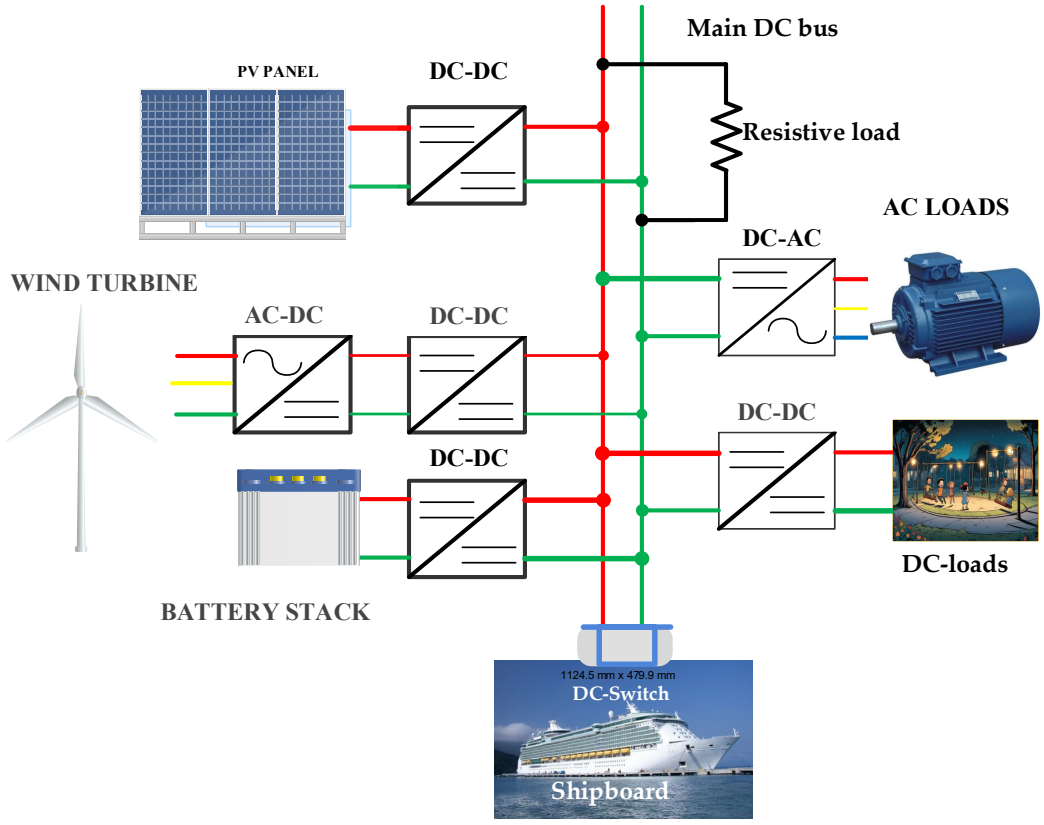


Figure 2.6: DC microgrid supplying PPLs.

2.1.9 Existing Control Strategies

Control strategies are essential for isolated DC/DC converters such as the DAB and QAB, where dynamic stability, efficiency and reliability are crucial. The literature usually divides them into classical and advanced methods [42]. Classical (linear)

methods, including proportional-integral (PI), proportional-integral-derivative (PID), proportional-derivative (PD), proportional-resonant (PR) and state-feedback controllers, are well established because of their simple structure and their ability to guarantee small-signal stability. They work well in steady conditions but are limited under large-signal disturbances, parameter uncertainty and the nonlinear behaviour of CPLs and PPLs [43].

To address these issues, nonlinear control strategies have been developed, including observer-based, adaptive, hybrid and artificial-intelligence-assisted controllers, MPC, and sliding-mode controllers such as ISMC, ASSOSMC, STSMC, TSOSMC, IHOSMC and MPC combined with ISMC [44]. In resonant DAB and QAB topologies, where keeping soft switching under varying loads is a major issue, these controllers are better suited to achieving large-signal stability, a fast transient response and resilience [45].

Classical Control Strategies: Classical control strategies remain the basis of converter control because they are simple, low-cost and proven. They are widely used in power-electronic systems to ensure small-signal stability and steady-state regulation, and they are the first choice in industry and the usual benchmark in research. The following paragraphs present the main classical strategies, PI, PID, PR, linear droop control (LDC), piecewise linear droop control (PWLDC), nonlinear droop control (NLDC), average current-mode control (ACMC) and voltage-mode control (VMC), with their principles, strengths and limitations for DAB and resonant converters. Each has specific strengths but notable limitations under large-signal disturbances or nonlinear loads.

Proportional Integral (PI) Control: PI control of DC/DC converters is reliable and widely used because it is easy to tune, easy to implement in digital controllers and regulates voltage and current well for small signals. Its limitations appear under large-signal disturbances and strongly nonlinear loads such as CPLs. Recent studies show

that PI is still the standard for converter control in DC microgrids [46]. PID control adds a derivative term to PI to increase damping and speed up the transient response. Because the derivative term can amplify measurement noise, derivative filtering or reduced-order designs are often used in high-frequency converters. Recent research covers these trade-offs and proposes PID variants that reduce noise and improve the dynamics [47]. Proportional-resonant (PR) control gives, in theory, an infinite gain at the target AC frequency and therefore zero steady-state error for sinusoidal signals, which is useful for harmonic compensation or for AC stages around resonant converters.

Recent work covers the digital implementation and tuning of PR controllers for modern power stages [48]. In linear droop control (LDC), used for the decentralised control of DC microgrids and parallel converters, the units share the load without communication because the output voltage of each converter drops linearly with its output current (fixed slope). LDC is simple and scalable but gives up tight bus-voltage regulation, so secondary control layers are often added [49]. Piecewise linear droop control (PWLDC) uses segmented V–I characteristics to balance the bus-voltage deviation and the load-sharing accuracy over different operating regions. Recent studies show its advantages for microgrids and nanogrids with many EVs and give guidance on choosing the segment set points; it is, however, still unable to control complex systems such as QAB, DAB and MIMO converters [50, 51]. Average current-mode control (ACMC) is a classical two-loop design with an outer voltage loop for regulation and an inner average inductor-current loop for fast current shaping. It improves current sharing and the dynamic response of parallel supplies; DAB-focused implementations and a recent monograph remain important references [52].

Voltage-mode control (VMC) is the simplest scheme: it uses only the output-voltage error to set the duty cycle or the phase shift. It is low-cost and easy to implement but usually gives slower current dynamics and weaker current sharing than current-mode control, so it is often combined with feedforward or an inner loop [53].

Transition to Advanced Control Strategies: In summary, classical strategies such as PI, PID, PR, droop-based methods, ACMC and VMC remain essential for converter regulation because they are simple and practical. Their effectiveness, however, is mainly limited to small signals and predictable operating conditions. Under large-signal disturbances, strong nonlinearities, CPLs or PPLs, their performance often deteriorates, leading to instability or a poor dynamic response.

These limitations call for advanced control strategies, which offer stronger robustness, adaptation and better performance under the demanding conditions typical of DAB, QAB and resonant converters. The next subsection therefore examines advanced approaches, starting with sliding mode control and extending to predictive, adaptive, observer-based, artificial intelligence (AI)-assisted and robust control.

2.1.10 Advanced Control Strategies

Classical strategies give reliable small-signal stability and steady-state regulation but often struggle with the nonlinear and time-varying conditions of DAB, QAB and resonant converters. CPLs and PPLs, wide load variations, parameter uncertainty and the need to keep soft switching over a wide range call for more advanced methods [42]. Advanced control strategies go beyond linear control by exploiting nonlinear dynamics, predictive optimisation, adaptation and learning. They offer better disturbance rejection, robustness to uncertainty and large-signal stability [54].

Classification of SMC and Higher-Order Sliding Mode Control: Sliding mode control (SMC) is widely used in DAB and resonant converters because it rejects matched disturbances, tolerates large parameter variations and copes well with CPLs [55]. The practical drawbacks of classical SMC are chattering and steady-state ripple, which have led to higher-order variants. Suboptimal second-order SMC (SSOSMC) lowers the switching activity [56]; super-twisting SMC (STSMC) gives a continuous control action

that keeps the robustness while nearly removing chattering [57]; twisting second-order SMC (TSOSMC) gives finite-time convergence under sign-changing uncertainties [58]; and integral higher-order SMC (IHOSMC) improves the steady-state accuracy [59].

Hybrid schemes such as model predictive control with integral sliding mode control (MPC with ISMC) add explicit constraint handling and prediction to the robustness of SMC, at the cost of a higher computational load. Recent DAB studies with super-twisting and second-order laws report higher efficiency, lower current stress and better transients than PI baselines, with more tuning effort and algorithmic complexity as the trade-off [60]. A further type is event-triggered SMC (ETSMC).

(a) Suboptimal Second-Order SMC (SSOSMC): The control input has two parts, $u = u_{\mathrm{eq}} + u_{\mathrm{sw}}$, where u_{eq} is the equivalent control and u_{sw} is the switching control. The switching part is the integral of a sign term, so it stays continuous:

$$u_{\mathrm{sw}}(t) = -k \int_0^t \operatorname{sgn}\left(\hat{S}(\tau)\right) d\tau \tag{2.3}$$

The equivalent part cancels the known dynamics and the disturbance estimated by an extended state observer (ESO):

$$u_{\mathrm{eq}} = \frac{1}{b_0}\left(-\alpha\lambda\hat{x}_2 \operatorname{sgn}(x_1)\,|x_1|^{\lambda-1} - \alpha_2 e - \hat{F}\right) \tag{2.4}$$

Here, $\hat{S}$ is the estimated sliding variable, $k > 0$ is the switching gain, b_0 is the nominal input gain, $\hat{F}$ is the ESO estimate of the lumped disturbance, e is the tracking error, $\hat{x}_2$ is the observer state, and α, α_2 and λ are controller parameters.

The integral switching keeps the plant input continuous while preserving second-order sliding robustness, and the ESO provides active disturbance rejection. The controller and observer parameters are, however, coupled: the gains and the ESO bandwidth must be coordinated with the chosen sliding function and model terms, and poor coordination can weaken the disturbance cancellation. Tuning the ESO and controller gains together improves the robustness and effectiveness of this controller [61].

In second-order SMC with the sliding variable $S = c_1 x_1 + x_2$, the control acts through its rate $\dot{u}$, which appears in the second derivative of S:

$$\ddot{S} = h(x_1, x_2, u, t) + \beta_3 \dot{u} \tag{2.5}$$

where x_1 and x_2 are the states, $c_1 > 0$ is the surface gain, $h(\cdot)$ collects the lumped dynamics and β_3 is the input gain. Because the controller sets $\dot{u}$, the actual input u stays continuous. One study added the integral of x_1 to the sliding variable:

$$S = c_1 x_1 + x_2 + c_2 \int_0^t x_1(\tau)\, d\tau \tag{2.6}$$

where $c_2 > 0$ is the integral gain. The integral term removes the steady-state error of x_1 and improves the output voltage of buck converters. The gains c_1 and c_2 are updated online by a zero-crossing logic. The performance relies on reliable zero-crossing detection, and $\dot{S}$ and $\dot{u}$ are sensitive to noise without proper filtering; this is the main limitation [62]. A better tuning method is needed to overcome it.

Another study implemented the super-twisting algorithm on a six-degree-of-freedom articulated intervention autonomous underwater vehicle (AUV) and compared adaptive-gain super-twisting with generalised super-twisting, with and without a higher-order sliding observer when the velocities are not measured. The method gives a continuous actuator command while enforcing second-order sliding. Its limitations are non-trivial gain tuning and dependence on the specific AUV and operating conditions. A prescriptive gain-selection procedure, a clear analysis of the observer bandwidth–noise trade-off and wider comparisons under identical constraints would improve its portability [63].

(b) Super-Twisting SMC (STSMC): An adaptive super-twisting controller built on a global integral terminal sliding surface has been designed for finite-time tracking under uncertainties and actuator faults: the adaptive mechanism handles the nonlinear uncertainty, and the super-twisting structure keeps the input continuous (low chattering). Its advantages are finite-time convergence, robustness to uncertainty and faults, and less

chattering. Its limitations are that the evidence comes only from simulations and that the design adds tuning effort (integral terminal surface with adaptive gains) [64].

An adaptive-gain generalised super-twisting SMC has been used in both the speed and current loops of a permanent magnet synchronous machine (PMSM) drive, with a filtered high-gain observer that estimates the lumped disturbances and reduces noise. It improves robustness and transients with less chattering and outperforms fixed-gain designs.

Its limitations are that the high-gain observer introduces a bandwidth–noise trade-off and needs careful parameter selection, and that its use depends on modelling and relative-degree assumptions. Clear coordinated tuning rules (observer bandwidth against adaptive-gain rates) and saturation and constraint handling in the adaptive law for inverter-limited operation would improve it [65]. A generalised super-twisting controller can be constructed through a nonlinear change of coordinates and a time scaling: stability is ensured in the transformed system and then mapped back to the original variables, which yields finite-time convergence for a broader class of perturbations than the standard super-twisting algorithm (STA).

The standard STA drives a sliding variable σ and its derivative to zero in finite time with the continuous control law [54]:

$$u = -k_1|\sigma|^{1/2}\,\mathrm{sign}(\sigma) + v, \qquad \dot{v} = -k_2\,\mathrm{sign}(\sigma), \qquad k_1, k_2 > 0, \tag{2.7}$$

where u is the control input, σ is the sliding variable, v is the integral state, and k_1 and k_2 are the gains. In the generalised controller, the constant gains k_1 and k_2 are replaced by state-dependent gains built from the plant coefficient and the perturbation bounds. This structure is largely theoretical: the added design complexity and the state-dependent gains can hinder direct implementation, and these are its main limitations. Practical tuning rules for the main gains based on disturbance estimation would ease gain selection and handle time-varying uncertainty in applications [66].

(c) Twisting Second-Order SMC (TSOSMC): A continuous version of the twisting second-order sliding controller preserves finite-time convergence while eliminating chattering, retaining fast and robust dynamics, and offering a simple step-by-step gain-selection procedure. It assumes, however, that the disturbances vary in a predictable (Lipschitz) manner, and it relies on linear matrix inequality tools for gain synthesis, which adds setup complexity before hardware deployment [59].

Adapting the twisting action by monitoring the zero crossings of the sliding variable, and minimising the control effort required at each crossing, reduces chattering without sacrificing response speed. Hardware tests on an electronic throttle show a lower steady-state error and faster settling than conventional twisting and comparable variants, although validation on a single actuator leaves robustness across different plants and noise levels unproven [67]. When a single second-order sliding-mode controller regulates the DC-bus, DC–DC, and DC–AC stages, simulations show good regulation under load and frequency disturbances, and the use of one controller simplifies system-level design. The performance is, however, sensitive to gain selection: too small a gain yields a slow response, whereas too large a gain causes overshoot. Because the evidence is mainly simulation-based, tuning guidelines and experimental (hardware) validation are still required [68].

(d) Integral Higher-Order SMC (IHOSMC): An integral higher-order sliding-mode framework provides finite-time robustness and removes the reaching phase by starting the system on the sliding surface, i.e., $S(0) = 0$. Its guarantees, however, rely on strict smoothness assumptions and on accurate derivative estimates, which sensor noise can corrupt. For orders $r > 2$, the implementation effort and the tuning risk on embedded platforms increase further. Successful deployment therefore requires noise-tolerant differentiation, careful management of the computational load, and explicit handling of actuator limits with anti-windup [69].

Integral super-twisting control preserves finite-time behaviour with smoother actuation and is designed to remove the reaching phase under persistent disturbances. The supporting evidence is, however, application-specific: model errors, disturbance spectra, and sampling effects are hardly examined, although they usually reveal residual reaching-like transients when the initial condition is not set correctly. The reported gains in energy use and responsiveness are notable, but the sensitivity to gain selection and to practical constraints has not been fully characterised; wider parameter sweeps, Monte Carlo disturbance tests, and cross-platform validation with clear tuning guidelines would be needed to support stronger claims [70].

An adaptive integral HOSMC achieves smooth control without requiring strict bounds on the uncertainty. The design nevertheless assumes matched uncertainties and a correct initialisation of the integral surface; if the initial condition is wrong, a short reaching phase can still occur, which weakens the claim of robustness from $t = 0$. The method also remains sensitive to derivative estimation and to actuator saturation in the combined control channel. A convincing hardware implementation would require anti-windup, noise-aware differentiation, and a documented gain-tuning procedure supported by statistics across operating points [71].

(e) Model Predictive Control with Integral Sliding Mode Control (MPC with ISMC): An observer-free controller combines integral sliding mode, which acts from $t = 0$, with robust model predictive control (MPC) to enforce constraints and improve performance in discrete time. The integral surface is designed by an optimal projection that also attenuates part of the unmatched disturbances, and input-to-state practical stability is established through simulations and a laboratory demonstration. The method is, however, restricted to linear discrete-time plants, its experimental range is limited, and little guidance is given on how to balance the sliding gains against the MPC weights [72].

In a tube-MPC with integral SMC architecture, the MPC optimises a nominal trajectory while the integral sliding mode keeps the real plant inside a robust tube around it, and iterative invariant-set computations guarantee that the constraints are met. Closed-loop stability is proved, and examples show that the scheme applies to nonlinear time-delay plants. Its main limitation is that validation is mostly simulation-based: the tube and boundary-layer parameters must be sized manually from the disturbance bounds, and little guidance is given for handling tight current and voltage limits and saturation in both layers [73].

A model-free, distributed integral-sliding predictive controller for multi-agent systems with communication delays combines an MPC-style prediction mechanism, an integral sliding action, and active delay compensation. Simulations and a multi-motor experiment show a lower tracking error and better robustness to delays. However, the method was developed for an application domain other than power converters, depends on the quality of the delay compensation and on data-driven gain selection, and does not consider converter-specific limits or processor timing budgets [74].

(f) Event-Triggered SMC (ETSMC): An event-triggered super-twisting design based on input-to-state stability guarantees a positive minimum time between events, which prevents infinitely many triggering events in a finite time; it reduces the computational load, relieves chattering, and is verified in hardware-in-the-loop (HIL) tests. Its limitations are that it addresses only the super-twisting algorithm with simulation and HIL evidence, that parameter selection still requires expert tuning, and that the plant classes considered are limited. It could be improved by noise-aware co-tuning rules for the gains and trigger thresholds, by including actuator limits, and by reporting tests on real hardware with fast dynamics [75].

Another study proposed an event-triggered fault-tolerant SMC for networked systems with delay, packet loss and actuator faults. It used an H_∞ synthesis and showed

considerable savings in transmissions in a gas turbine case study. Its limitations are the simulation-only validation, no explicit guarantee of the minimum inter-event time (MIET), and assumptions on the delay bounds and fault models that may be too restrictive for fast hardware. It could be improved by MIET guarantees, hardware trials with measured delays and co-design rules for the trigger thresholds and SMC gains [76].

A review of recent advances in event-triggered control (ETC) identifies current best practices and open problems for ETSMC. Because it evaluates ETC in general, it gives high-level guidelines rather than ready-to-use ETSMC rules. Its co-design and data-driven concepts could be applied directly to ETSMC, for example by learning trigger thresholds with stability certificates and including packet-loss models in ETSMC proofs and tests [77].

Types of Reaching Laws in Sliding Mode Control: The reaching law determines how the system state approaches the sliding surface during the reaching phase, and therefore the mathematical form of the controller depends on this choice. This section compares the main families of reaching laws to support their practical design and modification. The comparison considers convergence speed, chattering suppression, robustness to uncertainty, and implementation complexity, and outlines the strengths and limitations of each family [78].

(a) Constant Plus Proportional Reaching Law (CPPRL)

The constant plus proportional reaching law (CPPRL) is:

$$\dot{S} = -kS - \varepsilon\,\mathrm{sgn}(S), \qquad k > 0,\ \varepsilon > 0 \tag{2.8}$$

The proportional term $-kS$ drives the state to the sliding surface faster when $|S|$ is large. A large gain, however, increases chattering, while a small gain increases the reaching time and reduces chattering. To manage this trade-off, the initial parameters should be chosen carefully and a small boundary layer or adaptive gains added [79].

(b) Adaptive Switching Power Reaching Law (ASPRL)

One study proposed a new reaching law to overcome the limitations of the CPPRL:

$$\begin{cases} \dot{S} = \hat{u} - \lambda_1 |x|^{\alpha} \operatorname{sgn}(S), \\ \alpha = \int \lambda_1 |S| \, dt - \int \lambda_2 S \, dt \end{cases} \tag{2.9}$$

where $\hat{u}$ is the nominal reaching law, obtained by setting the derivative of the sliding surface to zero; λ_1 and λ_2 are positive design constants of the integral terms; α is the adaptive exponent; and $S(t)$ is the sliding surface. Compared with the traditional law, it gave faster convergence and less chattering [80].

(c) Power Rate Reaching Law (PRRL)

When the state is far from the sliding surface, this reaching law closes the gap quickly; as the trajectory approaches the surface, the law softens the approach and lowers the correction effort [81]. This fast-far, gentle-near behaviour gives fast overall convergence with little chattering, which reduces actuator stress and prevents high-frequency oscillation around the surface:

$$\dot{S}_i = -k_i |S_i|^{\alpha} \operatorname{sgn}(S_i), \qquad 0 < \alpha < 1, \; i = 1, \; k_i > 0 \tag{2.10}$$

where S_i is the sliding variable, k_i is the gain (larger k_i gives a stronger attraction to the surface), α is the power exponent that shapes the convergence rate, and $\operatorname{sgn}(\cdot)$ is the switching (discontinuous) part [82].

(d) Inverse Hyperbolic Sine Reaching Law (IHSRL)

The inverse hyperbolic sine reaching law updates the sliding variable as:

$$\sigma(k+1) = \sigma(k) - \frac{1}{\gamma} \operatorname{arcsinh}\big(\gamma \sigma(k)\big) - \beta \operatorname{sgn}\big(\sigma(k)\big) \tag{2.11}$$

where $\sigma(k)$ denotes the sliding variable at sample k, $\sigma(k+1)$ is the sliding variable one step ahead under the proposed reaching law, $\gamma > 0$ is the tuning parameter that scales the argument and gain of the inverse hyperbolic sine, $\beta > 0$ is the discontinuous (sign) gain that speeds up reaching and adds robustness, $\operatorname{arcsinh}(\cdot)$ is the inverse hyperbolic

sine, and $x(k) \in \mathbb{R}^n$ is the state vector at sample k. This reaching law achieves a smaller boundary layer and lower control effort than traditional reaching laws, with simple and explicit adjustment via β and γ, and smoother behaviour at the surface. Its limitations include residual switching from the $\mathrm{sgn}(\cdot)$ term and dependence on a disturbance bound.

To reduce these effects, a smooth boundary layer (e.g., sat or $\tanh$) can replace $\mathrm{sgn}(\cdot)$, a disturbance or load observer can be added to allow a smaller β, and γ can be scheduled to be larger far from the surface and smaller near it [83].

(e) Constant Rate Reaching Law (CRRL): The constant rate reaching law is [81]:

$$\dot{S} = -Q\ \mathrm{sgn}(S), \qquad Q = \mathrm{diag}(q_i),\ q_i > 0, \tag{2.12}$$

which drives each sliding variable to zero at the constant speed $|\dot{S}_i| = q_i$ and reaches the surface in the finite time $t_{r,i} = |S_i(0)|/q_i$. Its drawbacks are chattering caused by the discontinuous sign term (worse for large q_i), a slow approach for small q_i, a reaching speed that does not depend on the distance from the surface, and sensitivity to noise and sampling [81]. These issues can be mitigated by replacing $\mathrm{sgn}(S)$ with a boundary-layer saturation, $\dot{S} = -Q\ \mathrm{sat}(S/\vartheta)$, by adaptive gains $q_i(S)$, by smooth laws such as $\dot{S} = -\alpha \tanh(S/\vartheta)$ or $\dot{S} = -(\alpha/\gamma)\,\mathrm{arcsinh}(\gamma S)$, by higher-order sliding modes, and by careful tuning of the discrete-time implementation [84, 85].

Model Predictive Control (MPC): MPC predicts the evolution of the converter and optimises the control action subject to constraints. This is attractive for DAB and QAB converters, where the ZVS, current and voltage limits matter and the coupling between variables is strong. Finite-control-set MPC chooses the switching states directly for fast dynamics; continuous-control-set MPC gives smoother duty-cycle or phase commands; nonlinear MPC (NMPC) improves accuracy by using nonlinear models; and hybrid schemes (e.g., MPC with an observer or MPC with ISMC) combine prediction with disturbance rejection or robust sliding surfaces. Recent DAB studies

consistently show better voltage regulation and soft switching over wide ranges. The drawbacks are sensitivity to model mismatch, the effort of tuning the cost function and the computational burden on high-frequency hardware [86].

Backstepping Control (BSC): Backstepping designs stabilising control laws recursively with a Lyapunov function, which gives large-signal stability guarantees for nonlinear converter models [87]. Variants include adaptive backstepping (online parameter adaptation) and observer-based backstepping (state and disturbance estimation). In DAB applications, backstepping has shown stronger robustness and faster transients than PI and passivity-based controllers, particularly for power reversals and input-voltage steps. Its main limitations are the need for a detailed and accurate model and a design complexity that grows with the order of the system [88].

Passivity-Based Control (PBC): PBC shapes the stored energy to enforce passivity, which is valuable when DABs feed CPLs with a negative incremental impedance or interact with resonant tanks [89, 90]. Recent DAB work shows that PBC can stabilise bidirectional power flow with CPLs and improve the large-signal behaviour in hardware. Its effectiveness comes from rigorous energy shaping and damping injection; its drawbacks are a heavy modelling effort, sensitivity to unmodelled parasitics and sometimes conservative performance if the shaped energy is not well chosen [91].

Synergetic Control (SC): SC defines macro-variables that drive the system to a manifold with smooth, finite-time convergence, and it often reaches a robustness comparable to SMC without chattering. It has been validated on power-converter test beds (buck and boost converters and inverters) and has begun to appear in wide-range EV chargers that include DAB modules [92]. Its strengths are robust, chattering-free dynamics and a Lyapunov-based design; its limitations are the non-trivial synthesis of

the macro-variables, few standard tuning procedures and few DAB-specific application guides [93].

H_∞ Robust Control: H_∞ control minimises the worst-case gain from disturbance to output and gives formal robustness guarantees against plant uncertainty and external disturbances; loop-shaping variants combine classical frequency-domain intuition with modern robustness [94]. In DAB and DC microgrid applications, H_∞ control has been proposed to keep the performance over wide operating ranges and uncertain parameters. It is strong in theory and increasingly practical with linear matrix inequality (LMI) and Riccati-equation solvers; its main drawbacks are the modelling depth, the design complexity and the cost of implementation on embedded targets [95].

Artificial Intelligence and Machine-Learning-Based Control: Hybrid controllers combine complementary strengths, such as SMC with an artificial neural network (robustness with learning-based adaptation), MPC with an observer (constraint handling with disturbance estimation), and SMC with a double-integral super-twisting law (finite-time accuracy with reduced chattering). These schemes improve disturbance rejection, current stress, and efficiency over wide operating ranges in grid-connected DAB and QAB converters and prototypes, at the cost of higher integration and tuning complexity and heavier computation [96, 97]. Physics-informed neural networks (PINNs) can also be combined with advanced controllers to improve their robustness and effectiveness [98].

2.1.11 Existing Stabilisation Techniques and Disturbance Rejection Methods

Nonlinear dynamics, parameter variations, the negative-impedance effect of constant power loads (CPLs) and the power imbalance caused by pulsed power loads (PPLs) can

all make DC/DC converters unstable. Such conditions often cause oscillations, a poor transient response and voltage collapse. Stabilisation techniques are therefore needed to ensure reliable operation, fast dynamics and tight voltage regulation [99].

These techniques fall into three categories: (i) disturbance rejection methods, such as the linear and nonlinear extended state observers (LESO and NLESO), which estimate and cancel disturbances; (ii) passivity and energy-based methods, such as Brayton–Moser theory, passivity-based control and active damping, which reshape the system energy and inject damping; and (iii) impedance-shaping methods, such as virtual resistance, virtual inductance and passive damping, which improve the source–load impedance interaction [95]. Each category addresses converter instability from a different angle.

Passivity and Energy-Based Methods: Passivity-based control (PBC) stabilises DC/DC converters by reshaping their energy function and enforcing power dissipation. When the closed loop satisfies the passivity condition, PBC guarantees asymptotic stability even with nonlinear dynamics and destabilising CPLs and PPLs. Brayton–Moser mixed potential theory, energy shaping and damping injection (active or passive) are widely used to restore passivity and suppress oscillations.

(a) Passivity-Based Control

PBC is mainly a stabilisation technique: it reshapes the energy of the system and injects damping so that the converter is passive and inherently stable, even with destabilising loads such as CPLs and PPLs. It also rejects disturbances indirectly, because a passive system dissipates external disturbances instead of amplifying them, which improves robustness without estimating them [95].

(b) Brayton–Moser Mixed Potential Theory

The voltage stability of DC MGs will play a key role in future hybrid AC/DC distribution networks and is essential for their safety [95]. The large-disturbance

stability of DC MGs with resistors, inductors, capacitors and CPLs can be studied with Brayton–Moser mixed potential theory. Brayton and Moser established three theorems for analysing the stability of systems with nonlinear elements under large disturbances [100].

(c) Active Damping Technique

Active damping reproduces the effect of parallel passive components by changing the control of the active components of the system. Because the damping is written in software, it is more flexible than passive components. If the feeder consists only of passive components, the control of the load converter may have to be modified to implement active damping, or an auxiliary circuit can be added in parallel with the load to damp the system [101].

Impedance Shaping Methods: (a) Passive Damping Technique

Passive damping is a common way of addressing the negative incremental impedance of CPLs and the power imbalance sometimes caused by PPLs: the input filter is modified to increase its damping. This is done by adjusting the filter elements or adding resistors, capacitors or inductors in parallel, in series or in cascade with the filter inductor or capacitor. Added passive components, however, increase the cost, weight, volume and losses of the system. Ideally, the input filter should be designed from the start with enough damping and low losses [102].

(b) Virtual Impedance

Virtual impedance is a control technique that emulates an impedance (usually a resistance or an inductance) in software to improve converter stability [103]. A current-dependent term in the control loop increases the effective output impedance of the converter, compensates for the negative impedance of CPLs and suppresses oscillations during load transients without a physical, lossy component. It can consist of a virtual resistance, a virtual inductance and sometimes a virtual capacitance [104].

Disturbance Rejection Methods: In practice, DAB and QAB converters operate with bus-voltage sag and ripple, parameter variations (e.g., leakage inductance and effective dead time), measurement noise, and digital control delays. In addition, CPLs introduce a negative incremental resistance that can degrade the stability margins [105, 106], while pulsed-power loads cause rapid power steps that excite resonances, threaten ZVS, and raise device current stress [107]. With resistive loads the problem is milder, but input ripple and parameter drift remain. The controller sees all these influences as disturbances that must be rejected quickly while respecting regulation, current-stress, efficiency, and ZVS limits. Active disturbance rejection control (ADRC) combines three blocks: a tracking differentiator (TD) that smooths the reference and provides a clean reference derivative, avoiding overshoot and noise amplification; an extended state observer (ESO) that estimates the plant states and a lumped total disturbance online; and a state-error feedback law, either nonlinear (NLSEF) or linear, that uses the ESO outputs to cancel the estimated disturbance and reduce the plant to a chain of integrators [87].

Linear Extended State Observer (LESO): An LESO adds the lumped disturbance as an extra state of the plant model and estimates it, together with the states, through linear error injection tuned by a single bandwidth. This simplifies the tuning of linear ADRC (LADRC) and has been shown to improve the dynamic response and output impedance of DABs compared with PI control. Its advantages are a compact structure, one-parameter bandwidth tuning, and robustness to parameter spread [108]. Recent series-correction LESOs track ramp and sinusoidal disturbances faster and remove the steady-state error of a plain LESO while keeping the same bandwidth. The main drawbacks of a standard LESO are that a higher bandwidth, needed for fast disturbances, amplifies sensor noise in the estimate, and that it tracks step disturbances exactly but leaves a steady-state error for ramps and sinusoids [109].

Nonlinear Extended State Observer (NLESO): An NLESO estimates the disturbance for feedforward cancellation using nonlinear error injection, such as Han's fal function or sliding-mode terms. In power converters, it is often combined with sliding-mode control for robust and fast rejection of model mismatch and load steps [110]. Its advantages are potentially faster convergence, high robustness to uncertainty, and more accurate estimates of fast disturbances, as reported in converter and inverter applications. Its drawbacks are more complex tuning, possible chattering that must be smoothed, and sensitivity to mismatched disturbances if the observer is not properly designed [111].

2.1.12 Research Gaps (RG)

Control strategies and stabilisation techniques for DAB and QAB converters in LVDC MGs have been studied extensively. With practical CPLs and PPLs, however, these systems are dominated by interactions, and their stability and performance depend strongly on the network impedances and the digital implementation. The review above reveals the following research gaps.

RG-1 Impedance-based stability assessment under CPL and PPL with realistic non-idealities: Existing studies usually assess the stability of DAB and QAB converters with simplified averaged models, and they rarely combine averaged, small-signal, harmonic, impedance-based and Nyquist analyses under practical CPL and PPL conditions. As a result, the combined influence of the converter dynamics, the network impedance and the digital implementation is not fully understood [5, 112].

RG-2 Insufficient harmonic-consistent evaluation of currents and power flow: Winding currents and inter-port power flow are usually approximated by averaged or fundamental components, although PWM harmonics strongly affect the RMS current stress, the ZVS boundaries and the losses. Harmonic balance and symmetry-based

analyses show their importance, but a consistent workflow that links the modulation to the harmonic content and the stress metrics is not used systematically in validation [113, 114].

RG-3 Limited tools for interpreting multi-port harmonic interactions: QAB converters show complex harmonic coupling because of their several phase-shift variables, which leads to counter-intuitive behaviour such as port-to-port harmonic inversion. This complicates the interpretation of experiments and the diagnosis of mismatches between model and measurement. Symmetry-based formulations can simplify the analysis but are not widely used as practical interpretation tools [114].

RG-4 Unquantified trade-offs in nonlinear control schemes: Nonlinear and sliding-mode controllers improve disturbance rejection with CPLs and PPLs, but the trade-offs between robustness, voltage regulation (overshoot, settling time, ripple) and switching activity and chattering are not consistently quantified. It therefore remains unclear whether the performance gains come at the cost of higher stress or losses [44, 61].

RG-5 Inconsistent benchmarking and performance reporting: Controllers are often compared under different conditions and with different metrics, and stress and efficiency indicators are not consistently reported together with the regulation metrics. This limits reproducibility and hides controller-dependent effects [115, 116].

2.1.13 Models Used in this Thesis and their Assumptions

Table 2.1 collects the models used in the following chapters, the chapter in which each is used, its main assumptions, and how it was checked against a more detailed model.

Table 2.1: Models used in the thesis and their assumptions.

Model	**Ch.**	**Main assumptions**	**How it was checked**
Averaged power flow and current-to-phase map	3, 4	No losses; ideal square-wave bridge voltages; fixed switching frequency; values averaged over one switching period; $\lvert d_{ij}\rvert \le 0.5$	In steady state the converter currents equal the load currents in the detailed switching model
Harmonic (GHA) model	3	Periodic steady state; ideal switches; linear inductances	Odd harmonics within 5.2% of the switching model up to $k = 15$ (forward power); 11–37% at a small phase shift (dead time)
Linear port models	3, 4	Small changes around the operating point; forward-Euler discretisation (MPC)	LMI and simulation checks (Chapter 3)
DAB fundamental model, $i_o = K \sin\varphi$	5	Only the fundamental of each bridge voltage	Within $+8\%$ to -6.5% of the switching model for 30–90°; output impedance within about 2% (5–500 Hz)
CPL and PPL models	3–5	Constant power within the control bandwidth; PPL as sudden power steps	–
Minor-loop gain with the controller	5	Linear small-signal impedances	Output impedance matches a Simulink measurement by current injection

Chapter 3

Design and Comparative Evaluation of Robust Control Strategies for QAB Converters with Constant-Power Loads

3.1 Introduction

This chapter studies a QAB converter whose ports 3 and 4 supply resistive loads and CPLs, and addresses RG-2 to RG-5. It builds a harmonic model of the transformer currents, which gives the coefficients used by the controllers, and then designs and compares controllers for the two load ports.

Chapter objectives:

(i) Model the winding currents of the QAB with the generalised harmonic approximation (GHA), including the dead time, and check the model against a detailed switching simulation.

(ii) Derive the phase-shift sensitivity coefficients B_{13} and B_{24} from the harmonic model and use them in the control-oriented model of the two load ports.

(iii) Design the adaptive super-twisting sliding mode controller (ASTSMC) and prove

its stability with bounded adaptive gains.

(iv) Compare the ASTSMC with a feedforward-decoupled PID controller and an SMC with a nonlinear extended state observer (SMC–NLESO) under the same test events, limits and tuning procedure.

(v) Run the three controllers on the OPAL-RT OP5700 simulator (software-in-the-loop, SIL).

Main contributions of this chapter: C1 (harmonic model of the QAB transformer currents) and C2 (ASTSMC for the QAB with CPLs), as listed in Section 1.5.

3.2 Topology and Operating Principle of QAB Converter Supplying Constant Power Loads

Fig. 3.1 shows the QAB converter studied in this chapter. Its general features and applications were reviewed in Chapter 2; this section gives only what the models and controllers of this chapter need [117]. The converter has four full bridges, each connected to its own source or load and magnetically coupled through a four-winding high-frequency transformer (HFT). The HFT provides galvanic isolation and the voltage ratio between the ports, the phase shifts between the bridges set the power flow, and the power can flow in both directions; zero-voltage switching reduces the switching losses [118]. In this chapter, ports 1 and 2 are the $300\ V$ source ports, and ports 3 and 4 supply the $48\ V$ loads (resistor and CPL) [119].

The Y- and Δ-equivalent models used to describe the power flow between the ports are shown in Fig. 3.2. Since the DAB converter is a QAB converter with only two active ports, the DAB power-flow equations extend to the QAB [120].

With ideal square-wave bridge voltages and a fixed switching frequency, the average

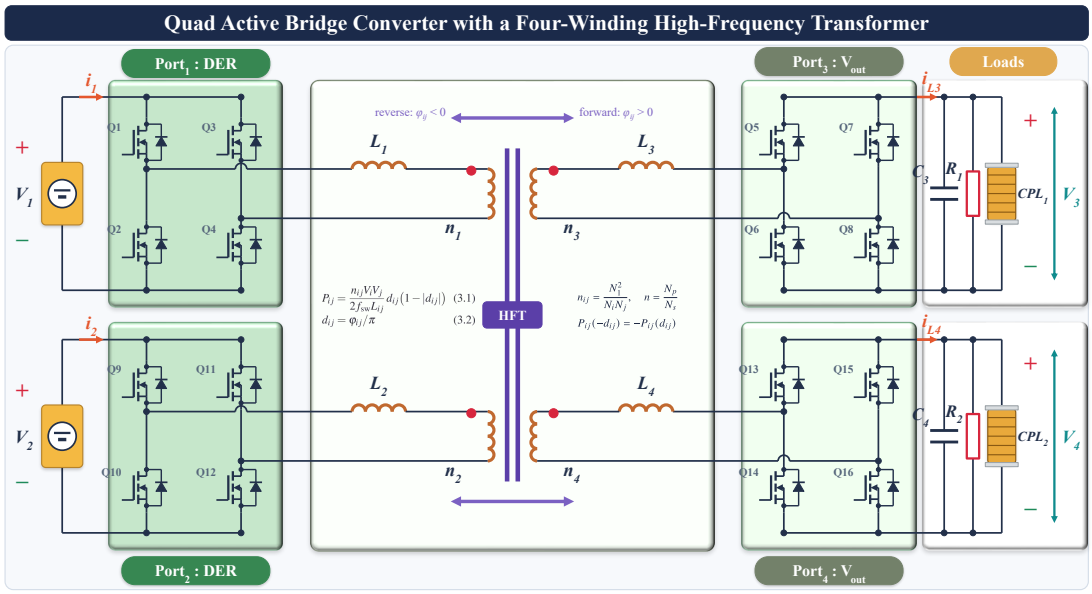


Figure 3.1: Schematic of the QAB converter.

power transferred between ports i and j over one switching period is:

$$P_{ij} = \frac{n_{ij}\, V_i\, V_j\, d_{ij}\,(1-|d_{ij}|)}{2 f_{sw}\, L_{ij}}, \qquad -\frac{1}{2} \le d_{ij} \le \frac{1}{2} \tag{3.1}$$

$$d_{ij} = \frac{\varphi_{ij}}{\pi}, \qquad \varphi_{ij} = \varphi_i - \varphi_j \tag{3.2}$$

where P_{ij} is the power transferred between ports i and j, n_{ij} is the turns ratio, V_i and V_j are the port voltages, and L_{ij} is the link inductance between the two ports in the Δ-equivalent circuit model (ECM).

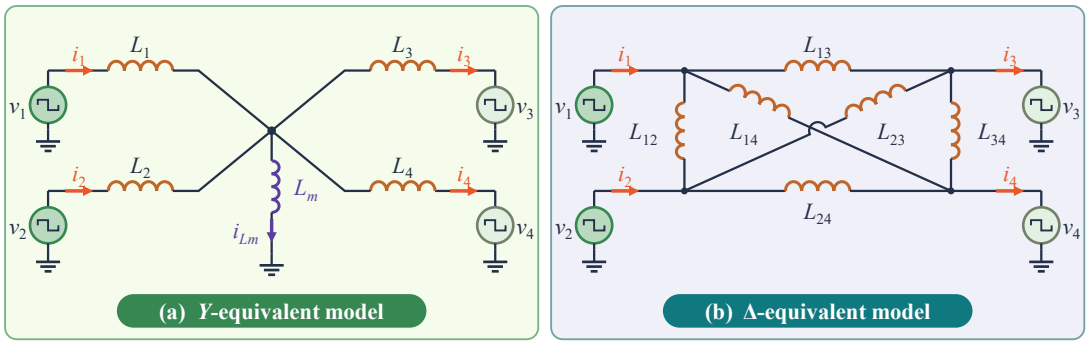


Figure 3.2: (a) Y-equivalent and (b) Delta-equivalent models of the QAB converter.

The phase-shift ratio d_{ij} is the phase shift φ_{ij} (in radians) divided by π. The largest

power is transferred at φ_{ij} = ±90°, so d_{ij} lies between $-\frac{1}{2}$ and $+\frac{1}{2}$. In the Δ-equivalent circuit, the link inductance $L_{ij} = L_{ji}$ is the equivalent inductance between ports i and j. Kirchhoff's voltage law relates it to the leakage inductances of the windings:

$$L_{ij} = L_i + L_j + \frac{L_i L_j}{L_p} + \frac{L_i L_j}{L_k}, \quad k \neq i, j;\ p \neq k \tag{3.3}$$

where L_i and L_j are the leakage inductances of windings i and j, and L_p and L_k are the leakage inductances of the other two windings. With equal leakage inductances of 75 μH per winding, Eq. (3.3) gives L_{ij} = 300 μH for every link. Rearranging Eq. (3.1) for $0 \leq d_{ij} \leq \frac{1}{2}$ gives the phase shift that transfers a given power through one link [121, 122]:

$$\varphi = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_{sw} L_{ij} P_{out}}{n_{ij} V_i V_j}}\right) \tag{3.4}$$

where φ is the phase shift between the two windings, f_{sw} is the switching frequency, P_{out} is the transferred power, and n_{ij} is the turns ratio. Fig. 3.3 shows the power that port 3 receives from both source ports, $P_3 = P_{13} + P_{23}$, as a function of the phase shift of bridge 3, for the converter of this chapter (Table 3.2): $V_1 = V_2$ = 300 V, f_{sw} = 14 kHz, $n = 300/70$ and L_{ij} = 300 μH. Because of the absolute value in Eq. (3.1), the curve is odd: a negative phase shift transfers the same power in the reverse direction. At the nominal operating point ($48\ V$, 2 Ω and a 150 W CPL per port), port 3 receives $1.30\ kW$ at a phase shift of 17.7°; the largest power, at ±90°, is $3.7\ kW$ at $48\ V$.

3.3 Analysis of Harmonics in QAB Converters

3.3.1 Estimated Winding Current Waveforms for Odd Harmonics

The winding currents of the QAB contain harmonics, caused mainly by the high-frequency switching of the semiconductor devices and by the pulse-width modulation (PWM) of the switches [121]. Core nonlinearities of the HFT (saturation, hysteresis)

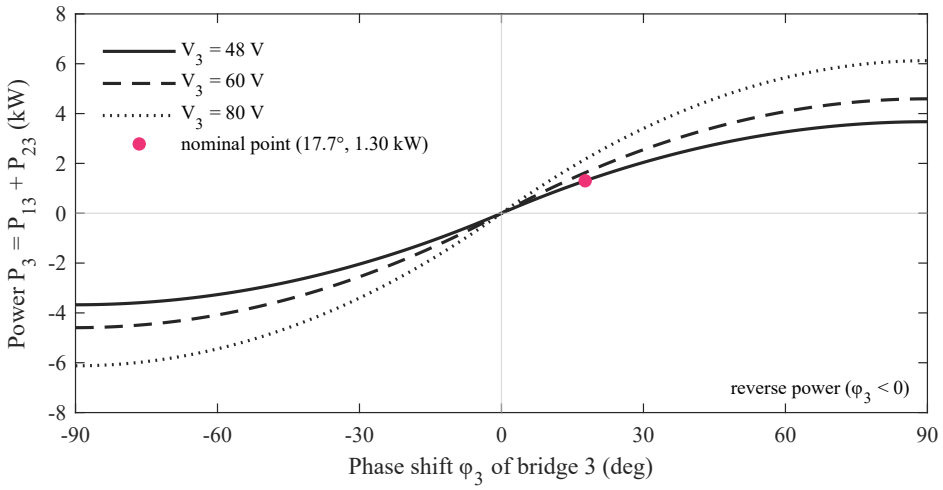


Figure 3.3: Power of port 3 against the phase shift of bridge 3.

and impedance mismatches between the windings and the loads distort the waveforms further [112]. Here, the generalised harmonic approximation (GHA), based on the Fourier series, is used to describe these harmonics in periodic steady state [113].

Because the bridge voltage $v_i(t)$ satisfies exact half-wave symmetry, $v_i(t + T/2) = -v_i(t)$, for any duty angle δ_i – the same zero-voltage notch applies symmetrically to both half-cycles of the switching waveform – its Fourier series contains only odd-order terms under ideal switching. This decomposition separates the fundamental, which carries the power, from the higher harmonics, which is useful for both power-flow control and harmonic analysis [123]. With $\theta = \omega t$, the voltage of port i is:

$$v_i(t) = \frac{4V_i}{\pi} \sum_{k=1,3,5,\ldots}^{2N+1} \frac{\cos(k\delta_i)}{k} \sin\big(k(\omega t - \phi_i)\big), \tag{3.5}$$

where V_i is the dc voltage of port i, δ_i is the duty (notch) angle, i.e., half the width of each zero-voltage interval, ϕ_i is the phase-shift angle of the bridge voltage, k is the odd harmonic order, N is the highest harmonic index retained, and $\omega = 2\pi f_{\mathrm{sw}}$ is the angular switching frequency.

The inductor current flowing between any two ports m and n in the Δ-equivalent

circuit is given by:

$$i_{mn}(t) = \frac{1}{L_{mn}} \int v_{mn}(t)\, dt = \frac{1}{L_{mn}} \int \left[v_m(t) - v_n(t) \right] dt, \tag{3.6}$$

where $i_{mn}(t)$ is the current flowing from port m to port n, $v_{mn}(t)$ is the voltage across the equivalent link inductance L_{mn}, and $v_m(t)$, $v_n(t)$ are the instantaneous bridge voltages of ports m and n [124]; in periodic steady state the integration constant is zero, so i_{mn} has no dc component. Substituting (3.5) and integrating term by term gives the odd-harmonic Fourier series of the link current:

$$\begin{aligned} i_{mn}(t) = \frac{4}{\pi \omega L_{mn}} \sum_{k=1,3,5,\ldots}^{2N+1} \frac{1}{k^2} \Big[& - V_m \cos(k\delta_m) \cos\big(k(\omega t - \phi_m)\big) \\ & + V_n \cos(k\delta_n) \cos\big(k(\omega t - \phi_n)\big) \Big] \end{aligned} \tag{3.7}$$

the $1/k^2$ weighting causes higher-order harmonics to decay rapidly. Because the two terms of the k-th harmonic have different phases, its magnitude depends on the phase difference $\phi_m - \phi_n$, as given by:

$$\begin{aligned} M_k(i_{mn}) &= \frac{4}{\pi \omega L_{mn} k^2} \sqrt{S_k}, \\ S_k &= A_k^2 + B_k^2 - 2 A_k B_k \cos\big(k(\phi_m - \phi_n)\big), \\ A_k &= V_m \cos(k\delta_m), \quad B_k = V_n \cos(k\delta_n). \end{aligned} \tag{3.8}$$

The waveform itself is given by (3.7); the harmonic magnitudes determine its RMS value and bound its peak value by:

$$I_{mn,\mathrm{rms}} = \sqrt{\sum_{k=1,3,5,\ldots}^{2N+1} \frac{M_k^2(i_{mn})}{2}}, \qquad \max_t |i_{mn}(t)| \le \sum_{k=1,3,5,\ldots}^{2N+1} M_k(i_{mn}). \tag{3.9}$$

Fig. 3.4 shows the port-3 winding current, the sum of its three link currents, built up from its odd harmonics at the operating point of Section 3.3.3 ($V_1 = V_2 = 300$ V, $V_3 = V_4 = 48$ V, $\phi_3 = 11.1°$, $\phi_4 = -3.7°$). The fundamental alone (amplitude 49.6 A) gives a sinusoid; adding $k = 3, 5, \ldots, 11$ produces the piecewise-linear shape with a peak of 67.8 A. Due to the $1/k^2$ attenuation, the low-order harmonics dominate the waveform, and the terms above $k = 7$ change it only near the switching edges.

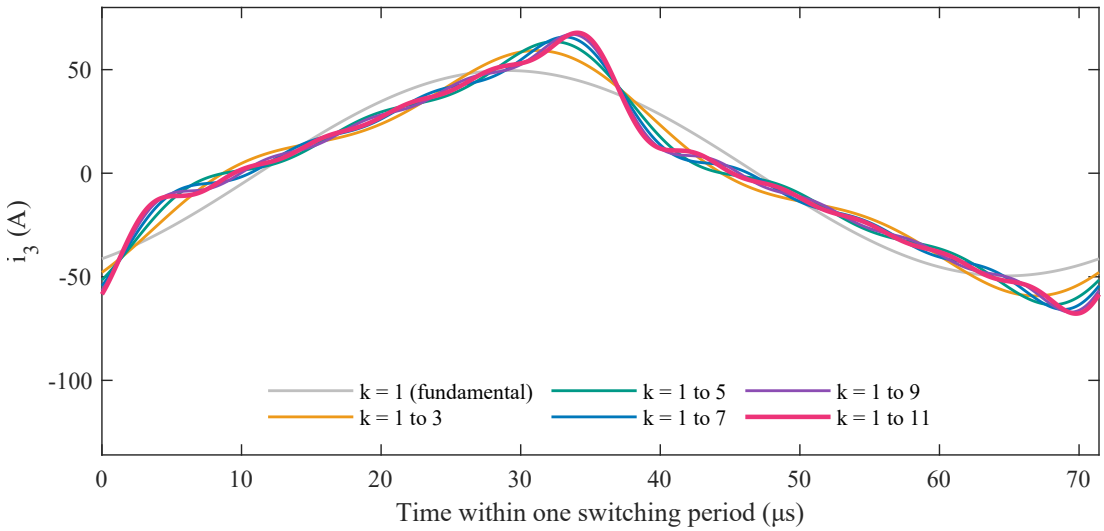


Figure 3.4: Port-3 winding current built from its odd harmonics (GHA model).

3.3.2 Estimated Winding Current Waveforms for Even Harmonics

Even-order harmonics cannot arise from the ideal bridge voltages, since a single waveform cannot satisfy both $v_i(t + T/2) = -v_i(t)$ and $v_i(t + T/2) = +v_i(t)$. A practical source of distortion is the switch dead time: during t_{dead} at each commutation, neither device of the commutating leg conducts, and the leg output is clamped by the freewheeling diode to the dc rail selected by the direction of the bridge current rather than by the commanded PWM level [114]. The perturbed port voltage is given by:

$$v_i'(\theta) = v_i(\theta) + \sum_{e \in \mathcal{E}_i} \left[v_i^{\text{cl}}(e) - v_i(\theta) \right] \mathbb{1}_{[e,\, e+\Delta\theta_{\text{dead}})}(\theta), \qquad i_i(\theta) = \sum_{n \neq i} i_{in}(\theta), \tag{3.10}$$

where $\theta = \omega t$, $\mathcal{E}_i = \{\phi_i + \delta_i,\ \phi_i + \pi - \delta_i,\ \phi_i + \pi + \delta_i,\ \phi_i + 2\pi - \delta_i\}$ are the nominal switching edges of port i, $\Delta\theta_{\text{dead}} = \omega t_{\text{dead}}$ is the dead time expressed as an angle, $\mathbb{1}_{[\cdot)}$ is the indicator function of the dead-time window, i_i is the total bridge current of port i, and $v_i^{\text{cl}}(e)$ is the bridge voltage obtained when the commutating leg is clamped to the negative rail for $i_i(e) > 0$ and to the positive rail for $i_i(e) < 0$, the other leg being unchanged; for $\delta_i = 0$ it reduces to $v_i^{\text{cl}}(e) = -\operatorname{sgn}\big(i_i(e)\big) V_i$. The harmonic coefficients of the perturbed link voltage $v'_{mn}(\theta) = v'_m(\theta) - v'_n(\theta)$ are obtained by

numerical integration:

$$a_k = \frac{1}{\pi}\int_0^{2\pi} v'_{mn}(\theta)\cos(k\theta)\,d\theta, \qquad b_k = \frac{1}{\pi}\int_0^{2\pi} v'_{mn}(\theta)\sin(k\theta)\,d\theta, \qquad k = 1,2,3,\ldots \tag{3.11}$$

and the corresponding current harmonic magnitude follows from the link inductance:

$$M_k(i_{mn}) = \frac{\sqrt{a_k^2 + b_k^2}}{k\,\omega\,L_{mn}}. \tag{3.12}$$

In periodic steady state with identical devices, the link currents are half-wave antisymmetric, $i_i(\theta+\pi) = -i_i(\theta)$, so the dead-time perturbation is also half-wave antisymmetric and $v'_i(\theta+\pi) = -v'_i(\theta)$ still holds: symmetric dead time changes the odd harmonics, but it produces no even harmonics. Even harmonics appear only when the two half-cycles differ, for example through unequal dead times or device voltage drops, unequal duty angles, or a dc bias of the transformer. Section 3.3.3 quantifies both cases with the switching simulation.

3.3.3 Check of the Harmonic Model against the Switching Simulation

The GHA model was checked against the detailed switching model of the converter that is also used for all controller results of this chapter (Section 3.7.1). The operating point is $V_1 = V_2 = 300$ V, $V_3 = V_4 = 48$ V, $f_{sw} = 14$ kHz, $L_{ij} = 300$ μH, $n = 300/70$ and a dead time of 200 ns, with the ASTSMC in closed loop; port 3 is a load (2 Ω and a 150 W CPL, $\phi_3 = 11.1°$, 1304 W), and port 4 is a 600 W source (reverse power, $\phi_4 = -3.7°$, 593 W). The model is solved with a fixed step of 51 ns, so that one switching period has exactly $M_p = 1400$ samples, and the winding currents are taken in steady state, from $t = 0.08$ s, over exactly $N = 20$ switching periods (1.43 ms). Harmonic k then falls exactly on point kN of the fast Fourier transform (FFT), so no window function is needed and there is no spectral leakage; the amplitude of harmonic k is

$c_k = 2|X[kN]|$, with $X[m] = \mathrm{FFT}(i)/(NM_p)$. For each odd harmonic, the GHA amplitude M_k (the sum of the three link currents of the winding) is compared with c_k through the deviation $|M_k - c_k|/c_k$, and the even harmonics are measured by the ratio $r_{\mathrm{even}} = \sqrt{\sum_{k\,\mathrm{even}} c_k^2}\big/\sqrt{\sum_{k\,\mathrm{odd}} c_k^2}$. The same run is repeated with the dead time of the second half-cycle 51 ns longer, to test the effect of an asymmetry, and the results do not change when the time step is halved. Fig. 3.5 and Table 3.1 show the result. At the forward-power port 3, the odd harmonics of the model agree with the simulation within 5.2% up to $k = 15$, and the reconstructed waveform lies on the simulated one. At the reverse-power port 4, the fundamental, which carries the power, agrees within 3.6%, but the higher harmonics deviate by 11–37%: the phase shift is only 3.7° (about 0.7 μs), so the 200 ns dead time, which the ideal model of Eq. (3.7) does not contain, changes the waveform edges much more. With equal dead times in both half-cycles, the even harmonics are only 0.018% (port 3) and 0.023% (port 4) of the odd content. When one half-cycle has 51 ns more dead time, they rise to 0.30% and 0.97%, by factors of 16 and 43, which confirms that even harmonics indicate an asymmetry between the half-cycles.

Table 3.1: Winding-current harmonics: GHA model against the switching simulation.

	Port 3 (forward power)			**Port 4 (reverse power)**		
k	Model (A)	Simulation (A)	Deviation (%)	Model (A)	Simulation (A)	Deviation (%)
1	49.58	50.24	1.3	41.87	40.40	3.6
3	10.93	11.46	4.6	6.58	5.92	11.2
5	6.03	6.36	5.2	3.23	2.81	15.0
7	4.03	4.25	5.1	2.03	1.73	17.7
9	2.91	3.05	4.8	1.40	1.16	20.4
11	2.17	2.26	4.2	0.99	0.80	24.0
13	1.64	1.70	3.3	0.71	0.55	29.3
15	1.24	1.27	2.0	0.52	0.38	37.4
Even, equal half-cycles	0.018% of the odd content			0.023% of the odd content		
Even, +51 ns in one half	0.30%			0.97%		

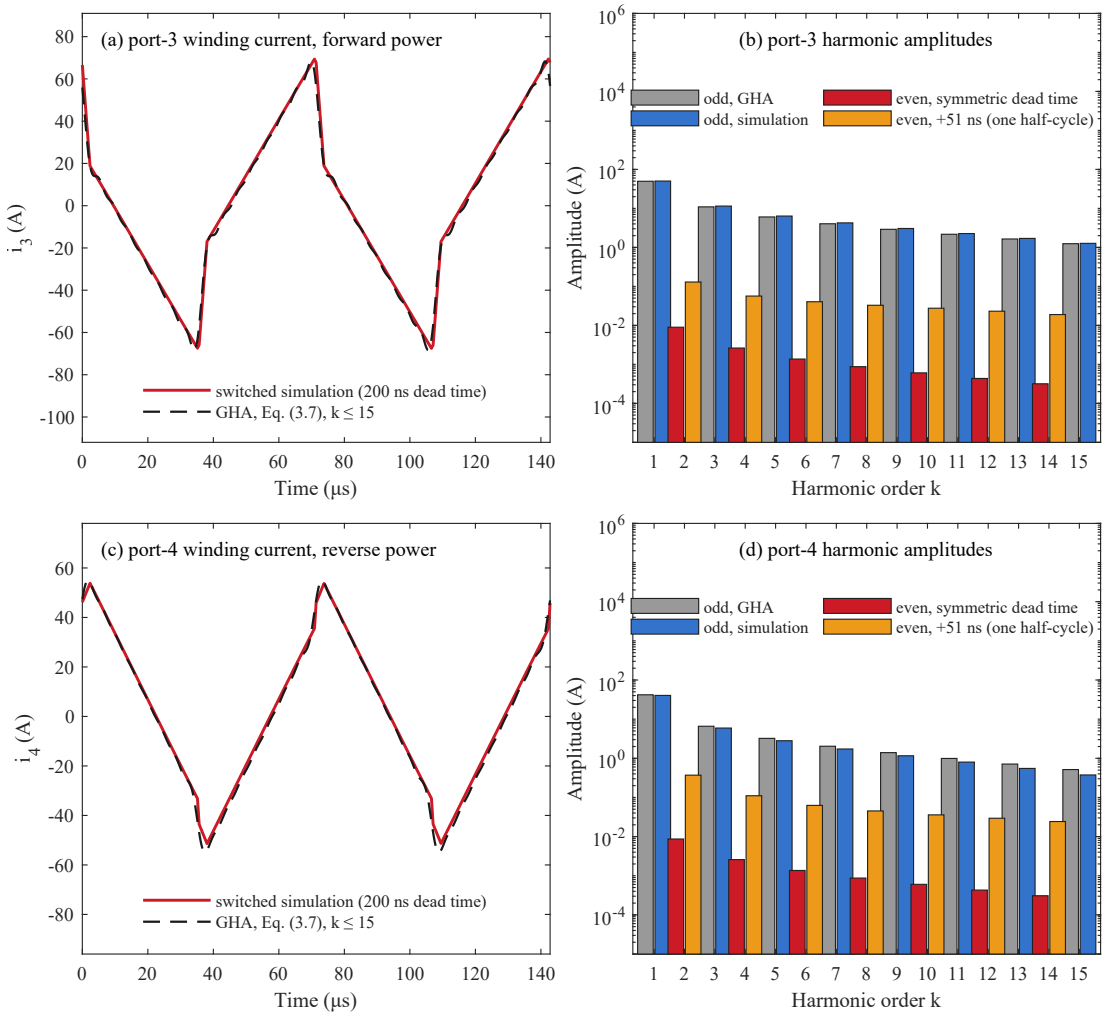


Figure 3.5: Winding currents and harmonics: GHA model against switching simulation.

3.4 Control Strategies and Disturbance Rejection

3.4.1 Sliding Mode Control (SMC)

Sliding mode control (SMC) is a robust nonlinear method for the uncertainties and nonlinearities of the QAB converter [122]. It has two phases: the reaching phase and the sliding phase. It gives a fast dynamic response and accurate power-flow regulation, even under large disturbances. Its main drawback is chattering, i.e. high-frequency oscillations that (i) increase switching losses, (ii) reduce efficiency and (iii) stress the components [125]. The adaptive super-twisting SMC (ASTSMC) of Section 3.5 reduces

chattering while keeping the robustness of SMC. The dynamic response also depends on the reaching law, which sets how fast the sliding surface is reached. The conventional reaching law, with a constant plus proportional rate, is:

$$\dot{S} = -\gamma \, \mathrm{sign}(S) - \kappa S, \qquad \gamma > 0, \; \kappa > 0. \tag{3.13}$$

The proportional term $-\kappa S$ forces the state to approach the switching manifold faster when S is large. Multiplying (3.13) by S gives $\frac{d}{dt}\frac{1}{2}S^2 = -\gamma|S| - \kappa S^2 \leq -\gamma|S|$, so the switching manifold is reached within the finite time $t_r \leq |S(0)|/\gamma$. The merit of this reaching law is its simplicity: if γ is too small, the reaching time is too long, whereas a too large γ causes severe chattering. The loads are connected to ports 3 and 4, which are the regulated output ports. Their sliding surfaces are defined as:

$$S_i = e_i + \lambda_i \int e_i \, dt, \qquad e_i = v_{\mathrm{ref},i} - v_{c_i}, \qquad i \in \{3, 4\}, \tag{3.14}$$

where e_i is the voltage-tracking error, $v_{\mathrm{ref},i}$ is the reference voltage, and v_{c_i} is the measured output (capacitor) voltage of port i. Differentiating (3.14) and using the capacitor dynamics of (3.16) gives $\dot{S}_i = -\big(i_{Li} - i_{\mathrm{load},i}\big)/C_i + \lambda_i e_i$. Equating this to the reaching law (3.13) and solving for the current that the converter must deliver to the output filter gives the conventional SMC law:

$$u_i = i_{\mathrm{load},i} + C_i\big(\lambda_i e_i + \gamma \, \mathrm{sign}(S_i) + \kappa S_i\big), \qquad i \in \{3, 4\}, \tag{3.15}$$

where λ_i is the integral gain of the sliding surface, γ is the switching gain, κ is the proportional reaching gain, and $\mathrm{sign}(S_i)$ is the discontinuous term for sliding-mode enforcement. Every term of (3.15) is a current; the command u_i is the average current that port i must deliver to its output filter. Eq. (3.15) requires the total load current $i_{\mathrm{load},i}$, which includes the CPL current and is not measured.

3.4.2 Nonlinear Extended State Observer (NLESO)

The NLESO improves the robustness of the controller by estimating both the states and the disturbances while it runs. Unlike linear observers, it uses nonlinear gain functions to handle uncertainties and external disturbances [126]. It follows the extended-state principle of active disturbance rejection control, in which every unknown term acting on the plant is lumped into one *total disturbance* that is estimated as an additional (extended) state and then cancelled by feedforward [127]. Its main features are an extended state model that allows accurate estimation in nonlinear, time-varying systems, the estimation of both internal and external disturbances, and feedforward compensation that cancels the estimated disturbance [128]. Combined with SMC, the NLESO allows a smaller switching gain γ, which reduces chattering while keeping the system stable under varying conditions.

The NLESO is derived from Kirchhoff's current law (KCL) applied to the output filters of ports 3 and 4 in Fig. 3.2. At the output node of port i, the average current delivered by bridge i divides between the filter capacitor, which carries $C_i\, dv_{c_i}/dt$, and the load. The resulting capacitor voltage dynamics of ports 3 and 4 are given by:

$$\begin{cases} C_3 \dfrac{dv_{c_3}}{dt} = i_{L3} - i_{\mathrm{load},3}, \\ C_4 \dfrac{dv_{c_4}}{dt} = i_{L4} - i_{\mathrm{load},4}, \end{cases} \tag{3.16}$$

where v_{c_3} and v_{c_4} are the output (capacitor) voltages of ports 3 and 4; i_{L3} and i_{L4} are the average rectified output currents delivered by bridges 3 and 4 to their output filters (the output stage contains no dc-side inductor; the leakage inductances act on the ac side of the bridges); $i_{\mathrm{load},3}$ and $i_{\mathrm{load},4}$ are the total load currents at ports 3 and 4, including resistive and CPLs; and C_3 and C_4 are the filter capacitors of ports 3 and 4. Each port supplies a resistive load, which draws $v_{c_i}/R_{\mathrm{load},i}$ by Ohm's law, in parallel with a CPL, which draws $P_{\mathrm{CPL},i}/v_{c_i}$ because its power $P_{\mathrm{CPL},i} = v_{c_i}\, i_{\mathrm{CPL},i}$ is held constant. The load

currents of ports 3 and 4 are therefore given by:

$$i_{\mathrm{load},i} = \frac{v_{c_i}}{R_{\mathrm{load},i}} + \frac{P_{\mathrm{CPL},i}}{v_{c_i}}, \qquad i \in \{3,4\}, \tag{3.17}$$

where $R_{\mathrm{load},3}$ and $R_{\mathrm{load},4}$ are the resistive loads and $P_{\mathrm{CPL},3}$ and $P_{\mathrm{CPL},4}$ are the constant power loads supplied by ports 3 and 4, respectively.

3.4.3 NLESO for Resolving Instability Caused by CPLs

The CPLs introduce nonlinear dynamics that can cause instability if not properly controlled [129, 130]. Differentiating the CPL term of Eq. (3.17) with respect to the port voltage gives the incremental resistance of the CPL:

$$r_{\mathrm{CPL},i} = \left(\frac{\partial}{\partial v_{c_i}} \frac{P_{\mathrm{CPL},i}}{v_{c_i}} \right)^{-1} = -\frac{v_{c_i}^2}{P_{\mathrm{CPL},i}} < 0, \qquad i \in \{3,4\}, \tag{3.18}$$

where $r_{\mathrm{CPL},i}$ is the small-signal (incremental) resistance seen by the output filter of port i. Because $r_{\mathrm{CPL},i}$ is negative, a drop in v_{c_i} increases the CPL current, which discharges C_i further and opposes the damping provided by $R_{\mathrm{load},i}$; this negative damping is the source of the instability. The NLESO is used to counter it: it estimates the output voltage and the total disturbance current of each port, which includes the CPL current, so that the controller can compensate for the effect of the CPLs and stabilise the system [131]. The observer has two states for each port $i \in \{3,4\}$, detailed in the following subsections.

3.4.4 Total Disturbance Current

Equation (3.16) contains two currents that the controller does not know: the load current $i_{\mathrm{load},i}$ of Eq. (3.17), which is not measured, and the current i_{Li} that bridge i actually delivers, which differs from the current command u_i of Eq. (3.15) whenever the phase-shift modulation does not realise the command exactly. Adding and subtracting u_i on the right-hand side of Eq. (3.16) leaves them unchanged and gives:

$$C_i \frac{dv_{c_i}}{dt} = u_i - \Big[i_{\mathrm{load},i} - \big(i_{Li} - u_i\big) \Big], \qquad i \in \{3,4\}. \tag{3.19}$$

The bracketed term of Eq. (3.19) is defined as the total disturbance current of port i:

$$d_i = i_{\mathrm{load},i} - \big(i_{Li} - u_i\big), \qquad i \in \{3, 4\}, \tag{3.20}$$

where d_i is the total disturbance current of port i (A), which combines the unmeasured load current of Eq. (3.17) with the mismatch $i_{Li} - u_i$ between the delivered bridge current and its command. When the bridge delivers exactly its command ($i_{Li} = u_i$), d_i equals the load current $i_{\mathrm{load},i}$. Substituting Eq. (3.20) into Eq. (3.19) gives the disturbance form of the capacitor dynamics:

$$C_i \frac{dv_{c_i}}{dt} = u_i - d_i, \qquad i \in \{3, 4\}, \tag{3.21}$$

in which only v_{c_i} (measured) and u_i (computed by the controller) are known, and every unknown effect is collected in the single term d_i. Following the extended-state principle [127], d_i is treated as a second state of port i. With $x_{1i} = v_{c_i}$ and $x_{2i} = d_i$, Eq. (3.21) is written as the extended state model:

$$\dot{x}_{1i} = \frac{1}{C_i}\big(u_i - x_{2i}\big), \qquad \dot{x}_{2i} = h_i(t), \qquad i \in \{3, 4\}, \tag{3.22}$$

where x_{1i} is the capacitor voltage, x_{2i} is the total disturbance current (the extended state), and $h_i(t) = \dot{d}_i$ is its unknown rate of change, which is bounded because the load and the bridge current cannot change infinitely fast.

3.4.5 Capacitor Voltage Estimation

The observer reproduces the first line of Eq. (3.22) with the estimates in place of the true states and adds a correction driven by the measured voltage. The observer for the capacitor voltage is:

$$\dot{z}_{1i} = \frac{1}{C_i}\big(u_i - z_{2i}\big) + \beta_{i1}\ \mathrm{fal}\big(\tilde{v}_i, \alpha_1, \delta_1\big), \qquad \tilde{v}_i = v_{c_i} - z_{1i}, \tag{3.23}$$

where v_{c_i} is the measured capacitor voltage at port i ($i = 3$ for port 3 and $i = 4$ for port 4), z_{1i} is its estimate, z_{2i} is the estimate of the total disturbance current d_i, $\tilde{v}_i$ is

the voltage estimation error, β_{i1} is the observer gain of the voltage-estimation channel, which sets how fast z_{1i} converges to v_{c_i} (unit $\mathrm{V}^{1-\alpha_1}\,\mathrm{s}^{-1}$; it is a gain, not a voltage), and $\beta_{i1}\,\mathrm{fal}(\tilde{v}_i, \alpha_1, \delta_1)$ is the nonlinear correction term, with $\mathrm{fal}(\cdot)$ defined in Eq. (3.26) below and α_1 and δ_1 its exponent and linear-zone width for the voltage channel.

3.4.6 Disturbance Estimation

The second observer state integrates the same voltage estimation error to track the extended state $x_{2i} = d_i$. The total disturbance current is estimated by:

$$\dot{z}_{2i} = -\beta_{i2}\ \mathrm{fal}(\tilde{v}_i, \alpha_2, \delta_2)\,, \tag{3.24}$$

where β_{i2} is the observer gain of the disturbance-estimation channel, which sets how fast z_{2i} converges to d_i (unit $\mathrm{A\,V}^{-\alpha_2}\,\mathrm{s}^{-1}$), α_2 and δ_2 are the fal exponent and linear-zone width for the disturbance channel, and $\dot{z}_{2i}$ is the rate of change of the estimated disturbance [129, 131, 132]. The negative sign is required because an under-estimated disturbance makes the measured voltage fall below its estimate ($\tilde{v}_i < 0$), and z_{2i} must then increase.

The convergence of the observer is seen from its estimation errors $\tilde{v}_i = v_{c_i} - z_{1i}$ and $\tilde{d}_i = d_i - z_{2i}$. Subtracting Eq. (3.23) from the first line of Eq. (3.22), and Eq. (3.24) from its second line, gives the error dynamics:

$$\dot{\tilde{v}}_i = -\frac{\tilde{d}_i}{C_i} - \beta_{i1}\ \mathrm{fal}(\tilde{v}_i, \alpha_1, \delta_1)\,, \qquad \dot{\tilde{d}}_i = h_i(t) + \beta_{i2}\ \mathrm{fal}(\tilde{v}_i, \alpha_2, \delta_2)\,, \tag{3.25}$$

where $\tilde{d}_i$ is the disturbance estimation error. For small errors, where fal is linear with slope $k_j = \delta_j^{\alpha_j - 1}$ ($j \in \{1, 2\}$), Eq. (3.25) is a linear system with characteristic polynomial $s^2 + \beta_{i1} k_1 s + \beta_{i2} k_2 / C_i$, whose coefficients are both positive for positive gains, so both roots lie in the left half-plane and the errors decay. Choosing the gains as $\beta_{i1} = 2\omega_o\,\delta_1^{1-\alpha_1}$ and $\beta_{i2} = C_i\,\omega_o^2\,\delta_2^{1-\alpha_2}$ turns this polynomial into $(s + \omega_o)^2$, so both observer poles are placed at $s = -\omega_o$ and the observer is tuned by a single bandwidth

ω_o. With $\omega_o = 2\pi \cdot 400$ rad/s, $\alpha_1 = 0.75$, $\alpha_2 = 0.5$, and $\delta_1 = \delta_2 = 0.5$ V, this gives $\beta_{i1} \approx 4227\ \mathrm{V}^{0.25}\,\mathrm{s}^{-1}$; for example, a voltage estimation error of 0.1 V is corrected at about $2\omega_o \times 0.1 \approx 503$ V/s, i.e., with a time constant of about $1/(2\omega_o) \approx 0.2$ ms. Since $h_i(t)$ is bounded, $\tilde{v}_i$ and $\tilde{d}_i$ remain in a small neighbourhood of zero that shrinks as β_{i1} and β_{i2} increase, so $z_{1i} \to v_{c_i}$ and $z_{2i} \to d_i$ [127].

The fractional power function (fal) used in Eqs. (3.23)–(3.25) is defined as:

$$\mathrm{fal}(\xi, \alpha, \delta) = \begin{cases} |\xi|^{\alpha}\ \mathrm{sign}(\xi), & |\xi| > \delta, \\ \dfrac{\xi}{\delta^{1-\alpha}}, & |\xi| \le \delta, \end{cases} \tag{3.26}$$

where ξ is the observer estimation error, here $\xi = \tilde{v}_i = v_{c_i} - z_{1i}$; α is the nonlinearity exponent ($0 < \alpha < 1$); and $\delta > 0$ is the threshold for small errors [122, 127]. The two branches meet at $|\xi| = \delta$, where both equal $\delta^{\alpha}\,\mathrm{sign}(\xi)$, so fal is continuous. For large errors ($|\xi| > \delta$) the power $\alpha < 1$ makes the correction grow more slowly than the linear branch would, since $|\xi|^{\alpha} < |\xi|\,\delta^{\alpha-1}$, which limits the peaking of the estimates during transients; for small errors the linear branch has the slope $\delta^{\alpha-1}$, which exceeds unity for $\delta < 1$ and gives a higher gain near zero than a unit-slope linear observer and avoids the infinite slope of $|\xi|^{\alpha}$ at $\xi = 0$, which would cause chattering.

To incorporate the observer, the unmeasured load current $i_{\mathrm{load},i}$ in Eq. (3.15) is replaced by the disturbance estimate z_{2i}, which by Eq. (3.20) estimates the load current together with any bridge-current mismatch. The gains γ and κ of Eq. (3.15) are also allowed to differ between the ports. The control inputs of the SMC with NLESO for ports 3 and 4 are therefore:

Port 3:

$$u_3 = z_{23} + C_3\big[\lambda_3 e_3 + \gamma_3\ \mathrm{sign}(S_3) + \kappa_3 S_3\big] \tag{3.27}$$

Port 4:

$$u_4 = z_{24} + C_4\big[\lambda_4 e_4 + \gamma_4\ \mathrm{sign}(S_4) + \kappa_4 S_4\big] \tag{3.28}$$

where z_{23} and z_{24} are the NLESO estimates of the total disturbance currents of ports 3

and 4 from Eq. (3.24), used for feedforward compensation; u_3 and u_4 are the current commands of ports 3 and 4; C_3 and C_4 are the output filter capacitances; e_3 and e_4 are the voltage-tracking errors and S_3 and S_4 the sliding surfaces of Eq. (3.14); λ_3 and λ_4 are the integral gains of the sliding surfaces; γ_3 and γ_4 are the switching gains; and κ_3 and κ_4 are the proportional gains that stabilise the dynamics around the sliding surface.

The benefit of the observer follows from the closed-loop sliding dynamics. Differentiating Eq. (3.14) with a constant reference gives $\dot{S}_i = -\dot{v}_{c_i} + \lambda_i e_i$; substituting $\dot{v}_{c_i} = (u_i - d_i)/C_i$ from Eq. (3.21) and u_i from Eqs. (3.27) and (3.28), the terms $\lambda_i e_i$ cancel, and:

$$\dot{S}_i = -\gamma_i \operatorname{sign}(S_i) - \kappa_i S_i + \frac{\tilde{d}_i}{C_i}, \qquad \tilde{d}_i = d_i - z_{2i}, \qquad i \in \{3, 4\}. \tag{3.29}$$

Multiplying Eq. (3.29) by S_i gives $\frac{d}{dt}\frac{1}{2}S_i^2 \le -\big(\gamma_i - |\tilde{d}_i|/C_i\big)|S_i| - \kappa_i S_i^2$, so the sliding surface is reached in finite time whenever $\gamma_i > |\tilde{d}_i|/C_i$. Without the observer, the switching gain must cover the whole unknown load current, whereas with the NLESO it only has to cover the small estimation error $\tilde{d}_i$; a smaller γ_i can therefore be used, which is why the observer reduces chattering. The implemented law uses only measured voltages and observer states. The current commands are converted into phase shifts by Eq. (3.44).

3.4.7 Feedforward Decoupling of the Port Interactions

The decoupler derived here is common to all three controllers of this chapter. Although the commands u_{13} and u_{24} are named after the main power paths, all six link inductances of the Δ-equivalent model (Fig. 3.2) act on the output ports. Taking bridges 1 and 2 as the phase reference ($\phi_1 = \phi_2 = 0$), the phase shifts of bridges 3 and 4 are ϕ_3 and ϕ_4.

Applying Eq. (3.1) to every link, the powers delivered to the output ports are:

$$\begin{aligned} P_3 &= P_{13}(\phi_3) + P_{23}(\phi_3) + P_{43}(\phi_3 - \phi_4), \\ P_4 &= P_{14}(\phi_4) + P_{24}(\phi_4) + P_{34}(\phi_4 - \phi_3), \end{aligned} \tag{3.30}$$

while the 1–2 link transfers no active power, because bridges 1 and 2 switch in phase. Linearising Eq. (3.30) about the operating point, with the path gains $g_{ij} = \partial P_{ij}/\partial\phi = V_i' V_j' (1-2|d_{ij}|)/(2\pi f_{sw} L_{ij})$ obtained from Eq. (3.1), where V_i' are the primary-referred port voltages (V_1, V_2, nV_3, nV_4), gives:

$$\begin{bmatrix} \Delta P_3 \\ \Delta P_4 \end{bmatrix} = \underbrace{\begin{bmatrix} g_{13} + g_{23} + g_{34} & -g_{34} \\ -g_{34} & g_{14} + g_{24} + g_{34} \end{bmatrix}}_{\mathbf{G}} \begin{bmatrix} \Delta\phi_3 \\ \Delta\phi_4 \end{bmatrix}. \tag{3.31}$$

The cross paths 2–3 and 1–4 act on the same phase shift as the main paths 1–3 and 2–4 and are therefore contained in the diagonal of $\mathbf{G}$. The 3–4 path is the only one that couples the two control channels, through the off-diagonal terms $-g_{34}$. Each controller is designed for a channel in which its command drives only the two source links into its port, $\Delta P_3 = (g_{13} + g_{23})u_{13}$ and $\Delta P_4 = (g_{14} + g_{24})u_{24}$. The decoupler therefore applies the phase shifts:

$$\begin{bmatrix} \phi_3 \\ \phi_4 \end{bmatrix} = \mathbf{G}^{-1}\mathbf{A} \begin{bmatrix} u_{13} \\ u_{24} \end{bmatrix}, \qquad \mathbf{A} = \operatorname{diag}\big(g_{13} + g_{23},\ g_{14} + g_{24}\big), \tag{3.32}$$

so that ΔP_3 depends only on u_{13} and ΔP_4 only on u_{24} at the operating point. For equal commands, $u_{13} = u_{24} = u$, the decoupler returns $\boldsymbol{\phi} = [u,\ u]^{\mathsf{T}}$: equal commands pass unchanged and only their difference is corrected. $\mathbf{G}$ is invertible for all positive path gains, because it is diagonally dominant, and it is evaluated every control period at the applied phase shifts and the measured, primary-referred port voltages. Because $\mathbf{G}$ depends on the operating point, the residual coupling away from it, and any mismatch in the link inductances, act as a bounded disturbance on each port; they are part of the total disturbance d_i of Eq. (3.20) for the SMC–NLESO and of the lumped uncertainty

Δ_i for the ASTSMC (Section 3.8.3). Their effect on the PID controller is analysed in Section 3.8.4.

3.5 Proposed Adaptive Super Twisting Sliding Mode Controller (ASTSMC)

The SMC–NLESO estimates and compensates the disturbance, but its discontinuous switching term acts directly on the command, which causes chattering, and its fixed gains must be sized for the worst disturbance [133]. The proposed adaptive super-twisting SMC (ASTSMC) keeps the same observer and decoupler, makes the applied control continuous, and adjusts its gains to the size of the tracking error, so that large gains act only during transients [134]. Section 3.7 compares the two controllers under the same tests: the ASTSMC settles faster and moves its control signal about four times less, while the SMC–NLESO has the smaller overshoot. The ASTSMC is designed in five steps. First, the sliding surfaces express the voltage-tracking objective. Second, an equivalent control is derived from the averaged model of the QAB; it supplies the phase shift that keeps the output voltages on their references when the model is exact. Third, the gains of the super-twisting algorithm are made adaptive, so that they are large only during transients. Fourth, the adaptive super-twisting switching terms are added to reject the model errors and disturbances that the equivalent control cannot cancel. Fifth, the two parts are summed, the sign function is smoothed by a boundary layer, and the unmeasured load current is replaced by its NLESO estimate, which gives the implemented control law.

Step 1 – Sliding surfaces. To regulate the output voltages of ports 3 and 4, the sliding surfaces σ_3 and σ_4 are defined as the voltage-tracking errors, so that $\sigma_i = 0$ means that

the output voltage of port i equals its reference (the desired state), as given by:

$$\begin{cases} \sigma_3 = V_3 - V_{3,\mathrm{ref}}, \\ \sigma_4 = V_4 - V_{4,\mathrm{ref}} \end{cases} \tag{3.33}$$

a plain voltage error is sufficient here, without the integral term used for the SMC in Eq. (3.14), because the integral part of the super-twisting algorithm (Step 4) already removes the steady-state error. Moreover, σ_i has relative degree one with respect to the phase shift, since the phase shift appears directly in $\dot{V}_i$ (Eq. (3.38)), which is the condition required by the super-twisting algorithm.

Step 2 – Equivalent control. The control law consists of two parts: an equivalent control, which keeps the output voltage on the sliding surface ($\dot{\sigma}_i = 0$) when the model is exact, and a switching term, which drives σ_i to zero and rejects the model errors and disturbances that the equivalent control cannot cancel. The equivalent control is established by enforcing the sliding conditions $\sigma_3 = 0$ and $\sigma_4 = 0$, which ensures steady-state tracking [132]. It is derived from the averaged model of ports 3 and 4, which is obtained from the Fourier series and the switching functions of the QAB [132]. The derivation is given below for port 3, which is supplied by port 1 through the path $1 \leftrightarrow 3$; port 4 follows in the same way by replacing the indices $1 \to 2$ and $3 \to 4$.

(a) Starting point. The output voltage of port 3 is governed by the capacitor equation of Eq. (3.16), $C_3\, dV_3/dt = i_{L3} - i_{\mathrm{load},3}$, with $V_3 \equiv v_{c_3}$. The load current does not depend on the control; therefore, the model is obtained by expressing the average bridge current i_{L3} as a function of the phase shift ζ_{13} and of V_3.

(b) Bridge voltages. With square-wave operation ($\delta_i = 0$) in Eq. (3.5), the bridge voltage of port 1 and the bridge voltage of port 3 referred to the primary side, which

lags by ζ_{13}, are given by:

$$\begin{cases} v_1(\theta) = \dfrac{4V_{\text{in},1}}{\pi} \displaystyle\sum_{n=0}^{N} \dfrac{\sin\big((2n+1)\theta\big)}{2n+1}, \\ v_3'(\theta) = \dfrac{4a_1V_3}{\pi} \displaystyle\sum_{n=0}^{N} \dfrac{\sin\big((2n+1)(\theta-\zeta_{13})\big)}{2n+1}, \end{cases} \tag{3.34}$$

where $\theta = \omega t$, $a_1 = N_{p,1}/N_{s,1}$ is the turns ratio of the path $1 \leftrightarrow 3$, and $n \in \{0, 1, \ldots, N\}$ is the harmonic index, so that the odd harmonic orders $2n+1 = 1, 3, 5, \ldots, 2N+1$ are retained.

(c) Link current. Each harmonic of the voltage difference $v_1 - v_3'$ drives a current through the series impedance of the link, $Z[n] = |Z[n]|\, e^{j\phi_{z,3}[n]}$, evaluated at the $(2n+1)$-th harmonic (for a series R–L link, $Z[n] = R_{13} + j(2n+1)\omega L_{13}$). Each current harmonic therefore equals the voltage harmonic divided by $|Z[n]|$ and lags it by $\phi_{z,3}[n]$, which gives:

$$\begin{aligned} i_{13}(\theta) = \frac{4}{\pi} \sum_{n=0}^{N} \frac{1}{(2n+1)\,|Z[n]|} \Big[& V_{\text{in},1} \sin\big((2n+1)\theta - \phi_{z,3}[n]\big) \\ & - a_1V_3 \sin\big((2n+1)(\theta-\zeta_{13}) - \phi_{z,3}[n]\big)\Big]. \end{aligned} \tag{3.35}$$

(d) Rectification and averaging. Bridge 3 rectifies the secondary current $a_1 i_{13}$ with its switching function $s_3(\theta) = \pm 1$, which is in phase with v_3' and has the Fourier series $s_3(\theta) = \frac{4}{\pi} \sum_{n=0}^{N} \sin\big((2n+1)(\theta-\zeta_{13})\big)/(2n+1)$. The current delivered to C_3, averaged over one switching period, is $i_{L3} = \frac{1}{2\pi} \int_0^{2\pi} a_1\, i_{13}(\theta)\, s_3(\theta)\, d\theta$. Because sinusoids of different orders are orthogonal, only the products of equal orders remain, and the mean of two sinusoids of equal order with amplitudes X and Y and phase difference ψ is $XY\cos\psi/2$. This gives:

$$i_{L3} = \frac{8a_1}{\pi^2} \sum_{n=0}^{N} \frac{V_{\text{in},1}\cos\big((2n+1)\zeta_{13} - \phi_{z,3}[n]\big) - a_1V_3\cos\big(\phi_{z,3}[n]\big)}{(2n+1)^2\,|Z[n]|}. \tag{3.36}$$

The first term is the current transferred from port 1, which is controlled by ζ_{13}; the second term is the current that the bridge voltage of port 3 drives through the resistive part of its own link, which is zero for a purely inductive link ($\phi_{z,3}[n] = \pi/2$). For the

fundamental component of a lossless link, Eq. (3.36) reduces to the well-known DAB relation $i_{L3} = 8a_1 V_{\mathrm{in},1} \sin\zeta_{13}/(\pi^2 \omega L_{13})$.

(e) Linearisation. Eq. (3.36) is nonlinear in ζ_{13} because of the cosine. To obtain a model in which the control enters linearly, as required to solve for the equivalent control, the cosine is expanded in a first-order Taylor series around the operating-point phase shift $\zeta_{13,0}$, as given by:

$$\begin{aligned}\cos\big((2n+1)\zeta_{13} - \phi_{z,3}[n]\big) \approx \cos\big((2n+1)\zeta_{13,0} - \phi_{z,3}[n]\big) \\ + (2n+1)\sin\big(\phi_{z,3}[n] - (2n+1)\zeta_{13,0}\big)\big(\zeta_{13} - \zeta_{13,0}\big).\end{aligned} \tag{3.37}$$

Substituting Eqs. (3.36) and (3.37) into the capacitor equation of step (a) and dividing by C_3 gives $dV_3/dt = A_3 V_3 + B_{13}\zeta_{13} + D_3\, i_{\mathrm{load},3} + r_3$, where A_3, B_{13}, and D_3 collect the coefficients of V_3, ζ_{13}, and $i_{\mathrm{load},3}$, respectively (they are given explicitly in Eqs. (3.39)–(3.41) below), and r_3 is the constant remainder of the linearisation. For a predominantly inductive link ($\phi_{z,3}[n] \approx \pi/2$), each term of r_3 is proportional to $\sin x - x\cos x \approx x^3/3$ with $x = (2n+1)\zeta_{13,0}$; r_3 is therefore small and is neglected in the nominal model, and any residual part acts as a slowly varying matched disturbance that is rejected by the integral part of the super-twisting term (Step 4). Applying the same steps to port 4 gives the averaged model:

$$\begin{cases} \dfrac{dV_3}{dt} = A_3 V_3 + B_{13}\,\zeta_{13} + D_3\, i_{\mathrm{load},3}, \\ \dfrac{dV_4}{dt} = A_4 V_4 + B_{24}\,\zeta_{24} + D_4\, i_{\mathrm{load},4}, \end{cases} \tag{3.38}$$

where V_3 and V_4 are the output voltages, $V_{3,\mathrm{ref}}$ and $V_{4,\mathrm{ref}}$ are the reference voltages, A_3 and A_4 are the coefficients that set how the output voltages evolve, Eq. (3.39), B_{13} and B_{24} are the phase-shift sensitivity coefficients, Eq. (3.40), and D_3 and D_4 are the load-current input coefficients:

$$\begin{cases} A_3 = -\dfrac{8\,N_{p,1}^2}{\pi^2\, C_3\, N_{s,1}^2} \displaystyle\sum_{n=0}^{N} \frac{\cos\big(\phi_{z,3}[n]\big)}{(2n+1)^2\,|Z[n]|}, \\ A_4 = -\dfrac{8\,N_{p,2}^2}{\pi^2\, C_4\, N_{s,2}^2} \displaystyle\sum_{n=0}^{N} \frac{\cos\big(\phi_{z,4}[n]\big)}{(2n+1)^2\,|Z[n]|} \end{cases} \tag{3.39}$$

$$\begin{cases} B_{13} = \dfrac{8\,V_{\mathrm{in},1}\,N_{p,1}}{\pi^2\,C_3\,N_{s,1}} \displaystyle\sum_{n=0}^{N} \dfrac{\sin\big(\phi_{z,3}[n] - (2n+1)\,\zeta_{13,0}\big)}{(2n+1)\,|Z[n]|}, \\ B_{24} = \dfrac{8\,V_{\mathrm{in},2}\,N_{p,2}}{\pi^2\,C_4\,N_{s,2}} \displaystyle\sum_{n=0}^{N} \dfrac{\sin\big(\phi_{z,4}[n] - (2n+1)\,\zeta_{24,0}\big)}{(2n+1)\,|Z[n]|} \end{cases} \tag{3.40}$$

where n is the harmonic index of Eq. (3.34), and $|Z[n]|$ and $\phi_{z,i}[n]$ ($i \in \{3,4\}$) are the magnitude and phase angle of the link impedance at the $(2n+1)$-th harmonic, as defined in step (c). $V_{\mathrm{in},1}$ and $V_{\mathrm{in},2}$ are the dc input voltages of ports 1 and 2. $N_{p,1}, N_{s,1}$ and $N_{p,2}, N_{s,2}$ are the numbers of primary and secondary turns for the power-transfer paths $1 \leftrightarrow 3$ and $2 \leftrightarrow 4$, respectively. C_3 and C_4 are the output capacitors of ports 3 and 4 (see Fig. 3.1). Finally, $\zeta_{13,0}$ and $\zeta_{24,0}$ are the steady-state (operating-point) phase shifts used to evaluate the sensitivities B_{13} and B_{24}. A_i is negative, because the bridge voltage of port i drives a current through the resistive part of its own link impedance, which damps the output voltage; for a purely inductive link ($\phi_{z,i}[n] = \pi/2$), $A_i = 0$.

$$D_3 = -\frac{1}{C_3}, \qquad D_4 = -\frac{1}{C_4}, \tag{3.41}$$

because the load current enters the capacitor dynamics of Eq. (3.16) directly as $-i_{\mathrm{load},i}/C_i$; the load current itself is given by Eq. (3.17), with $R_{\mathrm{load},3}$ and $R_{\mathrm{load},4}$ the resistive loads and $P_{\mathrm{CPL},3}$ and $P_{\mathrm{CPL},4}$ the CPLs. With $|Z[n]|$ in Ω, C_i in F, and ζ in rad, $[A_i] = \mathrm{s}^{-1}$, $[B_{ji}] = \mathrm{V\,s^{-1}\,rad^{-1}}$, and $[D_i] = \mathrm{F}^{-1}$, so that every term of Eq. (3.38) is in $\mathrm{V\,s^{-1}}$. Since the derivative of the sliding surface is set to zero and the references are constant, $\dot{\sigma}_i = \dot{V}_i = 0$ ($i \in \{3,4\}$), and Eq. (3.38) is rewritten as:

$$\begin{cases} 0 = A_3 V_3 + B_{13}\,\zeta_{13} + D_3\,i_{\mathrm{load},3}, \\ 0 = A_4 V_4 + B_{24}\,\zeta_{24} + D_4\,i_{\mathrm{load},4}. \end{cases} \tag{3.42}$$

Solving for the phase shifts and substituting $D_i = -1/C_i$ gives:

$$\begin{cases} \zeta_{13} = -\dfrac{A_3 V_3 + D_3\,i_{\mathrm{load},3}}{B_{13}} = \dfrac{i_{\mathrm{load},3}/C_3 - A_3 V_3}{B_{13}}, \\ \zeta_{24} = -\dfrac{A_4 V_4 + D_4\,i_{\mathrm{load},4}}{B_{24}} = \dfrac{i_{\mathrm{load},4}/C_4 - A_4 V_4}{B_{24}}, \end{cases} \tag{3.43}$$

where ζ_{13} and ζ_{24} are the phase shifts between ports 1 and 3 and between ports 2

and 4 of the QAB. Eq. (3.43) is the general harmonic form of the equivalent control: it shows that the required phase shift grows with the load current and is scaled by the sensitivity B_{13} or B_{24}. However, it requires the harmonic impedance sums and the operating-point phase shift $\zeta_{13,0}$ or $\zeta_{24,0}$ to be evaluated online, which is impractical in a real-time controller. For implementation, the averaged (fundamental-component) relation is therefore used instead. At the averaged level, the bridge current that port i receives from both source ports is $i_{Li} = \bar{I}_i\, d_i(1 - |d_i|)$ with $d_i = \zeta_i/\pi$, and $\dot{\sigma}_i = 0$ requires $i_{Li} = i_{\mathrm{load},i}$. Solving for the phase shift that delivers a commanded current u gives the current-to-phase map of Eq. (3.44), which inverts the averaged power-transfer characteristic exactly and needs only known parameters and measured voltages:

$$\Phi_i(u) = \operatorname{sign}(u)\,\frac{\pi}{2}\left(1 - \sqrt{1 - \frac{4|u|}{\bar{I}_i}}\right), \qquad \bar{I}_i = n\left(\frac{V_{\mathrm{in},1}}{2f_{\mathrm{sw}}L_{1i}} + \frac{V_{\mathrm{in},2}}{2f_{\mathrm{sw}}L_{2i}}\right), \tag{3.44}$$

where $n = N_p/N_s$ is the turns ratio, L_{1i} and L_{2i} are the link inductances between the source ports and port i, and $\bar{I}_i/4$ is the largest current that port i can receive ($|\zeta_i| = \pi/2$). The equivalent control laws are therefore given by:

$$\begin{cases} u_{13,\mathrm{eq}} = \Phi_3\big(i_{\mathrm{load},3}\big), \\ u_{24,\mathrm{eq}} = \Phi_4\big(i_{\mathrm{load},4}\big), \end{cases} \tag{3.45}$$

where $u_{13,\mathrm{eq}}$ and $u_{24,\mathrm{eq}}$ are the equivalent control laws, in radians, based on the load currents. Eqs. (3.42) and (3.43) are therefore not implemented directly; they are given for insight. Their role is to define the equivalent control as the phase shift that makes $\dot{\sigma}_i = 0$ in the averaged model of Eq. (3.38), and to show how this phase shift depends on the load current. Eq. (3.45) enforces the same condition through the averaged current-to-phase map. The averaged model of Eq. (3.38) is also used in the stability analysis of Section 3.8.3, where it defines the closed-loop sliding dynamics and the lumped uncertainty that the equivalent term leaves uncancelled.

Step 3 – Adaptive gains. A fixed-gain STSMC must use gains large enough for the worst-case disturbance, which causes unnecessary chattering and control effort during normal operation. The proposed ASTSMC therefore adjusts its gains to the size of the tracking error:

$$\begin{cases} k_1 = k_{1,\min} + \varrho_1 \, |\sigma_3|, \\ k_2 = k_{2,\min} + \varrho_2 \, |\sigma_4|, \\ k_3 = k_{3,\min} + \varrho_3 \, |\sigma_3|, \\ k_4 = k_{4,\min} + \varrho_4 \, |\sigma_4| \end{cases} \tag{3.46}$$

where $k_{i,\min}$ are the minimum gains, ϱ_1, ϱ_2, ϱ_3, and ϱ_4 are the adaptation rates, and σ_3 and σ_4 are the sliding surfaces. Eq. (3.46) is a state-dependent (algebraic) adaptation law rather than an integral law of the form $\dot{k}_i = \varrho_i|\sigma|$. This choice is deliberate: an integral law increases the gains monotonically as long as $\sigma \neq 0$, and since σ never becomes exactly zero in a sampled, switched converter, the gains would drift upward and amplify chattering. With Eq. (3.46), each gain rises in proportion to the instantaneous tracking error during a transient and returns to its minimum value $k_{i,\min}$ once the output voltage is regulated, so that $k_{i,\min} \leq k_i(t)$ always holds and the gains remain bounded whenever σ_3 and σ_4 are bounded. No bound on the disturbance appears in Eq. (3.46): $k_{i,\min}$ and ϱ_i are fixed design constants, and the Lyapunov analysis in Section 3.8.3 shows that, for any bounded disturbance, the sliding variables and all four gains remain bounded and the sliding variables converge in finite time to a residual set whose size decreases as ϱ_i increases. The resulting bounds of the adaptive gains (Step 7 of Section 3.8.3) are:

$$k_{j,\min} \leq k_j(t) \leq k_{j,\max} = k_{j,\min} + \varrho_j \, \bar{\sigma}_i, \qquad \bar{\sigma}_i = \max\{|\sigma_i(0)|, \; \bar{\varepsilon}_i\}, \qquad j \in \{1, 2, 3, 4\}, \tag{3.47}$$

where $i = 3$ for k_1 and k_3, $i = 4$ for k_2 and k_4, and $\bar{\varepsilon}_i$ is the residual set of Eq. (3.73). With the tuned values of Table 3.2 and the largest error of the tests ($\bar{\sigma}_i = 12$ V), the gains stay within $k_1, k_2 \in [0.047, \, 0.451]$ rad $\mathrm{V}^{-1/2}$ and $k_3, k_4 \in [23.1, \, 208]$ rad/s, and

the integral states of the super-twisting algorithm are limited to $|\nu_i| \le \bar{\nu}_i = 0.5$ rad by the anti-windup law of Eq. (3.52).

Step 4 – Adaptive super-twisting switching terms. The equivalent control stabilises the system by ensuring the nominal power transfer, but it cannot reject unmodelled dynamics, CPL changes, or load-estimation errors. This is the task of the ASTSMC switching terms of the paths $1 \leftrightarrow 3$ and $2 \leftrightarrow 4$, given by:

$$\begin{cases} u_{\mathrm{sw},13} = -k_1 \sqrt{|\sigma_3|}\, \mathrm{sgn}(\sigma_3) - \displaystyle\int_0^t k_3\, \mathrm{sgn}(\sigma_3)\, dt, \\ u_{\mathrm{sw},24} = -k_2 \sqrt{|\sigma_4|}\, \mathrm{sgn}(\sigma_4) - \displaystyle\int_0^t k_4\, \mathrm{sgn}(\sigma_4)\, dt \end{cases} \tag{3.48}$$

The first term, proportional to $\sqrt{|\sigma_i|}$, acts strongly when the voltage error is large and gently near $\sigma_i = 0$. The second term integrates $\mathrm{sgn}(\sigma_i)$; its output is therefore continuous even though $\mathrm{sgn}(\cdot)$ is discontinuous, and it builds up the correction needed to cancel slowly varying (Lipschitz) disturbances such as CPL steps, in the same way as an integral action. Together, the two terms drive both σ_i and $\dot{\sigma}_i$ to zero in finite time with a continuous control signal, which is why the super-twisting algorithm produces much less chattering than first-order SMC, whose discontinuous term acts directly on the command. The gains k_1 and k_2 (in $\mathrm{rad\,V^{-1/2}}$) set the proportional-like action, and k_3 and k_4 (in $\mathrm{rad\,s^{-1}}$) set the integral-like action; all four are adapted by Eq. (3.46). Fig. 3.6 illustrates the control diagram used for both the simulation and the SIL runs of the proposed controller. The ASTSMC combines a sliding surface, the super-twisting algorithm (STA), adaptive gains and the feedforward decoupler. The NLESO of Section 3.4.2 is reused to provide the load-current estimate needed by the equivalent term, and the same diagram also contains the SMC–NLESO benchmark controller.

Together, the sliding surfaces, the disturbance estimate and the saturation handling keep the loop stable and limit chattering.

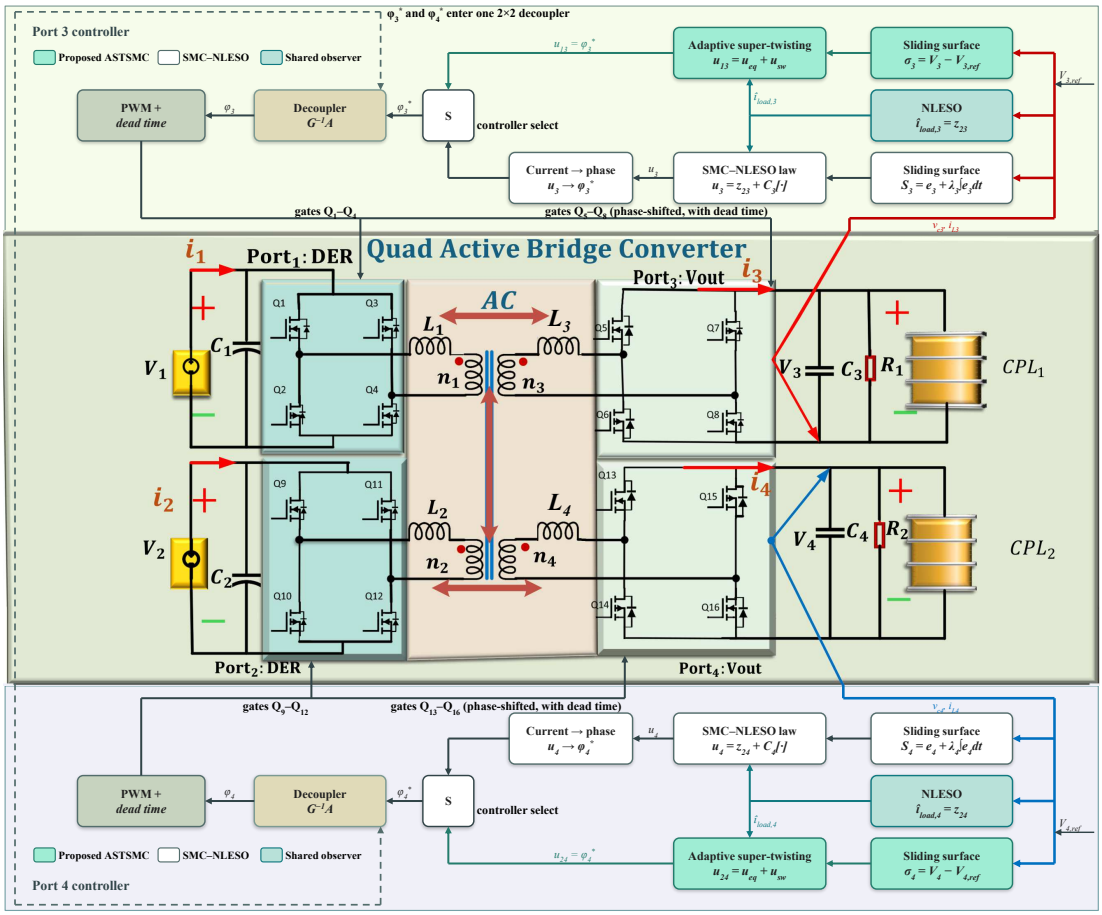


Figure 3.6: Control diagram of the QAB converter controllers.

Step 5 – Total command, boundary layer, and observer. The ASTSMC command is the sum of the equivalent and switching terms, based on Fig. 3.6, as given by:

$$\begin{cases} u_{13} = u_{13,\mathrm{eq}} + u_{\mathrm{sw},13}, \\ u_{24} = u_{24,\mathrm{eq}} + u_{\mathrm{sw},24}. \end{cases} \tag{3.49}$$

To mitigate chattering, the sign function is replaced by the saturation function:

$$\mathrm{sat}\left(\frac{\sigma_i}{\varepsilon_i}\right) = \begin{cases} +1, & \dfrac{\sigma_i}{\varepsilon_i} > 1, \\ \dfrac{\sigma_i}{\varepsilon_i}, & |\sigma_i| \le \varepsilon_i, \\ -1, & \dfrac{\sigma_i}{\varepsilon_i} < -1, \end{cases} \qquad i \in \{3, 4\}, \tag{3.50}$$

where σ_i is the sliding surface of port i and $\varepsilon_i > 0$ is the boundary-layer width: outside the layer ($|\sigma_i| > \varepsilon_i$) the function equals $\mathrm{sign}(\sigma_i)$, and inside it varies linearly, which removes the discontinuity that causes chattering. The final control law, Eq. (3.51), is obtained from Eq. (3.49) by evaluating the equivalent term with the observer estimate of the load current and replacing $\mathrm{sgn}(\sigma_i)$ by $\mathrm{sat}(\sigma_i/\varepsilon_i)$ by:

$$\begin{cases} u_{13} = \Phi_3\big(\hat{i}_{\mathrm{load},3}\big) - k_1\sqrt{|\sigma_3|}\,\mathrm{sat}\Big(\dfrac{\sigma_3}{\varepsilon_3}\Big) - \displaystyle\int_0^t k_3\,\mathrm{sat}\Big(\dfrac{\sigma_3(\tau)}{\varepsilon_3}\Big)\,d\tau, \\ u_{24} = \Phi_4\big(\hat{i}_{\mathrm{load},4}\big) - k_2\sqrt{|\sigma_4|}\,\mathrm{sat}\Big(\dfrac{\sigma_4}{\varepsilon_4}\Big) - \displaystyle\int_0^t k_4\,\mathrm{sat}\Big(\dfrac{\sigma_4(\tau)}{\varepsilon_4}\Big)\,d\tau, \end{cases} \tag{3.51}$$

where u_{13} and u_{24} are the final phase-shift commands, in radians, regulating the power flow between ports $1 \leftrightarrow 3$ and $2 \leftrightarrow 4$, respectively; $u_{13,\mathrm{eq}}$ and $u_{24,\mathrm{eq}}$ are the equivalent (feedforward) terms; $u_{\mathrm{sw},13}$ and $u_{\mathrm{sw},24}$ are the adaptive super-twisting switching terms; $k_1, k_2, k_3, k_4 > 0$ are the adaptive gains of Eq. (3.46); $\hat{i}_{\mathrm{load},3}$ and $\hat{i}_{\mathrm{load},4}$ are the load currents estimated by the NLESO of Eqs. (3.23) and (3.24), with the measured bridge current as its known input ($u_i = i_{Li}$, so that $d_i = i_{\mathrm{load},i}$); $\varepsilon_3, \varepsilon_4 > 0$ are the boundary-layer widths used to mitigate chattering; and Φ_3, Φ_4 are the current-to-phase maps of Eq. (3.44), which contain the link inductances, the turns ratio, and the input voltages $V_{\mathrm{in},1}$ and $V_{\mathrm{in},2}$.

The load-current estimate is limited to the rated current, $\hat{i}_{\mathrm{load},i} = \mathrm{sat}_{\pm I_{\max}}(z_{2i})$. The integral terms of Eq. (3.51) are the internal super-twisting states ν_3 and ν_4. They are implemented with conditional integration (anti-windup), so that they stay within the limits $\pm\bar{\nu}_i$ set by the admissible phase-shift range:

$$\dot{\nu}_i = \begin{cases} -k_i\,\mathrm{sat}\big(\sigma_i/\varepsilon_i\big), & |\nu_i| < \bar{\nu}_i \text{ or } \nu_i\,\mathrm{sat}\big(\sigma_i/\varepsilon_i\big) > 0, \\ 0, & \text{otherwise}, \end{cases} \qquad i \in \{3,4\}. \tag{3.52}$$

Integration stops only when ν_i is at its limit and would move further outward, so $|\nu_i(t)| \le \bar{\nu}_i$ for all t if $|\nu_i(0)| \le \bar{\nu}_i$; this property is used in the stability analysis (Section 3.8.3). The limit satisfies $\bar{\nu}_i \le \pi/2 - |u_{ji,\mathrm{eq}}|_{\max}$, so that the command of Eq. (3.51) stays within

$|\phi| \le \pi/2$; with $|u_{ji,\mathrm{eq}}|_{\max} = \Phi_i(I_{\max}) = 0.84$ rad for $I_{\max} = 60$ A, $\bar{\nu}_i = 0.5$ rad. For a bumpless start, $\nu_i(0) = \phi_i(0) - \Phi_i\big(\hat{i}_{\mathrm{load},i}(0)\big)$. The controller is executed once per switching period (forward Euler), and its output is applied in the following period.

3.6 Benchmark Controller: Cascaded Feedforward-Decoupled PID

A conventional PID controller with the feedforward decoupler of Section 3.4.7 is the linear benchmark of this chapter. For each output port $i \in \{3, 4\}$, it has an outer voltage loop and an inner current loop. The outer loop generates the reference of the bridge output current from the voltage error $e_i = v_{\mathrm{ref},i} - v_{c_i}$, with a lead–lag network on its proportional path, and the inner loop generates the phase-shift command from the current error:

$$\begin{aligned} i^*_{Li}(s) &= \Big[K^v_p\, G_{\mathrm{ll}}(s) + \frac{K^v_i}{s}\Big] e_i(s), \qquad |i^*_{Li}| \le I_{\max}, \\ u^{\mathrm{PID}}_{ji}(s) &= \Big[K^c_p + \frac{K^c_i}{s}\Big]\big(i^*_{Li}(s) - i_{Li}(s)\big), \qquad |u^{\mathrm{PID}}_{ji}| \le \phi_{\max}, \end{aligned} \tag{3.53}$$

with the unity-dc-gain lead–lag network:

$$G_{\mathrm{ll}}(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}, \qquad \omega_z < \omega_p, \tag{3.54}$$

where K^v_p, K^v_i and K^c_p, K^c_i are the proportional and integral gains of the voltage and current loops, i_{Li} is the measured bridge output current, and $(j, i) \in \{(1, 3), (2, 4)\}$; the derivative gains are zero. The integral of the outer loop is kept outside G_{ll}, so that in steady state its state equals the load current.

Inner (current) loop. The bridge current follows the phase shift according to $i_{Li} = \bar{I}_i d_i(1 - |d_i|)$ (Eq. (3.44)), so on the time scale of the control period the inner plant is the static gain:

$$b_i = \frac{\partial i_{Li}}{\partial \phi_i} = \frac{\bar{I}_i}{\pi}\big(1 - 2|d_i|\big), \tag{3.55}$$

which equals 78 A/rad at the nominal operating point. With the PI current controller, the closed current loop is approximately first order:

$$\frac{i_{Li}(s)}{i^{*}_{Li}(s)} = \frac{b_i(K^c_p s + K^c_i)}{(1 + b_i K^c_p)s + b_i K^c_i} \approx \frac{\omega_{ci}}{s + \omega_{ci}}, \qquad \omega_{ci} = \frac{b_i K^c_i}{1 + b_i K^c_p}. \tag{3.56}$$

Outer (voltage) loop. Linearising Eqs. (3.16) and (3.17) about the operating point gives the outer plant:

$$\frac{\Delta v_{c_i}(s)}{\Delta i_{Li}(s)} = \frac{1}{sC_i + G_{\mathrm{inc},i}}, \qquad G_{\mathrm{inc},i} = \frac{1}{R_{\mathrm{load},i}} - \frac{P_{\mathrm{CPL},i}}{v^2_{c_i}}, \tag{3.57}$$

where $G_{\mathrm{inc},i}$ is the incremental load conductance, 0.435 S at the nominal point; the CPL contributes its negative part. If the CPL share of the load grows until $G_{\mathrm{inc},i} < 0$ (above 1152 W per port at 48 V), the open-loop pole $-G_{\mathrm{inc},i}/C_i$ moves into the right half-plane, which is the CPL-induced instability that every controller must overcome. The outer loop gain is:

$$L_{v,i}(s) = \Big[K^v_p G_{\mathrm{ll}}(s) + \frac{K^v_i}{s}\Big] \frac{\omega_{ci}}{s + \omega_{ci}} \, \frac{1}{sC_i + G_{\mathrm{inc},i}}. \tag{3.58}$$

The lead–lag network gives its largest phase lead, 55° for $\omega_p = 10\,\omega_z$, at $\sqrt{\omega_z \omega_p}$. With the design gains $K^v_p = 0.45$ A/V, $K^v_i = 200$ A/(V s), $\omega_z = 2\pi \cdot 80$ rad/s, $\omega_p = 2\pi \cdot 800$ rad/s, $K^c_p = 0.001$ rad/A and $K^c_i = 45$ rad/(A s), the current loop has $\omega_{ci} \approx 2\pi \cdot 520$ rad/s and $L_{v,i}$ crosses over at about 56 Hz with a phase margin of about 105°, ten times below the current loop. These are the initial gains; the common tuning of Section 3.7.2 changed them (Table 3.2), and the margins of the tuned loops are given in Section 3.8.4. The controller is discretised with the Tustin transform at T_c, the inner integrator is frozen when its output would leave $|\phi| \le \phi_{\max}$, and the commands u^{PID}_{13} and u^{PID}_{24} pass through the decoupler of Eq. (3.32).

3.7 Simulation Results

3.7.1 Simulation Set-Up, Test Events and Performance Indices

Type of test. All results in this section come from simulation: a detailed switching model of the two-input/two-output QAB converter of Fig. 3.1, written in MATLAB. It contains the four full bridges with single-phase-shift modulation and a dead time of 200 ns, the four-winding transformer represented by its Y-equivalent model (Fig. 3.2) with winding resistances and magnetising inductance, and the output capacitors with resistive loads and CPLs. It is integrated with a fixed step of 51 ns (1400 steps per switching period). The three controllers are executed as on a digital controller: once per switching period, on period-averaged measurements, with a one-period delay. All three use the same decoupler, Eq. (3.32), and the same rated-current limit $I_{\max}$ = 60 A: the PID and the SMC–NLESO limit their current commands, and the ASTSMC limits its phase-shift command to $\Phi_i(I_{\max})$. The three controllers were also implemented in MATLAB/Simulink; with the same gains, the Simulink results agree with the switching model (identical steady state, transient voltage deviations within 0.5 percentage points). With 2 Ω and a 150 W CPL, each output port delivers about 1.3 kW at the nominal point (2.6 kW in total), which is of the same order as QAB converters that have been built and tested, e.g. the 1 kW prototype of [117] and the set-up of [122]. Table 3.2 lists all converter values and all controller gains.

Test events. The same test events were applied to all three controllers (Table 3.3), all starting from V_3 = V_4 = 48 V and V_1 = V_2 = 300 V. Scenarios S1–S3 contain the load, reference and input-voltage changes of the earlier version of this study, and the common test C combines one event of each type per port, so that every controller faces exactly the same sequence.

Power balance. The load currents of these operating points follow from Eq. (3.17).

Table 3.2: Converter values and controller gains.

Converter		**Controllers**	
Switching frequency, control period	14 kHz, 71.4 μs	NLESO: ω_o, α_1, α_2, $\delta_1 = \delta_2$	$2\pi \cdot 400$ rad/s, 0.75, 0.5, 0.5 V
Input voltages V_1, V_2	300 V (270–350 V)	ASTSMC: $k_{1,\min} = k_{2,\min}$	0.0470 (0.012) rad $\mathrm{V}^{-1/2}$
Output voltages V_3, V_4	48 V (48–80 V)	ASTSMC: $\varrho_1 = \varrho_2$	0.0336 (0.012) rad $\mathrm{V}^{-3/2}$
Turns ratio n (ports 3, 4)	$300/70 = 4.29$	ASTSMC: $k_{3,\min} = k_{4,\min}$	23.05 (3) rad/s
Leakage inductances L_1–L_4	75 μH	ASTSMC: $\varrho_3 = \varrho_4$	15.37 (2) rad $\mathrm{V}^{-1}\mathrm{s}^{-1}$
Link inductances L_{ij}, Eq. (3.3)	300 μH	ASTSMC: ε_i, $\bar{\nu}_i$	0.3 V, 0.5 rad
Winding resistance, magnetising inductance	20 mΩ, 5 mH	SMC–NLESO: λ_i	12.6 (150) s^{-1}
Output capacitors C_3, C_4	950 μF	SMC–NLESO: κ_i	4939 (900) s^{-1}
Resistive loads $R_{\mathrm{load},3}$, $R_{\mathrm{load},4}$	2 Ω	SMC–NLESO: γ_i	67.2 (800) V/s
CPLs $P_{\mathrm{CPL},3}$, $P_{\mathrm{CPL},4}$	150 W	PID: K_p^v, K_i^v	1.764 (0.45) A/V, 280 (200) A/(V s)
Dead time	200 ns	PID: K_p^c, K_i^c	0.001 rad/A, 31.5 (45) rad/(A s)
Phase-shift limit $\phi_{\max}$	1.52 rad	PID: ω_z, ω_p	$2\pi \cdot 80$, $2\pi \cdot 800$ rad/s
Model time step	51 ns	Current limit (all)	$I_{\max} = 60$ A

Tuned values; initial design values in brackets.

Table 3.3: Test events, the same for all controllers.

Test	**Events**
S1	$P_{\mathrm{CPL},3}$ 150→180 W (0.200 s); $R_{\mathrm{load},3}$ 2→1.6 Ω (0.283 s); $R_{\mathrm{load},4}$ 2→1.6 Ω (0.333 s); $R_{\mathrm{load},3}$ 1.6→2 Ω (0.433 s); $P_{\mathrm{CPL},4}$ 150→220 W (0.500 s); $R_{\mathrm{load},4}$ 1.6→2 Ω (0.533 s)
S2	$V_{4,\mathrm{ref}}$ 48→80 V (0.25 s); $V_{3,\mathrm{ref}}$ 48→60 V (0.30 s)
S3	V_1 300→350 V (0.30 s); V_2 300→350 V (0.50 s)
C	E1: $V_{3,\mathrm{ref}}$ 48→60 V (0.10 s); E2: $V_{4,\mathrm{ref}}$ 48→60 V (0.15 s); E3: $P_{\mathrm{CPL},3}$ 150→300 W (0.25 s); E4: $P_{\mathrm{CPL},4}$ 150→300 W (0.30 s); E5: V_1 300→330 V (0.40 s); E6: V_2 300→270 V (0.45 s); E7: $R_{\mathrm{load},3}$ 2→1.6 Ω (0.55 s); E8: $R_{\mathrm{load},4}$ 2→1.6 Ω (0.60 s)

Time of each event in brackets.

At 48 V, each output port supplies $48/2 = 24$ A to the resistive load and $150/48 = 3.1$ A to the CPL, i.e. 27.1 A and 1.30 kW. At 60 V the current is $30 + 2.5 = 32.5$ A (1.95 kW), and at 80 V (S2) it is $40 + 1.9 = 41.9$ A (3.35 kW). In the common test, the CPL step E3 raises the port-3 current at 60 V to $30 + 5 = 35.0$ A (2.10 kW), and the load step E7 to $37.5 + 5 = 42.5$ A (2.55 kW). All these currents are below the current limit of 60 A and

the capacity $\bar{I}_i/4 = 77$ A of Eq. (3.44), and in steady state the average bridge current equals the load current, because the capacitor current of Eq. (3.16) averages to zero.

Performance indices. Every index belongs to one event with a known time t_e, at one port, and is computed from the event until the next event (at most 50 ms) by a script from the saved simulation data. The switching ripple is first removed by averaging the output voltage over each switching period:

$$\bar{v}[k] = \frac{1}{T_c} \int_{(k-1)T_c}^{kT_c} v_c(t)\, dt. \tag{3.59}$$

For a reference step from V_a to V_b, with $\Delta V = V_b - V_a$, the response is scaled as $x(t) = (\bar{v}(t) - V_a)/\Delta V$, and the indices are:

$$t_r = t_{0.9} - t_{0.1}, \quad t_p = \min\{t \geq t_e :\ x(t) \geq p\}, \qquad \mathrm{OS} = \max_t \frac{\bar{v}(t) - V_b}{\Delta V} \times 100\%, \tag{3.60}$$

where t_r is the rise (or fall) time and OS the overshoot in percent of the step. After a load, CPL or input-voltage change, when the reference stays at V_{ref}, the peak deviation is:

$$M_{\mathrm{dev}} = \max_t \frac{|\bar{v}(t) - V_{\mathrm{ref}}|}{V_{\mathrm{ref}}} \times 100\%. \tag{3.61}$$

The settling (or recovery) time is found by searching backwards from the end of the window for the last moment outside the $\pm 1\%$ band:

$$t_s = \max\{t \geq t_e :\ |\bar{v}(t) - V_{\mathrm{ref}}| > 0.01\, V_{\mathrm{ref}}\} + T_c - t_e, \tag{3.62}$$

with $t_s = 0$ if the voltage never leaves the band. The total error is $\mathrm{IAE} = \sum_k |V_{\mathrm{ref}}[k] - \bar{v}[k]|\, T_c$; the cross-coupling is the largest change of the other port's voltage during a reference step; and the steady-state control activity Δu is the standard deviation of the change of the phase-shift command from one period to the next. Every reported index was checked against four rules: nothing rises or settles faster than one control period, and nothing settles before it rises ($T_c \leq t_{0.1} < t_{0.9} \leq t_s$); overshoots and deviations are a few percent, never near 100%; the steady state satisfies the power balance above; and controllers are compared only for the same event, port and starting point.

3.7.2 Common Tuning of the Controllers

The initial gains of the three controllers follow different design rules: loop shaping for the PID (Section 3.6), the reaching condition for the SMC–NLESO (Section 3.8.2) and the Lyapunov conditions for the ASTSMC (Section 3.8.3). So that no controller is helped or hurt by its gains, all three were tuned again by the same procedure, with the same effort and the same rules:

1. *Tuning tests:* the common test C, the 32 V reference step of S2, and a reverse-power step in which port 4 changes from $2\ \Omega$ and 150 W to a 600 W source and back.
2. *Score to minimise* (lower is better): the total voltage error plus a penalty for the movement of the control signal,

$$J = \sum_{j} \mathrm{IAE}_j + \lambda_u \, \Delta u, \qquad \lambda_u = 0.5 \text{ mV s per mdeg}, \tag{3.63}$$

   where IAE_j is the IAE of tuning event j in mV s and Δu the steady-state control activity in millidegrees.
3. *Rules:* an overshoot of at most 5% on every reference step and a peak bridge current of at most 66 A ($I_{\max} + 10\%$). A stable gain set that breaks a rule receives the penalty $10^4 + 10^3 v$, where v is the size of the violation, so that every set that keeps the rules is preferred to every set that breaks them; an unstable set is rejected.
4. *Search:* three main gains per controller, multiplied by 0.5, 1 or 2 (27 sets) around the design values, then by 0.7, 1 or 1.4 around the best set, until the best set lies inside the searched range (at most six rounds).

Table 3.4 gives the result. The initial gains of the SMC–NLESO broke the overshoot rule (14% on the reference steps). The tuning reduced the score of the PID by 34% and that of the ASTSMC by 42%, and all tuned controllers keep both rules. The tuned ASTSMC has the lowest score, $J = 77.6$, followed by the SMC–NLESO (130.9) and

the PID (525.9).

Table 3.4: Result of the common tuning.

Controller	**Gain sets tried**	J **before**	J **after**	**Overshoot (%)**	**Peak current (A)**
PID	108	790.3	525.9	3.2	51.8
SMC–NLESO	162	broke the rules	130.9	1.3	64.1
ASTSMC	162	133.6	**77.6**	4.5	64.1

3.7.3 Scenarios S1–S3: Load, Reference and Input-Voltage Changes

Fig. 3.7 shows the output voltage of the affected port from 2 ms before to 30 ms after each of the ten events of S1–S3.

S1: load and CPL changes (panels (a)–(f)). The resistive-load steps are the most demanding events. For the $2 \rightarrow 1.6\ \Omega$ step at port 3, the voltage dip is 4.1% with the PID controller (recovery in 14.9 ms), 2.6% with the SMC–NLESO (1.1 ms) and 2.3% with the ASTSMC (0.6 ms). The ASTSMC also gives the smallest and the PID the largest deviation for the load step at port 4 and for the load removals at 0.433 and 0.533 s. The CPL steps of 30 W and 70 W cause dips of at most 1.1% (PID) and below 0.7% for the other two controllers, and a change at one port leaves the voltage of the other port within 0.12 V for all controllers.

S2: reference changes (panels (g), (h)). For the 32 V step at port 4, the ASTSMC settles within 2.1 ms with an overshoot of 0.8%, against 2.4 ms (SMC–NLESO, 1.0%) and 14.3 ms (PID, 3.2%). For the 12 V step at port 3, the settling times are 1.1 ms (ASTSMC, 4.5% overshoot), 1.2 ms (SMC–NLESO) and 6.1 ms (PID). The cross-coupling into the other port is at most 0.25 V for all controllers. During the 32 V step, the ASTSMC and the SMC–NLESO drive the phase shift to the limit that corresponds to $I_{\max}$ (41°) and their bridge currents peak at 62 A, while the PID current stays below 52 A. The peaks exceed $I_{\max}$ by up to 4 A because the limit acts on the command of the two source links, while the 3–4 link carries additional current during the step; they

stay within the 66 A rule of the tuning.

S3: input-voltage changes (panels (i), (j)). Since both source links feed each output port, each step disturbs both outputs. The deviations stay small: 0.77–0.85% for the ASTSMC and the SMC–NLESO and 0.91–0.94% for the PID, with recovery within 0.4 ms. The input voltages enter the current-to-phase map of Eq. (3.44) directly, so the SMC–NLESO and the ASTSMC, which use it, compensate the input-voltage change immediately.

3.7.4 Common Test C

Fig. 3.8 shows the response of the three controllers to the eight events of the common test C at the port that each event affects, and Table 3.5 gives the indices for the events at port 3 (the results for port 4 are similar). For the reference step E1, the ASTSMC gives the shortest settling time (1.14 ms, 16 control periods) and the smallest IAE (6.1 mV s), with an overshoot of 4.4%, within the 5% rule; the SMC–NLESO settles in 1.50 ms with the smallest overshoot (0.9%), and the PID needs 6.00 ms. For the resistive-load step E7, the ASTSMC gives the smallest dip (2.33%) and the fastest recovery (0.79 ms), against 2.61% and 1.21 ms for the SMC–NLESO and 4.06% and 14.86 ms for the PID. The CPL step E3 is handled almost equally well by the two SMC-based controllers (dips of 0.79 and 0.83%, the SMC–NLESO being slightly better), whose voltages do not leave the $\pm 1\%$ band, whereas the PID dips by 1.48% and needs 8.0 ms to recover. After the input-voltage step E5, the SMC–NLESO deviates least (0.40%), followed by the ASTSMC (0.46%) and the PID (0.56%). The cross-coupling into the other port stays below 0.2 V for all controllers.

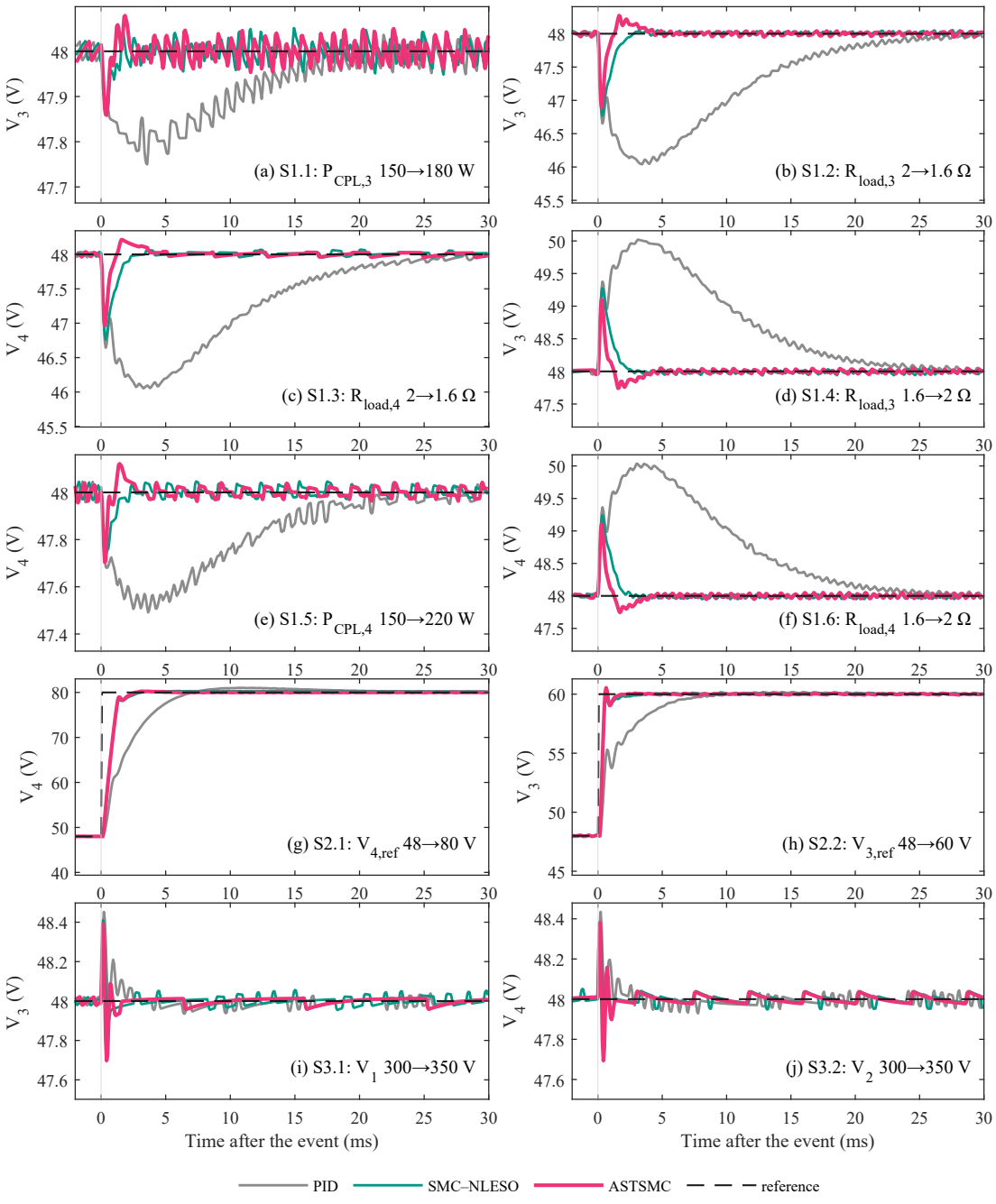


Figure 3.7: Output voltage after the events of scenarios S1–S3.

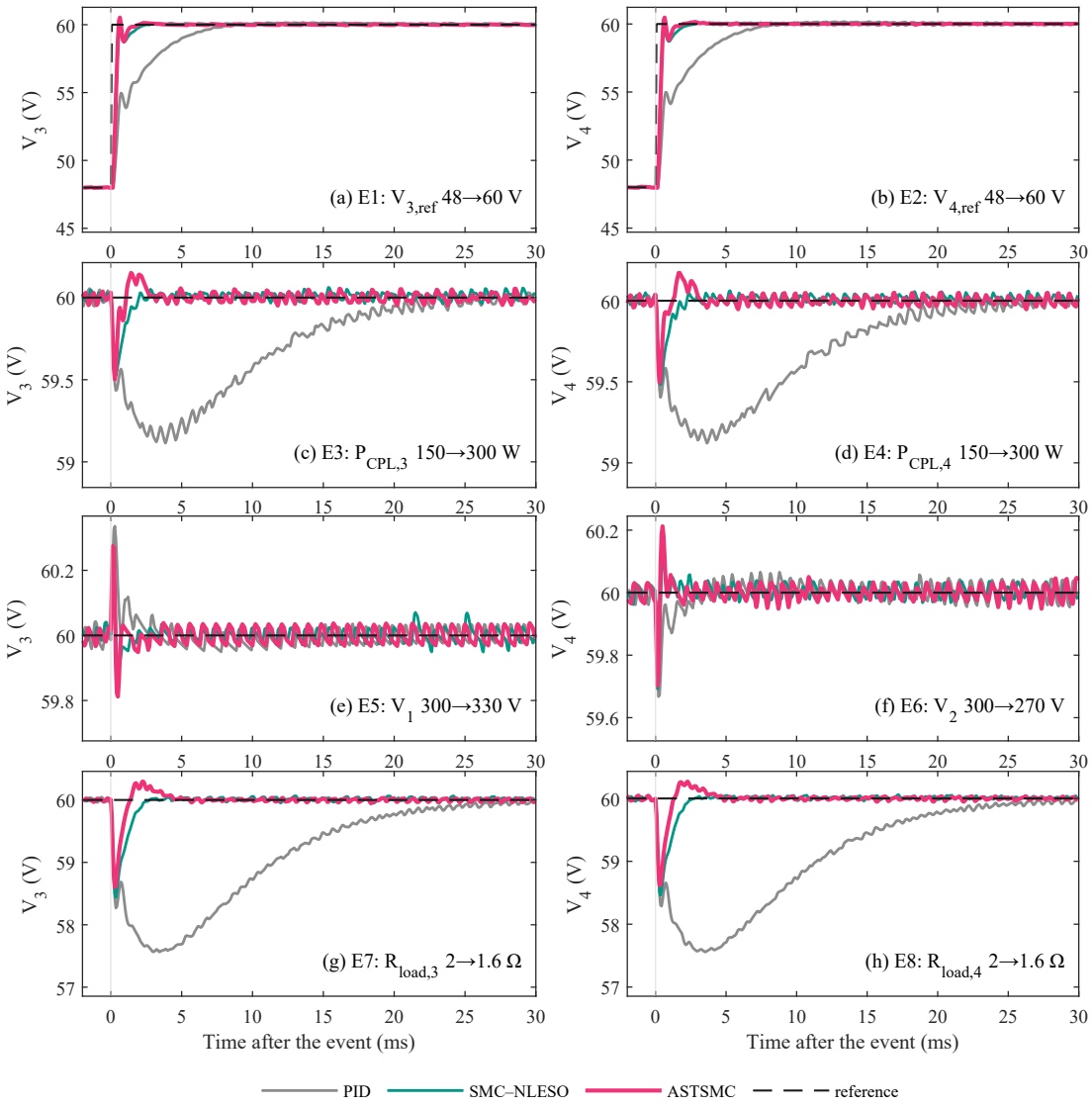


Figure 3.8: Common test C: output voltage after each event.

Table 3.5: Performance indices of test C at port 3.

	E1: $V_{3,\mathrm{ref}}$ **48→60 V**				**E3: CPL 150→300 W**		**E5:** V_1	**E7:** R **2→1.6 Ω**	
Controller	t_s (ms)	OS (%)	IAE (mV s)	other port (V)	dev. (%)	t_r (ms)	dev. (%)	dev. (%)	t_r (ms)
PID	6.00	1.32	23.3	**0.07**	1.48	8.00	0.56	4.06	14.86
SMC–NLESO	1.50	**0.87**	7.9	0.14	**0.79**	0	**0.40**	2.61	1.21
ASTSMC	**1.14**	4.38	**6.1**	0.19	0.83	0	0.46	**2.33**	**0.79**

Tuned gains. t_s: settling time; OS: overshoot; dev.: peak deviation; t_r: recovery time (0 if the voltage stayed in the ±1% band).

3.7.5 Bridge Currents, Control Inputs and Steady State

Figs. 3.9 and 3.10 show the bridge output current and the applied phase shift of the affected port after the same eight events. The currents settle at the values of the power balance after every event (32.5, 35.0 and 42.5 A at port 3), with transient deviations of at most 3.0 A from the new value for the CPL, input-voltage and load steps. Because the load sets the current, the three current waveforms differ only during the transients. The reference steps E1 and E2 produce the largest current peaks with the ASTSMC and the SMC–NLESO (62–64 A), which use the full rated current to reach the new voltage quickly. After an input-voltage rise (E5), the phase shift settles at a lower value, because a higher input voltage raises $\bar{I}_i$ in Eq. (3.44) and the same current is delivered with a smaller phase shift.

In steady state, before the first event, the output ripple (0.46 V peak-to-peak, set by the switching ripple) and the steady-state error (11 mV) are the same for all three controllers. The control activity Δu, which is the controller-induced oscillation discussed in Section 3.8.6, is 12.9 mdeg for the ASTSMC, against 40.7 mdeg for the PID and 53.0 mdeg for the SMC–NLESO, i.e. about four times larger than that of the ASTSMC.

3.7.6 Robustness Tests

To test the controllers beyond the scenarios above, further tests were run with the tuned gains and the same conditions: the largest CPL that each controller stabilises, at nominal values and with the link inductances or output capacitances $\pm 20\%$ off their nominal values (controller model unchanged); dead times from 51 to 816 ns; reverse power flow; pulsed CPLs; sensor noise and a computation delay of two control periods; simultaneous disturbances with unequal loads; a 100 Hz ripple and a ramp of the input voltages; start-up from 1 V; and a Monte Carlo study with 100 converters. In the Monte Carlo study, the leakage inductances L_1–L_4 and the output capacitances C_3 and C_4

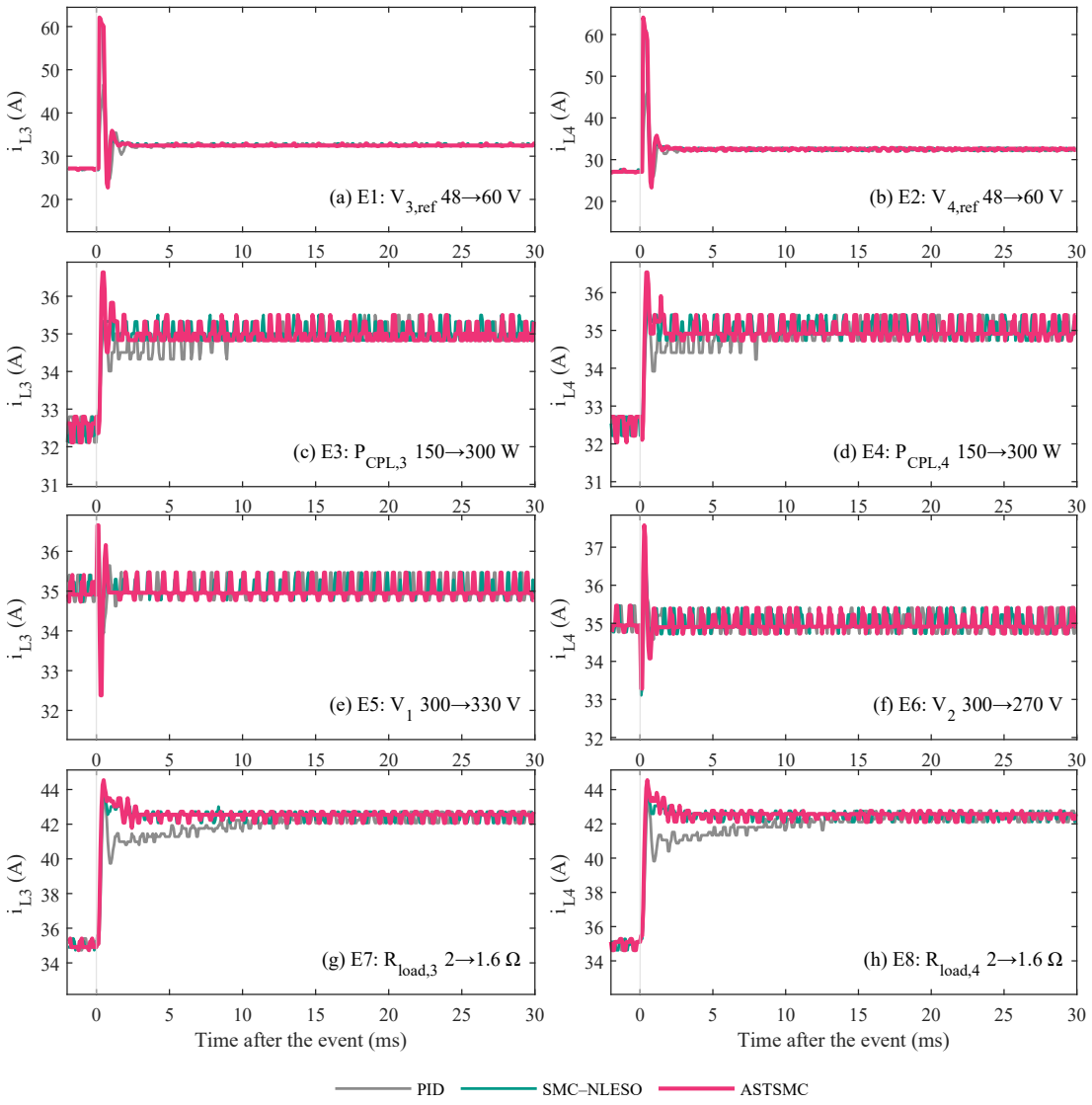


Figure 3.9: Common test C: bridge output current after each event.

were multiplied by random factors between 0.8 and 1.2, the turns ratios of ports 3 and 4 between 0.95 and 1.05, and the winding resistances between 0.5 and 2, with a fixed random seed, so that all controllers, with the nominal model and the tuned gains, were tested on the same 100 converters, each with the complete common test C. A run counted as stable if all voltages stayed finite and below 120 V, the affected voltage returned to the $\pm 1\%$ band within 50 ms after every event, and the port-3 voltage ended within 1 V of its reference. The sensor noise was added only to the measurements that

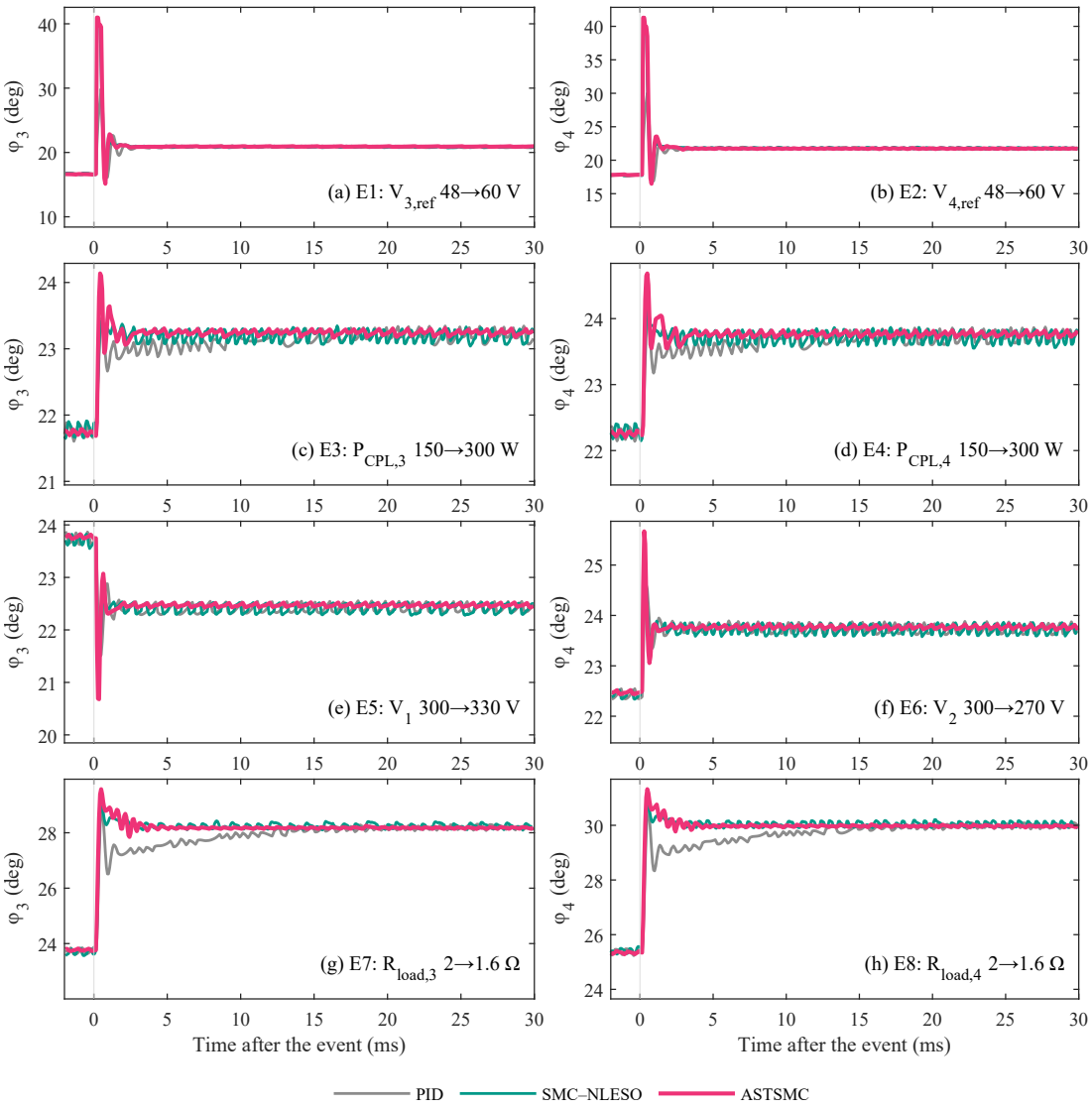


Figure 3.10: Common test C: applied phase shift after each event.

the controllers receive (standard deviation 0.1 V on the output voltages and 0.5 A on the bridge currents, new at every control period, the same noise for every controller).

Table 3.6 summarises the results (best value of each row in bold). The ASTSMC has the smallest error under reverse power flow, pulsed CPLs, simultaneous disturbances and start-up, the smallest load-step dip at every dead time and, in the Monte Carlo study, the smallest median load-step dip, and it shares the largest stable CPL (1500 W per port at nominal values) with the SMC–NLESO. Fig. 3.11 shows the largest CPL per

port that each controller stabilises; in the shaded band between the open-loop limit (G_{inc} = 0, 1152 W) and the rated-current limit (1728 W), the open loop is unstable and only the controller keeps the port stable. All controllers stabilise CPLs well above the open-loop limit, and all were stable in all 100 Monte Carlo converters. The dead time hardly affects any controller: with symmetric dead time, the even harmonics of the winding current stay at 0.015–0.017% of the odd content for every controller and every dead time, and a mismatch of 51 or 102 ns between the half-cycles raises them to 0.32–0.33%, which confirms the result of Section 3.3.3 in closed loop.

Table 3.6: Robustness tests with the tuned gains.

Test and index	**PID**	**SMC–NLESO**	**ASTSMC**
Largest stable CPL per port, nominal values (W)	1350	**1500**	**1500**
Largest stable CPL per port, link inductances +20% (W)	**1350**	1200	1200
Load-step dip at dead times of 51–816 ns (%)	4.1	2.6	**2.3**
Reverse power flow: largest error (V)	14.76	9.01	**7.46**
Pulsed CPL 150–600 W, 50 Hz: largest error (V)	2.57	1.47	**0.91**
Simultaneous disturbances, unequal loads: largest error (V)	2.20	1.39	**1.26**
Input-voltage ripple and ramp: largest error (V)	0.093	**0.048**	0.067
Start-up from 1 V: RMS error (V)	3.34	2.19	**2.17**
Sensor noise: largest error (V)	0.26	**0.17**	0.27
Two-period computation delay: largest error (V)	3.11	**0.06**	0.52
Monte Carlo, 100 converters: number stable	100	100	100
Monte Carlo: median load-step dip (%)	4.08	2.58	**2.35**
Monte Carlo: largest overshoot (%)	**2.0**	9.5	21.2

Best value in bold.

In the reverse-power test, port 4 and then port 3 became 600 W sources, so that the bridge current and the phase shift of each port changed sign (to about -3.7°), and finally both ports returned to forward operation. All three controllers stayed stable through both zero crossings, which confirms the bidirectional power flow of Eq. (3.1) in closed loop. The ASTSMC kept the voltage closest to its reference, but it returned to the $\pm 1\%$ band more slowly (5.0 ms) than the SMC–NLESO (3.3 ms), drew the highest peak current (53.8 A) and transferred the largest disturbance into the other port (0.94 V when port 4 reversed).

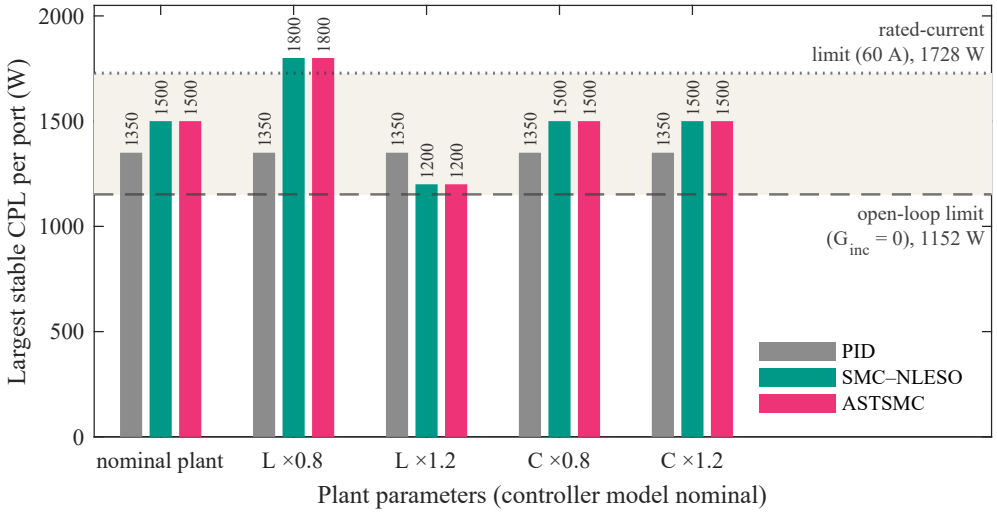


Figure 3.11: Largest stable CPL per port.

Limitations of the ASTSMC found by these tests. (i) With a computation delay of two control periods, its error rose to 0.52 V, against 0.06 V for the SMC–NLESO, while the PID oscillated with 3.1 V; the adaptive gains, which grow with the error, make the sampled loop more sensitive to extra delay. (ii) It is slightly more sensitive to sensor noise than the SMC–NLESO. (iii) Like the SMC–NLESO, it uses the full rated current during large transients. (iv) Its overshoot varies most with the plant values (median 4.5%, up to 21% in the worst of the 100 converters). (v) When it was tuned on the forward-power cases only and without the overshoot rule, its adaptation rate ϱ_1 grew to 0.066 rad $\mathrm{V}^{-3/2}$; the large gain produced by a reverse-power step then made the sampled loop oscillate, and 2 of the 100 Monte Carlo converters were unstable. Tuning over the whole operating range, as in Section 3.7.2, removed both effects, which shows that ϱ_i must be chosen with the computation delay and the whole operating range in mind.

3.8 Stability Analysis

This section establishes the stability of each closed loop and checks it against the simulation: the NLESO estimation error, on which both SMC-based controllers rely;

the reaching condition of the SMC–NLESO; the Lyapunov analysis of the ASTSMC; the margins of the PID controller; and the check of every result against the switching simulation with the tuned gains.

3.8.1 Convergence of the NLESO Estimation Error

In the linear band of $\mathrm{fal}(\cdot)$, the estimation errors obey Eq. (3.25), whose two poles are placed at $-\omega_o$ (Section 3.4.2). The error system is therefore exponentially stable, and its forced response to the disturbance rate $\dot{d}_i$ is bounded. Setting the derivatives in Eq. (3.25) to zero for a constant disturbance rate gives the steady-state errors:

$$\tilde{v}_i = -\frac{\dot{d}_i}{C_i\,\omega_o^2}, \qquad \tilde{d}_i = \frac{2\,\dot{d}_i}{\omega_o}, \tag{3.64}$$

so a constant disturbance ($\dot{d}_i = 0$) is estimated without error, a ramp is tracked with the lag $2\dot{d}_i/\omega_o$, and a step is recovered with the time constant $1/\omega_o = 0.4$ ms. Outside the linear band, $\alpha_j < 1$ lowers the observer gain for large errors, which limits peaking without changing the equilibrium. In the simulations, the load-current estimate of the ASTSMC has a steady-state error of 0.016 A RMS (0.048 A peak) against a load current of 27–43 A.

3.8.2 Reaching Condition of the SMC–NLESO

The closed-loop sliding dynamics of the SMC–NLESO are given by Eq. (3.29). The coupling from the other port changes the delivered bridge current i_{Li} and is therefore part of the total disturbance d_i of Eq. (3.20); it is estimated by the NLESO, and only its estimation error $\tilde{d}_i$ enters Eq. (3.29). With $V_i = \frac{1}{2}S_i^2$, the sliding surface is reached in finite time if the switching gain satisfies:

$$\gamma_i > \frac{1}{C_i}\sup_t |\tilde{d}_i(t)|. \tag{3.65}$$

Without the observer, the switching gain would have to cover the whole load current (about 27 A at the nominal point), i.e. $\gamma_i > 2.8 \times 10^4$ V/s. The tuned gains (Table 3.2) take the opposite approach: a small switching gain, $\gamma_i = 67.2$ V/s ($C_i\gamma_i = 0.064$ A), with a large proportional gain, $\kappa_i = 4939$ s^{-1}. With these gains Eq. (3.65) is not met most of the time, and the closed loop relies on the following bound: whenever $|\tilde{d}_i| \le \bar{d}_i$,

$$\frac{d}{dt}\Big(\frac{1}{2}S_i^2\Big) \le |S_i|\Big(\frac{\bar{d}_i}{C_i} - \gamma_i\Big) - \kappa_i S_i^2 < 0 \quad \text{for} \quad |S_i| > \bar{S}_i := \frac{\max\{0,\ \bar{d}_i/C_i - \gamma_i\}}{\kappa_i}, \tag{3.66}$$

so S_i stays bounded even while Eq. (3.65) is violated; the proportional term $\kappa_i S_i$ of the reaching law guarantees this bound. With the observer error found in the simulations ($\bar{d}_i = 0.40$ A in steady state and 8.0 A at most after an event), Eq. (3.66) gives $\bar{S}_i = 0.071$ V in steady state and 1.69 V after the largest events, which the simulation confirms (0.052–0.070 V and 1.57 V, Section 3.8.5). On the sliding surface, $S_i = 0$ gives $\dot{e}_i = -\lambda_i e_i$, so the tracking error decays with the time constant $1/\lambda_i$. Because the sign term is evaluated once per control period and acts with one period of delay, S_i chatters in a band whose width is of the order of a few $\gamma_i T_c$ ($\gamma_i T_c = 4.8$ mV). The tuned SMC–NLESO is therefore practically stable, with an ultimate bound set by κ_i rather than by γ_i.

3.8.3 Lyapunov Analysis of the ASTSMC

The analysis starts from the final control law, Eq. (3.51), and is written for port $i \in \{3, 4\}$ with its source port j, $(j, i) \in \{(1, 3), (2, 4)\}$; as in Eq. (3.46), k_{i-2} and k_i are the proportional and integral super-twisting gains of port i.

Step 1: closed-loop sliding dynamics. For a constant reference, Eqs. (3.33) and (3.16) give $\dot{\sigma}_i = \dot{V}_i = (i_{Li} - i_{\mathrm{load},i})/C_i$, where the bridge current is set by the command through the current-to-phase map, Eq. (3.44). With the integral state ν_i of Eq. (3.52), the open

loop and the command are:

$$\begin{aligned}\dot{\sigma}_i &= \frac{1}{C_i}\Big[i_{Li}\big(u_{ji}\big) - i_{\mathrm{load},i}\Big], \qquad u_{ji} = \Phi_i\big(\hat{i}_{\mathrm{load},i}\big) + s_i,\\ s_i &= -k_{i-2}\sqrt{|\sigma_i|}\,\mathrm{sat}(\sigma_i/\varepsilon_i) + \nu_i.\end{aligned} \tag{3.67}$$

Because Φ_i is the exact inverse of the bridge-current relation, the feedforward part delivers the estimated load current, $i_{Li}\big(\Phi_i(\hat{i}_{\mathrm{load},i})\big) = \hat{i}_{\mathrm{load},i}$, and by the mean-value theorem the switching part adds $\tilde{b}_i s_i$, where $\tilde{b}_i = \partial i_{Li}/\partial\phi$ of Eq. (3.55) is evaluated between $\Phi_i(\hat{i}_{\mathrm{load},i})$ and u_{ji}. With $\dot{\nu}_i = -k_i\,\mathrm{sat}(\sigma_i/\varepsilon_i)$, the closed-loop error dynamics of both ports are:

$$\begin{aligned}\dot{\sigma}_i &= \mathcal{B}_{ji}\Big(-k_{i-2}\sqrt{|\sigma_i|}\,\mathrm{sat}\Big(\frac{\sigma_i}{\varepsilon_i}\Big) + \nu_i\Big) + \Delta_i,\\ \dot{\nu}_i &= -k_i\,\mathrm{sat}\Big(\frac{\sigma_i}{\varepsilon_i}\Big), \qquad \mathcal{B}_{ji} = \frac{\tilde{b}_i}{C_i},\end{aligned} \tag{3.68}$$

where $\Delta_i = (\hat{i}_{\mathrm{load},i} - i_{\mathrm{load},i})/C_i + \delta_i$ is the lumped uncertainty, and δ_i collects the residual model error of the current-to-phase map (dead time, losses, the residual coupling left by the decoupler of Eq. (3.32)) and the parameter mismatch. The load-estimation part of Δ_i is bounded because the NLESO error dynamics are exponentially stable (Section 3.8.1). Every part of u_{ji} appears in the closed loop: the feedforward cancels the load current up to the estimation error in Δ_i, the proportional super-twisting term appears directly, and the integral term appears as the state ν_i. The incremental sensitivity $\mathcal{B}_{ji} = (\bar{I}_i/\pi C_i)(1 - 2|d_i|)$ is a different quantity from the coefficient B_{ji} of the averaged model, Eq. (3.40); it is positive but varies with the operating point, and for $|i_{Li}| \le I_{\max}$ and $V_1, V_2 \in [270, 350]$ V it lies in $[\mathcal{B}_{\min}, \mathcal{B}_{\max}] = [3.3\times10^4,\ 1.2\times10^5]$ V s^{-1}rad^{-1}.

Step 2: Lyapunov function. The Lyapunov candidate is a function of the sliding variables only; the control law enters through its derivative along the closed loop:

$$\mathcal{V} = \frac{1}{2}\sigma_3^2 + \frac{1}{2}\sigma_4^2, \qquad \dot{\mathcal{V}} = \sigma_3\dot{\sigma}_3 + \sigma_4\dot{\sigma}_4. \tag{3.69}$$

Step 3: bound outside the boundary layer. Substituting Eq. (3.68) and writing $\sigma_i\sqrt{|\sigma_i|} = |\sigma_i|^{3/2}\,\mathrm{sign}(\sigma_i)$ gives, for each port, the terms $-\mathcal{B}_{ji}k_{i-2}|\sigma_i|^{3/2}\,\mathrm{sat}(\sigma_i/\varepsilon_i)\,\mathrm{sign}(\sigma_i)+$

$\mathcal{B}_{ji}\sigma_i\nu_i+\sigma_i\Delta_i$. For $|\sigma_i| > \varepsilon_i$, $\mathrm{sat}(\sigma_i/\varepsilon_i) = \mathrm{sign}(\sigma_i)$, so the first term equals $-\mathcal{B}_{ji}k_{i-2}|\sigma_i|^{3/2} \le -\mathcal{B}_{\min}k_{i-2}|\sigma_i|^{3/2}$, and the other two are bounded by $|\sigma_i|\big(\mathcal{B}_{\max}|\nu_i| + |\Delta_i|\big) \le \Gamma_i|\sigma_i|$. The positive constants Γ_i, e.g. $\Gamma_i = \mathcal{B}_{\max}\bar{\nu}_i + \bar{\Delta}_i$ with $|\Delta_i| \le \bar{\Delta}_i$, are used only in the analysis and need not be known to implement the controller. The internal states are bounded, $|\nu_i| \le \bar{\nu}_i$, because of the anti-windup law of Eq. (3.52). Therefore:

$$\dot{\mathcal{V}} \le \sum_{i\in\{3,4\}} \Big(-\mathcal{B}_{\min}k_{i-2}|\sigma_i|^{3/2} + \Gamma_i|\sigma_i|\Big), \tag{3.70}$$

in which $-\mathcal{B}_{\min}k_{i-2}|\sigma_i|^{3/2}$ are the stabilising super-twisting terms and $\Gamma_i|\sigma_i|$ the effects of the integral action and of the bounded uncertainties.

Step 4: gain condition per port. The right-hand side of Eq. (3.70) is the sum of two decoupled terms, $\dot{\mathcal{V}} = \dot{\mathcal{V}}_3 + \dot{\mathcal{V}}_4$ with $\mathcal{V}_i = \frac{1}{2}\sigma_i^2$, each involving only its own sliding variable. Substituting the adaptive gains of Eq. (3.46) gives, for $|\sigma_i| > \varepsilon_i$, an explicit gain condition for each port:

$$\dot{\mathcal{V}}_i \le -|\sigma_i|\Big[\underbrace{\mathcal{B}_{\min}\big(k_{i-2,\min} + \varrho_{i-2}|\sigma_i|\big)\sqrt{|\sigma_i|}}_{g_i(|\sigma_i|)} - \Gamma_i\Big]. \tag{3.71}$$

Step 5: size of the residual set. The function $g_i(s)$ is continuous, strictly increasing and unbounded for $s \ge 0$, with $g_i(0) = 0$, so $g_i(\mu_i) = \Gamma_i$ has a unique positive root μ_i. Since $g_i(s) \ge \mathcal{B}_{\min}k_{i-2,\min}\sqrt{s}$ and $g_i(s) \ge \mathcal{B}_{\min}\varrho_{i-2}s^{3/2}$, the root satisfies:

$$\mu_i \le \min\Big\{\big(\Gamma_i/(\mathcal{B}_{\min}k_{i-2,\min})\big)^2,\ \big(\Gamma_i/(\mathcal{B}_{\min}\varrho_{i-2})\big)^{2/3}\Big\}. \tag{3.72}$$

For $|\sigma_i| > \mu_i$, $g_i(|\sigma_i|) > \Gamma_i$, so the bracket of Eq. (3.71) is positive, and:

$$\dot{\mathcal{V}}_i < 0 \quad \text{whenever} \quad |\sigma_i| > \bar{\varepsilon}_i := \max\{\varepsilon_i,\ \mu_i\}, \qquad i \in \{3,4\}. \tag{3.73}$$

Because the two conditions are decoupled, each sliding variable is attracted separately to its own residual set; it is not enough for only one of them to lie outside its boundary layer.

Step 6: finite-time convergence. For any margin $\eta_i > 0$, let μ_i^η be the root of $g_i(\mu) = \Gamma_i + \eta_i$. Whenever $|\sigma_i| \ge \max\{\varepsilon_i, \mu_i^\eta\}$, the bracket of Eq. (3.71) is at least η_i,

so $\frac{d}{dt}|\sigma_i| = \dot{\mathcal{V}}_i/|\sigma_i| \le -\eta_i$, and σ_i enters this set within the finite time $T_i \le |\sigma_i(0)|/\eta_i$ and stays in it. Since η_i is arbitrary, the sliding variables reach any neighbourhood of the residual set in finite time and converge to the set itself:

$$|\sigma_i| \le \bar{\varepsilon}_i, \qquad i \in \{3, 4\}. \tag{3.74}$$

Step 7: bounded adaptive gains. Since $\dot{\mathcal{V}}_i < 0$ outside the residual set, $|\sigma_i(t)|$ never exceeds $\bar{\sigma}_i := \max\{|\sigma_i(0)|,\ \bar{\varepsilon}_i\}$, and substituting this bound into Eq. (3.46) gives, for all $t \ge 0$:

$$\begin{aligned} k_{1,\min} \le k_1 \le k_{1,\min} + \varrho_1\bar{\sigma}_3, \quad k_{3,\min} \le k_3 \le k_{3,\min} + \varrho_3\bar{\sigma}_3, \\ k_{2,\min} \le k_2 \le k_{2,\min} + \varrho_2\bar{\sigma}_4, \quad k_{4,\min} \le k_4 \le k_{4,\min} + \varrho_4\bar{\sigma}_4, \end{aligned} \tag{3.75}$$

and after the reaching time the upper bounds reduce to $k_{j,\min} + \varrho_j\bar{\varepsilon}_i$. Because Eq. (3.46) is algebraic, the gains cannot drift upward once the error has decayed.

Role of the unknown disturbance bound. Γ_i does not appear in the control law; it enters only through μ_i in Eq. (3.72). If the disturbance is larger than expected, the term $\mathcal{B}_{\min}\varrho_{i-2}|\sigma_i|^{3/2}$ of Eq. (3.71) grows with the tracking error until it dominates Γ_i, so convergence to the residual set is kept and only its size grows; it can be reduced by increasing ϱ_{i-2} or narrowing ε_i. This is the precise sense in which the ASTSMC does not need a priori knowledge of the disturbance bound, and it guarantees practical finite-time stability.

Conservativeness of the bound. Steps 3–7 treat the integral state ν_i as a bounded perturbation, whereas in the super-twisting algorithm it is exactly the state that compensates Δ_i. The residual set of Eq. (3.74) is therefore conservative: with $\bar{\nu}_i = 0.5$ rad, $\Gamma_i \ge \mathcal{B}_{\max}\bar{\nu}_i = 6 \times 10^4$ V/s and $\mu_i \ge 13.4$ V; even with the largest $|\nu_i|$ found in the simulations (0.039 rad), $\mu_i \ge 1.8$ V, six times the boundary layer $\varepsilon_i = 0.3$ V. Steps 3–7 show that all signals and the adaptive gains stay bounded, but not that σ_i enters the boundary layer. This is shown next with a Lyapunov function that includes the integral state.

Step 8: super-twisting form. Let $z_i = \mathcal{B}_{ji}\nu_i + \Delta_i$ be the total perturbation, i.e. every term of Eq. (3.68) except the proportional super-twisting term, and $\rho_i = \dot{\mathcal{B}}_{ji}\nu_i + \dot{\Delta}_i$ the part of its rate that the controller does not set. For $|\sigma_i| > \varepsilon_i$, Eqs. (3.68) and (3.46) give:

$$\begin{aligned} \dot{\sigma}_i &= -\mathcal{B}_{ji}\big(k_{i-2,\min} + \varrho_{i-2}|\sigma_i|\big)|\sigma_i|^{1/2}\operatorname{sign}(\sigma_i) + z_i, \\ \dot{z}_i &= -\mathcal{B}_{ji}\big(k_{i,\min} + \varrho_i|\sigma_i|\big)\operatorname{sign}(\sigma_i) + \rho_i, \end{aligned} \tag{3.76}$$

which is the super-twisting algorithm with state-dependent gains and an uncertain, positive input gain $\mathcal{B}_{ji}$. Following Moreno and Osorio [135], the coordinates $\boldsymbol{\zeta}_i = \big[|\sigma_i|^{1/2}\operatorname{sign}(\sigma_i),\ z_i\big]^{\mathsf{T}}$ turn Eq. (3.76) into:

$$\dot{\boldsymbol{\zeta}}_i = \frac{1}{|\zeta_{i1}|}\Big(\mathbf{A}\big(\mathcal{B}_{ji}, |\sigma_i|\big)\boldsymbol{\zeta}_i + \mathbf{e}_2\,|\zeta_{i1}|\rho_i\Big), \qquad \mathbf{A}(\mathcal{B}, s) = \begin{bmatrix} -\frac{1}{2}\mathcal{B}\big(k_{i-2,\min} + \varrho_{i-2}s\big) & \frac{1}{2} \\ -\mathcal{B}\big(k_{i,\min} + \varrho_i s\big) & 0 \end{bmatrix}, \tag{3.77}$$

with $\mathbf{e}_1 = [1,0]^{\mathsf{T}}$ and $\mathbf{e}_2 = [0,1]^{\mathsf{T}}$.

Step 9: second Lyapunov function and LMI. For $\mathcal{W}_i = \boldsymbol{\zeta}_i^{\mathsf{T}}\mathbf{P}\boldsymbol{\zeta}_i$ with $\mathbf{P} = \mathbf{P}^{\mathsf{T}} \succ 0$, which is positive definite in (σ_i, z_i), if $|\rho_i| \le L$, the S-procedure gives $\dot{\mathcal{W}}_i \le -q\,|\boldsymbol{\zeta}_i|^2/|\zeta_{i1}|$ whenever there exist $\mathbf{P} \succ 0$, $\tau > 0$ and $q > 0$ that satisfy the linear matrix inequality (LMI):

$$\begin{bmatrix} \mathbf{A}^{\mathsf{T}}\mathbf{P} + \mathbf{P}\mathbf{A} + q\mathbf{I} + \tau L^2\mathbf{e}_1\mathbf{e}_1^{\mathsf{T}} & \mathbf{P}\mathbf{e}_2 \\ \mathbf{e}_2^{\mathsf{T}}\mathbf{P} & -\tau \end{bmatrix} \prec 0 \quad \text{for all} \quad (\mathcal{B}, s) \in \{\mathcal{B}_{\min}, \mathcal{B}_{\max}\} \times \{0, \bar{s}\}. \tag{3.78}$$

Because $\mathbf{A}(\mathcal{B}, s)$ is affine in $\mathcal{B}$ and in s separately, the left-hand side is multi-affine in $(\mathcal{B}, s)$, so its negativity at the four corners implies negativity on the whole box $[\mathcal{B}_{\min}, \mathcal{B}_{\max}] \times [0, \bar{s}]$.

Step 10: decay rate and reaching time. Since $|\zeta_{i1}| \le |\boldsymbol{\zeta}_i|$ and $\mathcal{W}_i \le \lambda_{\max}(\mathbf{P})|\boldsymbol{\zeta}_i|^2$, the LMI gives $\dot{\mathcal{W}}_i \le -q|\boldsymbol{\zeta}_i|$, and integrating $\frac{d}{dt}\sqrt{\mathcal{W}_i}$ gives the decay for $\varepsilon_i < |\sigma_i| \le \bar{s}$ and the time after which $|\sigma_i| \le \varepsilon_i$:

$$\dot{\mathcal{W}}_i \le -\frac{q\sqrt{\mathcal{W}_i}}{\sqrt{\lambda_{\max}(\mathbf{P})}}, \qquad T_i \le \frac{2\sqrt{\lambda_{\max}(\mathbf{P})\,\mathcal{W}_i(0)}}{q}. \tag{3.79}$$

Check with the tuned gains. With the tuned gains of Table 3.2, $\mathcal{B}_{ji} \in [3.3\times10^4,\ 1.2\times10^5]$ V s^{-1}rad^{-1} and $\bar{s}$ = 30 V, Eq. (3.78) was solved with the LMI Lab of MATLAB and is feasible for every $L \le 7.4\times10^5$ V/s^2. For $L = 3.7\times10^5$ V/s^2, $\mathbf{P} = \left[\begin{smallmatrix} 0.521 & -0.372 \\ -0.372 & 0.711 \end{smallmatrix}\right]$ and $q = 84.3$ (in scaled coordinates). The level set of $\mathcal{W}_i$ through the largest error in the tests, $\sigma_i(0)$ = 12 V, stays within $|\sigma_i| \le 19.2$ V < $\bar{s}$, and Eq. (3.79) gives $T_i \le 9.4$ ms from 0.3 V and $T_i \le 59$ ms from 12 V; these worst-case values are conservative compared with the reaching times of 0.5–1.3 ms found in Section 3.8.5.

Scope of the result. The bound $|\rho_i| \le L$ concerns the slowly varying part of the disturbance ($C_i L \approx 700$ A/s of load-current estimation error); steps of the load or of the reference reset the state (σ_i, z_i), and Eq. (3.79) applies again from the state after the step. Steps 8–10 also assume that the command stays within the rated-current limit and that the anti-windup law is inactive, $|\nu_i| < \bar{\nu}_i$; while a limit is active, the analysis applies again from the state at which it is released, whereas Steps 1–7 need only $|\nu_i| \le \bar{\nu}_i$, which the anti-windup law guarantees at all times. In the simulations the anti-windup law is never active ($|\nu_i| \le 0.039$ rad). Finally, the analysis is carried out for each port, and the coupling from the other port through the 3–4 link is part of Δ_i. This term is bounded for all admissible states, because the phase shifts are limited to $|\phi_i| \le \phi_{\max}$ and, by Eq. (3.1) with $d(1-|d|) \le 1/4$, the current that the 3–4 link can deliver to port 3 is at most $n^2 V_4/(8 f_{sw} L_{34})$. The result therefore holds for the coupled two-port converter. Inside the boundary layer the control is continuous, and finite-time convergence is replaced by ultimate boundedness; because the controller is executed once per switching period, the residual set scales with the square of the sampling period [136], and its actual size is found numerically in Section 3.8.5.

3.8.4 Small-Signal Stability of the PID Controller

The PID controller is linear, so its stability is assessed on the linearised plant: the phase-to-current gain b_i of Eq. (3.55) and the output stage of Eq. (3.57), with a delay of $1.5\,T_c$ for the computation delay and the period averaging. With the initial design gains, all loops had phase margins above $65°$. The common tuning traded part of this margin for speed: with the tuned gains (Table 3.7, Fig. 3.12(a,b)), the current loop has $79.3°$ and 16.7 dB, and the voltage loop $32.3°$ and 5.1 dB. Both loops are stable, but the tuned voltage loop now crosses over (1025 Hz) above the current loop (394 Hz).

To include the interaction of the bridges, the two ports were also analysed together as a two-input/two-output system: the bridge currents of Eq. (3.30) were linearised with respect to both phase shifts and both port voltages, the decoupler of Eq. (3.32) was linearised as implemented, and the controllers of both ports and the delay of $1.5\,T_c$ were included. Table 3.7 gives the margins of each loop with the loops of the other port closed (the smaller of the two ports) and the disk margin, which allows simultaneous gain and phase changes in both ports and is therefore stricter; Fig. 3.12(c,d) shows the voltage-loop gains. At the nominal point, the decoupler removes the phase coupling exactly, and the single-port margins are reproduced. Operating points with unequal ports reduce the margins; the worst case is reverse power flow at port 4, with $24.1°$ and 3.6 dB, because the voltage coupling is not removed by the decoupler. An error of $\pm 50\%$ in the decoupler's model of the 3–4 link is tolerated. Without the decoupler, however, the PID voltage loop is close to instability ($19.6°$, 1.4 dB, disk margin 0.5 dB). For the two SMC-based controllers, the coupling is part of the bounded disturbance of each port, d_i in Eq. (3.20) and Δ_i in Eq. (3.68), so the results of Sections 3.8.2 and 3.8.3 hold in the presence of the coupling.

Table 3.7: Small-signal margins of the PID controller.

Case	**Current loop** (PM, GM)	**Voltage loop** (PM, GM)	**Disk margin**
Single port, nominal point	79.3°, 16.7 dB	32.3°, 5.1 dB	–
Two ports, nominal (48/48 V), exact decoupler	79.3°, 16.7 dB	32.3°, 5.1 dB	3.5 dB, 22.8°
Unequal ports, S2 (60/80 V)	79.3°, 17.5 dB	32.8°, 5.3 dB	3.6 dB, 23.1°
Reverse power at port 4 (−600 W)	77.1°, 15.1 dB	24.1°, 3.6 dB	2.4 dB, 15.4°
Decoupler model of g_{34}: −50%	78.4°, 15.4 dB	31.5°, 4.0 dB	2.3 dB, 15.2°
Decoupler model of g_{34}: +50%	80.7°, 17.5 dB	37.7°, 5.8 dB	3.5 dB, 22.8°
No decoupler	78.8°, 13.4 dB	19.6°, 1.4 dB	0.5 dB, 3.4°

Tuned gains, delay $1.5\,T_c$. PM: phase margin and GM: gain margin of each loop; disk margin of the voltage loops of both ports.

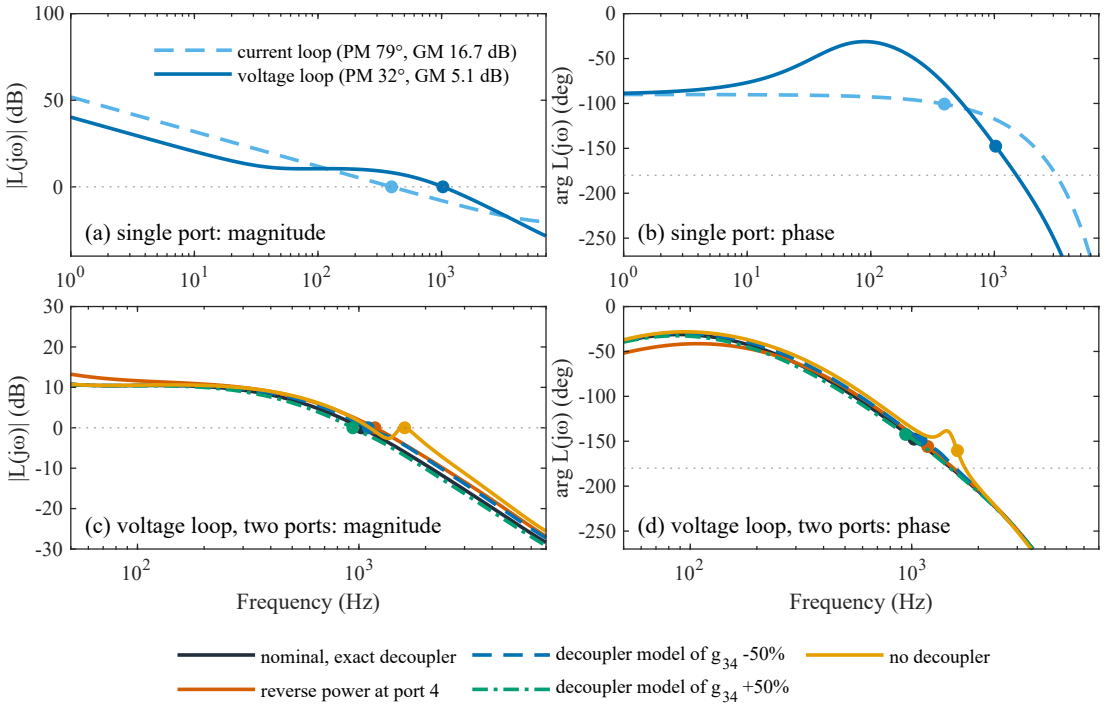


Figure 3.12: Loop gains of the PID controller.

3.8.5 Numerical Check of the Stability Results

The analytical results were checked against the switching simulation with the eight events of the common test C. For each event, Table 3.8 gives the peak of the sliding variable, the time after which it stays inside the boundary layer $|\sigma_i| \le \varepsilon_i$, and the largest $|\sigma_i|$ or $|S_i|$ from 20 ms after the event until the next one (the residual). The signals are those computed by the controllers, logged once per control period. Fig. 3.13 zooms in on the CPL step E3: (a, b) the sliding variables S_i of the SMC–NLESO, Eq. (3.14),

and σ_i of the ASTSMC, Eq. (3.33) (of opposite sign for the same dip, because S_i uses $e_i = v_{\mathrm{ref},i} - v_{c_i}$ and $\sigma_i = V_i - V_{i,\mathrm{ref}}$), and (c, d) the Lyapunov functions $V_S = \frac{1}{2}(S_3^2 + S_4^2)$ and $\mathcal{V}$ of Eq. (3.69). Fig. 3.14 covers the whole test.

Table 3.8: Check of the stability results over test C.

	ASTSMC			**SMC–NLESO**	
Event	Peak (V)	Reach (ms)	Residual (V)	Peak (V)	Residual (V)
E1: $V_{3,\mathrm{ref}}$ 48→60 V	12.02	1.29	0.043	12.04	0.057
E2: $V_{4,\mathrm{ref}}$ 48→60 V	12.03	1.29	0.054	11.99	0.056
E3: $P_{\mathrm{CPL},3}$ 150→300 W	0.498	0.50	0.054	0.486	0.053
E4: $P_{\mathrm{CPL},4}$ 150→300 W	0.506	0.50	0.053	0.531	0.059
E5: V_1 300→330 V	0.275	0	0.038	0.238	0.070
E6: V_2 300→270 V	0.298	0	0.052	0.311	0.056
E7: $R_{\mathrm{load},3}$ 2→1.6 Ω	1.400	1.00	0.054	1.569	0.067
E8: $R_{\mathrm{load},4}$ 2→1.6 Ω	1.380	1.07	0.052	1.545	0.052

Peak and residual of $|\sigma_i|$ or $|S_i|$; reach: time until $|\sigma_i|$ stays inside $\varepsilon_i = 0.3$ V.

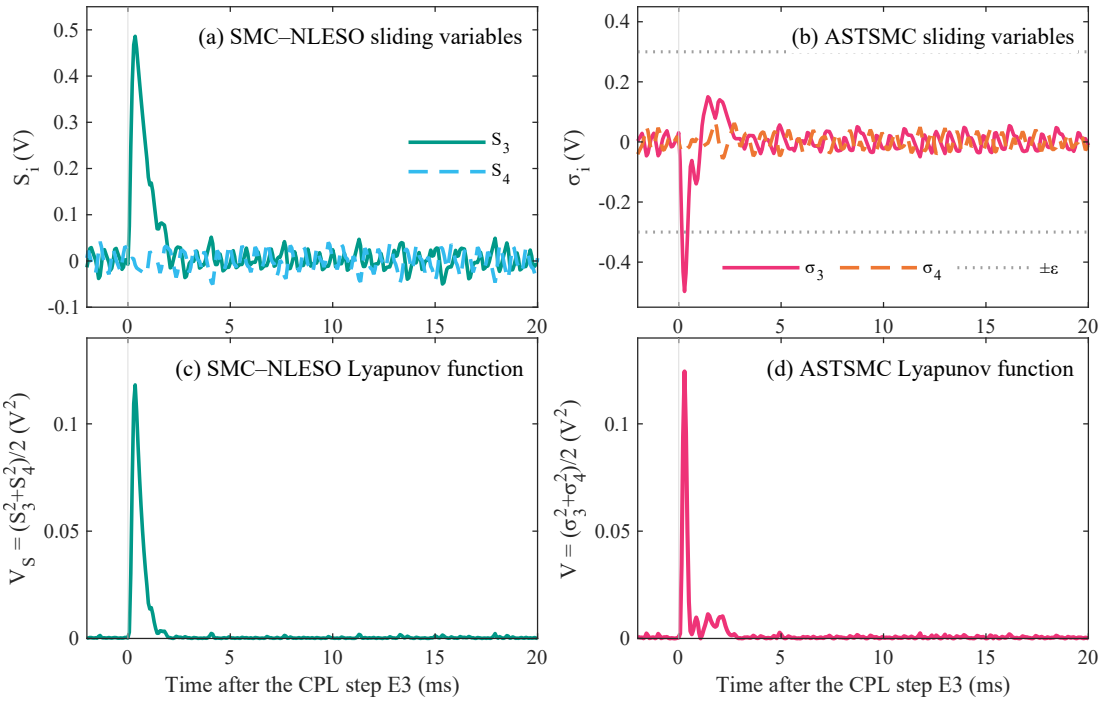


Figure 3.13: Sliding variables and Lyapunov functions after the CPL step E3.

ASTSMC. After every event, the sliding variables return into the boundary layer within 1.3 ms and then stay below 0.055 V, as Eq. (3.79) predicts, far inside the

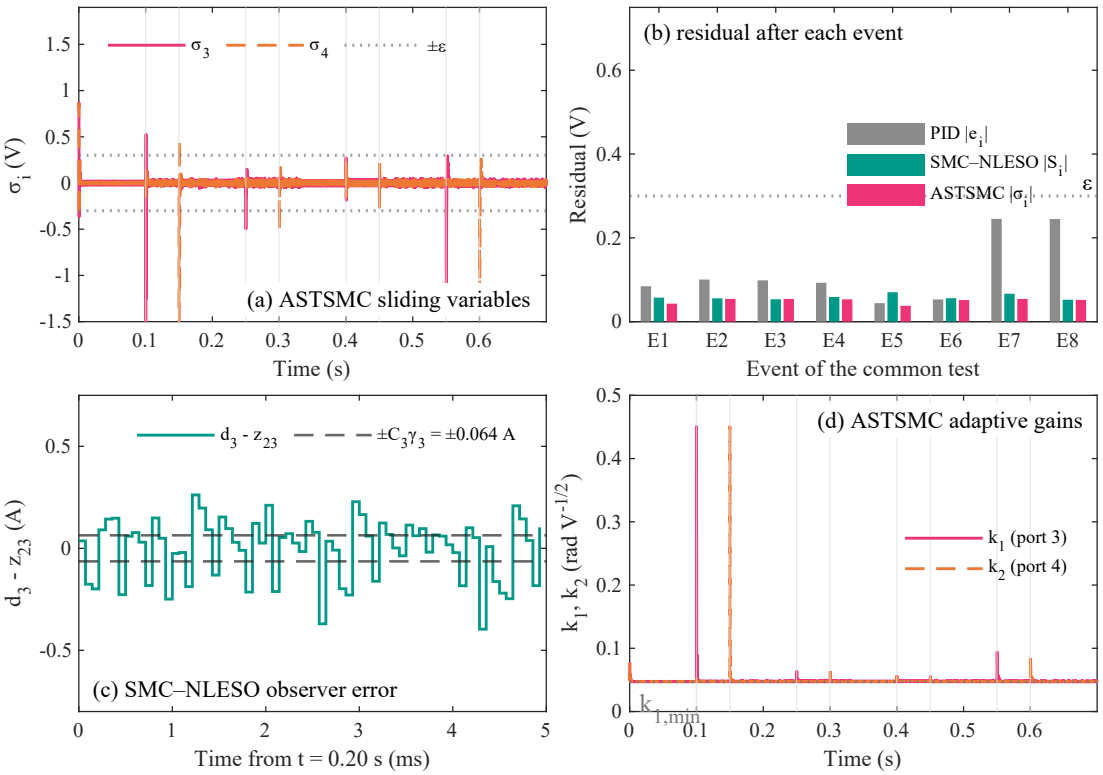


Figure 3.14: Check of the stability results over the common test.

conservative bound of Eq. (3.74) (Fig. 3.14(a,b)). The adaptive gains stay within the bounds of Eq. (3.75): $k_1 \in [0.047,\ 0.451]$ rad $\mathrm{V}^{-1/2}$ and $k_3 \in [23.1,\ 208]$ rad/s, where the upper values equal $k_{\min} + \varrho \max|\sigma_i|$ for the largest error of 12 V, and between events the gains return to $k_{1,\min}$ and $k_{3,\min}$ (Fig. 3.14(d)). The integral states stay below $|\nu_i| = 0.039$ rad, far from the limit $\bar{\nu}_i = 0.5$ rad, so the anti-windup law is never active. Because the controller is sampled and its output is applied one period later, $\mathcal{V}$ does not decrease at every sample outside the boundary layer (it decreases in 82% of those samples), but its envelope decays to the residual set after every event (Fig. 3.13).

SMC–NLESO. The observer error has a steady-state RMS value of 0.14 A (peak 0.40 A) and exceeds $C_i\gamma_i = 0.064$ A in about 70% of the control periods, so the reaching condition of Eq. (3.65) does not hold with the tuned gains (Fig. 3.14(c)). After every event, S_i nevertheless returns to the band predicted by Eq. (3.66): its residual of 0.052–0.070 V lies within the bound $\bar{S}_i = 0.071$ V, slightly above the residual of the ASTSMC

(0.038–0.054 V), and its peak after the load steps (1.57 V) lies within the transient bound of 1.69 V. The Lyapunov functions of the two controllers after the CPL step reach similar peaks (about 0.12 V^2), return within about 2 ms and then stay close to zero.

PID. The PID controller returns to steady state after every event, as the margins of Table 3.7 predict; its residual tracking error from 20 ms after an event is 0.04–0.10 V, and 0.25 V after the slowly recovering load steps E7 and E8 (Fig. 3.14(b)).

3.8.6 Link Between the Harmonic Analysis and the Controller

The harmonic analysis of Section 3.3.3 is used in the controller design. The plant coefficients A_i and B_{ji} of Eqs. (3.39) and (3.40) are sums over the same odd harmonics that produce the winding currents of Eq. (3.7). The fundamental alone carries only $8/\pi^2$ of the square-wave power, so a feedforward based on it would give 0.69 rad instead of 0.31 rad at the nominal point; the equivalent control therefore uses the exact relation of Eq. (3.44), which includes all odd harmonics.

The link also works in the other direction. By Eq. (3.8), every current harmonic depends on the phase shift set by the controller, so an oscillation of the control signal disturbs all harmonics of the link currents at once. A smooth control signal therefore also gives cleaner link currents. In steady state, the gains of the ASTSMC fall back to their minimum values and its control signal moves by only 12.9 mdeg, whereas the sign term of the SMC–NLESO changes its control signal in steps, by 53.0 mdeg (Section 3.7.5).

3.9 Execution on the OPAL-RT Simulator (Software-in-the-Loop)

Type of test. The switching QAB model of Section 3.7.1 was also run with each of the three controllers on an OPAL-RT OP5700 simulator (RT-LAB 2024.1, MATLAB/Simulink R2022b; set-up in Fig. 3.15). This is a software-in-the-loop (SIL) test: the controller and the converter model run together on the simulator, and no real converter or separate controller board is involved. Each model contains the switching power stage, the period-averaged measurements, the controller with the tuned gains of Table 3.2, the decoupler and the one-period computation delay. The bridge voltages of the four ports and the winding currents of ports 3 and 4 were sent to the analog outputs and recorded with a four-channel oscilloscope (seven or eight captures per controller). They show steady-state operation and are compared with the steady states of scenario S1.

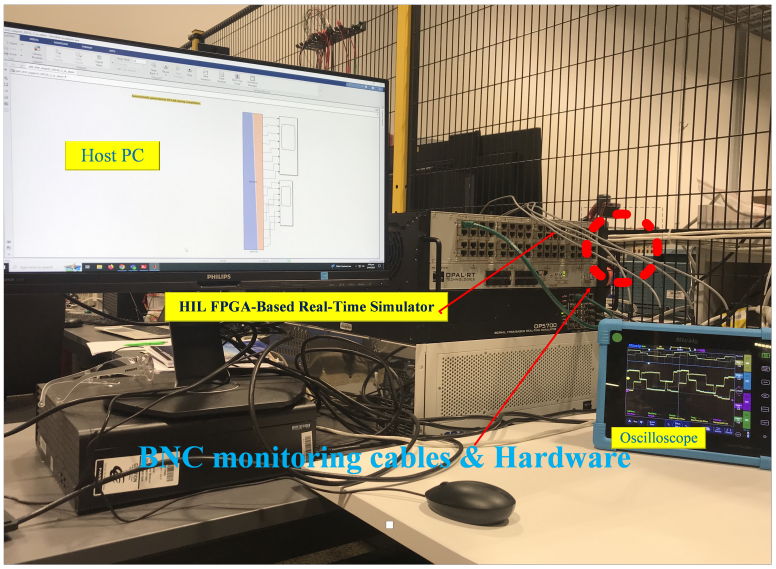


Figure 3.15: OPAL-RT OP5700 simulator set-up.

Execution speed. The step of $T/700 = 102$ ns of the Simulink models (a phase-shift resolution of $0.51°$) is much shorter than the 2.4 μs that the simulator processor

needs for one step of the switching model, so the model did not run in real time: the switching frequency measured on the oscilloscope was 578–625 Hz instead of 14 kHz, i.e. 22–24 times slower than real time. The captures are therefore a time-scaled run of the switching model on the simulator hardware. Time scaling does not change the phase shifts or the waveform shapes, and the time scale of Fig. 3.16 is converted to converter time with the measured switching period. Because the recorded amplitudes were not consistent between channels that should carry equal voltages (analog-output scaling 1/30 for the primary voltages and 1/10 for the other signals), the comparison uses the phase shifts and the normalised waveform shapes.

Comparison with the simulation. Fig. 3.16 shows the primary and secondary bridge voltages of one capture of each controller, with the phase shift φ marked. In all captures the two primary voltages switch together, the two secondary voltages lag them by φ, and the winding currents have the piecewise-linear shape of Eq. (3.7). Table 3.9 compares all captures with the simulation. The phase shift between the primary and the secondary bridge voltages is 17.3–18.9° for the ASTSMC and 19.0–22.8° for the other two controllers, against 16.6–17.7° in the simulation. The mean difference of 1–3° is of the order of the time resolution of the captures ($1.7°$ per pixel at 400 μs/div and $0.9°$ at 200 μs/div) and of the edge delay caused by the 200 ns dead time ($1.0°$ at 14 kHz); the two ASTSMC captures recorded at 200 μs/div give exactly the simulated $17.3°$. The normalised winding currents, digitised over one switching period, coincide with the simulated winding current: the correlation coefficient is 0.999–1.000.

Table 3.9: OPAL-RT captures against the switching simulation.

Controller	**OPAL-RT φ (°)**	**Simulation φ (°)**	**Current correlation**
PID	19.0–22.8 (20.3)	16.8–17.7	0.999–1.000
SMC–NLESO	19.0–20.3 (19.7)	16.8–17.5	0.999–1.000
ASTSMC	17.3–18.9 (18.1)	16.6–17.6	1.000

Mean in brackets.

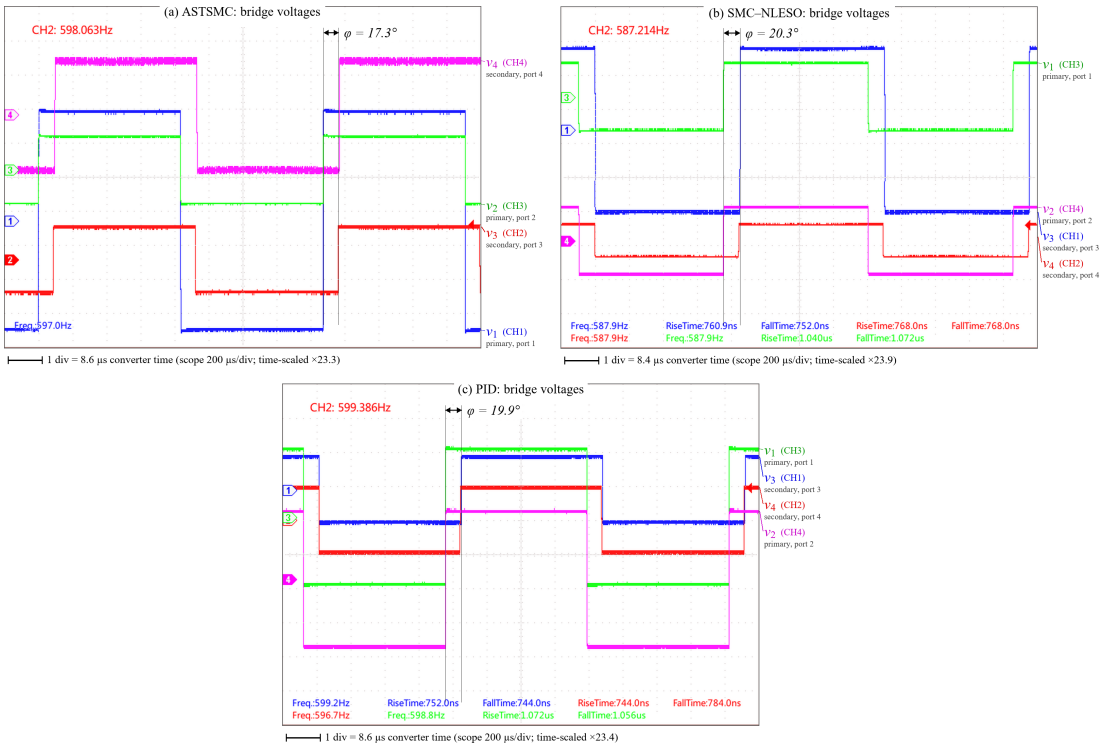


Figure 3.16: Bridge voltages on the OPAL-RT OP5700 (SIL).

3.10 Summary

This chapter answered Research Objectives 1 to 3 for a QAB converter whose ports 3 and 4 supply resistive loads and CPLs.

Harmonic model (C1). The winding currents consist mainly of odd harmonics that decay as $1/k^2$. The GHA model, which includes the dead time and the six links of the Δ-model, agrees with the detailed switching simulation within 5.2% up to the 15th harmonic at the forward-power port. Even harmonics are negligible with equal half-cycles (0.018–0.023% of the odd content) and only indicate an asymmetry (0.30–0.97% with 51 ns of dead-time mismatch). The same harmonic sums give the coefficients B_{13} and B_{24} of the control model, and show why the feedforward must use the exact current-to-phase map rather than the fundamental only (0.31 rad instead of 0.69 rad).

ASTSMC (C2). Under one common set of test events and one common tuning procedure, the ASTSMC had the lowest tuning score (J = 77.6, against 130.9 for the

SMC–NLESO and 525.9 for the PID). It settled a 48→60 V reference step in 1.14 ms (SMC–NLESO 1.50 ms, PID 6.00 ms) and gave the smallest dip after a $2 \rightarrow 1.6\ \Omega$ load step (2.33%, recovery 0.79 ms, against 2.61% and 1.21 ms for the SMC–NLESO and 4.06% and 14.86 ms for the PID). It stabilised CPLs up to 1500 W per port (PID 1350 W), had the smallest error under reverse power flow (7.46 V) and pulsed CPLs (0.91 V), and its control signal moved about four times less than that of the SMC–NLESO (12.9 against 53.0 mdeg). The Lyapunov analysis proves practical finite-time stability with bounded adaptive gains, without a priori knowledge of the disturbance bound, and the simulation confirms it: the sliding variables return into the boundary layer within 1.3 ms after every event.

Limits. The ASTSMC has the largest overshoot on reference steps (4.4%, up to 21% over 100 random converters) and is the most sensitive of the three controllers to an extra computation delay (0.52 V against 0.06 V for the SMC–NLESO with two extra periods). The SMC–NLESO gave the smallest overshoot and CPL dip. All results come from simulation; the OPAL-RT runs (SIL) were slower than real time and confirm only the steady-state operating point and waveforms (phase shifts within 1–3°, current correlation 0.999–1.000). The controllers were not tested on QAB hardware.

Chapter 4

Nonlinear Control Strategies for QAB Converters with Pulsed Power Loads

4.1 Introduction

This chapter extends Chapter 3 to pulsed-power loads (PPLs), whose large and sudden current steps at ports 3 and 4 test the transient performance of the controllers. It addresses RG-4 and RG-5.

Chapter objectives.

(i) Review QAB and pulsed-power converters and compare them on common criteria (Table 4.1).

(ii) Customise three known nonlinear controllers for the coupled ports 3 and 4 of a QAB resonant converter supplying PPLs: the adaptive suboptimal second-order sliding mode controller (ASSOSMC), the integral higher-order sliding mode controller (IHOSMC), and the combined model predictive control with integral sliding mode control (CMPC–ISMC), with one shared decoupler.

(iii) Compare the three controllers under one test ($48\ V$ regulation, a 100→200 W PPL step and the same limits) in simulation and on the OPAL-RT OP5700 simulator

(software-in-the-loop, SIL), using the voltage change, the current, the control input and the efficiency.

Main contribution of this chapter: C3 (three nonlinear controllers customised for the QAB with PPLs), as listed in Section 1.5.

4.2 QAB Converter Topology and Dynamic Analysis

4.2.1 Topology of the QAB Resonant Converter with PPLs

This chapter studies control strategies and the stability of the QAB converter with single phase shift (SPS) modulation. The aim is a control framework that is robust, keeps the voltage deviations small and handles the transient energy demand of pulsed loads in grid-connected DC MGs [137]. Fig. 4.1 shows the QAB converter, which has two input ports (V_1 and V_2) and two output ports (V_3 and V_4).

The ports are connected through a high-frequency transformer (HFT) with two primary and two secondary windings. The PPLs impose sudden, large current transients, which create complex dynamic interactions between the ports [137]. This configuration makes the QAB suitable for isolated, high-efficiency power sharing between several ports, but it also needs advanced control to keep the voltage stable and to limit the interaction between ports [138].

The QAB gives more flexibility in controlling the energy transfer between several sources and loads than conventional topologies such as the DAB or LLC converters, which is important in DC MGs with changing demand. It is therefore well suited to studying robust and predictive controllers that handle coupled port dynamics and keep the system stable under small and large transients. This advantage, however, also makes the control more complex, especially with PPLs [139].

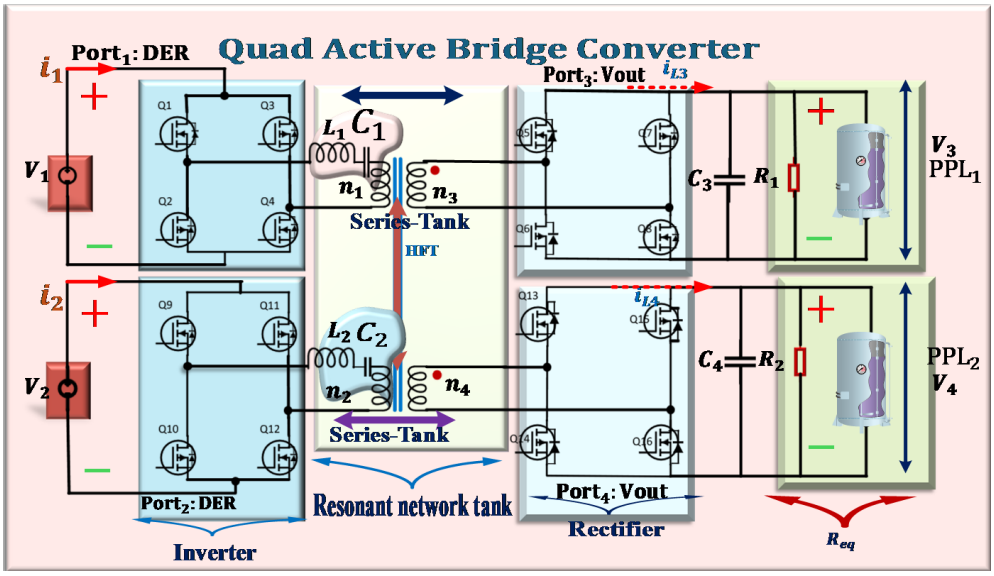


Figure 4.1: QAB resonant converter supplying PPLs.

4.2.2 Comparative Analysis of Pulsed Power Converters

Table 4.1 gives a qualitative overview of 22 publications on QAB converters and pulsed power technologies. It covers the proposed converter architecture, the control method, the application, the performance and the main advances or limitations. Fig. 4.2 summarises the same 22 publications.

Each row corresponds to one study, and the columns rate the number of switches and components, the voltage stress, the converter and control complexity, the cost, the efficiency, the power density, the input and output voltage range, the weight and the stability. Each parameter is rated from 1 to 5, where 5 is the most favourable, 1 the least favourable, and 0 means not applicable (N/A). This overview shows the trade-offs between topologies, helps to identify research trends and guides the choice of converter designs for pulsed power and grid-connected applications.

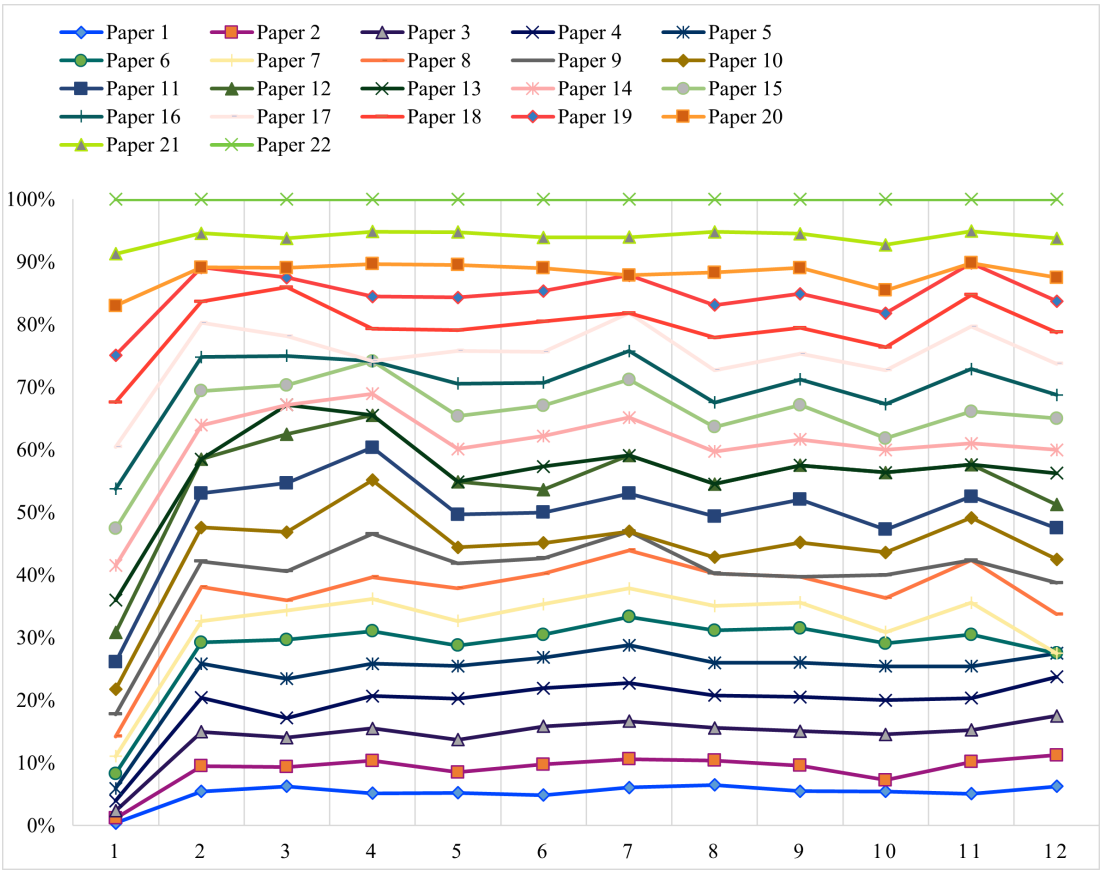


Figure 4.2: Multicriteria analysis of pulsed power load converter topologies.

4.3 Control Strategies and Stability Analysis for a QAB Converter

4.3.1 Combined Model Predictive Control-Integral Sliding Mode Control (CMPC–ISMC)

A QAB converter supplying PPLs experiences sharp transients, voltage fluctuations and complex interactions between ports, which make it difficult to control even though it transfers power between several ports effectively. Conventional controllers such as sliding mode control (SMC) and super-twisting sliding mode control (STSMC) struggle to keep it stable under these fast dynamics [140]. Fast voltage regulation, reduced coupling between ports, soft switching and robustness to uncertainties and disturbances

Table 4.1: Comparison of QAB converters with pulsed power loads.

No	Ref	Components	Switches	Voltage Stress	Converter Complexity	Control Complexity	Cost	Efficiency	Power Density	Input/Output Voltage Range	Weight	Stability
1	[138]	High	8+	Reduced	High	High	High	Very High	High	700–800 V / 250–500 V	Moderate	Excellent
2	[143]	Medium	6+	Moderate	Moderate	High	Med.	Good	Medium	100 V	Reduced	Improved
3	[144]	High	Multiple	Moderate	High	Very High	High	High	High	500–900 V / 270–750 V	Moderate	Very High
4	[145]	High	Multiple	Moderate	Very High	Very High	High	High	High	400–800 V / 400–48 V	Moderate	Excellent
5	[146]	High	12+	Moderate	High	High	High	High	High	400–800 V	Medium	Good
6	[147]	Medium	6+	Reduced	Moderate	Moderate	Med.	High	Improved	300 V / 28–100 V	Reduced	Stable
7	[148]	Medium	4+	Moderate	Moderate	High	Med.	Good	Moderate	28 V	Moderate	Stable
8	[149]	High	Multiple	Low	High	High	High	Good	High	300–800 V / 28–72 V	High	Very High
9	[150]	Moderate	N/A	Variable	Moderate	Low	Low	N/A	N/A	400 V / 50–400 V	N/A	High
10	[151]	High	Few	Very High	Low	Low	Low–Med.	Low	High	380–600 V, 280–450 V	High	Moderate
11	[152]	High	16+	Moderate	High	High	High	Very High	Very High	150–450 V / 300–800 V	Low	High
12	[153]	High	16+	Medium	High	Moderate	High	High	High	2–4 kV / 400–1000 V	Moderate	Good
13	[154]	Model	Varies	Varies	N/A	Moderate	N/A	N/A	N/A	N/A	N/A	High
14	[155]	High	8+	Low	High	High	High	High	Compact	380–400 V / 48–72 V	Low	Good
15	[156]	High	Multiple	Moderate	High	High	Good	Good	High	48–200 V	Reduced	High
16	[157]	High	8+	Moderate–High	High	Moderate	Med.	Good	Moderate	600–800 V / 200–500 V	High	Good
17	[158]	High	Multiple	Controlled	High	High	High	High	Moderate	600 V	High	High
18	[159]	Medium	8	Moderate	Moderate	High	Med.–High	High	Moderate	300 V / 300 V	Moderate	High
19	[160]	High	6+	Reduced	High	High	High	High	High	400–750 V / 48–300 V	Reduced	High
20	[161]	Model	Varies	Configurable	High	Medium	N/A	Optimised	Topology-based	100–800 V / 48–500 V	N/A	Design-based
21	[162]	High	8+	Reduced	High	High	High	Very High	High	700–800 V / 250–500 V	Moderate	Excellent
22	[163]	High	Multiple	Moderate	High	Very High	High	High	High	600–800 V / 48–300 V	Moderate	Very High

are all required [141]. These demands motivate nonlinear and predictive controllers such as the CMPC–ISMC, the adaptive suboptimal second-order sliding mode controller (ASSOSMC) and the integral higher-order sliding mode controller (IHOSMC) [142]. MPC, although conservative, enforces limits and gives optimal predictions over a finite horizon [142]. ISMC gives robustness, zero steady-state error and fast disturbance rejection through an integral sliding surface and a nonlinear corrective action [60]. The hybrid CMPC–ISMC combines these strengths to handle the PPL dynamics with good tracking. Its equations are derived from the QAB converter model of Fig. 4.1. The model considers a QAB converter with power flowing from port 1 to port 3 and from port 2 to port 4, starting with the capacitor-voltage dynamics at ports 3 and 4:

$$\begin{cases} C_3 \dfrac{dv_{c_3}(t)}{dt} = i_{L_3}(t) - \left(\dfrac{v_{c_3}(t)}{R_{\text{load},3}} + \dfrac{P_{\text{PPL},3}}{v_{c_3}(t)} \right), \\ C_4 \dfrac{dv_{c_4}(t)}{dt} = i_{L_4}(t) - \left(\dfrac{v_{c_4}(t)}{R_{\text{load},4}} + \dfrac{P_{\text{PPL},4}}{v_{c_4}(t)} \right) \end{cases}$$

where $v_{c_i}(t)$ is the capacitor voltage, $i_{L_i}(t)$ is the current delivered by the converter (the control input), $\frac{v_{c_i}(t)}{R_{\text{load},i}}$ is the resistive-load current, $\frac{P_{\text{PPL},i}}{v_{c_i}(t)}$ is the PPL equivalent current, and C_i is the port capacitance ($i \in \{3, 4\}$). The tracking error for ports 3 and 4 is defined as:

$$\begin{cases} e_3(t) = v_{\text{ref},3}(t) - v_{c_3}(t), \\ e_4(t) = v_{\text{ref},4}(t) - v_{c_4}(t) \end{cases}$$

where $v_{\text{ref},3} = v_{\text{ref},4} = 48\,\text{V}$ is the reference voltage of ports 3 and 4. The integral sliding surfaces $S_i(t)$ of ports 3 and 4 are:

$$\begin{cases} S_3(t) = e_3(t) + \lambda_3 \displaystyle\int_0^t e_3(\tau)\, d\tau \\ S_4(t) = e_4(t) + \lambda_4 \displaystyle\int_0^t e_4(\tau)\, d\tau \end{cases} \tag{4.1}$$

where $S_i(t)$ combines the error and its integral, and $\lambda_i > 0$ is the integral weight that improves steady-state tracking. The derivative of the sliding surface is:

$$\begin{cases} \dot{S}_3(t) = \dot{e}_3(t) + \lambda_3\, e_3(t) \\ \dot{S}_4(t) = \dot{e}_4(t) + \lambda_4\, e_4(t) \end{cases} \tag{4.2}$$

Differentiating the tracking error of Eq. (4.3.1) and substituting $\frac{dv_{c_i}(t)}{dt}$ from Eq. (4.3.1) into Eq. (4.2) gives the derivative of the sliding surface of ports 3 and 4:

$$\begin{cases} \dot{S}_3(t) = \dot{v}_{\mathrm{ref},3}(t) - \dfrac{1}{C_3}\left(i_{L_3}(t) - \dfrac{v_{c_3}(t)}{R_{\mathrm{load},3}} - \dfrac{P_{\mathrm{PPL},3}}{v_{c_3}(t)}\right) + \lambda_3\big(v_{\mathrm{ref},3}(t) - v_{c_3}(t)\big) \\ \dot{S}_4(t) = \dot{v}_{\mathrm{ref},4}(t) - \dfrac{1}{C_4}\left(i_{L_4}(t) - \dfrac{v_{c_4}(t)}{R_{\mathrm{load},4}} - \dfrac{P_{\mathrm{PPL},4}}{v_{c_4}(t)}\right) + \lambda_4\big(v_{\mathrm{ref},4}(t) - v_{c_4}(t)\big) \end{cases} \tag{4.3}$$

Chattering Mitigation with Saturation Function (SAT): The aim of the ISMC is to drive the sliding variable to zero with the reaching law:

$$\begin{cases} \dot{S}_3(t) = -\varepsilon\ \mathrm{sat}\left(\dfrac{S_3(t)}{\delta}\right) - \gamma\, S_3(t) \\ \dot{S}_4(t) = -\varepsilon\ \mathrm{sat}\left(\dfrac{S_4(t)}{\delta}\right) - \gamma\, S_4(t) \end{cases} \tag{4.4}$$

where $\varepsilon,\ \gamma > 0$ are the gains that set the convergence, $\delta > 0$ is the width of the boundary layer, and $\mathrm{sat}\left(\frac{S_i(t)}{\delta}\right)$ is the saturation function, defined as:

$$\mathrm{sat}\left(\frac{S_i(t)}{\delta}\right) = \begin{cases} +1, & \dfrac{S_i(t)}{\delta} > 1, \\ \dfrac{S_i(t)}{\delta}, & |S_i(t)| \le \delta, \\ -1, & \dfrac{S_i(t)}{\delta} < -1, \end{cases} \tag{4.5}$$

The reaching law with chattering mitigation is enforced by setting Eq. (4.5) equal to Eq. (4.3), which gives Eq. (4.6).

$$\begin{aligned} \dot{S}_i(t) &= \dot{v}_{\mathrm{ref},i}(t) - \frac{1}{C_i}\left(i_{L_i}(t) - \frac{v_{c_i}(t)}{R_{\mathrm{load},i}} - \frac{P_{\mathrm{PPL},i}}{v_{c_i}(t)}\right) + \lambda_i\big(v_{\mathrm{ref},i}(t) - v_{c_i}(t)\big) \\ &= -\varepsilon\ \mathrm{sat}\big(S_i(t)/\delta\big)\ -\ \gamma\, S_i(t). \end{aligned} \tag{4.6}$$

where $i \in \{3, 4\}$ for ports 3 and 4. Solving Eq. (4.6) for the required current $i_{L_i}(t)$ gives Eq. (4.7).

$$\begin{aligned} i_{L_i}(t) = C_i\Bigg[&\dot{v}_{\mathrm{ref},i}(t) + \lambda_i\, e_i(t) + \frac{1}{C_i}\left(\frac{v_{c_i}(t)}{R_{\mathrm{load},i}} + \frac{P_{\mathrm{PPL},i}}{v_{c_i}(t)}\right) \\ &+ \varepsilon\ \mathrm{sat}\big(S_i(t)/\delta\big) + \gamma\, S_i(t)\Bigg] \end{aligned} \tag{4.7}$$

Assuming that the states are measured, a proportional-integral feedback is used in place of $\dot{v}_{\mathrm{ref},i}(t)$ to generate the control input $u_{\mathrm{ISMC},i}(t)$. With $u_{\mathrm{ISMC},i}(t) = i_{L_i}(t)$, the final ISMC control law for ports 3 and 4 is:

$$\begin{aligned} u_{\mathrm{ISMC},i}(t) = k_i\Big(v_{\mathrm{ref},i}(t) - v_{c_i}(t) + \lambda_i \int_0^t \big(v_{\mathrm{ref},i}(\tau) - v_{c_i}(\tau)\big)\, d\tau\Big) \\ + \left(\frac{v_{c_i}(t)}{R_{\mathrm{load},i}} + \frac{P_{\mathrm{PPL},i}}{v_{c_i}(t)}\right) \\ + C_i\, \varepsilon\, \mathrm{sat}\left(\frac{v_{\mathrm{ref},i}(t) - v_{c_i}(t) + \lambda_i \int_0^t \big(v_{\mathrm{ref},i}(\tau) - v_{c_i}(\tau)\big)\, d\tau}{\delta}\right) \\ + C_i\, \gamma\, S_i(t), \qquad i \in \{3,4\}. \end{aligned} \tag{4.8}$$

where $i \in \{3,4\}$ denotes ports 3 and 4; $k_i\, e_i(t)$ is the proportional tracking action; $\lambda_i \int_0^t e_i(\tau)\, d\tau$ is the integral action ensuring zero steady-state error; λ_i is the integral gain; k_i is the proportional gain; $C_i\, \varepsilon\, \mathrm{sat}(\cdot)$ is the boundary-layer switching term; and $C_i\, \gamma\, S_i(t)$ is the linear sliding-surface damping term. The ISMC is highly robust to uncertainties and PPL disturbances, but on its own it cannot optimise the performance while enforcing operating constraints. Adding MPC gives optimal, constraint-aware control. Although MPC rejects disturbances more slowly, the resulting hierarchical CMPC–ISMC combines the constraint handling of MPC with the fast robustness of ISMC.

Stability analysis of the ISMC: Consider the Lyapunov function $V_i(t) = \frac{1}{2} S_i^2(t)$ for $i \in \{3,4\}$. Using the reaching law of Eq. (4.4), its time derivative is:

$$\dot{V}_i(t) = S_i(t)\dot{S}_i(t) = -\varepsilon\, S_i(t)\, \mathrm{sat}\Big(\tfrac{S_i(t)}{\delta}\Big) - \gamma\, S_i^2(t) \le 0. \tag{4.9}$$

Moreover, for $|S_i(t)| \ge \delta$, $\mathrm{sat}(S_i/\delta) = \mathrm{sign}(S_i)$ and hence $\dot{V}_i \le -\varepsilon|S_i| - \gamma S_i^2 < 0$, which guarantees finite-time reaching to the boundary layer $|S_i(t)| \le \delta$. Inside $|S_i(t)| \le \delta$, $\mathrm{sat}(S_i/\delta) = S_i/\delta$ and $\dot{S}_i = -(\varepsilon/\delta + \gamma)S_i$, implying exponential convergence of $S_i(t)$ to zero (practical convergence with boundary layer). Therefore, the ISMC ensures bounded closed-loop signals and robust voltage regulation under PPL disturbances [60].

Pulsed-load characterisation: To improve reproducibility and reflect realistic pulsed-load behaviour, the PPL at ports 3 and 4 is modelled as a time-varying constant-power load, $i_{\mathrm{PPL},i}(t) = P_{\mathrm{PPL},i}(t)/v_{c_i}(t)$, $i \in \{3,4\}$. Instead of an ideal instantaneous square pulse, $P_{\mathrm{PPL},i}(t)$ is implemented as a trapezoidal periodic pulse with finite rise and fall times to emulate practical pulse generation and conversion limits. The pulse profile is fully defined by the baseline power $P_{\min}$, pulse magnitude P_{Δ}, rise time t_r, flat-top duration t_{on}, fall time t_f, and period T; the pulse energy is $E_{\mathrm{pulse}} = P_{\Delta}\big(t_{\mathrm{on}} + \frac{t_r+t_f}{2}\big)$. In addition, a staircase excitation (100–200 W increments) is applied to represent multi-level pulsed loads. All pulse parameters $(P_{\min}, P_{\Delta}, t_r, t_{\mathrm{on}}, t_f, T)$ are reported to ensure repeatability.

Mathematical Equation for Model Predictive Control (MPC): The QAB port dynamics of Eq. (4.3.1) are linearised and discretised about a nominal operating point of ports 3 and 4, whose steady-state values are defined below:

$$\begin{cases} v_{c_3}^{*},\ i_{L_3}^{*},\ \Delta\varphi_3^{*} \\ v_{c_4}^{*},\ i_{L_4}^{*},\ \Delta\varphi_4^{*} \end{cases} \tag{4.10}$$

the corresponding small-signal perturbations about the operating point are defined as perturbations are:

$$\begin{cases} \overline{v}_{c_3}(t) = v_{c_3}(t) - v_{c_3}^{*} \\ \overline{v}_{c_4}(t) = v_{c_4}(t) - v_{c_4}^{*} \end{cases} \tag{4.11}$$

$$\begin{cases} \overline{i}_{L_3}(t) = i_{L_3}(t) - i_{L_3}^{*} \\ \overline{i}_{L_4}(t) = i_{L_4}(t) - i_{L_4}^{*} \end{cases} \tag{4.12}$$

$$\begin{cases} \overline{\Delta\varphi_3}(t) = \Delta\varphi_3(t) - \Delta\varphi_3^{*} \\ \overline{\Delta\varphi_4}(t) = \Delta\varphi_4(t) - \Delta\varphi_4^{*} \end{cases} \tag{4.13}$$

This gives the linearised capacitor-voltage dynamics of ports 3 and 4 in Eq. (4.11).

where $(\cdot)^{*}$ denotes the nominal value at the operating point, $v_{c_i}^{*}$ is the steady-state

capacitor voltage (V), $i_{L_i}^*$ is the steady-state port inductor current (A), and $\Delta\varphi_i^*$ is the steady-state phase-shift command (rad), for $i \in \{3,4\}$. Here, $\Delta\varphi_i(t)$ denotes the commanded phase shift between the reference/input bridge and the bridge associated with port i, and t denotes time (s).

(a) Linearised load-port capacitor dynamics (including PPL term): At each load port, the total load current is modelled as a resistive load in parallel with a pulsed power load: $i_{\text{load},i}(t) = v_{c_i}(t)/R_{\text{load},i} + P_i(t)/v_{c_i}(t)$, where $P_i(t)$ represents the (time-varying) PPL power level. Linearising $i_{\text{load},i}$ about $(v_{c_i}^*, P_i^*)$ yields:

$$\bar{i}_{\text{load},i}(t) = \left(\frac{1}{R_{\text{load},i}} - \frac{P_i^*}{(v_{c_i}^*)^2}\right)\overline{v}_{c_i}(t) + \frac{1}{v_{c_i}^*}\,\overline{P}_i(t), \qquad i \in \{3,4\}, \tag{4.14}$$

where $\overline{P}_i(t) = P_i(t) - P_i^*$ is treated as an exogenous disturbance due to the PPL steps. Substituting (4.14) into the capacitor KCL $C_i\dot{v}_{c_i} = i_{L_i} - i_{\text{load},i}$ gives the linearised capacitor-voltage dynamics:

$$C_i\frac{d\,\overline{v}_{c_i}(t)}{dt} = \bar{i}_{L_i}(t) - G_i\,\overline{v}_{c_i}(t) - \frac{1}{v_{c_i}^*}\,\overline{P}_i(t), \qquad i \in \{3,4\}, \tag{4.15}$$

with the incremental (small-signal) load conductance:

$$G_i \triangleq \left(\frac{1}{R_{\text{load},i}} - \frac{P_i^*}{(v_{c_i}^*)^2}\right), \qquad i \in \{3,4\}. \tag{4.16}$$

(b) Linearised inductor-current: To construct a state-space prediction model suitable for MPC, the port inductor current dynamics are approximated in an averaged form as:

$$L_i\,\frac{d\,\bar{i}_{L_i}(t)}{dt} = -\,\overline{v}_{c_i}(t) - R_{L_i}\,\bar{i}_{L_i}(t) + k_{\varphi,i}\,\overline{\Delta\varphi_i}(t), \qquad i \in \{3,4\}, \tag{4.17}$$

where L_i and R_{L_i} denote the effective port inductance (H) and its lumped series resistance (Ohm), respectively. The gain $k_{\varphi,i}$ quantifies the sensitivity of the averaged port-equivalent excitation voltage $v_{\text{eq},i}$ with respect to the phase shift $\Delta\varphi_i$:

$$k_{\varphi,i} \triangleq \left.\frac{\partial v_{\text{eq},i}}{\partial\Delta\varphi_i}\right|_{(v_{c_i}^*,\, i_{L_i}^*,\, \Delta\varphi_i^*)}, \qquad i \in \{3,4\}. \tag{4.18}$$

This gain can be obtained analytically from the adopted QAB steady-state power-transfer relation, or numerically by applying a small perturbation about the operating point.

(c) State-space model and explicit matrices $\mathbf{A}_i, \mathbf{B}_i$: For MPC design, the state and input vectors are defined as:

$$\begin{cases} \mathbf{x}_i(t) = \begin{bmatrix} \overline{v}_{c_i}(t) \\ \overline{i}_{L_i}(t) \end{bmatrix}, \qquad u_i(t) = \overline{\Delta\varphi}_i(t), \qquad i \in \{3,4\}. \end{cases} \tag{4.19}$$

where $\overline{(\cdot)}$ denotes small-signal (deviation) quantities around the operating point, C_i is the port capacitance, L_i is the equivalent series inductance, R_{L_i} is the inductor series resistance, $v_{c_i}^*$ is the nominal capacitor-voltage operating point used for linearisation, $k_{\varphi,i}$ is the small-signal gain relating the incremental phase shift $u_i(t) = \overline{\Delta\varphi}_i(t)$ to the inductor-current dynamics, and G_i is defined in (4.16).

Combining (4.15) and (4.17) gives the continuous-time linear model:

$$\dot{\mathbf{x}}_i(t) = \mathbf{A}_i\,\mathbf{x}_i(t) + \mathbf{B}_i\,u_i(t) + \mathbf{E}_i\,d_i(t), \qquad i \in \{3,4\}, \tag{4.20}$$

where $d_i(t) \triangleq \overline{P}_i(t)$ is the PPL power disturbance, and the matrices are explicitly as follows:

$$\mathbf{A}_i = \begin{bmatrix} -\dfrac{G_i}{C_i} & \dfrac{1}{C_i} \\ -\dfrac{1}{L_i} & -\dfrac{R_{L_i}}{L_i} \end{bmatrix}, \qquad \mathbf{B}_i = \begin{bmatrix} 0 \\ \dfrac{k_{\varphi,i}}{L_i} \end{bmatrix}, \qquad \mathbf{E}_i = \begin{bmatrix} -\dfrac{1}{C_i v_{c_i}^*} \\ 0 \end{bmatrix}, \tag{4.21}$$

with G_i defined in (4.16). Here, $\mathbf{x}_i(t) \in \mathbb{R}^2$ is the deviation state vector (V, A), $u_i(t) \in \mathbb{R}$ is the incremental phase-shift input (rad), and $d_i(t) = \overline{P}_i(t) \in \mathbb{R}$ is the PPL power disturbance (W); $\dot{(\cdot)}$ denotes the time derivative. Accordingly, $\mathbf{A}_i \in \mathbb{R}^{2\times2}$, $\mathbf{B}_i \in \mathbb{R}^{2\times1}$, and $\mathbf{E}_i \in \mathbb{R}^{2\times1}$, where $\mathbf{E}_i$ is the disturbance-input matrix.

(d) Discretisation and prediction model: The models in (4.20) are discretised using the forward Euler method with sampling period $T_s = 1 \times 10^{-3}\,\mathrm{s}$ by:

$$\mathbf{x}_i(k{+}1) = \mathbf{A}_{id}\,\mathbf{x}_i(k) + \mathbf{B}_{id}\,u_i(k) + \mathbf{E}_{id}\,d_i(k), \qquad i \in \{3,4\}, \tag{4.22}$$

where

$$\mathbf{A}_{id} = \mathbf{I} + T_s\mathbf{A}_i, \qquad \mathbf{B}_{id} = T_s\mathbf{B}_i, \qquad \mathbf{E}_{id} = T_s\mathbf{E}_i, \qquad i \in \{3,4\}. \tag{4.23}$$

where $k \in \mathbb{Z}_{\geq 0}$ denotes the discrete-time index, and $\mathbf{I}$ is the 2×2 identity matrix (consistent with $\mathbf{x}_i \in \mathbb{R}^2$). The prediction horizon is set to $N = 10$ steps (i.e., a prediction window of $NT_s = 10\ \mathrm{ms}$). For $j = 0, \ldots, N-1$, the predicted states evolve as:

$$\mathbf{x}_i(k{+}j{+}1|k) = \mathbf{A}_{id}\,\mathbf{x}_i(k{+}j|k) + \mathbf{B}_{id}\,u_i(k{+}j|k) + \mathbf{E}_{id}\,d_i(k{+}j|k). \tag{4.24}$$

Here, $(\cdot|k)$ denotes a quantity predicted at time instant k, and $j = 0, \ldots, N-1$ is the prediction-step index over the horizon N. Over each prediction window, $d_i(k{+}j|k)$ is assumed piecewise constant to capture PPL step changes.

(e) MPC optimisation (receding-horizon implementation): At each sampling instant k, the control sequence $\{u_i(k|k), \ldots, u_i(k{+}N{-}1|k)\}$ is obtained by minimising:

$$\begin{aligned} J_i = &\sum_{j=0}^{N-1} \Big(\mathbf{x}_i(k{+}j|k) - \mathbf{x}_{i,\mathrm{ref}}\Big)^{\top} \mathbf{Q}_i \Big(\mathbf{x}_i(k{+}j|k) - \mathbf{x}_{i,\mathrm{ref}}\Big) \\ &+ \sum_{j=0}^{N-1} u_i(k{+}j|k)^{\top} R_i\, u_i(k{+}j|k), \end{aligned} \tag{4.25}$$

where J_i is the finite-horizon cost, $\mathbf{x}_{i,\mathrm{ref}} = [0 \;\; 0]^{\top}$ is the regulation target for the deviation states, $\mathbf{Q}_i \succeq 0$ and $R_i > 0$ are weighting matrices (typically $\mathbf{Q}_i \in \mathbb{R}^{2\times 2}$ and $R_i \in \mathbb{R}^{1\times 1}$ for the single-input case), and $(\cdot)^{\top}$ denotes the transpose.

subject to the discrete-time model (4.24) and actuator constraints such as:

$$u_{i,\min} \leq u_i(k{+}j|k) \leq u_{i,\max}, \qquad \Delta u_{i,\min} \leq \Delta u_i(k{+}j|k) \leq \Delta u_{i,\max}, \tag{4.26}$$

where $\mathbf{Q}_i \succeq 0$ and $R_i > 0$ are tuning weights, $\mathbf{x}_{i,\mathrm{ref}} = [0 \;\; 0]^{\top}$ corresponds to regulation

of deviations to zero, and $\Delta u_i(k) = u_i(k) - u_i(k-1)$ limits the phase-shift slew rate. Only the first optimal move is applied (receding horizon):

$$u_i(k) = u_i^\star(k|k), \qquad i \in \{3,4\}. \tag{4.27}$$

where $(\cdot)^\star$ denotes the optimiser of (4.25) subject to (4.24) and (4.26).

(f) Integration of CMPC with ISMC (robustification): The CMPC provides the nominal incremental phase-shift command $u_i^{\mathrm{MPC}}(k)$ based on (4.22)–(4.27). To enhance robustness against modelling errors and fast PPL transients, the ISMC term adds a bounded corrective action:

$$\begin{aligned} u_i(k) &= u_i^{\mathrm{MPC}}(k) + u_i^{\mathrm{ISMC}}(k), \\ u_i^{\mathrm{ISMC}}(k) &= -K_i \,\mathrm{sat}\Big(\tfrac{S_i(k)}{\phi_i}\Big), \quad i \in \{3,4\}. \end{aligned} \tag{4.28}$$

where $S_i(k)$ is the selected sliding manifold for port i, $K_i > 0$ is the ISMC gain, $\phi_i > 0$ defines the boundary layer, and $\mathrm{sat}(\cdot)$ mitigates chattering. This CMPC–ISMC structure preserves the predictive optimal behaviour while ensuring robust disturbance rejection during pulsed-load step changes.

Optimisation-based MPC for Ports 3 and 4: The MPC control action is obtained by minimising a quadratic objective function over the prediction horizon N. For each port $i \in \{3,4\}$, the cost function is defined as:

$$\begin{cases} J^{(3)} = \displaystyle\sum_{k=0}^{N-1} \Big(\mathbf{x}_k^{(3)\top} \mathbf{Q}^{(3)} \mathbf{x}_k^{(3)} + u_k^{(3)\top} R^{(3)} u_k^{(3)} \Big) + \mathbf{x}_N^{(3)\top} \mathbf{\Pi}^{(3)} \mathbf{x}_N^{(3)} \\ J^{(4)} = \displaystyle\sum_{k=0}^{N-1} \Big(\mathbf{x}_k^{(4)\top} \mathbf{Q}^{(4)} \mathbf{x}_k^{(4)} + u_k^{(4)\top} R^{(4)} u_k^{(4)} \Big) + \mathbf{x}_N^{(4)\top} \mathbf{\Pi}^{(4)} \mathbf{x}_N^{(4)} \end{cases} \tag{4.29}$$

where $J^{(i)}$ is the MPC objective function for port i, $\mathbf{x}_k^{(i)}$ and $u_k^{(i)}$ are the predicted state and input at prediction step k, and $(\cdot)^\top$ denotes the transpose operator. The matrices $\mathbf{Q}^{(i)} \succeq 0$ and $R^{(i)} \succ 0$ are the state- and input-weighting matrices, respectively, and $\mathbf{\Pi}^{(i)} \succeq 0$ is the terminal-state weighting matrix. For the state definition in Eq. (4.29),

$\mathbf{x}_k^{(i)} \in \mathbb{R}^2$ and $u_k^{(i)} \in \mathbb{R}$.

MPC weight selection: The MPC weights were selected by (i) normalising the states and input by their expected operating ranges, (ii) initialising the weights using a Bryson-type guideline, and (iii) refining them through a brief parametric sweep under representative 100–200 W PPLs steps to balance fast voltage recovery against limited control effort. In this research, scalar weights were used (since $\mathbf{x}_k^{(i)} \in \mathbb{R}^2$ and $u_k^{(i)} \in \mathbb{R}$), and the same set was adopted for ports 3 and 4 for symmetry. The final values are $\mathbf{Q}^{(3)} = \mathbf{Q}^{(4)} = \mathbf{I}$, $R^{(3)} = R^{(4)} = 0.1$, and $\mathbf{\Pi}^{(3)} = \mathbf{\Pi}^{(4)} = 2.2367\,\mathbf{I}$.

Sensitivity: Increasing $Q^{(i)}$ improves tracking speed (faster voltage recovery) but increases actuation effort and current stress, whereas increasing $R^{(i)}$ yields smoother control action at the expense of slower recovery.

Sequential Control Execution in MPC: At each sampling instant, only the first element of the optimal control sequence is applied (receding-horizon principle), i.e.:

$$\begin{cases} u_{\mathrm{MPC},3}(t) = u_{0,3}^{*}(t_k), & t \in [\, t_k,\, t_{k+1}\,], \\ u_{\mathrm{MPC},4}(t) = u_{0,4}^{*}(t_k), & t \in [\, t_k,\, t_{k+1}\,]. \end{cases} \tag{4.30}$$

The terminal sets $\mathcal{X}_{N,i}$ are selected to ensure recursive feasibility and closed-loop stability. The final CMPC–ISMC input of ports 3 and 4 adds the ISMC term to the MPC action:

$$\begin{cases} u_3(t) = u_{\mathrm{MPC},3}(t) + u_{\mathrm{ISMC},3}(t) \\ u_4(t) = u_{\mathrm{MPC},4}(t) + u_{\mathrm{ISMC},4}(t) \end{cases} \tag{4.31}$$

Eq. (4.31) represents the core composite control law of the proposed CMPC with ISMC scheme, where the smooth predictive action $u_{\mathrm{MPC},i}(t)$ is augmented by the robust corrective term $u_{\mathrm{ISMC},i}(t)$ to improve tracking and disturbance rejection. The resulting $u_i(t)$ is then used to generate the phase-shift command applied to the PWM modulator (subject to practical saturation/decoupling constraints where applicable).

4.3.2 Adaptive Suboptimal Second-Order Sliding Mode Controller (ASSOSMC)

The ASSOSMC is a nonlinear control strategy that ensures finite-time convergence of both the output error and its derivative, while significantly reducing the chattering typically associated with classical Sliding Mode Control (SMC). This controller is particularly well-suited for power electronic converters operating under uncertainties and nonlinear loads, such as PPLs. In this study, the ASSOSMC regulates the capacitor voltages of a QAB resonant converter supplying PPLs. For ports 3 and 4 (Fig. 4.1 and Eq. (4.3.1)), the sliding variables, defined as in [60, 130], and their dynamics are:

$$\begin{cases} \sigma_3(t) = v_{c_3}(t) - v_{c_3}^* \\ \sigma_4(t) = v_{c_4}(t) - v_{c_4}^* \end{cases} \tag{4.32}$$

$$\begin{cases} \dot{\sigma}_3(t) = \dfrac{1}{C_3}\left[i_{L_3}(t) - \dfrac{v_{c_3}(t)}{R_{\text{load},3}} - \dfrac{P_{\text{PPL},3}}{v_{c_3}(t)} \right] - \dot{v}_{c_3}^*(t) \\ \dot{\sigma}_4(t) = \dfrac{1}{C_4}\left[i_{L_4}(t) - \dfrac{v_{c_4}(t)}{R_{\text{load},4}} - \dfrac{P_{\text{PPL},4}}{v_{c_4}(t)} \right] - \dot{v}_{c_4}^*(t) \end{cases} \tag{4.33}$$

where $v_{c_3}^*$ and $v_{c_4}^*$ are the reference voltages (both $48\,\text{V}$), v_{c_3} and v_{c_4} denote the tracking (measured) capacitor voltages, and i_{L_3}, i_{L_4} represent the measured inductor currents for ports 3 and 4, respectively. To develop an ASSOSMC for the QAB converter, the system dynamics are reformulated using auxiliary variables. This allows the controller to regulate both the tracking error and its derivative, which gives robust and fast convergence even with unknown loads. The auxiliary variables of the ASSOSMC are:

$$\begin{cases} \zeta_{1,i}(t) = \sigma_i(t), \\ \zeta_{2,i}(t) = \dot{\sigma}_i(t). \end{cases} \tag{4.34}$$

where $\zeta_{1,i}(t)$ is the sliding variable, and $\zeta_{2,i}(t)$ represents the derivative of the sliding variable, with $i \in \{3, 4\}$ corresponding to ports 3 and 4. To improve performance and

reduce chattering, an adaptive gain $\alpha_i(t)$ is introduced:

$$\alpha_i(t) = \begin{cases} \alpha^*, & \text{if } \left(\zeta_{1,i}(t) - \frac{1}{2}\zeta_{\max,i}(t)\right)\left(\zeta_{\max,i}(t) - \zeta_{1,i}(t)\right) > 0, \\ 1, & \text{otherwise.} \end{cases} \tag{4.35}$$

where $\alpha^* > 1$ is the boosted adaptive-gain value applied while $\zeta_{1,i}(t)$ is between the origin and its estimated peak $\zeta_{\max,i}(t)$ (i.e., while still approaching the sliding surface), and the gain reverts to 1 once this condition no longer holds; $\zeta_{\max,i}(t)$ is defined numerically in Eq. (4.37) below. To ensure a sufficiently strong sliding motion, the parameters β_3 and β_4 of the ASSOSMC are:

$$\begin{cases} \beta_3 > \max\left(\dfrac{\varsigma_3}{\alpha_3\vartheta_{\min}}, \dfrac{4\varsigma_3}{3\vartheta_{\min} - \alpha_3(t)\vartheta_{\max}}\right), \\ \beta_4 > \max\left(\dfrac{\varsigma_4}{\alpha_4\vartheta_{\min}}, \dfrac{4\varsigma_4}{3\vartheta_{\min} - \alpha_4(t)\vartheta_{\max}}\right), \end{cases} \tag{4.36}$$

where $\vartheta_{\min}$ and $\vartheta_{\max}$ denote the lower and upper bounds of the function $\vartheta_i(t)$, with $i \in \{3, 4\}$ corresponding to ports 3 and 4. The requirements and inequality conditions for β_3 and β_4 are specified in [60]. The final control law of the ASSOSMC for ports 3 and 4 is obtained by combining Eqs. (4.35) and (4.36):

$$\begin{cases} u_3(t) = -\mu_3\,\beta_3\,\operatorname{sign}\left(\zeta_{1,3}(t) - \frac{1}{2}\,\zeta_{\max,3}(t)\right) \\ u_4(t) = -\mu_4\,\beta_4\,\operatorname{sign}\left(\zeta_{1,4}(t) - \frac{1}{2}\,\zeta_{\max,4}(t)\right) \end{cases} \tag{4.37}$$

where $u_3(t)$ and $u_4(t)$ are the control inputs for ports 3 and 4, ς_i represents the upper bound on the uncertainties and disturbance terms, and $\mu_3 = \mu_4 = 0.011$ denote the sliding variable scaling factors that adaptively adjust the control action. Furthermore, $\zeta_{\max,3} = \zeta_{\max,4} = 0.5$ stand for the estimated maximum values of $\zeta_{1,3}(t)$ and $\zeta_{1,4}(t)$, which are used to regulate the control effort, while β_3 and β_4 are positive robustness gains for ports 3 and 4, selected to dominate bounded modelling uncertainties and disturbances. Chattering is mitigated by replacing the ideal discontinuous $\operatorname{sign}(\cdot)$ with

the boundary-layer saturation function $\mathrm{sat}(\cdot)$ [54], defined below:

$$\mathrm{sat}(x) = \begin{cases} 1, & x > 1, \\ x, & |x| \le 1, \\ -1, & x < -1, \end{cases} \tag{4.38}$$

where x is the normalised argument; outside the boundary layer ($|x| > 1$) the function equals $\mathrm{sign}(x)$, and inside it ($|x| \le 1$) it varies linearly, which removes the discontinuity that causes chattering. Replacing $\mathrm{sign}(\cdot)$ in Eq. (4.37) by the saturation function of Eq. (4.38) gives the implemented discrete-time ASSOSMC law:

$$\begin{cases} u_3(k) = -\,\mu_3\,\beta_3\ \mathrm{sat}\left(\dfrac{\zeta_{1,3}(k) - \frac{1}{2}\,\zeta_{\max,3}}{\delta_3}\right) \\ u_4(k) = -\,\mu_4\,\beta_4\ \mathrm{sat}\left(\dfrac{\zeta_{1,4}(k) - \frac{1}{2}\,\zeta_{\max,4}}{\delta_4}\right) \end{cases} \tag{4.39}$$

where $\delta_3 > 0$ and $\delta_4 > 0$ are the boundary-layer thicknesses, so that $x = \left(\zeta_{1,i}(k) - \frac{1}{2}\zeta_{\max,i}\right)/\delta_i$ in Eq. (4.38); k is the discrete-time index ($t = kT_s$, with sampling period T_s), and $u_3(k)$ and $u_4(k)$ are the ASSOSMC control inputs applied to ports 3 and 4, respectively (held constant over each sampling interval via a zero-order hold).

4.3.3 Integral Higher-Order Sliding Mode Controller (IHOSMC)

In QAB resonant converters supplying PPLs, the IHOSMC reduces chattering, but its robustness can suffer from a slow or unpredictable reaching phase, a degraded transient response with possible overshoot or oscillations, and reaching times that vary strongly with noise, delays and switching constraints. It is therefore important to benchmark the IHOSMC against other robust controllers [164]. Starting from the capacitor dynamics of ports 3 and 4 in Eq. (4.3.1) (Fig. 4.1), the tracking error is:

$$\begin{cases} \varrho_3(t) = v_{c_3}(t) - v_{c_3}^{\mathrm{ref}} \\ \varrho_4(t) = v_{c_4}(t) - v_{c_4}^{\mathrm{ref}} \end{cases} \tag{4.40}$$

From the capacitor dynamics of ports 3 and 4:

$$\begin{cases} \dfrac{d\varrho_3(t)}{dt} = \dfrac{dv_{c_3}(t)}{dt} - \dfrac{1}{C_3}\left(i_{L_3}(t) - \dfrac{v_{c_3}(t)}{R_{\text{load},3}} - \dfrac{P_{\text{PPL},3}}{v_{c_3}(t)}\right) \\ \dfrac{d\varrho_4(t)}{dt} = \dfrac{dv_{c_4}(t)}{dt} - \dfrac{1}{C_4}\left(i_{L_4}(t) - \dfrac{v_{c_4}(t)}{R_{\text{load},4}} - \dfrac{P_{\text{PPL},4}}{v_{c_4}(t)}\right) \end{cases} \tag{4.41}$$

where $v_{c_3}^{\text{ref}} = v_{c_4}^{\text{ref}} = 48\,\text{V}$, $R_{\text{load},3} = R_{\text{load},4} = 2\,\Omega$ are the fixed resistive loads, $C_3 = C_4 = 95\,\mu\text{F}$ are the filter capacitors at ports 3 and 4, and $P_{\text{PPL},3}$, $P_{\text{PPL},4}$ denote the measured active powers whose maximum values for each port are $1500\,\text{W}$. The inductor current is expressed as:

$$i_{L_i}(t) = g_i(t)\,u_i(t) + b_i(t) \tag{4.42}$$

where $u_i(t)$ is the control variable for port $i \in \{3, 4\}$, $g_i(t)$ is the effective control gain which depends on the operating point of the system, and $b_i(t)$ is the uncertainty term. Rearranging Eq. (4.40) and Eq. (4.41) and substituting $i_{L_3}(t)$ and $i_{L_4}(t)$ gives the system dynamics:

$$\begin{cases} \dfrac{d\varrho_i}{dt} = \dfrac{1}{C_i}\left(g_i u_i + b_i - \dfrac{v_{c_i}}{R_{\text{load},i}} - \dfrac{P_{\text{PPL},i}}{v_{c_i}}\right) - \dot{v}_{c_i}^{\text{ref}}(t) & (4.43) \\ \dfrac{d\varrho_i(t)}{dt} = f_{1,i}(t) + f_{2,i}(t)\,u_i(t). & (4.44) \end{cases}$$

where $P_{\text{PPL},3}$ and $P_{\text{PPL},4}$ denote the measured active powers for ports 3 and 4, respectively, and $v_{c_3}(t)$, $v_{c_4}(t)$ are the tracking capacitor voltages at ports 3 and 4.

Define

$$f_{1,i}(t) = \frac{1}{c_i}\left(b_i(t) - \left(\frac{v_{c_i}(t)}{R_{\text{load},i}} + \frac{P_{\text{PPL},i}}{v_{c_i}(t)}\right)\right) \in [-H_i, H_i],$$

and

$$f_{2,i}(t) = \frac{1}{C_i}\,g_i(t) \in [g_{\min,i}, g_{\max,i}],$$

where C_i is the filter capacitor of port i ($C_3 = C_4 = 95\,\mu\text{F}$, as defined above), $H_i = \max_t|f_{1,i}(t)|$, $g_{\min,i} = 0.7$, and $g_{\max,i} = 1.35$. To mitigate chattering, the sign law (4.45) is replaced by the saturation-based reaching law of Eqs. (4.46) and (4.47), where $\xi_i(t)$

is the integral higher-order sliding surface defined in Eq. (4.48):

$$\dot{u}_i(t) = -K_i \, \mathrm{sign}\big(\xi_i(t)\big) \tag{4.45}$$

$$\mathrm{sat}\left(\frac{\xi_i(t)}{\phi}\right) = \begin{cases} 1, & \xi_i/\phi > 1, \\ \xi_i/\phi, & |\xi_i/\phi| \le 1, \\ -1, & \xi_i/\phi < -1, \end{cases} \tag{4.46}$$

$$\begin{cases} \dot{\xi}_3(t) = -K_3 \, \mathrm{sat}\left(\dfrac{\xi_3(t)}{\phi}\right) \\ \dot{\xi}_4(t) = -K_4 \, \mathrm{sat}\left(\dfrac{\xi_4(t)}{\phi}\right) \end{cases} \tag{4.47}$$

where $K_3 = K_4 = 25700$ is the control gain of ports 3 and 4 and $\phi > 0$ is the boundary-layer parameter that reduces chattering. This modification ensures continuous control near the sliding surface and retains finite-time convergence. The integral higher-order surface, with gains $\gamma_{1,2,3}$, is:

$$\xi_i(t) = \gamma_1 \int_0^t \varrho_i(\tau)\, d\tau + \gamma_2 \, \varrho_i(t) + \gamma_3 \, \frac{d\varrho_i(t)}{dt} \tag{4.48}$$

$$\dot{\xi}_i(t) = \gamma_1 \, \varrho_i(t) + \gamma_2 \, \dot{\varrho}_i(t) + \gamma_3 \, \ddot{\varrho}_i(t). \tag{4.49}$$

To improve controller robustness and suppress the impact of measurement noise, the second derivative of the tracking error $\varrho_i(t)$ is approximated and filtered, which gives a smooth and reliable signal for the IHOSMC control law. Because the controller operates in discrete time, only sampled values such as $\varrho_i(t),\ \varrho_i(t-\Delta t),\ \varrho_i(t-2\Delta t)$ are available. Using a Taylor series, the first derivative of the tracking error is:

$$\dot{\varrho}_i(t) \approx \frac{\varrho_i(t) - \varrho_i(t-\Delta t)}{\Delta t}. \tag{4.50}$$

and the second derivative is estimated as:

$$\frac{d^2\varrho_i(t)}{dt^2} \approx \frac{\dfrac{d\varrho_i(t)}{dt} - \dfrac{d\varrho_i(t-\Delta t)}{dt}}{\Delta t} \tag{4.51}$$

To further suppress noise and achieve a smooth signal, the second derivative is passed

through a first-order low-pass filter:

$$\left(\frac{d^2\varrho_i}{dt^2}\right)_{\text{filt}} = (1-\vartheta)\left(\frac{d^2\varrho_i}{dt^2}\right)(t-\Delta t) + \alpha\,\frac{d^2\varrho_i(t)}{dt^2}, \tag{4.52}$$

with $\alpha = \frac{T_s}{\tau+T_s},\ \tau = 10^{-3},\ \Delta t = T_s$ (the sampling interval). To derive the final IHOSMC control law, the derivative of the sliding surface is equated to a saturation-based reaching law to guarantee finite-time convergence. By substituting the system dynamics and the filtered second derivative into this relation, the resulting control input ensures robust error regulation. Equating Eqs. (4.47) and (4.52) yields:

$$\gamma_1\,\varrho_i + \gamma_2\,\dot{\varrho}_i + \gamma_3\,\ddot{\varrho}_i = -\,K_i\,\mathrm{sat}\left(\frac{\xi_i}{\phi}\right) \tag{4.53}$$

$$\ddot{\varrho}_i = \frac{-\,K_i\,\mathrm{sat}\left(\frac{\xi_i}{\phi}\right) - \gamma_1\,\varrho_i - \gamma_2\,\dot{\varrho}_i}{\gamma_3} \tag{4.54}$$

Substituting $\dot{\varrho}_i(t)$ from the system dynamics gives:

$$\dot{\varrho}_i = f_{1,i} + f_{2,i}\,u_i, \tag{4.55}$$

$$u_i = \frac{\dot{\varrho}_i - f_{1,i}}{f_{2,i}}, \tag{4.56}$$

To derive the control law, the sliding surface equation is first differentiated to estimate the second derivative $\ddot{\varrho}_i(t)$. Substituting $\ddot{\varrho}_i(t)$ and $\dot{\varrho}_i(t)$ into the sliding surface dynamics gives:

$$\gamma_1\,\varrho_i + \gamma_2(f_{1,i} + f_{2,i}\,u_i) + \gamma_3\,\ddot{\varrho}_i = -\,K_i\,\mathrm{sat}\left(\frac{\xi_i}{\phi}\right) \tag{4.57}$$

Rearranging Eq. (4.58) to isolate the control input $u_i(t)$ and dividing both sides by $\gamma_2 f_{2,i}(t)$ gives the final control law for ports 3 and 4:

$$u_3 = \frac{-\,f_{1,3} - \gamma_1\,\varrho_3 - \gamma_2\,\frac{d\varrho_3}{dt} - \gamma_3\,\frac{d^2\varrho_3}{dt^2} - K_3\,\mathrm{sat}\left(\frac{\xi_3}{\phi}\right)}{f_{2,3}} \tag{4.58}$$

$$u_4 = \frac{-\,f_{1,4} - \gamma_1\,\varrho_4 - \gamma_2\,\frac{d\varrho_4}{dt} - \gamma_3\,\frac{d^2\varrho_4}{dt^2} - K_4\,\mathrm{sat}\left(\frac{\xi_4}{\phi}\right)}{f_{2,4}} \tag{4.59}$$

where u_i is the port input for $i \in \{3,4\}$, $f_{1,i}$ cancels matched disturbances, $f_{2,i}$ normalises the control by the (bounded) gain, and $\gamma_{1,2,3}, K_i, \phi$ shape the IHOSMC transient and chattering trade-offs. To avoid the singularity of the PPL model $i_{\mathrm{PPL},i}(t) = P_{\mathrm{PPL},i}(t)/v_{c_i}(t)$

as $v_{c_i}(t) \to 0$, the denominator is regularised using a minimum-voltage threshold $v_{\min} = 5\,\mathrm{V}$. Specifically, an effective voltage $\tilde{v}_{c_i}(t) = \max\big(v_{c_i}(t),\, 5\,\mathrm{V}\big)$ is used so that $i_{\mathrm{PPL},i}(t) = P_{\mathrm{PPL},i}(t)/\tilde{v}_{c_i}(t)$ remains bounded during large disturbances. This safeguard is applied consistently in both the simulations and the OPAL-RT software-in-the-loop implementation. The equations of the three controllers (CMPC–ISMC, ASSOSMC and IHOSMC) were derived from the QAB resonant converter of Fig. 4.1; each controller is applied separately, with the same feedforward decoupler.

Decoupling Controller for Inter-Port Coupling Compensation: Although the ISMC laws in Eq. (4.8) generate the required (virtual) control inputs $u_{\mathrm{ISMC},3}(t)$ and $u_{\mathrm{ISMC},4}(t)$, the QAB exhibits strong coupling between ports through the multi-winding transformer and the resonant network [3]. A 2×2 feedforward decoupling block therefore maps the two control channels into realisable PWM phase-shift commands.

Step 1: Define the virtual control vector. From Eq. (4.8), define the ISMC virtual control vector for ports 3 and 4 as:

$$\mathbf{u}(t) = \begin{bmatrix} u_{\mathrm{ISMC},3}(t) \\ u_{\mathrm{ISMC},4}(t) \end{bmatrix}. \tag{4.60}$$

Step 2: Coupled small-signal current–phase model. Around an operating point $\boldsymbol{\phi}^\star = \begin{bmatrix}\phi_3^\star & \phi_4^\star\end{bmatrix}^\top$, the coupled QAB port-current variations can be locally approximated by:

$$\Delta\mathbf{i}_L(t) = \mathbf{G}\,\Delta\boldsymbol{\phi}(t), \qquad \Delta\mathbf{i}_L(t) = \begin{bmatrix} \Delta i_{L_3}(t) \\ \Delta i_{L_4}(t) \end{bmatrix}, \quad \Delta\boldsymbol{\phi}(t) = \begin{bmatrix} \Delta\phi_3(t) \\ \Delta\phi_4(t) \end{bmatrix}. \tag{4.61}$$

where the coupling matrix $\mathbf{G}$ is the Jacobian detailed in [3, 151]:

$$\mathbf{G} = \begin{bmatrix} g_{33} & g_{34} \\ g_{43} & g_{44} \end{bmatrix} = \left[\begin{matrix} \dfrac{\partial i_{L_3}}{\partial \phi_3} & \dfrac{\partial i_{L_3}}{\partial \phi_4} \\ \dfrac{\partial i_{L_4}}{\partial \phi_3} & \dfrac{\partial i_{L_4}}{\partial \phi_4} \end{matrix} \right]\Bigg|_{\boldsymbol{\phi}^\star}. \tag{4.62}$$

Here, g_{33} and g_{44} are the direct gains, whereas g_{34} and g_{43} capture cross-coupling between ports 3 and 4.

Baseline Controller: Conventional PI with Feedforward Decoupling: A conventional proportional-integral (PI) controller with a feedforward decoupling network is included as an established baseline for regulating the QAB converter supplying PPLs and fixed resistive loads. It is tested under the same operating conditions as the AS-SOSMC, the IHOSMC and the CMPC–ISMC customised in this chapter, to compare their practicality and performance [165]. Fig. 4.3 shows the voltages and currents of ports 3 and 4 with the PI controller and feedforward decoupling. At $t = 0.02\,\mathrm{s}$, the PPL disturbance makes the port-3 voltage drop to $44.5\,\mathrm{V}$ and the port-3 current rise to $27.5\,\mathrm{A}$. At $t = 0.04\,\mathrm{s}$, the port-4 voltage falls to $44.2\,\mathrm{V}$ while the port-4 current rises to $30\,\mathrm{A}$. Although the PI controller maintains regulation during PPL operation, coupling effects between the ports remain.

Impact of resonant-parameter mismatches: In practice, the resonant-tank parameters and transformer turns ratio may deviate from their nominal values due to component tolerances, temperature drift, and unmodelled parasitics. Such mismatches mainly affect the phase-shift–to–tank-current (and phase-shift–to–power) mapping used by the predictive model and can be treated as a bounded uncertainty. Accordingly, the closed-loop sliding dynamics can be written as:

$$\dot{S}_i(t) = -\varepsilon\,\mathrm{sat}\big(S_i(t)/\delta\big) - \gamma S_i(t) + d_i(t), \qquad |d_i(t)| \le \bar{d}_i,\;\; i \in \{3,4\}, \tag{4.63}$$

where $S_i(t)$ is the sliding (mismatch) variable for port $i \in \{3,4\}$, $\dot{S}_i(t)$ denotes its time derivative, $\varepsilon > 0$ is the nonlinear reaching gain, $\mathrm{sat}(\cdot)$ is the saturation function used to mitigate chattering, $\delta > 0$ is the boundary-layer thickness, $\gamma > 0$ is the linear damping gain, and $d_i(t)$ is a lumped disturbance term accounting for resonant-parameter errors and unmodelled dynamics, assumed bounded by $|d_i(t)| \le \bar{d}_i$ with $\bar{d}_i > 0$. Since

the ISMC stability has already been established via a Lyapunov argument, the same conclusion holds under bounded mismatches by selecting the reaching gain $\varepsilon > \bar{d}_i$ (with δ setting the accuracy–chattering trade-off). Quantitatively, $\pm 20\%$ variations in (L_r, C_r) and $\pm 5\%$ in n around the nominal values are evaluated, and the resulting peak voltage deviation $\Delta V_{\max}$ (and settling time) at ports 3 and 4 is reported, confirming robust regulation with bounded transients under the tested mismatch levels.

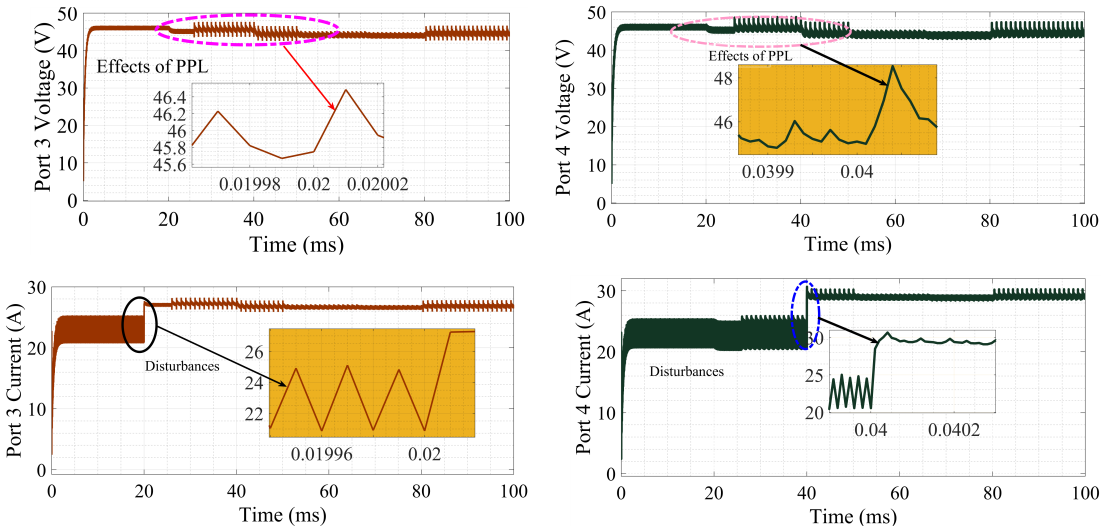


Figure 4.3: PI with feedforward decoupling.

Step 3: Feedforward decoupling law. To reduce interaction, the decoupler computes the phase-shift corrections as:

$$\Delta\phi(t) = \mathbf{H}\,\Delta\mathbf{i}_c(t), \qquad \mathbf{H} = \mathbf{G}^{-1}, \tag{4.64}$$

where $\Delta\mathbf{i}_c(t)$ is the two-channel current command entering the decoupler. In this work, $\Delta\mathbf{i}_c(t)$ is taken as the ISMC virtual control vector, i.e., $\Delta\mathbf{i}_c(t) = \mathbf{u}(t)$.

For the 2×2 case, the determinant of $\mathbf{G}$ is:

$$\det(\mathbf{G}) = g_{33}g_{44} - g_{34}g_{43}, \tag{4.65}$$

and the decoupling matrix can be written explicitly as:

$$\mathbf{H} = \frac{1}{\det(\mathbf{G})} \begin{bmatrix} g_{44} & -g_{34} \\ -g_{43} & g_{33} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}. \tag{4.66}$$

The decoupled phase-shift corrections (the Mux–matrix block) are therefore:

$$\begin{cases} \Delta\phi_3(t) = h_{11}\, u_{\mathrm{ISMC},3}(t) + h_{12}\, u_{\mathrm{ISMC},4}(t), \\ \Delta\phi_4(t) = h_{21}\, u_{\mathrm{ISMC},3}(t) + h_{22}\, u_{\mathrm{ISMC},4}(t). \end{cases} \tag{4.67}$$

Step 4:Regularised decoupling. When $\mathbf{G}$ is ill-conditioned, a damped least-squares decoupler can be used:

$$\mathbf{H}_\lambda = (\mathbf{G}^\top \mathbf{G} + \lambda \mathbf{I})^{-1} \mathbf{G}^\top, \qquad \lambda > 0, \tag{4.68}$$

and $\mathbf{H}$ in Eq. (4.64) is replaced by $\mathbf{H}_\lambda$.

Step 5: Phase saturation and PWM generation. Finally, the PWM phase-shift commands are obtained by adding the corrections to the nominal phase shifts and applying saturation limits:

$$\begin{cases} \phi_3(t) = \phi_3^\star + \mathrm{sat}\big(\Delta\phi_3(t), \Delta\phi_{\max}\big), \\ \phi_4(t) = \phi_4^\star + \mathrm{sat}\big(\Delta\phi_4(t), \Delta\phi_{\max}\big), \end{cases} \tag{4.69}$$

where $\Delta\phi_{\max}$ denotes the maximum allowable phase deviation and the resulting $\phi_3(t)$ and $\phi_4(t)$ are passed to the PWM block to generate the gate signals.

Fig. 4.4 shows the QAB resonant converter with the three controllers (CMPC–ISMC, ASSOSMC and IHOSMC); each is applied separately with the feedforward decoupler.

4.4 Simulation Results

4.4.1 Test Conditions and Performance Indices

Type of test. The results of this section come from simulation of the QAB resonant converter in MATLAB/Simulink; Section 4.4.7 gives the runs on the OPAL-RT OP5700

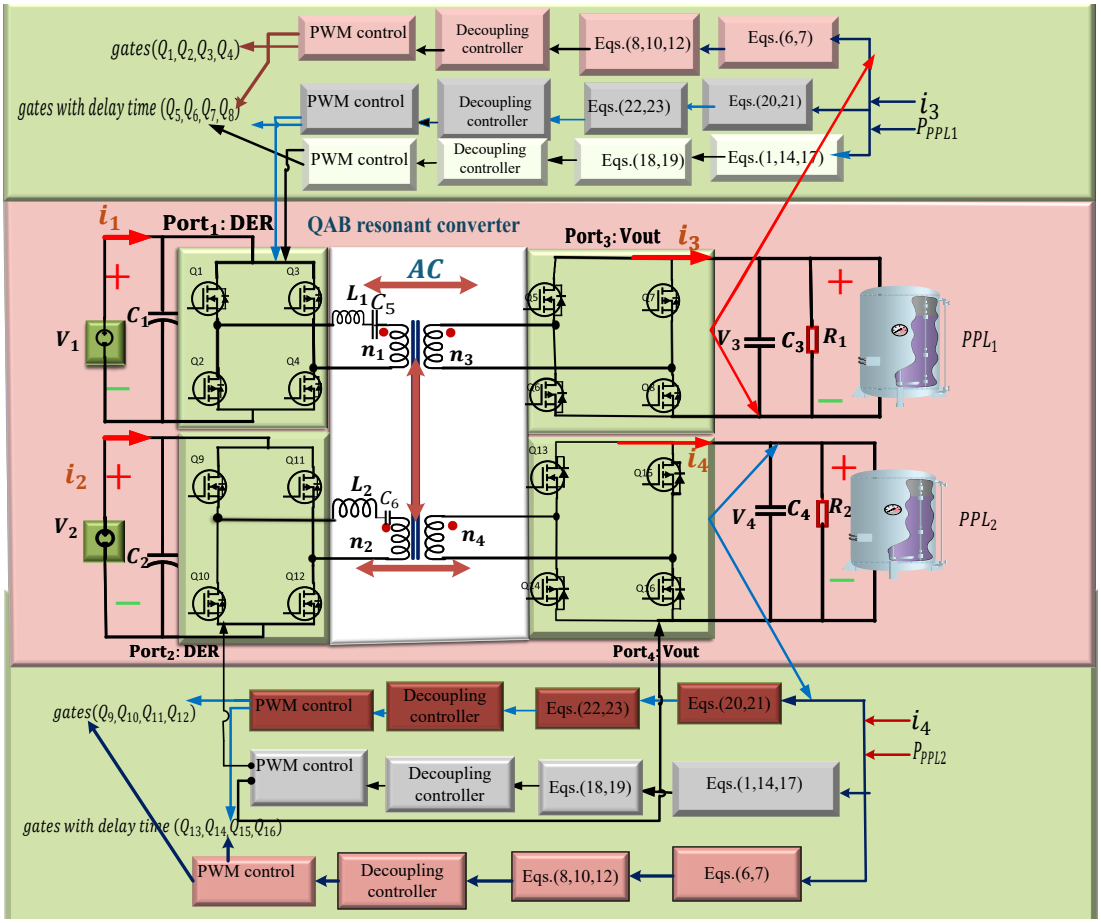


Figure 4.4: QAB converter with nonlinear controllers.

simulator (SIL). The three controllers (ASSOSMC, IHOSMC and CMPC–ISMC) were applied one at a time to the same converter, each with the feedforward decoupler of Eqs. (4.64)–(4.69), under the same test: 48 V regulation of ports 3 and 4 with resistive loads of 2 Ω, and a PPL step from 100 to 200 W at t = 1 s (port 3) and at t = 2 s (port 4). Table 4.2 lists the values used.

Performance indices. The comparison uses indices that are read directly from the voltage, current and power curves: the largest voltage change of each port after the PPL step (ΔV_3, ΔV_4), the change of the port current, the range of the control input, and the total efficiency $\eta_{\text{tot}} = (\bar{P}_3 + \bar{P}_4)/(\bar{P}_1 + \bar{P}_2)$, where $\bar{P}_1$–$\bar{P}_4$ are the port powers averaged over the same steady-state window for all controllers. Time-based indices (rise and

Table 4.2: Converter, test and controller settings.

Parameter	**Value**
Input voltages V_1, V_2	300 V
Reference voltages $V_{3,\mathrm{ref}}$, $V_{4,\mathrm{ref}}$; resistive loads	48 V; 2 Ω
Output filter capacitors C_3, C_4	95 μF
PPL step	100→200 W at t = 1 s (port 3) and t = 2 s (port 4)
Rated power per port	1500 W
MPC: sampling period, horizon	T_s = 1 ms, N = 10 (10 ms ahead)
MPC weights	$\mathbf{Q}^{(i)} = \mathbf{I}$, $R^{(i)} = 0.1$, $\mathbf{\Pi}^{(i)} = 2.2367\,\mathbf{I}$
ASSOSMC: $\mu_3 = \mu_4$, $\zeta_{\max,3} = \zeta_{\max,4}$	0.011, 0.5
IHOSMC: gain limits; voltage guard	0.7–1.35; $\tilde{v}_{c_i} \geq 5$ V
Efficiency window (steady state, all controllers)	t = 2.1166–2.8610 s

settling times) are not reported for this chapter, because the controllers act on a 1 ms sampling grid (MPC) and the earlier values, measured on the raw switching waveforms, were shorter than one control step.

4.4.2 Estimated State-Space Trajectories

Fig. 4.5 shows that the IHOSMC begins with a substantial initial error and exhibits sharp directional changes, indicating strong corrective action and possible chattering near the sliding surface. In contrast, the CMPC–ISMC shows a smooth, spiral-like convergence,

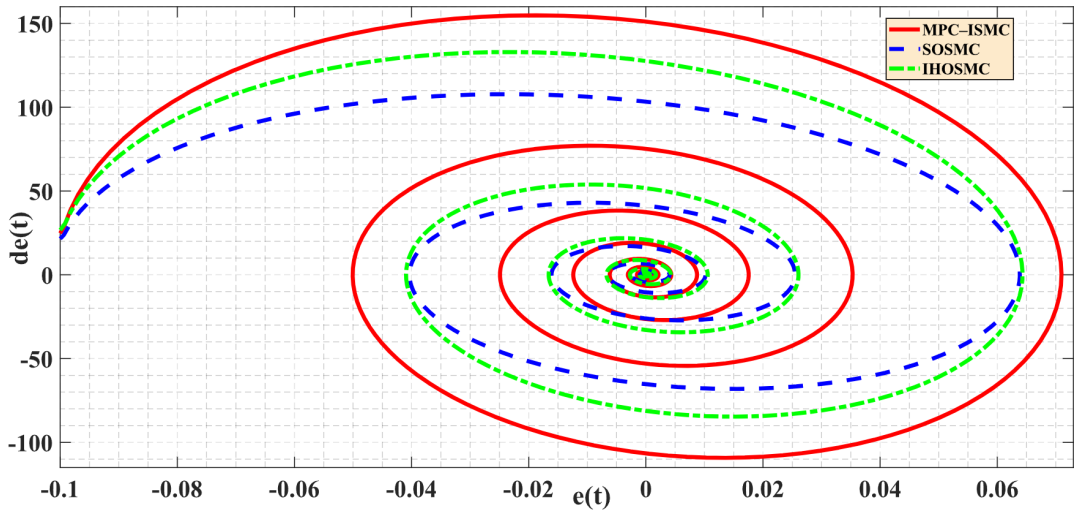


Figure 4.5: State-space trajectories of the three controllers.

reflecting its predictive nature and well-damped response. The ASSOSMC starts closer to the vertical axis and converges quickly with little oscillation.

4.4.3 Simulation Results of the ASSOSMC Controller

Fig. 4.6 shows that, when the PPL increases from 100 to 200 W, the voltage changes by $\Delta V_3 = 0.5$ V at port 3 ($t = 1$ s) and by $\Delta V_4 = 0.3$ V at port 4 ($t = 2$ s), while the port currents rise by about 5 A, from about 25 to 30 A. Fig. 4.7 shows the control inputs of

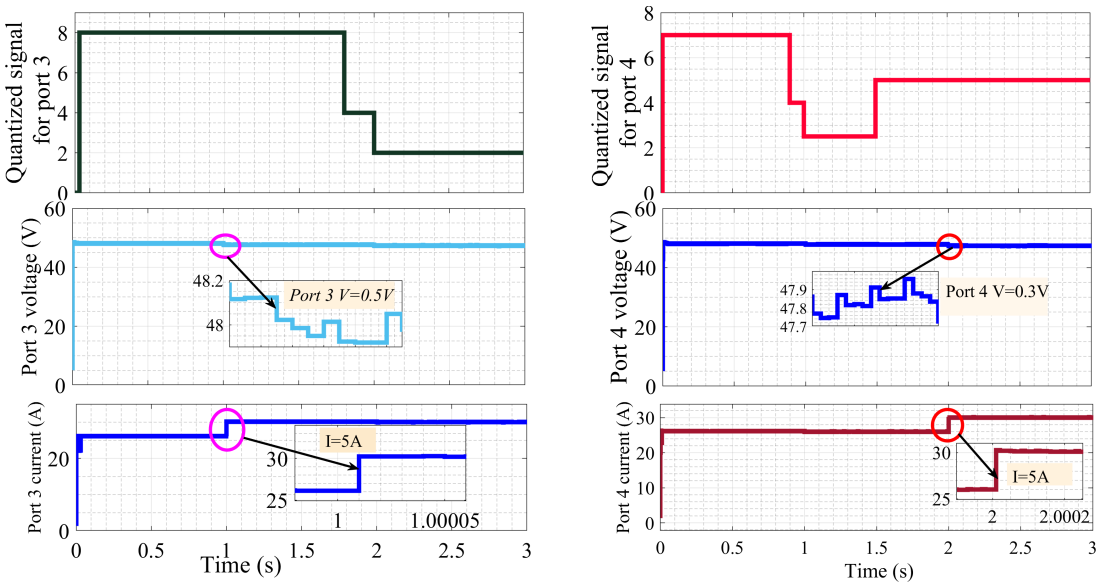


Figure 4.6: ASSOSMC: voltages and currents under the PPL step.

ports 3 and 4 during the same test. Before the PPL step at $t = 1$ s, the port-3 control input u_3 is constant at about 0.055. After the step from 100 to 200 W, the argument of the saturation function in Eq. (4.8) crosses the boundary layer repeatedly, so u_3 switches between about 0.055 and -0.028 (the dark band in Fig. 4.7); this is chattering of the ASSOSMC. The port-4 control input u_4 behaves in the same way after its PPL step at $t = 2$ s. The transferred power of each port rises from about 1250 to 1350 W at its step.

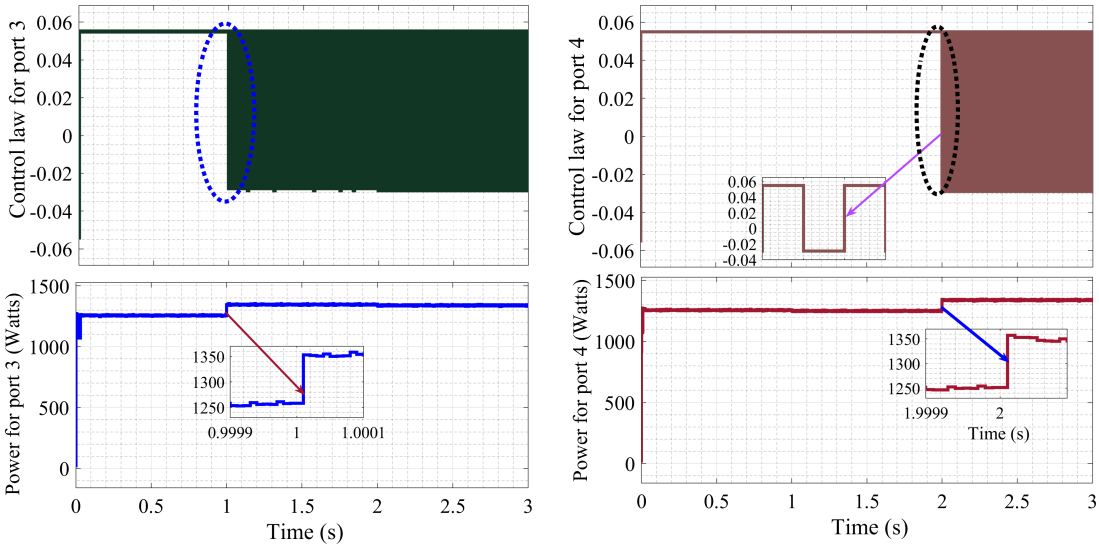


Figure 4.7: ASSOSMC: control inputs and powers under the PPL step.

4.4.4 Simulation Results of the IHOSMC Controller

Fig. 4.8 shows the voltages and currents of ports 3 and 4 with the IHOSMC. When the PPL at port 3 increases from 100 to 200 W at t = 1 s, the port-3 voltage drops by 3.0 V and the current rises by 2.5 A; when the PPL at port 4 increases at t = 2 s, the port-4 voltage drops by 2.8 V and the current rises by 2.6 A.

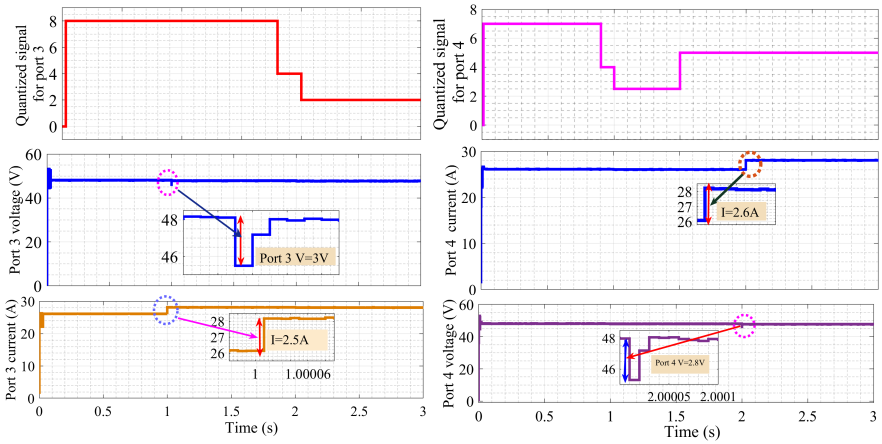


Figure 4.8: IHOSMC: voltages and currents under the PPL step.

Fig. 4.9 shows the corresponding control inputs. The port-3 control input u_3 changes to about 1.2 and then drops to about -2 at t = 2 s, whereas u_4 increases from about 1.5

to 2.1 at t = 2 s in response to the load increase. These are the largest control-input changes of the three controllers.

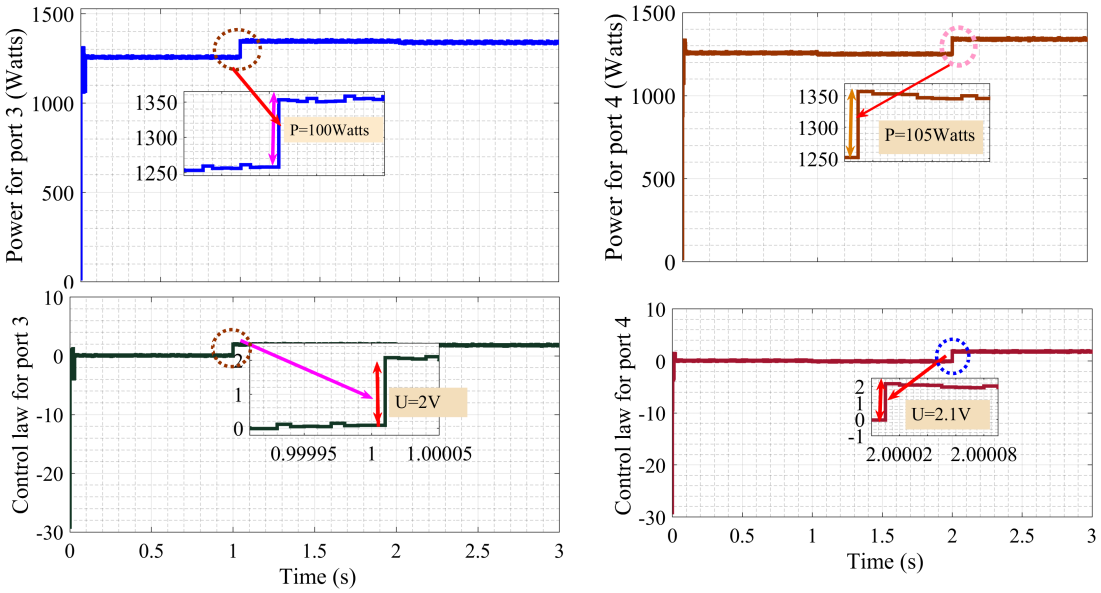


Figure 4.9: IHOSMC: control inputs of ports 3 and 4 (same test).

4.4.5 Simulation Results of the CMPC–ISMC Controller

Fig. 4.10 shows the voltages and currents with the CMPC–ISMC. After the PPL steps, the port-3 voltage drops by 3.5 V with a current increase of 2.4 A, and the port-4 voltage drops by 4.2 V with a current increase of 2.5 A.

Fig. 4.11 shows the control inputs of ports 3 and 4 with their active powers. The control input u_3 changes to about 0.2 and then decreases to about -0.1 at t = 2 s, while u_4 varies from about 0.25 to -0.4 as the load increases; the control inputs change smoothly, without the switching band of the ASSOSMC.

4.4.6 Comparison of the Three Controllers

Table 4.3 compares the three controllers in the simulation. The ASSOSMC keeps the voltage change smallest (0.5 and 0.3 V, against 3.0/2.8 V for the IHOSMC and 3.5/4.2 V

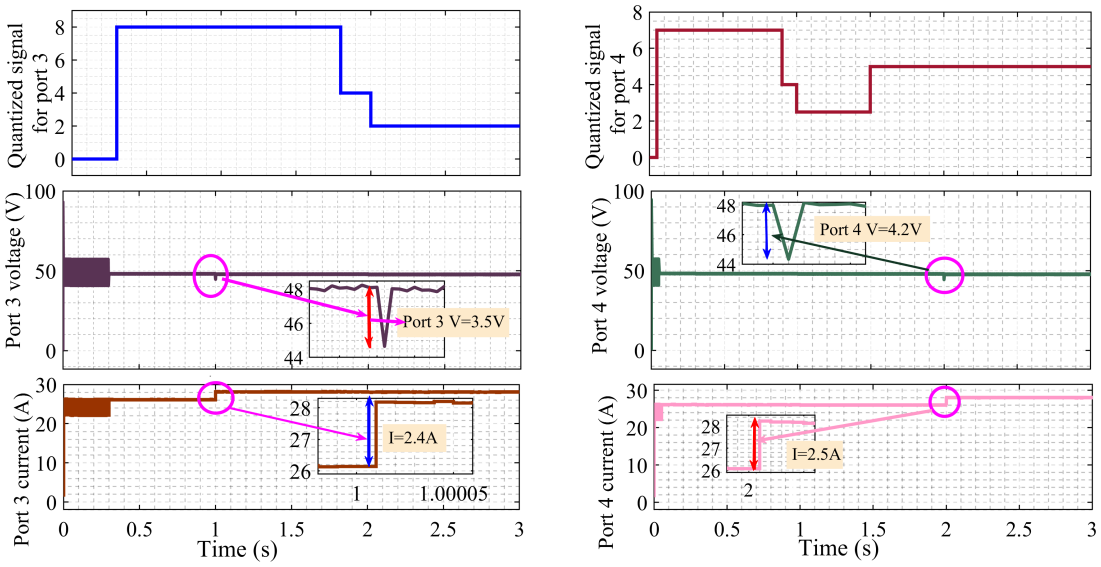


Figure 4.10: CMPC–ISMC: voltages and currents under the PPL step.

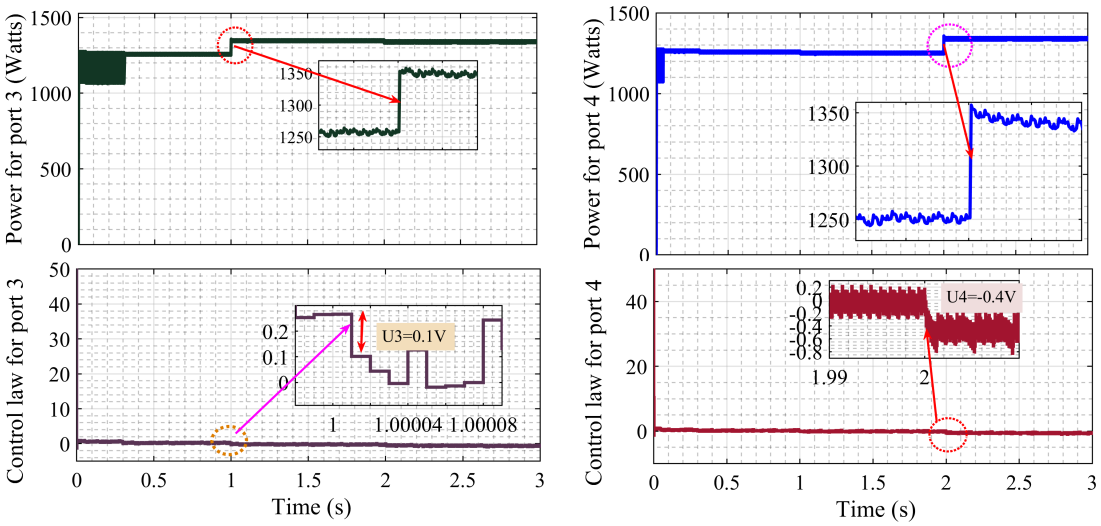


Figure 4.11: CMPC–ISMC: control inputs and active powers of ports 3 and 4 (same test).

for the CMPC–ISMC), at the cost of the largest current change (about 5 A) and a chattering control input. The CMPC–ISMC draws the smallest current change and has the smoothest control input, but the largest voltage change. The IHOSMC lies between them, with the largest control-input changes. Over the common steady-state window (t = 2.1166–2.8610 s), computed from the averaged port powers, the CMPC–ISMC has the highest total efficiency ($\eta_{\text{tot}} \approx 90.78\%$), followed closely by the ASSOSMC

(90.72%) and the IHOSMC (89.06%).

Table 4.3: Comparison of the three controllers.

Index	**ASSOSMC**	**IHOSMC**	**CMPC–ISMC**
Voltage change ΔV_3 / ΔV_4	**0.5 / 0.3 V**	3.0 / 2.8 V	3.5 / 4.2 V
Current change at the step	about 5 A	2.5 / 2.6 A	**2.4 / 2.5 A**
Control input	Chattering between 0.055 and -0.028	Largest changes	**Smooth, moderate**
Total efficiency η_{tot}	90.72%	89.06%	**90.78%**
Main weakness	Chattering of u; largest current change	Largest control effort	Largest voltage change

Simulation, PPL step 100→200 W at 48 V.

4.4.7 Execution on the OPAL-RT Simulator (Software-in-the-Loop)

The three controllers were also run on the OPAL-RT OP5700 simulator with the converter model (set-up in Fig. 3.15 of Chapter 3). This is a software-in-the-loop (SIL) test: the controller and the converter model run together on the simulator, and no real converter or separate controller board is involved. The input voltage is 300 V and the output voltage 48 V; the PPL is connected by a stair signal at t = 0.03 s (ports 1 and 3) and t = 0.01 s (ports 2 and 4) and then stepped from 100 to 200 W. The analog outputs of the simulator are scaled (the scaling of each signal is given with each figure).

4.4.7.1 Results of the ASSOSMC Controller

Fig. 4.12 presents the active power under stair-triggered PPLs. For ports 1 and 3, connecting the PPL at 0.03 s increases the transferred power from 1076 to 1265 W, and the PPL step from 100 to 200 W at 2 s raises it from 1260 to 1440 W.

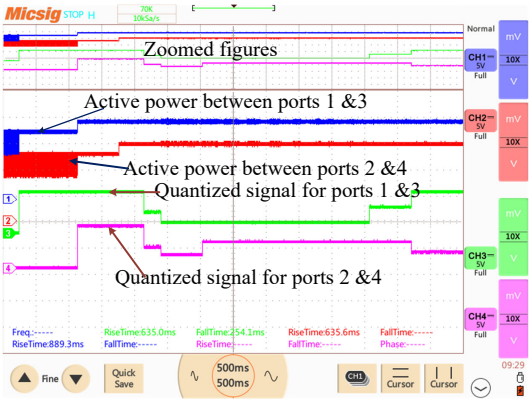


Figure 4.12: ASSOSMC on the OPAL-RT OP5700 (SIL): active power.

Figs. 4.13 and 4.14 show the transformer waveforms between ports 1 and 3 and between ports 2 and 4. The input voltage is 300 V (scaled by 1/30) and the output voltage 48 V (scaled by 1/5). The measured delay is 250 ns between ports 1 and 3 and 2.8 μs between ports 2 and 4, and the winding current is about 30 A (scaled by 1/5).

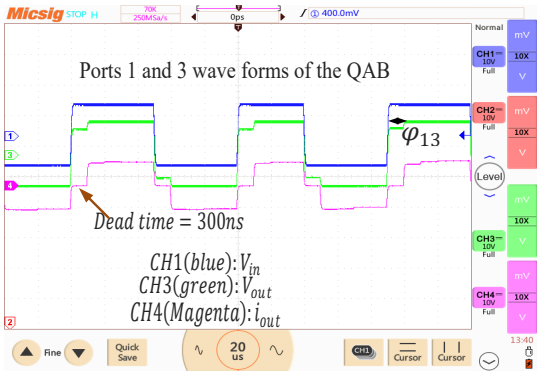


Figure 4.13: ASSOSMC (SIL): waveforms at ports 1 and 3.

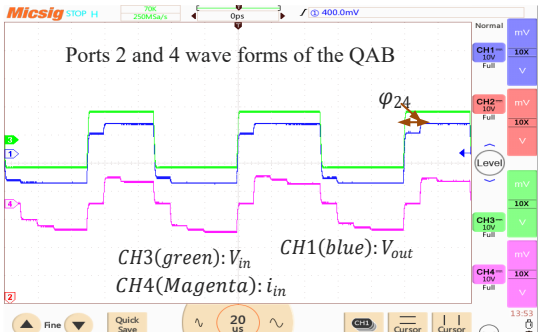


Figure 4.14: ASSOSMC (SIL): waveforms at ports 2 and 4.

4.4.7.2 Results of the IHOSMC Controller

Fig. 4.15 presents the active power under stair-triggered PPLs. For ports 1 and 3, the quantised PPL steps increase the transferred power from 1080 to 1260 W at 0.03 s and to 1350 W at 1 s, when the PPL rises from 100 to 200 W. For ports 2 and 4, a similar PPL profile raises the active power from 1080 to 1264 W at 0.01 s and to 1387 W at 2 s, close to the rated 1500 W.

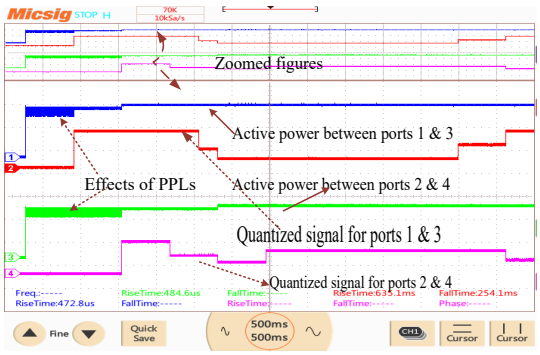


Figure 4.15: IHOSMC on the OPAL-RT OP5700 (SIL): active power.

Figs. 4.16 and 4.17 show the transformer waveforms with a 300 V input (scaled by 1/27) and a 48 V output (scaled by 1/5). The model includes a dead time of 330 ns; the phase shifts between the bridges are 0.02–0.08 rad, and the measured delay between the ports is 290 ns.

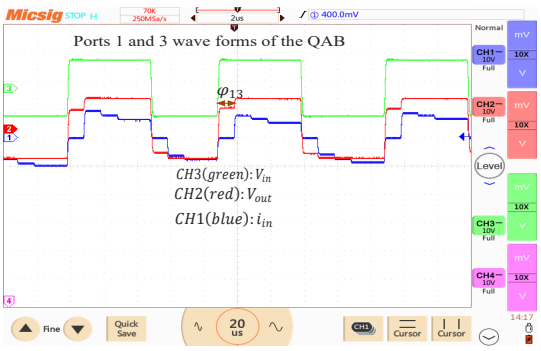


Figure 4.16: IHOSMC (SIL): waveforms at ports 1 and 3.

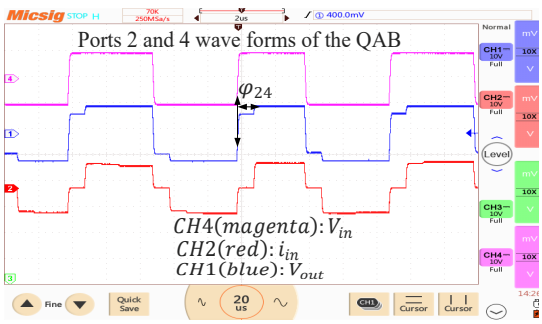


Figure 4.17: IHOSMC (SIL): waveforms at ports 2 and 4.

4.4.7.3 Results of the CMPC–ISMC Controller

Fig. 4.18 presents the active power under quantised PPL steps. For ports 1 and 3, the stair-triggered PPL increases the transferred power from 1070 to 1260 W at 0.03 s and to 1345 W at 1 s, when the PPL rises from 100 to 200 W. For ports 2 and 4, the stair PPL profile raises the active power from 1080 to 1260 W at 0.01 s when the PPL is connected.

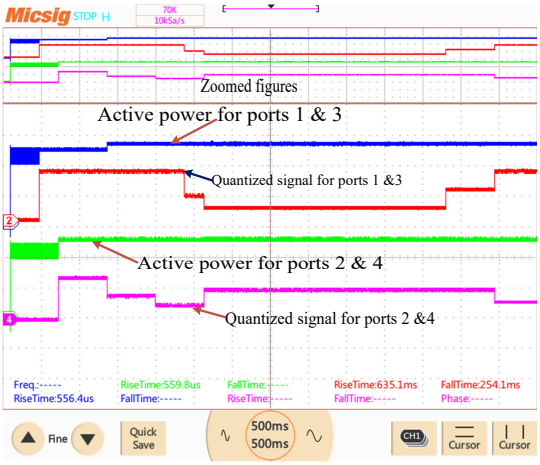


Figure 4.18: CMPC–ISMC on the OPAL-RT OP5700 (SIL): active power.

Figs. 4.19 and 4.20 show the transformer waveforms with a 300 V input (scaled by 1/27) and a 48 V output (scaled by 1/5). The model includes a dead time of 350 ns, and the phase shifts between the bridges are 0.01–0.05 rad.

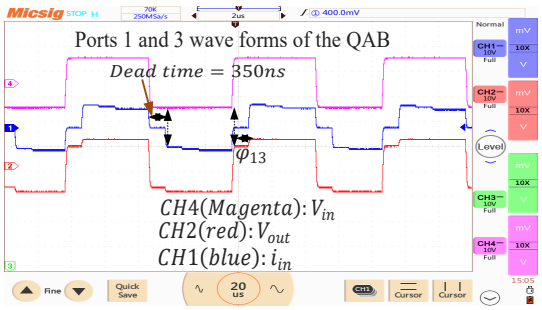


Figure 4.19: CMPC–ISMC (SIL): waveforms at ports 1 and 3.

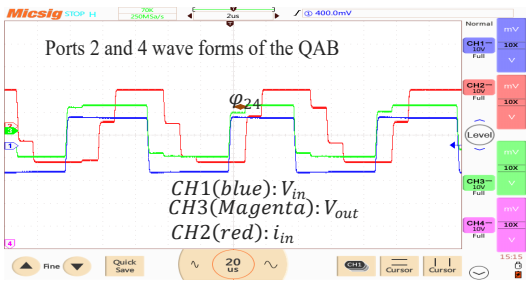


Figure 4.20: CMPC–ISMC (SIL): waveforms at ports 2 and 4.

4.5 Summary

This chapter compared three nonlinear controllers customised for a QAB resonant converter whose ports 3 and 4 supply PPLs: the ASSOSMC, the IHOSMC and the CMPC–ISMC, each with the same feedforward decoupler. It addresses Research

Objectives 2 and 3 (effect of the loads and comparison of controllers). For a PPL step from 100 to 200 W at 48 V, the ASSOSMC kept the voltage change smallest (0.5/0.3 V, against 3.0/2.8 V for the IHOSMC and 3.5/4.2 V for the CMPC–ISMC) at almost the same total efficiency as the CMPC–ISMC (90.72% against 90.78%; IHOSMC 89.06%), but with the largest current change and a chattering control input. The CMPC–ISMC gave the smoothest control input and the smallest current change, at the cost of the largest voltage change. *Limits:* one pulsed-load pattern was tested; the results come from simulation and from SIL runs on the OPAL-RT simulator, and the controllers were not tested on QAB hardware.

Chapter 5

Systematic Disturbance-Rejection Methods for DAB Converters and their SIL Validation

5.1 Introduction

Ensuring robust voltage regulation in DAB converters for DC MGs remains a challenge, particularly under CPLs, which reduce system damping and cause voltage oscillations [28, 166]. Model complexity, parameter drift and uncertain disturbances make reliable control harder [131, 167]. Advanced phase-shift strategies and resonant topologies such as the LLC and SRC can improve performance, but they often make the system more complex and may not cope with fast-changing conditions [137, 145, 168]. The negative incremental impedance from CPLs can result in instability, increased switching losses, and reduced system efficiency, especially during load transients [169, 170]. To address these limitations, this chapter derives a variable-gain sliding mode control (VGSMC) for the DAB and compares four disturbance-rejection methods built on it or benchmarked against it: the VGSMC without a disturbance estimate, the VGSMC with a linear

extended state observer (SMC–LESO), the VGSMC with a physics-informed neural network (PINN) disturbance estimator (PINN–SMC), and a twisting second-order sliding mode control (TSOSMC).

Chapter objectives.

(i) Derive the VGSMC step by step from the weaknesses of the conventional reaching laws, and prove its stability.

(ii) Design a PINN that estimates the unknown disturbance current at the output node, trained with data and with the physics of the node, and use it inside the VGSMC (PINN–SMC).

(iii) Compare the VGSMC, the SMC–LESO, the PINN–SMC and the TSOSMC under the same test scenarios, gains and limits in simulation, and check the stability of each closed loop with the minor-loop gain.

(iv) Run the controllers on the OPAL-RT OP5700 simulator (SIL).

Main contribution of this chapter: C4 (the VGSMC and the PINN disturbance estimator for the DAB with CPLs), as listed in Section 1.5.

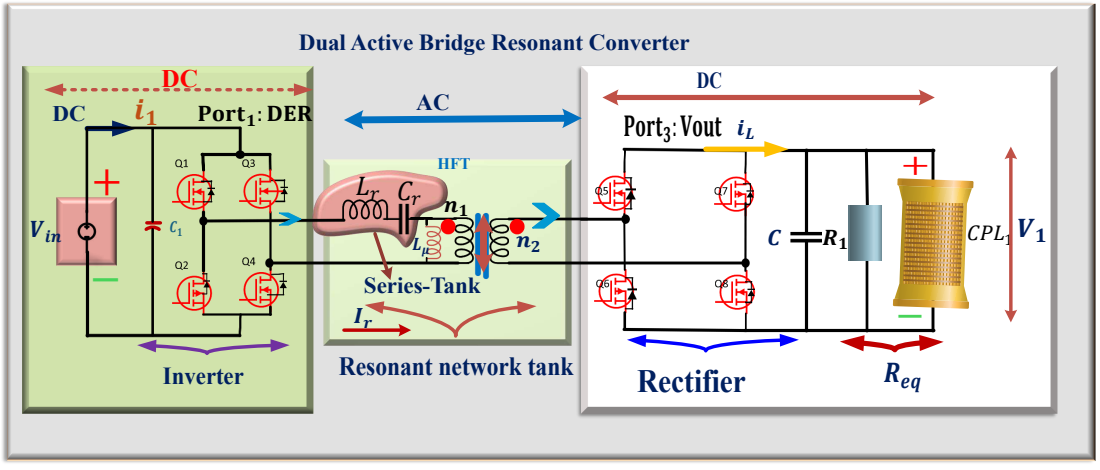


Figure 5.1: Resonant DAB converter supplying a CPL.

5.2 Modelling of the DAB Resonant Converter

The equivalent resistance R_{eq} of the converter of Fig. 5.1 is found with the first-harmonic approximation, in which the resonant tank is driven by the fundamental components of the square-wave bridge voltages and the output rectifier with its load is replaced by an equivalent ac resistance. The fundamental component of the rectifier input current, referred to the primary side, is given by:

$$I_r(t) = \frac{n\pi I_0}{2} \sin(\omega t), \tag{5.1}$$

and the fundamental component of the rectifier input voltage, referred to the primary side, is given by:

$$V_r(t) = \frac{4V_0}{n\pi} \sin(\omega t), \tag{5.2}$$

where V_0 and I_0 are the dc output voltage and current, $n = N_s/N_p$ is the transformer turns ratio, and ω is the switching angular frequency. Since $V_r(t)$ and $I_r(t)$ are in phase, the equivalent resistance is their ratio, as given by:

$$R_{\text{eq}} = \frac{V_r(t)}{I_r(t)} = \frac{\dfrac{4V_0}{n\pi}}{\dfrac{n\pi I_0}{2}} = \frac{8V_0}{n^2\pi^2 I_0} = \frac{8R_{\text{load}}}{n^2\pi^2}, \tag{5.3}$$

where $R_{\text{load}} = V_0/I_0$ is the dc load resistance. With the transformer ratio n, the transfer function from the input to the output voltage of Fig. 5.1 is:

$$H(j\omega) = n \frac{R_{\text{eq}}}{R_{\text{eq}} + j\omega L_r + \dfrac{1}{j\omega C_r}}, \tag{5.4}$$

where L_r and C_r are the inductance and capacitance of the series resonant tank. The characteristic impedance R_0, the resonant angular frequency ω_0, and the quality factor Q of the tank are:

$$R_0 = \sqrt{\frac{L_r}{C_r}}, \qquad \omega_0 = \frac{1}{\sqrt{L_r C_r}}, \qquad Q = \frac{R_0}{R_{\text{eq}}}. \tag{5.5}$$

Since $\omega L_r - 1/(\omega C_r) = R_0\,(\omega/\omega_0 - \omega_0/\omega)$, dividing the numerator and denominator of Eq. (5.4) by R_{eq} simplifies the transfer function and its magnitude to:

$$H(j\omega) = \frac{n}{1 + jQ\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right)}, \qquad \left|H(j\omega)\right| = \frac{n}{\sqrt{1 + Q^2\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right)^2}}. \tag{5.6}$$

The impedance of the series resonant tank in Fig. 5.1 is:

$$Z_1(s) = sL_r + \frac{1}{sC_r}, \tag{5.7}$$

where s is the Laplace variable ($s = j\omega$ in the frequency domain). The dc load is modelled as a fixed resistance in parallel with a constant power load (CPL), so that the load resistance used in Eq. (5.3) is:

$$R_{\text{load}} = \left(\frac{1}{R_{\text{fixed}}} + \frac{1}{R_{\text{CPL}}}\right)^{-1}, \tag{5.8}$$

where R_{fixed} is the fixed resistive load and R_{CPL} is the equivalent resistance of the CPL at the operating point. The input impedance of the resonant DAB converter of Fig. 5.1 is then:

$$Z_{\text{in}}(s) = Z_1(s) + R_{\text{eq}}. \tag{5.9}$$

The minor-loop gain shows how the converter impedance interacts with the load. A large value can cause instability, especially with CPLs, whereas a smaller value improves stability but may slow the response. The transfer function from source to load (voltage divider) and the corresponding minor loop gain are given by:

$$H_{\text{div}}(s) = \frac{R_{\text{eq}}}{Z_1(s) + R_{\text{eq}}} = \frac{1}{1 + T_{\text{minor}}(s)}, \tag{5.10}$$

$$T_{\text{minor}}(s) = \frac{Z_1(s)}{R_{\text{eq}}}. \tag{5.11}$$

The Q-factor is a measure of resonance sharpness and damping: a high value ($Q > 5$) indicates a potential for oscillation (underdamped), a low value ($Q < 0.5$) an overdamped and sluggish response, and a moderate value ($Q \approx 1$) a good balance between the two. The normalised resonant gain $|G(j\omega)| = |H(j\omega)|/n$, which shows how the gain varies

with different Q values, peaks at $\omega = \omega_0$, and its sharpness is controlled by Q, as given by:

$$\left|G(j\omega)\right| = \frac{1}{\sqrt{1 + Q^2\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}}. \tag{5.12}$$

The minor-loop gain $T_{\text{minor}}(s)$ shows how the interaction between source and load varies with frequency and is used to assess stability. The transfer function $H(s)$ shows how the input voltage is transferred to the output. The input impedance $Z_{\text{in}}(s)$ shows how the converter appears to the source for different CPL values, and $Z_1(s)$ is the impedance of the resonant tank. The equivalent resistance R_{eq} combines the CPL and the resistive load and affects the power flow and the damping. Table 5.1 provides a ranked evaluation of 19 resonant converter configurations.

Each performance metric (number of components, voltage stress, converter complexity, control complexity, cost, power density, input/output voltage range, efficiency and stability analysis) is scored from 1 (lowest) to 5 (highest), and 0 means not applicable (N/A). Fig. 5.2 rates an example resonant DAB converter against eleven criteria. It scores well on control complexity, input and output voltage range, efficiency and stability, which are important for reliable DC microgrids, but only moderately on cost and voltage stress. The chart shows the trade-offs between the design aspects and the need for a well-balanced control strategy. The controllers of this chapter (VGSMC, SMC–LESO, PINN–SMC and TSOSMC) address the shortcomings of the conventional techniques in stability, chattering and dynamic adaptability.

5.3 Variable-Gain Sliding Mode Control (VGSMC)

A key limitation of conventional SMC is chattering, i.e. high-frequency oscillations around the sliding surface that cause switching losses and performance degradation; the reaching law determines how fast and how smoothly the system reaches the sliding

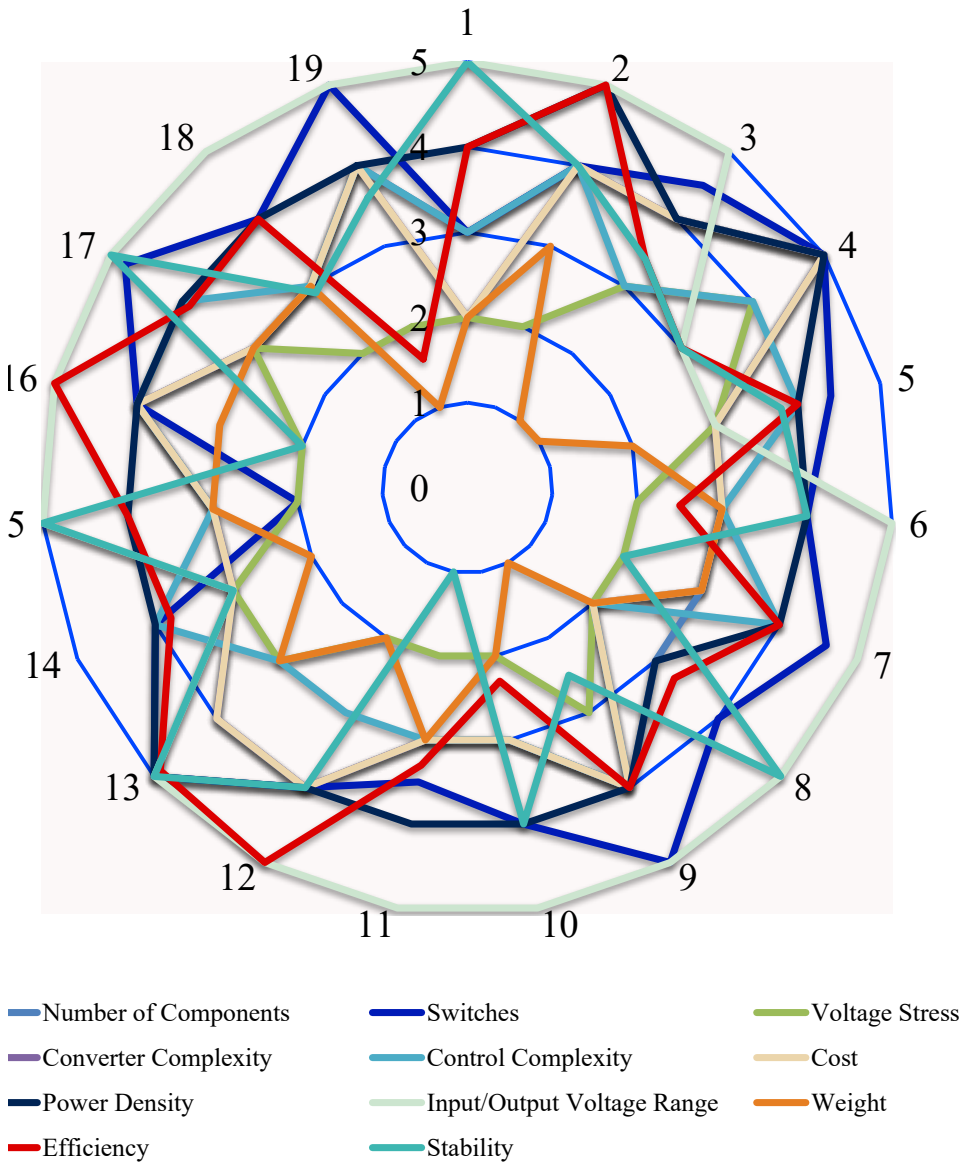


Figure 5.2: Performance analysis of resonant converter configurations.

Table 5.1: Ranked performance of DAB resonant converters.

No.	Ref.	Number of Components	Switches	Voltage Stress	Converter Complexity	Control Complexity	Cost	Power Density	Input/Output Voltage Range	Weight	Efficiency	Stability
1	[172]	Moderate	4	Low	Low	Medium	Low	High	Wide	Light	High	Good
2	[173]	High	>4	Low	High	High	Very High	Wide	Medium	High	Good	Good
3	[174]	High	6+	Medium	High	Medium	High	Wide	Heavy	High	Good	Good
4	[28]	Very High	Many	High	Very High	High	Very High	Moderate	Moderate	Heavy	Moderate	Moderate
5	[175]	Medium	8	Medium	Medium	High	Medium	High	Moderate	Light	High	Good
6	[176]	Moderate	8	Low	Medium	Medium	Medium	High	Wide	Medium	High	Good
7	[177]	Moderate	8	Low	Medium	High	Medium	High	Wide	Medium	High	Good
8	[178]	Moderate	8	Low	Low	Low	Low	Medium	Wide	Light	High	Excellent
9	[179]	High	>8	Medium	High	High	High	High	Wide	Heavy	High	Good
10	[180]	Moderate	8	Low	Medium	Medium	Medium	High	Wide	Light	High	Good
11	[181]	Moderate	8	Low	Medium	Medium	Medium	High	Wide	Medium	High	Good
12	[166]	High	8	Low	High	Medium	High	High	Wide	Light	Very High	Good
13	[167]	High	>8	Medium	High	Medium	High	Very High	Very Wide	Medium	Very High	Excellent
14	[168]	Medium	6–8	Medium	Medium	High	Medium	High	Moderate	Light	High	Good
15	[169]	Moderate	8	Low	Medium	Medium	Medium	High	Wide	Medium	High	Excellent
16	[170]	High	8	Low	High	High	High	High	Wide	Medium	Very High	Good
17	[182]	Moderate	8	Medium	Medium	High	Medium	High	Wide	Medium	High	Good
18	[183]	Medium	8	Low	Medium	Medium	Medium	High	Wide	Medium	High	Good
19	[184]	High	8+	Low	High	High	High	High	Wide	Heavy	High	Excellent

surface [122, 171]. This section derives, step by step, a variable-gain reaching law that removes the weaknesses of the conventional reaching laws of Chapter 2. The resulting VGSMC is the common law of the three SMC-based controllers of this chapter: the VGSMC itself uses no disturbance estimate, and the SMC–LESO and the PINN–SMC add the estimate of the LESO (Section 5.3.5) or of the PINN (Section 5.4.5).

5.3.1 Output-Node Model and Current-to-Phase Map

Step 1 – the converter. The current balance at the output capacitor, with a resistive load, a CPL and an unknown disturbance current d_i (losses, parameter changes, unknown load), is:

$$C\,\dot{V}_0 = i_o - \frac{V_0}{R} - \frac{P_{\mathrm{CPL}}}{V_0} - d_i, \tag{5.13}$$

where C is the output capacitance, V_0 the output voltage, i_o the average current delivered by the DAB to the output node, R the resistive load and P_{CPL} the CPL power. With the first-harmonic approximation of Section 5.2, the fundamental bridge voltages $\hat{v}_1 = 4V_{\mathrm{in}}/\pi$ and $\hat{v}_2 = 4nV_0/\pi$ exchange power through the net reactance of the tank, $X = \omega_s L_{\mathrm{eq}} - 1/(\omega_s C_r)$, where $L_{\mathrm{eq}} = L_r + L_{\mathrm{lk1}} + n^2 L_{\mathrm{lk2}}$ is the total series inductance and $\omega_s = 2\pi f_s$:

$$P = \frac{\hat{v}_1 \hat{v}_2 \sin\varphi}{2X} = \frac{8nV_{\mathrm{in}}V_0}{\pi^2 X}\sin\varphi, \qquad i_o = \frac{P}{V_0} = K\sin\varphi, \qquad K = \frac{8nV_{\mathrm{in}}}{\pi^2 X}, \tag{5.14}$$

where φ is the phase shift between the two bridges and K is the largest output current, reached at $\varphi = 90°$ ($K = 42$ A at 300 V for the converter of Table 5.3). Every controller of this chapter first computes the current $i_{o,\mathrm{ref}}$ that it needs and then turns it into a phase shift with the same map, allowing only forward power:

$$\varphi = \arcsin\Big(\min\Big\{\max\Big\{\frac{i_{o,\mathrm{ref}}}{K}, 0\Big\}, 1\Big\}\Big), \qquad \varphi \in [0, \pi/2], \tag{5.15}$$

with K calculated from the measured input voltage. This map replaces the inner current loop of a dc-inductor converter, which the resonant DAB does not have.

5.3.2 Sliding Variable and the Limits of the Conventional Reaching Laws

Step 2 – the sliding variable. With the voltage error $e = V_{\mathrm{ref}} - V_0$, the sliding variable adds the integral of the error:

$$s = e + \zeta \int_0^t e\, d\tau, \qquad \zeta > 0. \tag{5.16}$$

When $s = 0$, $\dot{e} = -\zeta e$, so the error decays with the time constant $1/\zeta$. The integral makes a constant disturbance leave no lasting voltage error: in Laplace form $E(p) = \frac{p}{p+\zeta} S(p)$, so e goes to zero even if s stays at a small constant.

Step 3 – how s changes. For a constant reference, $\dot{e} = -\dot{V}_0$, and Eq. (5.13) gives:

$$\dot{s} = -\frac{1}{C}\Big(i_o - \frac{V_0}{R} - \frac{P_{\mathrm{CPL}}}{V_0} - d_i\Big) + \zeta e. \tag{5.17}$$

Setting $\dot{s} = 0$ gives the current that would keep s at zero, $i_{o,\mathrm{eq}} = V_0/R + P_{\mathrm{CPL}}/V_0 + d_i + C\zeta e$. Since R, P_{CPL} and d_i are not known exactly, the controller uses nominal values R_n, P_n, C_n, and an estimate $\hat{d}_i$ of the disturbance ($\hat{d}_i = 0$ in the VGSMC). Everything that the controller does not know is collected in one term:

$$\Delta = \frac{1}{C}\Big[\Big(\frac{V_0}{R} - \frac{V_0}{R_n}\Big) + \Big(\frac{P_{\mathrm{CPL}}}{V_0} - \frac{P_n}{V_0}\Big) + \big(d_i - \hat{d}_i\big)\Big], \qquad |\Delta| \le \bar{\Delta}. \tag{5.18}$$

Step 4 – constant-rate reaching law (CRRL, Eq. (2.12)*).* Asking for $\dot{s} = -\varepsilon\,\mathrm{sgn}(s)$ gives $\dot{s} = -\varepsilon\,\mathrm{sgn}(s) + \Delta$ and, with $\mathcal{V} = \frac{1}{2}s^2$:

$$\dot{\mathcal{V}} = s\dot{s} \le -(\varepsilon - \bar{\Delta})\,|s|, \qquad t_r \le \frac{|s(0)|}{\varepsilon - \bar{\Delta}}. \tag{5.19}$$

Its weaknesses are: (L1) it works only if $\varepsilon > \bar{\Delta}$, so the gain must be as large as the worst disturbance and is used all the time, even near $s = 0$; (L2) the sign function jumps between -1 and $+1$, and because the controller runs in steps of T_s, s cannot stay at zero but jumps around it in a band of about εT_s [185], so the phase command chatters; (L3) s approaches zero at the same speed whether it is far or near, so a fast response from far away needs a large ε, which makes (L1) and (L2) worse.

Step 5 – constant-plus-proportional reaching law (CPPRL, Eq. (2.8)*).* Adding a term proportional to s, $\dot{s} = -\varepsilon\,\mathrm{sgn}(s) - \gamma s$, gives the reaching time (for $\Delta = 0$) $t_r = \frac{1}{\gamma}\ln\big(1+\gamma|s(0)|/\varepsilon\big)$, so s moves faster when it is far from zero and ε can be smaller. Two weaknesses remain: (L4) near zero the sign term still dominates, so the law still chatters; (L5) γ has one fixed value: a large γ amplifies sensor noise, because s contains the measured voltage, and a small γ is slow.

Step 6 – boundary layer. Replacing $\mathrm{sgn}(s)$ by $\mathrm{sat}(s/\vartheta)$, which equals s/ϑ inside the band $|s| \le \vartheta$ and ± 1 outside it, removes the jumps (L2, L4). Inside the band the law is linear, $\dot{s} = -(\varepsilon/\vartheta + \gamma)s + \Delta$, and s stays in the small band $|s| \le \bar{\Delta}/(\varepsilon/\vartheta + \gamma)$ instead of reaching zero exactly. The saturation function is:

$$\mathrm{sat}(x) = \begin{cases} x, & |x| \le 1, \\ \mathrm{sign}(x), & |x| > 1. \end{cases} \tag{5.20}$$

5.3.3 Variable-Gain Reaching Law and Control Law

Step 7 – variable gains. To remove the fixed trade-off between speed and noise, both gains are made to depend on the distance from the sliding surface:

$$\varepsilon(s) = \varepsilon_0 + \alpha|s|, \qquad \gamma(s) = \gamma_0 + \beta|s|, \qquad \varepsilon_0, \gamma_0 > 0,\ \alpha, \beta \ge 0, \tag{5.21}$$

which gives the variable-gain reaching law:

$$\dot{s} = -\big(\varepsilon_0 + \alpha|s|\big)\,\mathrm{sat}\Big(\frac{s}{\vartheta}\Big) - \big(\gamma_0 + \beta|s|\big)\,s. \tag{5.22}$$

Far from the surface the gains are large, so s returns quickly (L3, L5); near the surface they fall back to the small base values ε_0 and γ_0, so there is little chattering and little noise (L1, L2, L5). Unlike the power-rate reaching law (PRRL, Eq. (2.10)), there is no sign jump; and unlike integral-type adaptive gains ($\dot{\varepsilon} = \rho|s|$), the gains depend only on the present s, so they stay bounded whenever s is bounded.

Step 8 – the control law. Setting Eq. (5.17), written with the nominal values and the

estimate $\hat{d}_i$, equal to Eq. (5.22) and solving for the current gives:

$$i_{o,\mathrm{ref}} = \frac{V_0}{R_n} + \frac{P_n}{V_0} + \hat{d}_i + C_n\Big(\zeta e + \big(\varepsilon_0 + \alpha|s|\big)\mathrm{sat}\Big(\frac{s}{\vartheta}\Big) + \big(\gamma_0 + \beta|s|\big)s\Big). \tag{5.23}$$

The first two terms give the expected load current, $C_n\zeta e$ cancels the integral part of $\dot{s}$, and the last two terms are the variable-gain reaching action. The VGSMC uses $\hat{d}_i = 0$; the SMC–LESO and the PINN–SMC use the same law with $\hat{d}_i$ from the LESO or the PINN.

Step 9 – from current to phase shift. The current command is turned into the phase shift by Eq. (5.15). When φ is at its limit, the integral in s is paused (anti-windup), so that it does not build up. The controller runs every $T_s = 10\ \mu$s with a delay of one step.

5.3.4 Stability of the VGSMC

Step 10 – Lyapunov analysis. Without saturation of φ and with $C = C_n$, Eqs. (5.17) and (5.23) give $\dot{s} = -\varepsilon(s)\,\mathrm{sat}(s/\vartheta) - \gamma(s)s + \Delta$. With $\mathcal{V} = \frac{1}{2}s^2$ and $|s| > \vartheta$:

$$\dot{\mathcal{V}} = s\dot{s} \le -|s|\,g(|s|), \qquad g(r) = \beta r^2 + (\alpha + \gamma_0)\,r + \varepsilon_0 - \bar{\Delta}. \tag{5.24}$$

$\mathcal{V}$ decreases whenever $g(|s|) > 0$. If $\varepsilon_0 > \bar{\Delta}$, g is always positive, $\frac{d}{dt}|s| \le -(\varepsilon_0 - \bar{\Delta})$, and s reaches the boundary layer within $(|s(0)| - \vartheta)/(\varepsilon_0 - \bar{\Delta})$. If $\varepsilon_0 \le \bar{\Delta}$, g is positive for $|s| > r^*$, with

$$r^* = \frac{-(\alpha + \gamma_0) + \sqrt{(\alpha + \gamma_0)^2 + 4\beta(\bar{\Delta} - \varepsilon_0)}}{2\beta}, \tag{5.25}$$

so $|s|$ still decreases until it is inside $|s| \le \max\{\vartheta, r^*\}$. This is the key difference from the CRRL of Step 4: the loop stays stable even when the small base gain ε_0 is smaller than the worst disturbance (L1). A larger disturbance only widens the final band a little, and larger α, β or γ_0 make it narrower. Inside the band, $\dot{s} = -k(s)s + \Delta$ with $k(s) \ge k_{\mathrm{in}} = \varepsilon_0/\vartheta + \gamma_0$, so $|s|$ ends below $\bar{\Delta}/k_{\mathrm{in}}$, and by Step 2 the voltage error still goes to zero. If the real C differs from C_n, the reaching terms are multiplied by $C_n/C > 0$, which does not change the result.

Step 11 – gain values. ζ = 60 s^{-1}, so the error decays with the time constant $1/\zeta$ = 16.7 ms. ϑ = 0.5 V, about 1% of 48 V, inside the ±2% settling band. ε_0 = 30 V/s and γ_0 = 250 s^{-1}: inside the band s decays at k_{in} = 310 s^{-1} (time constant 3.2 ms), about five times faster than ζ, so s settles before e, and much slower than the 13.5 kHz switching and the 100 kHz sampling. α = 5 s^{-1} and β = 20 (V s)$^{-1}$: for a 12 V reference step ($|s|$ = 12 V), ε = 90 V/s and γ = 490 s^{-1}. At this point the controller asks for $C_n\gamma(s)s \approx 56$ A, but the converter can give at most $K \approx 42$ A, so φ goes to its limit of 90°; after a reference step the speed is therefore set by the converter, not by the gains.

Step 12 – the weakness that remains. Without an estimate ($\hat{d}_i = 0$), an unknown load current stays in Δ. Then s settles at a non-zero value, and the voltage error is removed only through the slow integral term, with the time constant $1/\zeta \approx 17$ ms. When the controller receives an estimate $\hat{d}_i \approx d_i$, this part of Δ is cancelled directly. This is why the disturbance estimators of the next sections are added. Table 5.2 summarises the steps.

Table 5.2: From the conventional reaching laws to the VGSMC.

Reaching law	**Form**	**Good point**	**Weakness**
Constant rate (CRRL)	$\dot{s} = -\varepsilon\,\mathrm{sgn}(s)$	Reaches zero in finite time	ε must exceed the worst disturbance at all times; chattering; same speed near and far
Constant plus proportional (CPPRL)	$\dot{s} = -\varepsilon\,\mathrm{sgn}(s) - \gamma s$	Faster when far from zero	Chattering near zero; one fixed γ trades speed against noise
Power rate (PRRL)	$\dot{s} = -k\lvert s\rvert^{a}\mathrm{sgn}(s)$	Softer near zero	Still jumps; slow when far if k is small
Boundary layer	$\mathrm{sgn} \to \mathrm{sat}(s/\vartheta)$	Smooth control, no chattering	Small band instead of zero; fixed gains
Variable gain (VGSMC)	$\dot{s} = -(\varepsilon_0 + \alpha\lvert s\rvert)\mathrm{sat}(s/\vartheta) - (\gamma_0 + \beta\lvert s\rvert)s$	Strong when far, gentle when near; bounded gains; ε_0 need not exceed the worst disturbance	An unknown load is removed only by the slow integral (Step 12)

5.3.5 Linear Extended State Observer (LESO)

The LESO estimates the disturbance current d_i of Eq. (5.13) from the measured output voltage [127, 128]. With the nominal model, Eq. (5.13) is written as $\dot{V}_0 = \frac{1}{C_n}\big(i_o - V_0/R_n - P_n/V_0\big) - x_2$, where the extended state $x_2 = d_i/C_n$ (plus the model error) is unknown but has a bounded rate. The observer copies this model and corrects it with the voltage error:

$$\dot{z}_1 = \frac{1}{C_n}\Big(i_o - \frac{V_0}{R_n} - \frac{P_n}{V_0}\Big) - z_2 + \beta_1(V_0 - z_1), \qquad \dot{z}_2 = -\beta_2(V_0 - z_1), \qquad \hat{d}_i = C_n z_2, \tag{5.26}$$

where z_1 is the estimate of V_0, z_2 the estimate of the disturbance divided by C_n, and β_1, β_2 the observer gains. The estimation errors $\tilde{v} = V_0 - z_1$ and $\tilde{x}_2 = x_2 - z_2$ obey $\dot{\tilde{v}} = -\tilde{x}_2 - \beta_1\tilde{v}$ and $\dot{\tilde{x}}_2 = \dot{x}_2 + \beta_2\tilde{v}$, with the characteristic polynomial $p^2 + \beta_1 p + \beta_2$. The choice $\beta_1 = 2\omega_o$, $\beta_2 = \omega_o^2$ places both poles at $-\omega_o$, so the observer is tuned by its bandwidth ω_o alone. The SMC–LESO is the VGSMC law of Eq. (5.23) with $\hat{d}_i = C_n z_2$:

$$i_{o,\mathrm{ref}} = \frac{V_0}{R_n} + \frac{P_n}{V_0} + C_n z_2 + C_n\Big(\zeta e + \varepsilon(s)\,\mathrm{sat}\Big(\frac{s}{\vartheta}\Big) + \gamma(s)\,s\Big). \tag{5.27}$$

5.4 PINN and Machine Learning Motivation

Physics-informed neural networks (PINNs) combine machine learning with physics-based modelling. Purely data-driven networks may overfit and predict poorly outside their training data; PINNs add the known equations of the system to the training objective, so the learned model must respect the physics of the converter. This is useful for resonant DAB converters, whose accurate models are strongly nonlinear and depend on the parameters, and where measurement noise and operating limits make classical identification and tuning difficult.

SMC is robust, but it can chatter and be sensitive to measurement noise when large switching gains are needed to cover the uncertainties (e.g., losses, parameter drift, mixed resistive and CPL loads). The PINN–SMC therefore uses physics-informed learning

to estimate the disturbance, so that the sliding-mode law needs smaller gains while keeping its robustness.

5.4.1 PINN Mathematical Formulation and Training

Following the standard PINN framework introduced and developed in [186], the converter is first written in a general nonlinear state-space form that encodes the available physics, which is expressed by:

$$\dot{x}(t) = f(x(t), u(t), \theta_p, t)\,, \qquad y(t) = g(x(t), u(t))\,, \tag{5.28}$$

where $x(t) \in \mathbb{R}^n$ is the state vector, $\dot{x}(t)$ is its time derivative, $u(t) \in \mathbb{R}^m$ is the input/modulation vector, θ_p is the vector of physical parameters (e.g., L, C, R, and transformer ratio), t denotes time, $y(t) \in \mathbb{R}^q$ is the measurable output vector, $f(\cdot)$ represents the nonlinear dynamics, and $g(\cdot)$ is the output map. A PINN uses a neural network $N_\theta(\cdot)$ (weights and biases collected in θ) to approximate unknown trajectories. In the general case, the network outputs a state estimate and hence an output estimate according to Eq. (5.29):

$$\hat{x}(t) = N_\theta\big(\psi(t)\big), \qquad \hat{y}(t) = g(\hat{x}(t), u(t))\,, \tag{5.29}$$

where $\psi(t)$ is the network input (feature vector) constructed from available signals (e.g., time, measured voltages/currents, and known references). Writing the PINN in terms of $\psi(t)$ is convenient for control applications because it allows direct use of measured signals and avoids requiring full-state measurement. To embed physics constraints into learning, a residual is formed by differentiating the network output and enforcing consistency with the governing state-space equations.

The network output is differentiated with respect to time (e.g., via automatic differentiation), and consistency with the governing model is enforced through the physics

residual defined as:

$$r(t) = \dot{\hat{x}}(t) - f(\hat{x}(t), u(t), \theta_p, t)\,, \tag{5.30}$$

where $r(t) \in \mathbb{R}^n$ is the physics residual. Ideally, $r(t) = 0$ if the learned trajectory satisfies the physical dynamics. Training typically combines a data-fitting loss and a physics-consistency loss [186]. For measured samples $\{t_i, y_i\}_{i=1}^{N_d}$, the data mismatch loss is calculated by:

$$\mathcal{L}_{\text{data}} = \frac{1}{N_d} \sum_{i=1}^{N_d} \|y_i - \hat{y}(t_i)\|_2^2\,, \tag{5.31}$$

where N_d is the number of data points, y_i is the measured output at time t_i, $\hat{y}(t_i)$ is the predicted output, and $\|\cdot\|_2$ denotes the Euclidean norm. Physics is enforced at collocation points $\{t_k\}_{k=1}^{N_c}$ in the training domain as:

$$\mathcal{L}_{\text{phys}} = \frac{1}{N_c} \sum_{k=1}^{N_c} \|r(t_k)\|_2^2\,, \tag{5.32}$$

where N_c is the number of collocation points and $r(t_k)$ is the residual evaluated at t_k. When initial conditions are known, they are included to ensure correct initialisation of the learned trajectory, which is expressed by:

$$\mathcal{L}_{\text{IC}} = \|\hat{x}(t_0) - x_0\|_2^2\,, \tag{5.33}$$

where t_0 is the initial time, x_0 is the known initial state, and $\hat{x}(t_0)$ is the PINN-predicted initial state.

A regularisation term is often added:

$$\mathcal{L}_{\text{reg}} = \|\theta\|_2^2, \tag{5.34}$$

where $\|\theta\|_2^2$ penalises large weights and biases.

All loss components are combined into one objective:

$$\mathcal{L}_{\text{PINN}} = \lambda_d \mathcal{L}_{\text{data}} + \lambda_p \mathcal{L}_{\text{phys}} + \lambda_c \mathcal{L}_{\text{IC}} + \lambda_r \mathcal{L}_{\text{reg}}, \tag{5.35}$$

where λ_d, λ_p, λ_c, and $\lambda_r > 0$ balance data fitting, physics satisfaction, initial-condition enforcement, and regularisation, respectively.

5.4.2 PINN Target: Lumped Disturbance at the DC Output Node

In this study, the PINN is not used as a post-filter on the SMC command. Instead, it is used as a physics-consistent disturbance estimator that provides an explicit feedforward compensation term. This design choice is motivated by the DC-side output-node dynamics of the DAB (Fig. 5.1), where the output-capacitor current balance provides a natural place to define a lumped uncertainty.

For the output capacitor C and output voltage $V_0(t)$, the ideal current balance is given by:

$$C\dot{V}_0(t) = i_L(t) - i_{\text{load}}(t), \tag{5.36}$$

where $i_L(t)$ is the converter current injected into the node and $i_{\text{load}}(t)$ is the total load current. Under mixed resistive and constant-power loading, the load current is described by:

$$i_{\text{load}}(t) = \frac{V_0(t)}{R} + \frac{P_{\text{CPL}}}{V_0(t)}, \tag{5.37}$$

where R is the resistive load and P_{CPL} is the constant-power load. In practice, losses, unmodelled dynamics, parameter drift, sensor bias, and non-ideal operating conditions introduce additional disturbances that are not explicitly captured by the nominal model.

The CPL behaviour causes deviations from Eqs. (5.36) and (5.37). These effects are captured by introducing a lumped disturbance current $d_i(t)$ (A), yielding:

$$C\dot{V}_0(t) = i_L(t) - \frac{V_0(t)}{R} - \frac{P_{\text{CPL}}}{V_0(t)} - d_i(t), \tag{5.38}$$

Estimating $d_i(t)$ therefore provides an explicit measure of the model mismatch acting at the DC output node.

Power-based form (when power is measured). If the instantaneous transferred power is measured as $P_{\text{in}}(t) \approx V_0(t)i_L(t)$, the inductor current follows from the measured power, and substituting it into Eq. (5.38) gives the power-based node dynamics, both

expressed below:

$$\begin{cases} i_L(t) \approx \dfrac{P_{\text{in}}(t)}{V_0(t)}, \\ C\dot{V}_0(t) = \dfrac{P_{\text{in}}(t)}{V_0(t)} - \dfrac{V_0(t)}{R} - \dfrac{P_{\text{CPL}}}{V_0(t)} - d_i(t). \end{cases} \tag{5.39}$$

This form uses the available measurements $\big(V_0, P_{\text{in}}\big)$ and is therefore well suited for online disturbance estimation.

5.4.3 PINN Disturbance Estimator and Node-Physics Residual

The PINN is designed to estimate the lumped disturbance current directly, as shown by:

$$\hat{d}_i(t) = N_\theta\big(\psi(t)\big), \tag{5.40}$$

where $\psi(t)$ is constructed from measurable signals. A practical choice that avoids algebraic loops in closed-loop implementation uses only measured/known quantities and, if needed, a delayed (previous-sample) control signal, as characterised by:

$$\psi(t) = \Big[V_0(t),\ P_{\text{in}}(t),\ \dot{V}_{0,f}(t),\ P_n\Big]^T, \tag{5.41}$$

where P_{in} is the measured power delivered to the output node, $\dot{V}_{0,f}$ the filtered derivative of the output voltage, and P_n the nominal CPL power known to the controller; all four are measured or known, so no algebraic loop arises. To enforce output-node physics, the estimator is trained (or fine-tuned) by minimising a residual derived from Eq. (5.39). Replacing $d_i(t)$ with $\hat{d}_i(t)$ yields the node-physics residual represented by:

$$r_d(t) = C\dot{V}_0(t) - \frac{P_{\text{in}}(t)}{V_0(t)} + \frac{V_0(t)}{R} + \frac{P_{\text{CPL}}}{V_0(t)} + \hat{d}_i(t), \tag{5.42}$$

which ideally satisfies $r_d(t) = 0$. Minimising $r_d(t)$ forces the learned $\hat{d}_i(t)$ to represent the current required to make the measured trajectories consistent with the capacitor-node physics. The corresponding physics loss is determined as:

$$\mathcal{L}_{\text{phys},d} = \frac{1}{N_c}\sum_{k=1}^{N_c} \|r_d(t_k)\|_2^2, \tag{5.43}$$

and can be appended to Eq. (5.35).

5.4.4 Rationale for Combining SMC with the PINN Disturbance Estimator

The key idea is that the PINN does not modify the SMC output directly. Instead, the estimated disturbance $\hat{d}_i(t)$ is injected into the control law as a feedforward compensation term. This reduces the uncertainty that the switching action must cover, so the switching gain can be smaller without losing robustness, which reduces chattering and the sensitivity to noise.

5.4.5 Final PINN–SMC Control Law

The PINN–SMC is the VGSMC law of Eq. (5.23) with the disturbance estimate supplied by the PINN:

$$i_{o,\mathrm{ref}}(t) = \frac{V_0(t)}{R_n} + \frac{P_n}{V_0(t)} + \hat{d}_i(t) + C_n\Big(\zeta e(t) + \varepsilon(s)\,\mathrm{sat}\Big(\frac{s(t)}{\vartheta}\Big) + \gamma(s)\,s(t)\Big), \quad (5.44)$$

where $i_{o,\mathrm{ref}}$ is the current command (A), V_0 the measured output voltage (V), R_n, P_n and C_n the nominal load resistance (Ω), CPL power (W) and output capacitance (F) used by the controller, $\hat{d}_i$ the disturbance current estimated by the PINN (A), $e = V_{\mathrm{ref}} - V_0$ the voltage error (V), s the sliding variable of Eq. (5.16), and $\varepsilon(s)$, $\gamma(s)$ the variable gains of Eq. (5.21). The current command is turned into the phase shift by Eq. (5.15). Because the PINN–SMC, the SMC–LESO and the VGSMC use the same law and the same gains, any difference between them comes from the disturbance estimate only.

Implemented estimator. The network has four inputs, two hidden layers of 32 neurons and one output (4-32-32-1). Its input vector uses only measured or known quantities, so no algebraic loop arises:

$$\psi = \big[V_0,\ P_o,\ \dot{V}_{0,f},\ P_n\big]^{\mathsf{T}}, \qquad \hat{d}_i = Q(p)\,N_\theta(\psi), \qquad Q(p) = \frac{\omega_q^2}{(p+\omega_q)^2}, \quad (5.45)$$

where P_o is the measured power delivered to the output node, $\dot{V}_{0,f}$ the derivative of V_0 filtered at the bandwidth ω_f, p the Laplace variable and $Q(p)$ a second-order low-pass filter on the network output. The filter is needed: without it, the estimator adds a nearly undamped mode at 473 Hz to the closed loop (damping ratio 0.013, peak minor-loop gain $|T_m|$ = 1.47), whereas with $\omega_f = \omega_q$ equal to the LESO bandwidth the peak of $|T_m|$ is 0.12 (Section 5.6.5). The output of the network is limited to ±40 A.

Training. The network is trained by minimising the loss of Eq. (5.35) with the node-physics residual of Eq. (5.42) as the physics part, with $\lambda_d = \lambda_p = 1$, $\lambda_r = 10^{-5}$ and no initial-condition term ($\lambda_c = 0$). The data come from 100 simulated runs with random reference, input-voltage, CPL and load changes: 60 forward-power runs with correct P_n; 20 runs with power in both directions (CPL from -900 to $+900$ W); and 20 more forward runs. In 40 of the runs, P_n is chosen independently of the true CPL, so that the PINN does not rely on correct load information. Eighty runs are used for training (20% of their samples with the true disturbance as label, the rest only through the physics residual) and 20 for checking. Training uses the Adam method for 100 rounds, with a learning rate of 3×10^{-3} halved every 30 rounds and small noise added to the inputs. On the 20 runs not used for training, the estimate has a root-mean-square (RMS) error of 1.24 A, a mean absolute error of 0.50 A, and a coefficient of determination $R^2 = 0.991$ (Fig. 5.3).

Fig. 5.4 shows how the controllers of this chapter fit together. In the *offline* stage (a), the PINN is trained on 100 simulated runs: the input vector ψ is built from the logged signals, and the network weights are updated to reduce the loss of Eq. (5.35), which combines the labelled data with the node-physics residual r_d of Eq. (5.42). In the *online* stage (b), the voltage error e gives the sliding variable s, the VGSMC law computes the current command $i_{o,\mathrm{ref}}$, and the current-to-phase map turns it into the phase shift φ of the DAB. The VGSMC, the SMC–LESO and the PINN–SMC differ only in the disturbance estimate $\hat{d}_i$ that enters the law: zero, the LESO estimate, or the

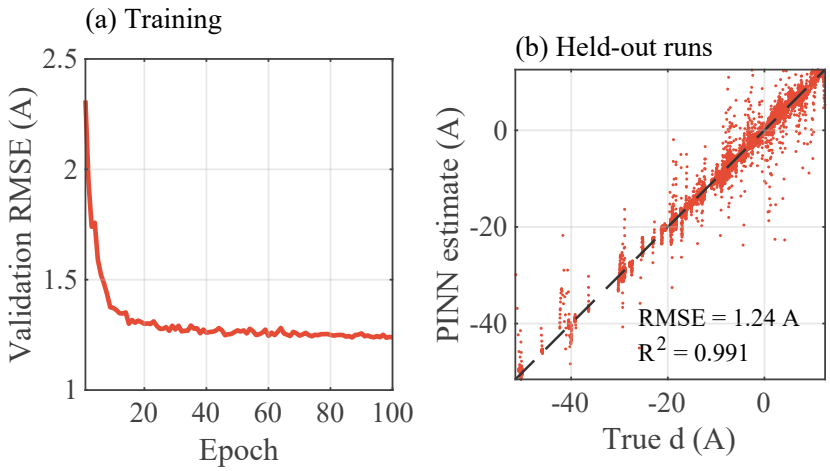


Figure 5.3: PINN training and test on new runs.

filtered output of the trained PINN. The TSOSMC replaces the sliding variable and the VGSMC law with the twisting law of Eq. (5.58) and uses the same current-to-phase map.

5.5 Twisting Second Order Sliding Mode Control (TSOSMC)

The TSOSMC reduces the chattering of first-order sliding mode control and is robust to disturbances and model uncertainty [187]. It drives both the sliding variable and its derivative to zero in finite time, which improves tracking. Because its control action is continuous, it suits high-frequency converters such as the DAB, where smooth voltage and current control is important [188].

It is used in this chapter as a known second-order benchmark without a disturbance estimator; adaptive gains could be added in future work [60].

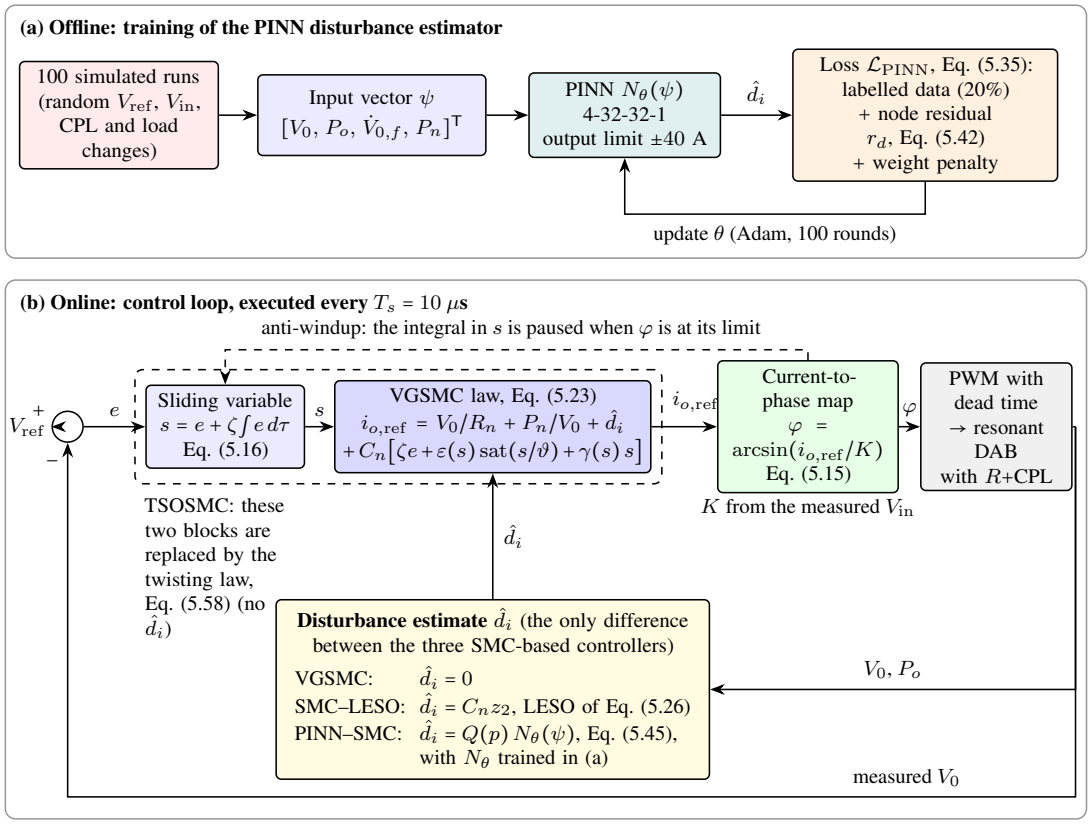


Figure 5.4: Controllers of this chapter: (a) offline PINN training; (b) online control loop.

5.5.1 Design of a TSOSM Controller for a DAB Resonant Converter

Consider a single-input single-output (SISO) system of the form:

$$\dot{x} = a(x,t) + b(x,t)\,u \tag{5.46}$$

$$\sigma = \sigma(x,t) \tag{5.47}$$

where $x \in \mathbb{R}^n$ and $\sigma : \mathbb{R}^n \times \mathbb{R} \to \mathbb{R}$ is a sufficiently smooth output function. Assume that the relative degree of σ with respect to the control input u is globally well-defined, uniform, time-invariant, and equal to r (i.e., u first appears in the r-th time derivative of σ).

DC-side output-voltage dynamics. The DC-side output-voltage dynamics of the resonant DAB converter are:

$$\dot{V}_0 = \frac{1}{C}\left(\frac{P_{\mathrm{tr}}(t)}{V_0} - \frac{V_0}{R} - \frac{P_{\mathrm{cpl}}}{V_0}\right) \tag{5.48}$$

where V_0 is the output voltage, $P_{\mathrm{tr}}(t)$ is the measured instantaneous transferred/output power at the DC-side port (e.g., $P_{\mathrm{tr}}(t) \approx V_0 i_L$), R is the fixed resistive load, P_{cpl} is the constant power consumed by the CPL, and C is the filter capacitor.

Tracking error and sliding variable selection. To apply the *twisting* second-order sliding-mode algorithm, the sliding variable must have *relative degree two* with respect to the actual actuator of the DAB (typically the phase-shift ϕ). The sliding variable is selected as:

$$e(t) = V_0(t) - V_{\mathrm{ref}}, \qquad \sigma(t) = e(t), \tag{5.49}$$

where V_{ref} is the constant voltage reference. From Eq. (5.48), the first derivative of σ becomes:

$$\dot{\sigma}(t) = \dot{e}(t) = \dot{V}_0(t) = \frac{1}{C}\left(\frac{P_{\mathrm{tr}}(t)}{V_0} - \frac{V_0}{R} - \frac{P_{\mathrm{cpl}}}{V_0}\right). \tag{5.50}$$

Differentiating Eq. (5.50) yields:

$$\ddot{\sigma}(t) = \ddot{V}_0(t) = \frac{d}{dt}\left[\frac{1}{C}\left(\frac{P_{\mathrm{tr}}(t)}{V_0(t)} - \frac{V_0(t)}{R} - \frac{P_{\mathrm{cpl}}}{V_0(t)}\right)\right], \tag{5.51}$$

which is nonlinear and includes $\dot{P}_{\mathrm{tr}}(t)$ and $\dot{V}_0(t)$ terms. Since the transferred power is modulated by the phase shift, it can be written as $P_{\mathrm{tr}}(t) = P(u, x, t)$ with $u = \phi$. Therefore, under standard higher-order sliding-mode assumptions, the second derivative of the sliding variable can be written in the affine form:

$$\ddot{\sigma}(t) = h(x,t) + g(x,t)\,u, \tag{5.52}$$

where $h(x,t)$ lumps the uncertainties and disturbances (including CPL effects and unmodelled dynamics) and $g(x,t)$ is the control gain describing how u affects $\ddot{\sigma}$. Assuming $h(x,t)$ and $g(x,t)$ are bounded, there exist positive constants H, $g_{\min}$, and

$g_{\max}$ such that:

$$|h(x,t)| \le H, \qquad 0 < g_{\min} \le g(x,t) \le g_{\max}. \tag{5.53}$$

Twisting second-order sliding-mode control (TSOSMC): sign-to-saturation implementation. For a relative-degree-two system of the form of Eq. (5.52), the ideal twisting SOSMC law is:

$$u(t) = -b_1 \operatorname{sgn}\big(\sigma(t)\big) - b_2 \operatorname{sgn}\big(\dot{\sigma}(t)\big), \qquad b_1 > b_2 > 0. \tag{5.54}$$

With the bounds of Eq. (5.53), σ and $\dot{\sigma}$ converge to zero in finite time when the twisting gains satisfy Eq. (5.55) [54]:

$$(b_1 - b_2)\, g_{\min} > H, \qquad (b_1 + b_2)\, g_{\min} - H > (b_1 - b_2)\, g_{\max} + H. \tag{5.55}$$

To mitigate chattering, the discontinuous $\operatorname{sgn}(\cdot)$ terms are replaced by saturation functions, giving:

$$u(t) = -b_1 \operatorname{sat}\!\left(\frac{\sigma(t)}{\vartheta_\sigma}\right) - b_2 \operatorname{sat}\!\left(\frac{\dot{\sigma}(t)}{\vartheta_{\dot{\sigma}}}\right), \qquad b_1 > b_2 > 0, \tag{5.56}$$

where the saturation function and its limits are given by:

$$\operatorname{sat}(x) = \begin{cases} 1, & x > 1, \\ x, & |x| \le 1, \\ -1, & x < -1, \end{cases} \qquad \Rightarrow \qquad \operatorname{sat}(x) \in [-1, 1], \tag{5.57}$$

where $u(t)$ is the control input of the affine model in Eq. (5.52), i.e., the control variable applied to the converter (in the implemented form below, the rate of a correction current); $\sigma(t)$ is the second-order sliding variable and $\dot{\sigma}(t)$ its time derivative; b_1 and b_2 are the twisting gains, with $b_1 > b_2 > 0$; and $\vartheta_\sigma > 0$ and $\vartheta_{\dot{\sigma}} > 0$ are the boundary-layer widths. The three cases of Eq. (5.57) cover every real x without overlap, and the branches meet at $x = \pm 1$, where $\operatorname{sat}(\pm 1) = \pm 1$, so the function is continuous and bounded; hence $\operatorname{sat}(\sigma/\vartheta_\sigma) \in [-1, 1]$ and $\operatorname{sat}(\dot{\sigma}/\vartheta_{\dot{\sigma}}) \in [-1, 1]$, and outside the boundary layers ($|\sigma| > \vartheta_\sigma$,

$|\dot{\sigma}| > \vartheta_{\dot{\sigma}}$) Eq. (5.56) reduces to the ideal twisting law of Eq. (5.54).

Implemented TSOSMC (current-rate form). In the DAB, the phase shift sets the output current almost directly (Eq. (5.14)), so $\sigma = V_0 - V_{\mathrm{ref}}$ has relative degree one with respect to φ. To obtain relative degree two, the twisting law acts on the rate of a correction current i_c:

$$\frac{di_c}{dt} = C_n\, u - \lambda_\ell\, i_c, \qquad i_{o,\mathrm{ref}} = \frac{V_{\mathrm{ref}}}{R_n} + \frac{P_n}{V_{\mathrm{ref}}} + i_c, \qquad u = -b_1\,\mathrm{sat}\Big(\frac{\sigma}{\vartheta_\sigma}\Big) - b_2\,\mathrm{sat}\Big(\frac{\dot{\sigma}}{\vartheta_{\dot{\sigma}}}\Big), \quad (5.58)$$

where u is the twisting control signal (V/s^2), λ_ℓ a small leak that stops i_c drifting, $\dot{\sigma}$ is obtained from a filter of bandwidth N, and $|i_c|$ is limited. The current command is turned into the phase shift by Eq. (5.15), as for the other controllers.

Comparison of the four controllers. All four controllers act on the same plant, the same measurements and the same current-to-phase map, Eq. (5.15), and are executed every $T_s = 10\ \mu$s with a one-step delay. The VGSMC, the SMC–LESO and the PINN–SMC share the law of Eq. (5.23) and its gains and differ only in the disturbance estimate $\hat{d}_i$: zero, the LESO estimate $C_n z_2$ of Eq. (5.26), or the PINN estimate of Eq. (5.45). The TSOSMC of Eq. (5.58) has no estimator and acts on the rate of a correction current. The next section compares the four controllers in simulation under the same test events.

5.6 Simulation Results

5.6.1 Simulation Set-Up, Tuning and Performance Indices

Type of test and models. All results of this section come from simulation in MATLAB/Simulink R2024b. Two models of the DAB of Fig. 5.1 are used. The average model uses the first-harmonic relation of Eq. (5.14), a first-order lag at $f_s/10$ for the tank, the output capacitor with the resistive load and a CPL with a 50 A current limit,

a one-step computation delay and the controllers sampled every 10 μs; it is used for all eight test scenarios and for the stability analysis. The switching model contains the two IGBT/diode bridges (R_{on} = 16 mΩ), the series L_r–C_r tank, the 300:70 transformer, the 950 μF input and 9.5 mF output capacitors, the resistive load and the CPL; it uses square-wave phase-shift modulation, a discrete solver with a 0.1 μs step (about 0.5° of phase resolution at 13.5 kHz), and the controllers act on the output current averaged over one switching period, as in the average model. In open loop with R = 2 Ω, the switching model follows $K \sin\varphi$ within +8% at 30° and −6.5% at 90°, and halving its time step to 0.05 μs changes V_0 by less than 0.01% (Fig. 5.12(a)). In closed loop, the two models give almost the same response (Fig. 5.12(b)). Tables 5.3 and 5.4 list the converter values and all controller gains.

Table 5.3: Converter values.

Parameter	**Value**	**Parameter**	**Value**
Input voltage V_{in}	300 V (280–400 V)	Leakage L_{lk1}, L_{lk2}	15, 15 μH
Output voltage V_0	48–60 V	Magnetising L_m	5 mH
Turns ratio n	300:70	Output capacitor C_o	9.5 mF
Switching frequency f_s	13.5 kHz	Input capacitor	950 μF
Resonant L_r, C_r	4.8 μH, 50 μF	Resistive load R	2 Ω
Tank reactance X; current gain K	24.8 Ω; 42 A at 300 V	CPL (current limit)	200–900 W (50 A)

Table 5.4: Controller values.

Parameter	**Value**	**Parameter**	**Value**
Control time step (one-step delay)	10 μs	LESO: ω_o	$2\pi \cdot 150$ rad/s
Nominal values C_n, R_n, P_n	9.5 mF, 2 Ω, 200 W	PINN: layers; filters	4-32-32-1; $2\pi \cdot 150$ rad/s
VGSMC: ζ, ϑ	60 s^{-1}, 0.5 V	$\omega_f = \omega_q$	
VGSMC: ε_0, α	30 V/s, 5 s^{-1}	PINN: output limit	40 A
VGSMC: γ_0, β	250 s^{-1}, 20 $(\text{V s})^{-1}$	TSOSMC: b_1, b_2	1.8×10^5, 9.6×10^4 V/s^2
		TSOSMC: ϑ_σ, $\vartheta_{\dot\sigma}$	2 V, 200 V/s
		TSOSMC: N, λ_ℓ, $\lvert i_c\rvert_{\max}$	$2\pi \cdot 150$ rad/s, 2 s^{-1}, 60 A

The same for all controllers where applicable.

Fair comparison. (i) The VGSMC, the SMC–LESO and the PINN–SMC use the same law and the same gains (Table 5.4) and differ only in $\hat{d}_i$. (ii) The LESO and the two PINN filters use the same bandwidth, $\omega_o = \omega_f = \omega_q = 2\pi \cdot 150$ rad/s, so neither estimator gains an advantage from being faster. (iii) The TSOSMC gains ($b_1 > b_2 > 0$) were chosen to give a similar closed-loop speed. (iv) All controllers use the same nominal values, time step, delay and current-to-phase map. (v) Unlike Chapter 3, there was no systematic gain search in this chapter; instead, all gains were halved and doubled (Table 5.8, last row), and the order of the controllers did not change, so the conclusions do not depend on one particular choice of gains.

Test events. The same eight scenarios were applied to all four controllers (Table 5.5). S1 is the earlier simulation sequence of this study and S2 the sequence used on the OPAL-RT simulator (Section 5.7).

Table 5.5: Test scenarios, the same for all controllers.

Test	**Events**
S1	V_{ref} 48→60 V at 20 ms; CPL 200→300 W at 30 ms; V_{in} 300→360 V at 100 ms
S2	V_{in} 300→400 V at 50 ms; V_{ref} 48→60 V at 150 ms; CPL 200→300 W at 250 ms
S3	R = 4 Ω; CPL 300→900 W at 50 ms (the load alone is then unstable: negative incremental resistance)
S4	V_{in} 360→280 V at 50 ms, back to 360 V at 150 ms
S5	Plant mismatch: C_o −30%, X +20%, R = 2.5 Ω; CPL 200→300 W at 50 ms; V_{ref} 48→60 V at 150 ms
S6	S1 with sensor noise: 0.5 V on V_0 and 2% on the measured power
S7	V_{ref} 60→48 V at 50 ms, back to 60 V at 150 ms
S8	Unknown extra 8 A load connected at 50 ms, removed at 150 ms

Performance indices. Every index is computed by a script from the saved simulation data, for one event at a time, from the event to the next event. With V_a and V_b the voltages before and after a reference change and $\Delta V = V_b - V_a$, the rise (or fall) time is the time from 10% to 90% of the change, the overshoot is $M_p = \max_t \operatorname{sgn}(\Delta V)[V_0(t) - V_b]/V_b \times 100\%$, and the settling time is the last moment outside the band $\pm\delta V_{\text{ref}}$, with $\delta = 2\%$ for reference changes (the usual choice when the converter current limits the

speed) and $\delta = 0.5\%$ for disturbances. After a disturbance, the drop (or rise) is the largest deviation below (or above) the reference in percent of V_{ref}. The total error is $\mathrm{IAE} = \int |V_{\mathrm{ref}} - V_0|\, dt$, and the reaching time is the time until the sliding variable, after leaving its band, is back inside $|s| \le \vartheta$.

5.6.2 Reference Changes (S1, S2, S7)

Figs. 5.5 and 5.6 show scenarios S1 (switching model) and S2 (average model), and Table 5.6 gives the indices of S2 and S7. After a reference change, all controllers drive the phase shift to its limit of 90° (Figs. 5.5(b) and 5.6(b)). The speed is then set by the largest current that the converter can give, $t_{\min} \approx C_o \Delta V / (K - i_{\mathrm{load}})$, about 9 ms at 300 V and 5 ms at 400 V, so the three SMC-based controllers respond almost equally fast (settling 5.5–5.7 ms in S2). The PINN–SMC settles fastest after the reference changes (5.54 ms in S2 and 4.71 ms after the 60→48 V step of S7). The TSOSMC is about four times slower (21 ms) with an overshoot of 3.75%.

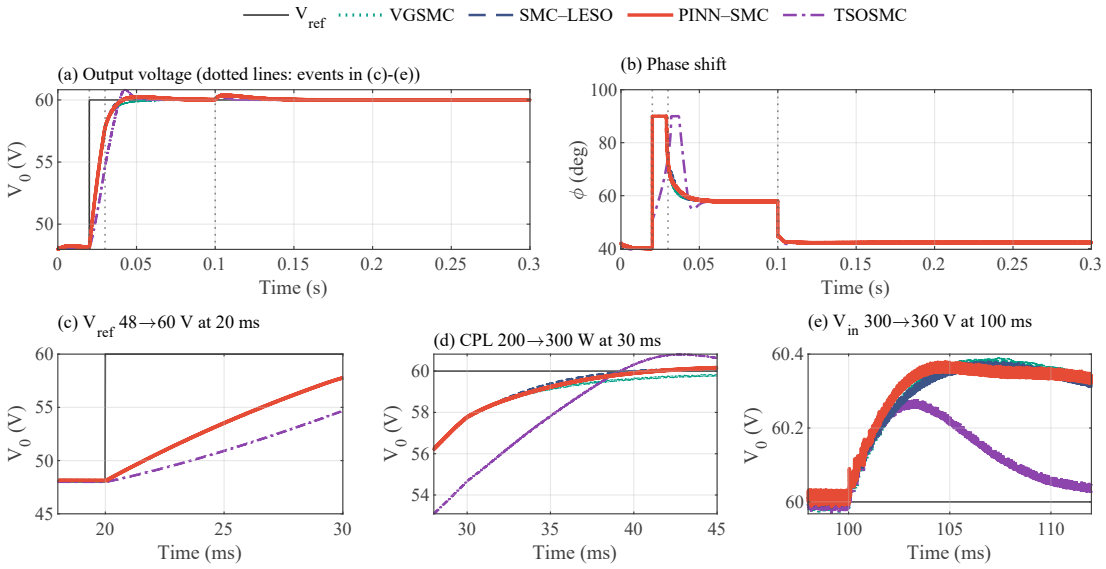


Figure 5.5: Scenario S1 (switching model).

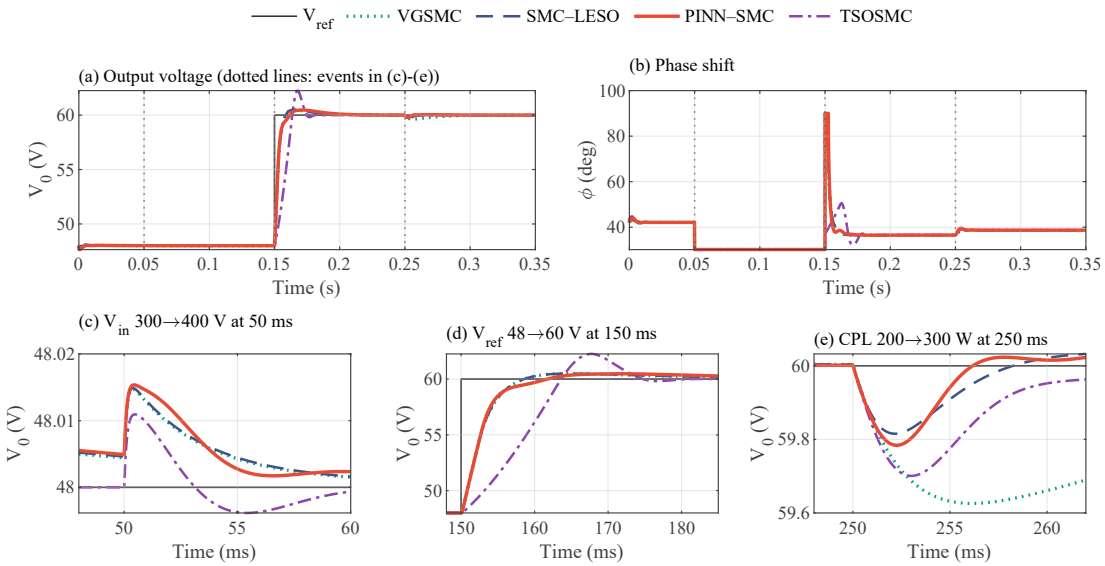


Figure 5.6: Scenario S2 (average model).

Table 5.6: Indices of the reference changes and the CPL step.

	S2: V_{ref} 48→60 V				**S2: CPL 200→300 W**		**S7: V_{ref} 60→48 V**		
	Rise (ms)	Reach (ms)	OS (%)	t_s (ms)	Drop (%)	t_s	Fall (ms)	US (%)	t_s (ms)
VGSMC (no estimator)	5.11	9.66	0.81	5.66	0.62	12.7 ms	4.70	1.16	5.54
SMC–LESO	5.10	9.64	0.81	5.65	**0.31**	in band	4.69	1.16	5.54
PINN–SMC	**4.99**	12.8	**0.79**	**5.54**	0.36	in band	**3.87**	**0.89**	**4.71**
TSOSMC	10.5	13.1	3.75	21.2	0.50	in band	10.5	4.76	21.9

Reference changes of S2 and S7; CPL step of S2.

5.6.3 Load Disturbances (S3, S8)

Fig. 5.7 shows the two load disturbances in the switching model: the CPL step from 300 to 900 W with $R = 4\ \Omega$ (S3), at which the load alone is unstable, and an unknown 8 A load connected and removed (S8). Here the disturbance estimate makes the difference. In S3 the voltage drop falls from 6.2% without an estimator (VGSMC, recovery 27.1 ms) to 3.7% with the PINN (5.2 ms) and 3.1% with the LESO (5.4 ms); the TSOSMC drops by 9.0% and needs 22.8 ms. In S8 the drops are 4.4% (VGSMC, 24.2 ms), 2.4% (PINN–SMC, 4.4 ms), 2.0% (SMC–LESO, 3.3 ms) and 4.2% (TSOSMC, 9.0 ms). Panels (e) and (f) show that both estimators follow the true disturbance current within a few milliseconds; the PINN estimate is slightly faster to rise but overshoots briefly.

Fig. 5.8 summarises the IAE of all scenarios and the indices of the load steps, and Table 5.7 isolates what the estimators add to the common law. Table 5.7 shows that the

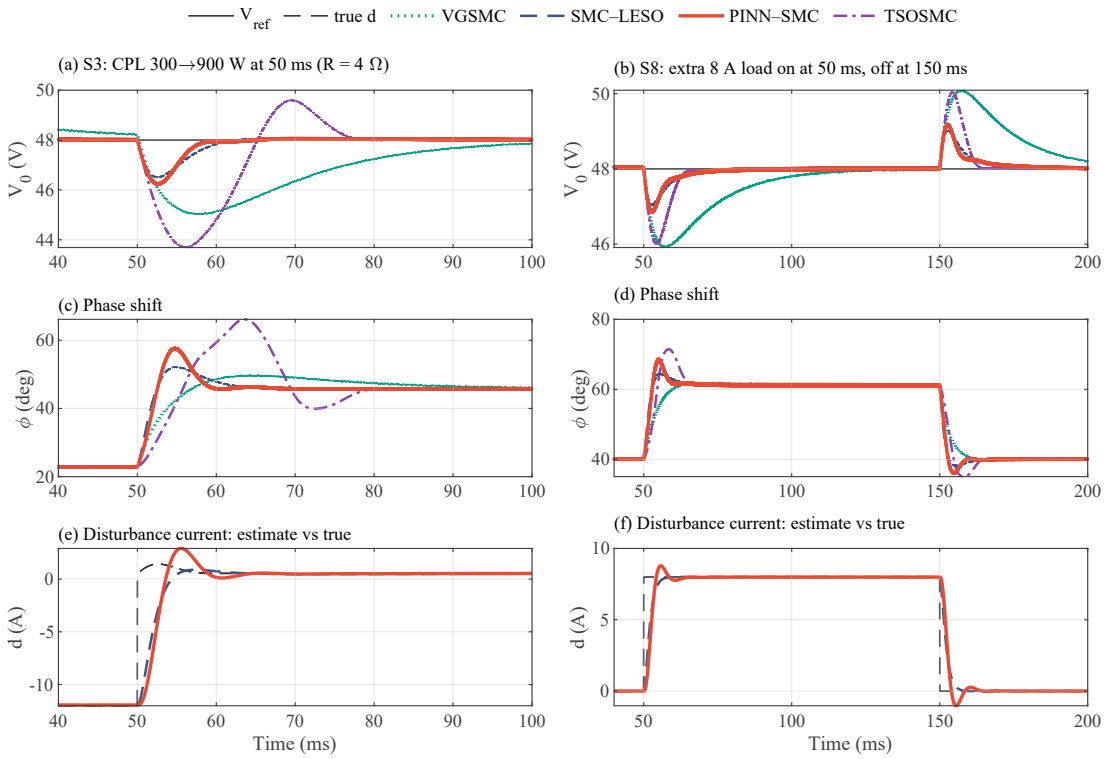


Figure 5.7: Load disturbances S3 and S8 (switching model).

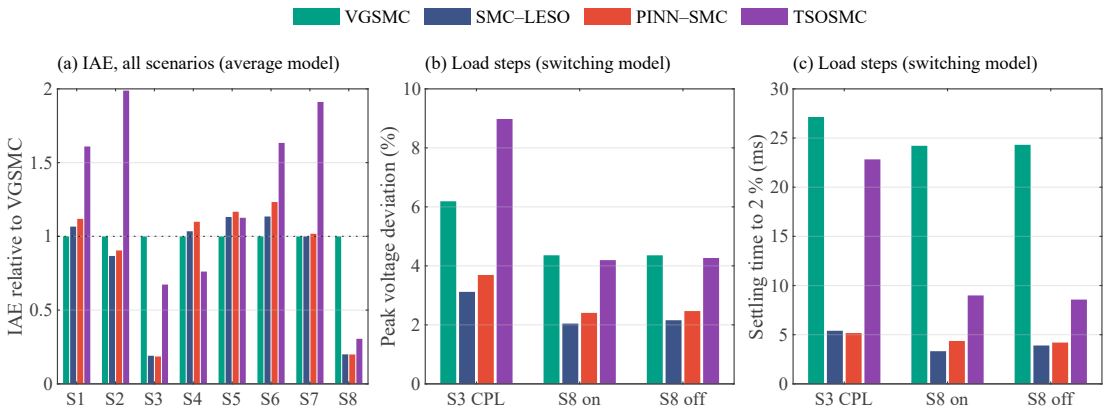


Figure 5.8: Performance indices of the four controllers.

VGSMC alone is stable in every test and, after a reference change, as fast as the other two, because the converter current sets the speed. After load changes, however, it has no estimate of the load, so its integral term must do all the work: the voltage drop is

Table 5.7: The common law with and without an estimator.

Test	**VGSMC**	**SMC–LESO**	**PINN–SMC**
S2: IAE (V s) / settling after the reference step (ms)	0.055 / 5.7	0.048 / 5.7	0.050 / 5.5
S2: drop after CPL 200→300 W (%) / recovery	0.62 / 12.7 ms	0.31 / in band	0.36 / in band
S3: drop / settling after CPL 300→900 W (%/ms)	6.2 / 27.1	3.1 / 5.4	3.7 / 5.2
S8: drop / settling after an extra 8 A load (%/ms)	4.4 / 24.2	2.0 / 3.3	2.4 / 4.4
S1: time for s to return after the reference step (ms)	> 80	18.4	20.8
Wrong load information (P_n = 0): drop / settling (%/ms)	6.9 / 26	3.2 / 4.5	3.8 / 4.5
Smallest stable capacitor at 900 W; slowest stable sampling	63 μF; 2.73 ms	95 μF; 2.38 ms	63 μF; 1.36 ms
Peak minor-loop gain $\lvert T_m \rvert$ (smaller is safer)	0.134	0.074	0.113

Without an estimator: VGSMC.

about twice as large and the recovery about five times slower. In S1, its sliding variable is still outside the band 80 ms after the step. This is the clearest measure of what the LESO and the PINN add. On the other hand, the VGSMC tolerates a smaller capacitor and slower sampling best, because it has no estimator that can be disturbed.

5.6.4 Robustness and Stress Tests

Fig. 5.9 shows the input-voltage sag (S4), the plant mismatch (S5), the sensor noise (S6) and the reference changes down and up (S7), and Fig. 5.10 the effect of the noise on the estimates. Table 5.8 gives further stress tests based on S3, and Table 5.9 the stability limits. With sensor noise (0.5 V on V_0 and 2% on the measured power), the SMC–LESO and the PINN–SMC are almost unchanged (drops of 3.2 and 3.8%, settling in 4.7 ms), whereas the TSOSMC drops by 9.7% and needs 31 ms; the PINN estimate is noisier than the LESO estimate (RMS error 0.91 A against 0.25 A in S6). With the tank reactance 20% off or with wrong load information (P_n = 0), the SMC–LESO and

the PINN–SMC recover in 4.5–6.5 ms. The smallest output capacitor that still gives a stable loop at 900 W is 63 μF for the VGSMC and the PINN–SMC and 95 μF for the SMC–LESO, against 981 μF for the TSOSMC; the slowest stable sampling period is 2.73 ms (VGSMC), 2.38 ms (SMC–LESO), 1.36 ms (PINN–SMC) and 0.90 ms (TSOSMC).

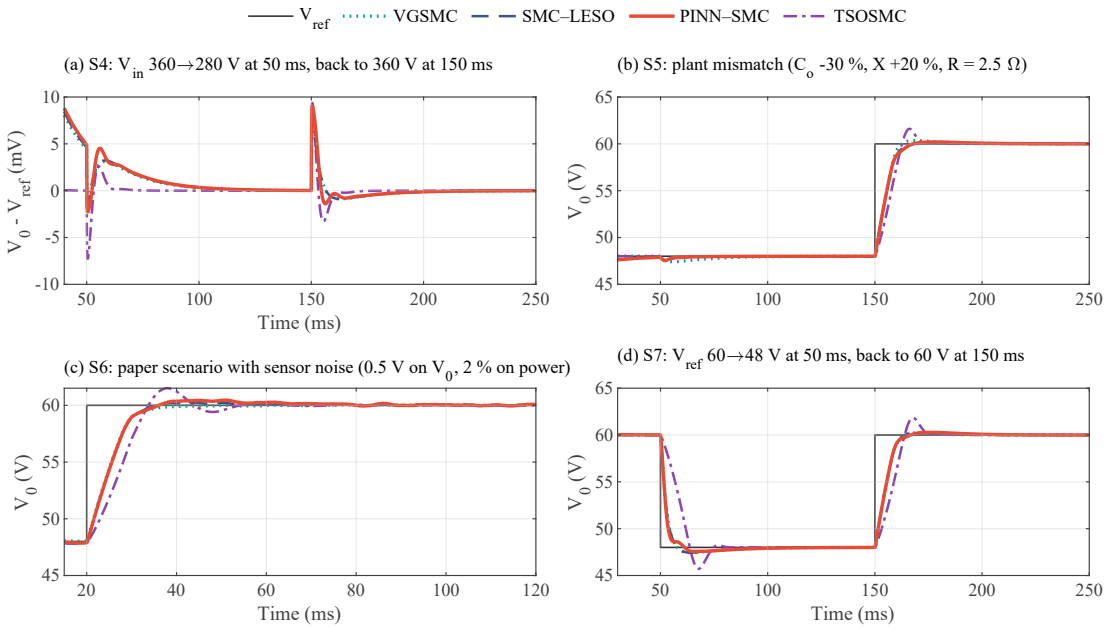


Figure 5.9: Robustness scenarios S4–S7.

Table 5.8: Stress tests based on S3.

Test	**Condition**	**VGSMC**	**SMC–LESO**	**PINN–SMC**	**TSOSMC**
Reference case (S3)	CPL 300→900 W, R = 4 Ω	6.0/25	**3.2/4.5**	3.8/**4.5**	8.8/21
Reverse power	800 W source, R = 8 Ω	8.1/29	**5.7/6.2**	6.8/7.2	22/31
Wrong load information	P_n = 0	6.9/26	**3.2/4.5**	3.8/**4.5**	8.8/21
Worst case	V_{in} = 280 V, C_o −50%, 1200 W	10.7/33	**5.9/6.9**	7.4/10	voltage lost
Slow sampling	T_s = 500 μs	7.4/25	**5.3**/6.5	5.9/**5.5**	13.3/49
Sensor noise	0.5 V, 2%	6.0/25	**3.2/4.7**	3.8/**4.7**	9.7/31
Tank value off	X × 1.2	7.7/29	**3.7**/6.5	4.3/**5.9**	10.4/18
Gains ×0.5 / ×2	all gains	8.2/53, 3.5/9.1	4.2/7.3, 2.2/2.3	5.1/6.2, 2.5/2.8	17.3/55, 5.1/5.9

Largest change (%) / settling time (ms); best in bold.

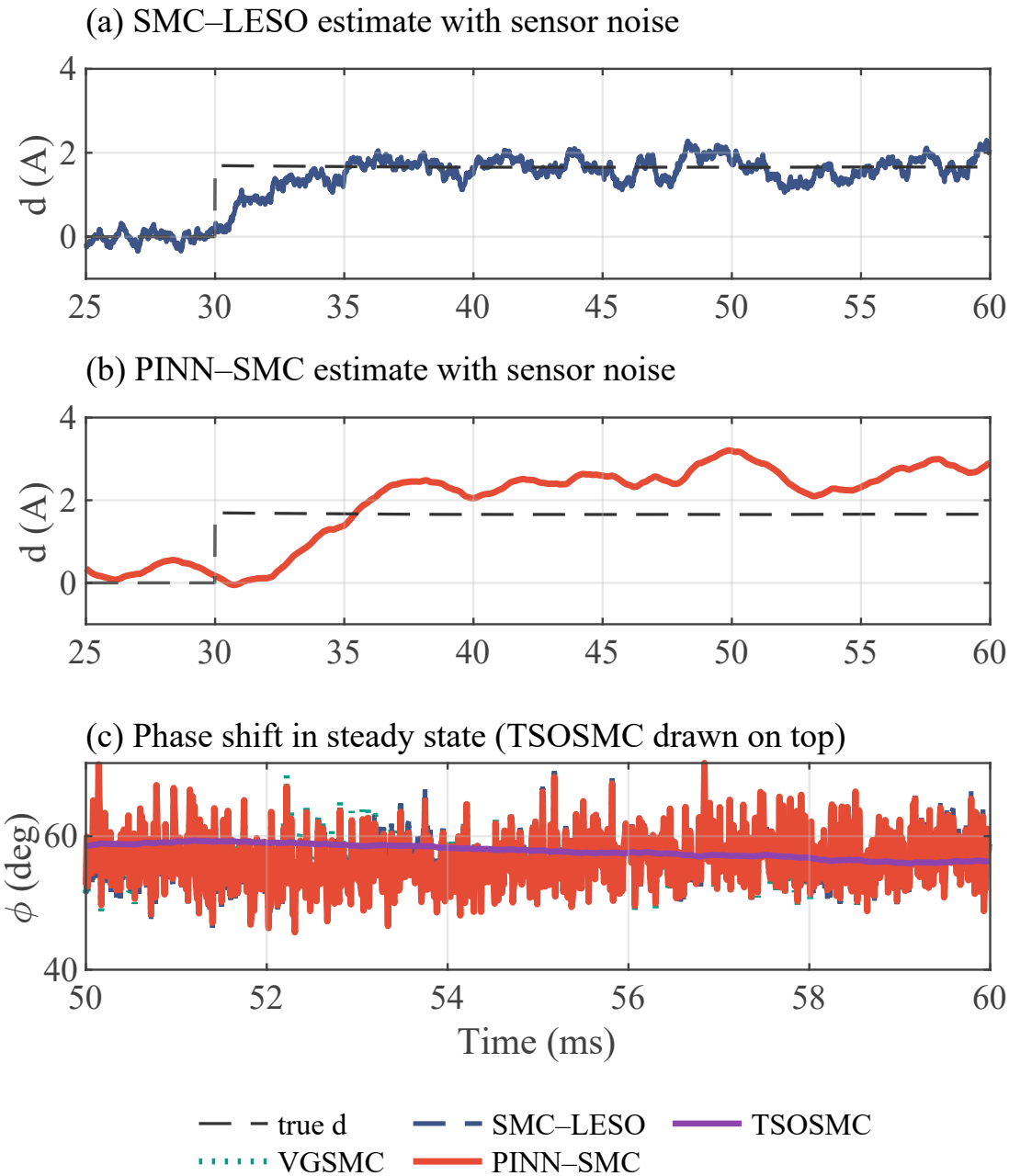


Figure 5.10: Scenario S6 with sensor noise.

Table 5.9: Stability limits.

What was changed	**VGSMC**	**SMC–LESO**	**PINN–SMC**	**TSOSMC**
CPL power (without control: unstable above 576 W)	all stable up to the 1440 W power limit			
Real C_o (controllers designed for 9.5 mF), 900 W	63 μF	95 μF	63 μF	981 μF
Slowest sampling that is still stable	2.73 ms	2.38 ms	1.36 ms	0.90 ms

R = 4 Ω, V_0 = 48 V, V_{in} = 300 V.

5.6.5 Stability Analysis with the Minor-Loop Gain

The stability of the converter–load interaction is checked with the minor-loop gain, now including each controller. Linearising the output node of Eq. (5.13) with the controller in the loop gives the closed-loop output impedance and the minor-loop gain:

$$Z_{\text{out}}(p) = \frac{1}{C_o p - Y_c(p)}, \qquad T_m(p) = \frac{Z_{\text{out}}(p)}{Z_{\text{load}}}, \qquad Z_{\text{load}} = \left(\frac{1}{R} - \frac{P_{\text{CPL}}}{V_0^2}\right)^{-1}, \quad (5.59)$$

where $Y_c(p)$ is the admittance that the controller adds at the output node (it contains the control law, the estimator and the delay) and Z_{load} is the incremental load impedance, which becomes negative when the CPL dominates. The loop is stable when the Nyquist curve of T_m does not encircle -1; a peak $|T_m|$ well below 1 gives a large margin. Without voltage control, the output pole $p = -(1/R - P_{\text{CPL}}/V_0^2)/C_o$ becomes unstable when $P_{\text{CPL}} > V_0^2/R = 576$ W at $R = 4\ \Omega$.

Fig. 5.11 shows the result. At the nominal point the output impedance of every controller stays far below the load impedance, and the peak of $|T_m|$ is 0.074 (SMC–LESO), 0.113 (PINN–SMC), 0.120 (TSOSMC) and 0.134 (VGSMC). When the CPL is increased with $R = 4\ \Omega$, all controllers stay stable up to the power limit of 1440 W, with $|T_m| < 0.15$. The analytical impedances agree with impedances measured in Simulink by current injection within about 2% between 5 and 500 Hz (Fig. 5.12(c)).

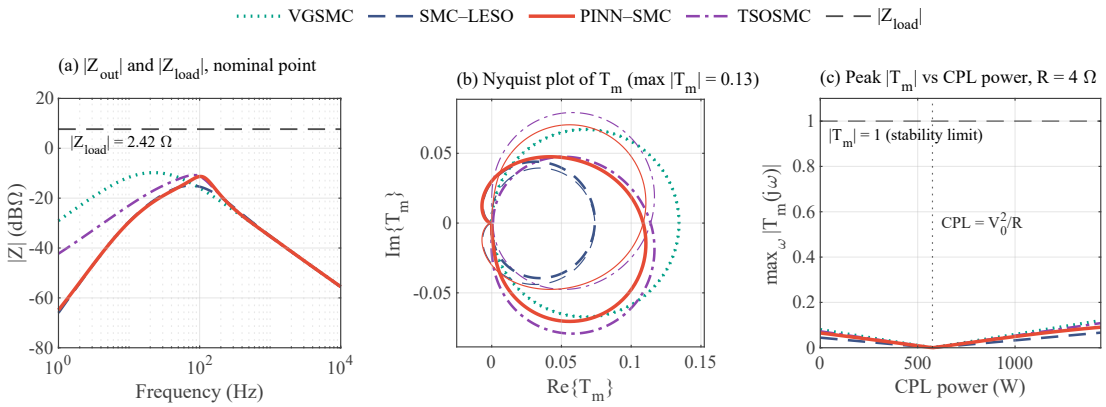


Figure 5.11: Minor-loop stability with each controller.

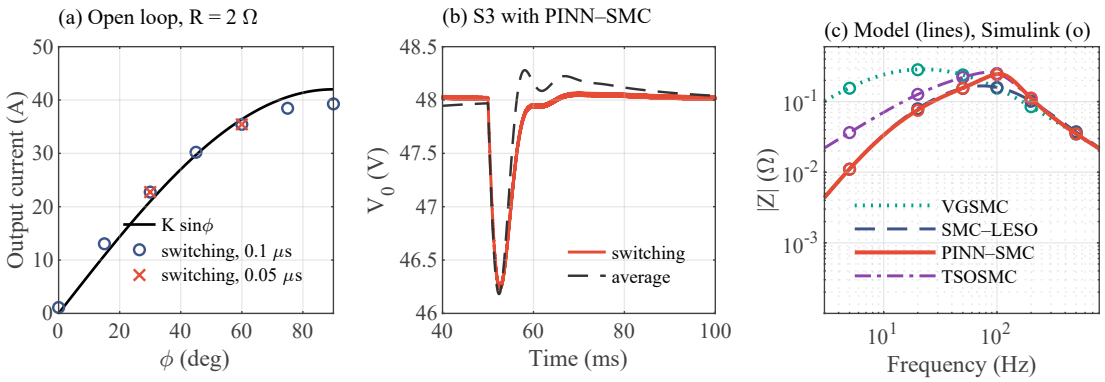


Figure 5.12: Checks of the DAB models.

5.6.6 Summary of the Simulation Results

Table 5.10 brings the main numbers together. The estimators reduce the total error after load changes by about 80%. The SMC–LESO gives the smallest drops, the smallest estimation error with noise and the largest stability margin; the PINN–SMC settles fastest after reference changes; the TSOSMC is two to four times slower. The PINN–SMC therefore performs about as well as the SMC–LESO, and clearly better than the TSOSMC and the SMC without an estimator.

Table 5.10: Summary of the four controllers.

	S2		**S3**	**S8**	**S6**	**Nominal point**
	IAE (V s)	t_s (ms)	drop / t_s (%/ms)	drop / t_s (%/ms)	estimate error (A)	peak $\lvert T_m \rvert$
VGSMC (no estimator)	0.055	5.7	6.2 / 27.1	4.4 / 24.2	–	0.134
SMC–LESO	**0.048**	5.7	**3.1** / 5.4	**2.0** / **3.3**	**0.25**	**0.074**
PINN–SMC	0.050	**5.5**	3.7 / **5.2**	2.4 / 4.4	0.91	0.113
TSOSMC	0.109	21.2	9.0 / 22.8	4.2 / 9.0	–	0.120

Best in bold.

5.7 Execution on the OPAL-RT Simulator (Software-in-the-Loop)

The controllers were also run on the OPAL-RT OP5700 simulator together with a model of the DAB (set-up in Fig. 3.15 of Chapter 3). This is a software-in-the-loop (SIL)

test: the controller and the converter model run together on the simulator, and no real converter or separate controller board is involved. The runs were made with the first implementation of the controllers, before the corrections of the models and of the PINN described in Sections 5.3–5.6.1. They show that the controllers run on the real-time simulator and the shape of the recorded waveforms; the quantitative comparison of the controllers is based on the simulations of Section 5.6. The signals of the simulator's analog outputs are scaled (the factors are given with each figure).

5.7.1 PINN–SMC

Fig. 5.13 shows the DAB signals on the simulator with the PINN–SMC. The input voltage is increased from 300 to 400 V at $t = 4$ s (scaled by 1/100); the input current is scaled by 1/5 (40 A), and the output voltage (48 V) and output current are scaled by 1/10. Fig. 5.14 shows the control input recorded in a separate run, in which the input voltage is increased from 300 to 400 V at $t = 1$ s, the voltage reference changes at $t = 2$ s, and the CPL increases from 200 to 300 W. The control input, starting at 7.8×10^{-3}, responds to these changes and stays bounded.

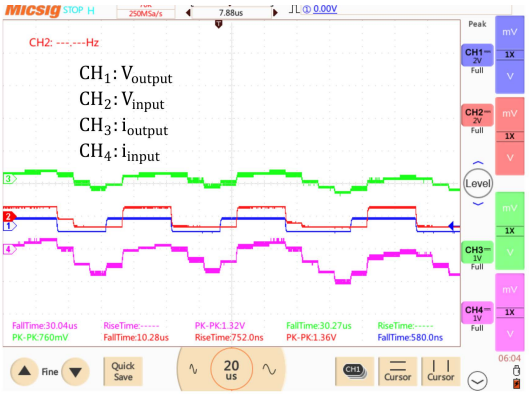


Figure 5.13: PINN–SMC on the OPAL-RT OP5700 (SIL): voltages and currents.



Figure 5.14: PINN–SMC on the OPAL-RT OP5700 (SIL): control input.

5.7.2 TSOSMC

The TSOSMC was run with input-voltage (300–400 V), reference (48–60 V) and CPL (200–250 W) changes; voltages and currents are scaled by 1/100 and 1/5 (Fig. 5.15). Its control input (Fig. 5.16) decreases from about 0.08 to 0 at $t = 1$ s and then to about -0.04; the CPL increase from 200 to 300 W at $t = 2$ s causes visible chattering and oscillation of the control input.

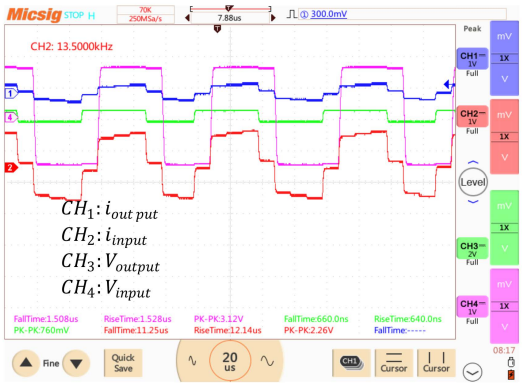


Figure 5.15: TSOSMC on the OPAL-RT OP5700 (SIL): DAB voltages and currents.

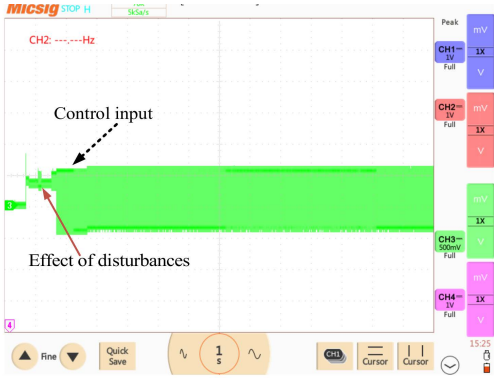


Figure 5.16: TSOSMC on the OPAL-RT OP5700 (SIL): control input.

5.7.3 SMC–LESO

Fig. 5.17 shows the DAB signals with the SMC–LESO. The input voltage is initially 300 V and increases to 360 V at $t = 2.5$ s, the CPL increases from 200 to 300 W at $t = 2$ s, and the voltage reference changes from 48 to 60 V at $t = 1$ s. The control input (Fig. 5.18) starts at 4.3, decreases to -0.05, and returns to 0.3 after the disturbance is removed at $t = 0.5$ s.

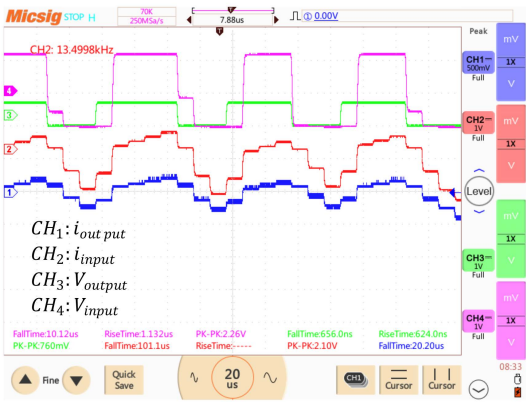


Figure 5.17: SMC–LESO on the OPAL-RT OP5700 (SIL): DAB voltages and currents.

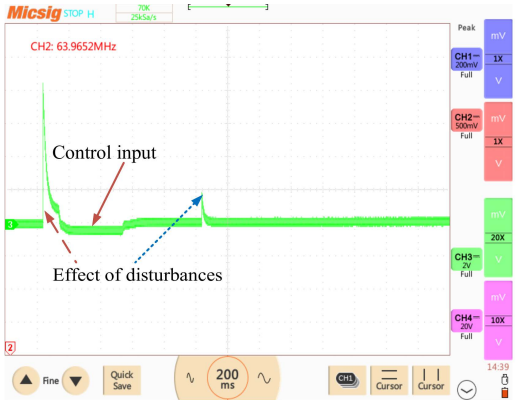


Figure 5.18: SMC–LESO on the OPAL-RT OP5700 (SIL): control input.

5.8 Summary

This chapter answered Research Objectives 3 and 4 for a resonant DAB converter supplying CPLs. The variable-gain reaching law (VGSMC) was derived step by step from the weaknesses of the conventional reaching laws; it is stable even when its base gain is smaller than the worst disturbance, and it is the common law of the three SMC-based controllers. Because the converter current is limited, these controllers react to a reference change at almost the same speed (settling 5.5–5.7 ms). The disturbance estimators make the difference after load changes: when the CPL rises from 300 to 900 W, the voltage drop falls from 6.2% without an estimator to 3.7% with the PINN and 3.1% with the LESO, and the recovery from 27.1 ms to about 5 ms. The PINN estimate is correct on runs not used for training (R^2 = 0.991), including reverse power and wrong load information. The PINN–SMC settles fastest after reference changes, while the SMC–LESO gives the smallest drops, is least sensitive to noise and has the largest stability margin. So the PINN–SMC performs about as well as the SMC–LESO, and clearly better than the TSOSMC and the SMC without an estimator; all controllers are stable up to the CPL power limit (minor-loop gain below 0.15). *Limits:* the results come from average and switching simulation models; the PINN needs training data and

a filter, and its estimate is noisier than that of the LESO; the OPAL-RT runs were made with the first implementation of the controllers; and the controllers were not tested on a physical converter.

Chapter 6

Conclusion and Future Research Directions

6.1 Key Findings

This thesis studied the control and stabilisation of QAB and DAB converters supplying resistive loads, CPLs and PPLs in LVDC microgrids. The findings below are reported with the conditions under which they were obtained; Table 6.1 summarises the studies, and Table 6.2 maps the findings to the research objectives of Section 1.4.

Harmonics of the QAB (C1, Chapter 3). The transformer winding currents of the QAB consist mainly of odd harmonics that decay as $1/k^2$. The harmonic model developed for the four-winding QAB with dead time agrees with the detailed switching simulation within 5.2% up to the 15th harmonic at the forward-power port; at a small phase shift ($3.7°$), where the dead time changes the switching edges most, the higher harmonics deviate by up to 37%. Even harmonics are negligible when the two half-cycles are equal (0.018–0.023% of the odd content) and grow only with an asymmetry (0.30–0.97% for 51 ns of dead-time mismatch), so they indicate an asymmetry rather than a property of the modulation. The same harmonic sums give the coefficients of the

control model and show why the feedforward must use the exact current-to-phase map: using only the fundamental would command 0.69 rad instead of 0.31 rad at the nominal point.

QAB with constant-power loads (C2, Chapter 3). Under one common set of test events and one common tuning procedure, the proposed ASTSMC had the lowest tuning score (J = 77.6, against 130.9 for the SMC–NLESO and 525.9 for the PID). It settled a 48→60 V reference step in 1.14 ms (SMC–NLESO 1.50 ms, PID 6.00 ms), and after a $2 \rightarrow 1.6\ \Omega$ load step it dropped by 2.33% and recovered in 0.79 ms (SMC–NLESO 2.61% and 1.21 ms; PID 4.06% and 14.86 ms). It stabilised CPLs up to 1500 W per port (PID 1350 W), had the smallest error under reverse power flow (7.46 V) and pulsed CPLs (0.91 V), and its control signal moved about four times less than that of the SMC–NLESO (12.9 against 53.0 mdeg). The Lyapunov analysis proves practical finite-time stability with bounded adaptive gains and without a priori knowledge of the disturbance bound, and the simulation confirms it: the sliding variables returned into the boundary layer within 1.3 ms after every event. The price is the largest overshoot on reference steps (4.4%, up to 21% over 100 random converters) and the largest sensitivity to an extra computation delay.

QAB with pulsed-power loads (C3, Chapter 4). For a PPL step from 100 to 200 W at 48 V, the customised ASSOSMC limited the voltage change to 0.5/0.3 V at ports 3 and 4 (IHOSMC 3.0/2.8 V; CMPC–ISMC 3.5/4.2 V) at almost the same total efficiency as the CMPC–ISMC (90.72% against 90.78%; IHOSMC 89.06%), but with the largest current change and a chattering control input. The CMPC–ISMC gave the smoothest control input and the smallest current change, at the cost of the largest voltage change.

DAB with learning-assisted control (C4, Chapter 5). The variable-gain reaching law (VGSMC) stays stable even when its base gain is smaller than the worst disturbance. After reference changes, the speed is limited by the converter current, so the three SMC-based controllers settle within 5.5–5.7 ms. After a CPL step from 300 to 900 W,

the voltage drop was 6.2% without an estimator, 3.7% with the PINN and 3.1% with the LESO, and the recovery fell from 27.1 ms to about 5 ms. The PINN estimate was correct on runs not used for training (R^2 = 0.991), including reverse power and wrong load information. The PINN–SMC therefore performs about as well as the SMC–LESO (it settles fastest after reference changes, while the SMC–LESO gives the smallest drops and is least sensitive to noise), and clearly better than the TSOSMC and the SMC without an estimator. All four controllers stayed stable up to the CPL power limit, with a peak minor-loop gain below 0.15.

OPAL-RT and hardware (C6, Appendix A). On the OPAL-RT OP5700 simulator, the QAB controllers of Chapter 3 ran 22–24 times slower than real time; the recorded phase shifts matched the simulation within 1–3° and the winding-current shapes with a correlation of 0.999–1.000. The laboratory DAB prototype confirmed correct switching with dead time and power transfer through the phase shift, in open loop.

Which controller for which need. The controllers were ranked only within each chapter, because each chapter uses a different converter and load. Table 6.3 brings the results together: for each need it names the best tested controller and what it costs.

Contributions. The original contributions of the thesis are the ASTSMC for the coupled QAB with CPLs (C2) and the PINN disturbance estimator used inside the VGSMC (C4b). The VGSMC reaching law (C4a) is an improvement of known variable-gain reaching laws; the harmonic model of the QAB (C1) and the three controllers for the QAB with PPLs (C3) are adaptations of known methods; the common test method (C5) is a method contribution; and the DAB prototype (C6) is engineering work (Tables 1.1 and 1.2).

Table 6.1: Summary of the studies in this thesis.

Ch.	Converter, load	Controllers (new or customised in bold)	Type of test	Main result	Main limit
3	QAB, 48 V ports; resistor + CPL	PID, SMC–NLESO, **ASTSMC**	Detailed switching simulation; SIL on OPAL-RT (slower than real time)	ASTSMC: settling 1.14 ms against 1.50–6.00 ms; load dip 2.33% against 2.61–4.06%; stable up to 1500 W CPL	Largest overshoot (4.4%); sensitive to extra delay; no hardware
4	QAB, 48 V ports; PPL 100→200 W	**ASSOSMC**, **IHOSMC**, **CMPC–ISMC**	Simulation; SIL on OPAL-RT	ASSOSMC: changes 0.5/0.3 V against up to 4.2 V; efficiency 90.72% against 90.78% (CMPC–ISMC)	One pulsed-load pattern; no hardware
5	Resonant DAB; resistor + CPL	VGSMC, SMC–LESO, TSOSMC, **PINN–SMC**	Average and switching simulation; SIL on OPAL-RT (first implementation)	PINN–SMC about as good as SMC–LESO; both much better than TSOSMC and VGSMC after load changes	PINN noisier than LESO; needs training data; no closed-loop hardware
App. A	DAB prototype	Phase shift only	Hardware, open loop	Correct gate signals, dead time and power transfer	Controllers not run on hardware

Table 6.2: Research objectives and main findings.

Objective	Main findings	Ch.	Limits
1. Modelling and stability	Harmonic model within 5.2% of the switching simulation up to $k = 15$; Lyapunov proof of the ASTSMC confirmed in simulation (σ back in band within 1.3 ms); with the controller included, the DAB minor-loop gain stays below 0.15 up to the power limit	3, 5	Harmonic model less accurate at small phase shifts; checked at chosen operating points
2. Effect of the loads	QAB without control unstable above 1152 W CPL, with control stable up to 1350–1500 W; DAB without control unstable above 576 W ($R = 4\ \Omega$), with control stable up to the 1440 W limit; PPL steps cause voltage changes of 0.3–4.2 V depending on the controller	3–5	Only the tested CPL and PPL levels
3. Comparing controllers	ASTSMC lowest tuning score and fastest; ASSOSMC smallest PPL voltage changes at almost the same efficiency; PINN–SMC about as good as SMC–LESO	3–5	Ranked only within each chapter
4. Learning-assisted control	PINN estimate correct on new runs ($R^2 = 0.991$); voltage drop after a large CPL step 3.7% against 6.2% without an estimator	5	DAB only; trained before use; noisier than LESO

Table 6.3: Which tested controller to choose for which need.

Need	Best tested	What it costs	Evidence
Fast response, load-change and reverse-power handling, QAB with CPLs	ASTSMC	Largest overshoot (4.4%); sensitive to extra delay	Tables 3.5, 3.6
Smallest overshoot and CPL dip; tolerance of extra computation delay, QAB	SMC–NLESO	Slower settling; control signal moves four times more	Tables 3.5, 3.6
Tight voltage under pulsed loads, QAB	ASSOSMC	Chattering of the control input; largest current change	Table 4.3
Smooth control input under pulsed loads, QAB	CMPC–ISMC	Largest voltage change; optimisation while running	Table 4.3
Load changes and noise, DAB with CPLs	SMC–LESO	Slightly slower after reference changes	Tables 5.10, 5.8
Fastest settling after reference changes, DAB	PINN–SMC	Needs training data and a filter; noisier estimate	Table 5.6

6.2 Practical Implementation Considerations

Computational delay. With two extra control periods of delay in the QAB of Chapter 3, the largest voltage error was 0.52 V with the ASTSMC, 0.06 V with the SMC–NLESO, and 3.11 V with the PID, which oscillated. The adaptive gains of the ASTSMC grow with the error, which makes the sampled loop more sensitive to extra delay; its adaptation rates must therefore be chosen with the computation delay in mind. In the DAB of Chapter 5, the slowest stable sampling period was 2.73 ms (VGSMC), 2.38 ms (SMC–LESO), 1.36 ms (PINN–SMC) and 0.90 ms (TSOSMC). Each ASTSMC cycle is a fixed sequence of algebraic operations without iterations or training, so its execution time is deterministic; it was not measured on a DSP in this work.

Measurement noise. Noise was added only to the measurements received by the controllers, with the same noise for every controller. With 0.1 V on the output voltages and 0.5 A on the bridge currents (QAB), the largest error was 0.17 V (SMC–NLESO), 0.26 V (PID) and 0.27 V (ASTSMC). With 0.5 V on the output voltage and 2% on the measured power (DAB, CPL step 300→900 W), the SMC–LESO and the PINN–SMC

were almost unchanged (drops of 3.2 and 3.8%, recovery in 4.7 ms), whereas the TSOSMC dropped by 9.7% and needed 31 ms; the PINN estimate was noisier than the LESO estimate.

Parameter uncertainty. In 100 QAB converters with inductances and capacitances changed by up to ±20% and turns ratios by up to ±5%, all controllers stayed stable; the ASTSMC had the smallest typical load-step dip (2.35%) but an overshoot of up to 21%. In the DAB, with the tank reactance 20% off or with wrong load information, the SMC–LESO and the PINN–SMC recovered in 4.5–6.5 ms, and the smallest output capacitor still stable at 900 W was 95 and 63 μF, against 981 μF for the TSOSMC. In the QAB with PPLs, resonant-parameter errors of ±20% in L_r, C_r and ±5% in n were treated as a bounded disturbance of the ISMC (Section 4.3.3).

Performance against complexity. Table 6.4 shows what each controller needs. The ASTSMC is the fastest but the most sensitive to delay; the PINN–SMC needs training data and a filter; the CMPC–ISMC solves an optimisation at every step; and the observer-based SMCs give a good balance between performance and complexity.

6.3 Limitations

- **Type of evidence.** The controllers were tested with detailed and averaged simulation models and by running them on the OPAL-RT OP5700 simulator (SIL). For the QAB controllers of Chapter 3, the OPAL-RT runs were slower than real time; they confirm the steady-state operating point and the waveforms, not the dynamic response. The OPAL-RT runs of Chapter 5 were made with the first implementation of the controllers. The laboratory DAB prototype confirmed correct switching and power transfer at about 50 V, but the closed-loop controllers were not run on it, and no QAB prototype was built. Closed-loop hardware validation was outside the scope of this research because of time constraints.

Table 6.4: What each controller needs.

Controller	Needs a model	Observer or estimator	Training before use	Optimisation while running	Weak point found
PID / PI with decoupling	partly	no	no	no	slow recovery after load change
SMC–NLESO / SMC–LESO	yes	yes	no	no	–
TSOSMC	partly	no	no	no	small C_o, slow sampling
ASTSMC	yes	NLESO	no	no	extra delay, overshoot varies
ASSOSMC	partly	no	no	no	chattering of the control input
IHOSMC	yes	no	no	no	largest control effort
CMPC–ISMC	yes	no	no	yes	largest PPL voltage change
PINN–SMC	partly	PINN	yes	no	noise; needs a filter

- **Tested conditions.** The results were obtained for 48–80 V load ports, input voltages of 270–400 V and powers up to about 2.6 kW (QAB) and 2 kW (DAB), for the tested CPL levels and one pulsed-load pattern. Whether the same controller would remain the best at higher power, at medium voltage, or in microgrids with many converters was not studied.

- **Scalability to medium- and high-power systems.** At higher power and voltage, insulation coordination, electromagnetic interference, thermal stress and protection requirements change the design, and the controllers would need to be checked again.

- **Large interconnected microgrids.** The controllers were evaluated on single converters. In microgrids with many distributed energy resources, interacting converters, communication delays and coordinated energy management, the results may change.

- **Models.** The harmonic model does not contain the semiconductor parasitic capacitances and the stray inductances of the layout, and it is less accurate at small phase shifts; the DAB results rely on a first-harmonic average model that was checked against a switching model.

6.4 Future Research Directions

Fig. 6.1 summarises six directions for future research.

1. **Hardware-in-the-loop tests and high-power prototypes.** Closed-loop tests of the controllers on real controller hardware, with the converter model running in real time on the FPGA of the simulator, and on a QAB prototype would include sensor noise, signal quantisation, gate-driver delay and transformer imperfections. They are the most direct proof of the benefit of the controllers and the next step of this work.

2. **Multiport converters, high-frequency transformers and hybrid AC/DC microgrids.** More ports or AC links enlarge the decoupling and harmonic models of this thesis. Designing the transformer together with the controller could reduce the port coupling at its source, which would simplify the controllers.

3. **Adaptive learning: reinforcement learning, online learning and digital twins.** The PINN of this thesis is trained before use. Learning during operation, or a digital twin that follows the real converter, could keep the controller accurate as components age, provided that stability is still guaranteed.

4. **Fault diagnosis, fault-tolerant control, cyber-security and resilience.** The disturbance estimates of the observers can reveal switch, sensor or capacitor faults, and converters that communicate need protection against false commands.

These functions are important for converters in critical loads such as data centres and electric vehicle charging.

5. **FPGA and system-on-chip implementation.** Faster hardware reduces the computation delay, to which the ASTSMC is the most sensitive of the tested controllers, and allows higher switching frequencies and smaller passive components.

6. **Coordinated control of interconnected DC microgrids.** Many converters with CPLs, renewable sources and storage interact and share power. The common test method of this thesis should be extended to groups of converters with communication delays, to show whether the controller ranking holds at the system level.

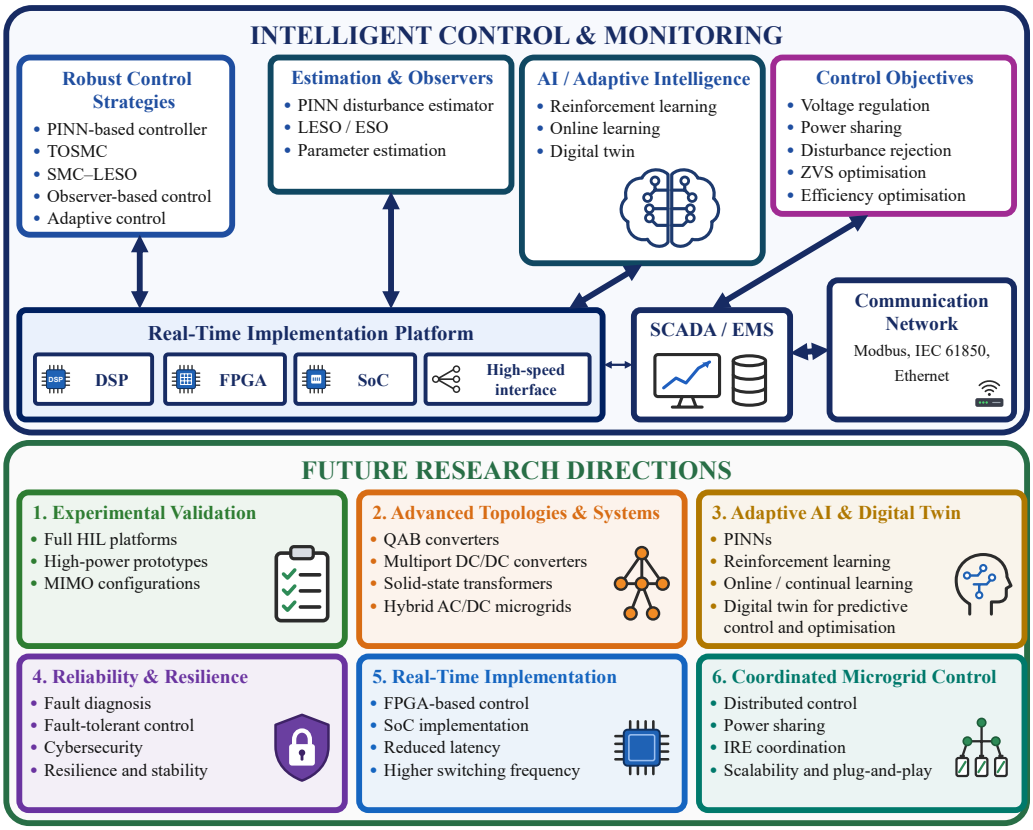


Figure 6.1: Summary of the future research directions.

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Appendix A

Laboratory-Scale DAB Converter Prototype and OPAL-RT Interface

A.1 Introduction

This appendix describes the laboratory-scale DAB converter prototype that was built in this research and its connection to the OPAL-RT OP5700 simulator, so that the experiment can be repeated. The prototype was run in open loop: the gate signals, with dead time and the phase shift between the bridges, were generated by the OPAL-RT simulator, without feedback control. The closed-loop controllers of Chapters 3–5 were not run on this hardware.

The primary H-bridge of the DAB converter, shown in Fig. A.1, is the main power stage: it generates the high-frequency AC voltage that transfers energy through the isolation transformer. This section describes the primary bridge and its sensing, gate-drive, protection and control-interface circuits.

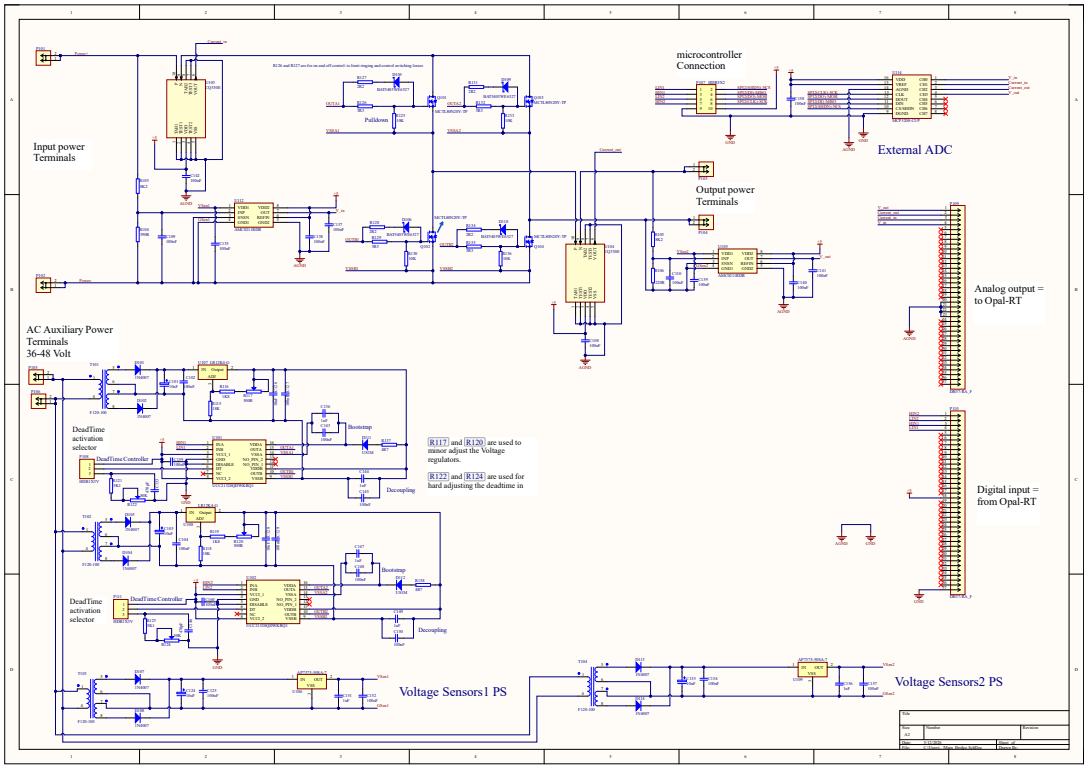


Figure A.1: Schematic diagram of the primary-side active bridge of the DAB converter.

A.1.1 H-Bridge Switching States

The primary H-bridge generates a bipolar voltage across the transformer primary by controlling four MOSFETs (Q_1–Q_4). When Q_1 and Q_4 are ON, a positive voltage $v_{AB} = +V_{\mathrm{dc}}$ is applied, whereas turning ON Q_2 and Q_3 produces a negative voltage $v_{AB} = -V_{\mathrm{dc}}$. Alternating between these states enables high-frequency power transfer through the transformer. A dead-time interval is inserted between these switching transitions to prevent shoot-through and ensure safe and reliable converter operation, as represented in Table A.1.

Table A.1: H-bridge switching states and primary voltage v_{AB}.

State	**Q1 (top-left)**	**Q2 (bot-left)**	**Q3 (top-right)**	**Q4 (bot-right)**
Positive half-cycle	ON	OFF	OFF	ON
Negative half-cycle	OFF	ON	ON	OFF
Dead-time	OFF	OFF	OFF	OFF

A.2 Component-by-Component Analysis

A.2.1 Input Power Terminals

The input power terminals connect the external DC source to the H-bridge and establish the primary-side voltage V_1. They must be capable of carrying the full converter current while maintaining low contact resistance and minimal parasitic inductance to reduce conduction losses, voltage overshoots, and switching-related EMI.

A.2.2 Input Filter Capacitors (Bulk and Decoupling)

Bulk and ceramic capacitors are connected across the DC bus to maintain a stable input voltage and reduce switching-induced disturbances. The bulk capacitors provide energy storage and suppress low-frequency voltage ripple, while the ceramic capacitors filter high-frequency noise generated by MOSFET switching. Together, they improve DC bus stability and reduce electromagnetic interference during converter operation. The resulting DC bus voltage ripple can be approximated as:

$$\Delta V_1 \approx \frac{I_1(1-D)}{f_s C_{bulk}} \tag{A.1}$$

where ΔV_1 is the DC bus voltage ripple, I_1 is the input current, D is the duty cycle, f_s is the switching frequency, and C_{bulk} is the total bulk capacitance.

A.2.3 Power MOSFETs (Q1–Q4)

Four N-channel MOSFETs (Q_1–Q_4) form the full H-bridge power stage of the DAB converter. These switches generate the high-frequency AC voltage required for power transfer through the isolation transformer. Their electrical characteristics, particularly on-state resistance and switching speed, directly affect converter efficiency, while ZVS helps minimise switching losses.

The key electrical parameters of the MOSFETs are listed in Table A.2.

Table A.2: Critical MOSFET parameters for H-bridge design.

Parameter	**Symbol**	**Design relevance**
Drain–source voltage rating	$V_{DS(max)}$	Must exceed $V_1 + V_{spike}$
On-state resistance	$R_{DS(on)}$	Conduction loss: $P_{cond} = I^2 R_{DS(on)}$
Gate threshold voltage	$V_{GS(th)}$	Determines gate drive voltage level
Input capacitance	C_{iss}	Determines gate charge and switching speed
Body diode forward voltage	V_f	Affects dead-time conduction loss

The switching performance of the MOSFETs directly influences the operating frequency and efficiency of the DAB converter. Fast-switching devices allow higher switching frequencies and support ZVS, which significantly reduces the switching losses. The ZVS condition is:

$$i_{L_s}(t_{dead}) > 0 \implies \phi > \phi_{ZVS,min} = 1 - \frac{V_2}{nV_1} \tag{A.2}$$

where n is the transformer turns ratio, $i_{L_s}(t_{dead})$ denotes the current flowing through the series inductance L_s at the dead-time instant t_{dead}, L_s is the equivalent series or transformer leakage inductance of the DAB converter, and t_{dead} is the dead-time interval inserted between switching transitions to prevent shoot-through.

The variable ϕ represents the normalised phase-shift ratio between the primary and secondary bridge voltages, while $\phi_{ZVS,min}$ denotes the minimum phase shift required to achieve ZVS. Furthermore, V_1 and V_2 are the primary-side and secondary-side DC voltages, respectively, and $n = N_p/N_s$ is the transformer turns ratio, where N_p and N_s

are the numbers of turns on the primary and secondary windings.

A.2.4 Gate Driver ICs

The gate-driver ICs convert the low-power PWM signals from the OPAL-RT simulator into high-current gate-drive signals for the MOSFETs (Fig. A.1). They allow fast switching, high-side gate control and accurate dead time, which improves the efficiency and reliability of the converter. The signal path from the OPAL-RT simulator to the MOSFET gate is:

$$\underbrace{V_{PWM} \approx 3.3\ \mathrm{V}}_{\text{Opal-RT digital output}} \xrightarrow{\text{Gate driver}} \underbrace{V_{GS} = 0 \text{ to } +15\ \mathrm{V}}_{\text{MOSFET gate}} \tag{A.3}$$

A.2.5 Gate Resistors (R_g)

Gate resistors are used to regulate the MOSFET switching speed and reduce voltage overshoots and EMI. Their value influences the switching energy loss, which can be approximated as:

$$E_{sw} \propto R_g \cdot C_{iss} \cdot f_s \cdot (V_1 + V_f)^2 \tag{A.4}$$

where E_{sw} is the switching energy loss, R_g is the gate resistance, C_{iss} is the MOSFET input capacitance, V_1 is the input DC voltage, and V_f is the MOSFET body-diode forward voltage.

A.2.6 Bootstrap Capacitors and Diodes

Bootstrap capacitors and diodes are used in the gate-driver circuit to provide the floating supply voltage required for driving the high-side MOSFETs. The bootstrap capacitor stores energy when the low-side switch is conducting and subsequently supplies the gate-drive voltage for the high-side switch. The minimum bootstrap capacitance can be

estimated as:

$$C_{boot} \geq \frac{Q_{gate,high} + I_{bias} T_s}{\Delta V_{boot}} \tag{A.5}$$

where C_{boot} is the bootstrap capacitance, $Q_{gate,high}$ is the high-side MOSFET gate charge, I_{bias} is the gate-driver bias current, T_s is the switching period, and ΔV_{boot} is the allowable bootstrap voltage droop. The bootstrap circuit is shown in the PCB schematic of Fig. A.1.

A.2.7 Snubber and Voltage Clamping Circuits

Snubber and voltage-clamping circuits, implemented using resistor–capacitor (RC) networks, are employed to suppress voltage spikes generated during MOSFET turn-off due to the converter inductance and parasitic layout inductance. These circuits protect the MOSFETs from excessive drain–source voltages and improve switching reliability. The resulting voltage spike can be approximated by:

$$V_{spike} = V_1 + (L_s + L_{stray}) \frac{di}{dt} \tag{A.6}$$

where V_{spike} is the transient voltage across the MOSFET, V_1 is the DC input voltage, L_s is the series inductance, L_{stray} is the stray inductance, and $\frac{di}{dt}$ is the current slew rate.

A.2.8 AC Auxiliary Power Supply Section

The AC auxiliary power supply provides isolated and regulated voltages required by the control circuitry, including the gate drivers, dead-time controllers, sensor amplifiers, and ADC. Electrical isolation from the main DC power bus improves safety and noise immunity, while stable supply rails ensure reliable operation of the converter control system. Typical output voltages include ± 15 V for gate drivers and analog circuits, $+5$ V for logic devices, and $+3.3$ V for digital interfaces.

A.2.9 OPAL-RT Interface Connectors

The OPAL-RT interface connectors provide communication between the H-bridge hardware and the OPAL-RT simulator, which generates the gate signals. They carry the control and feedback signals reliably and are immune to switching noise. The OPAL-RT connection is shown in Fig. A.2, and the connector functions are listed in Table A.3.

Table A.3: Opal-RT interface connector functions.

Connector	**Direction**	**Signals**
Analog output → Opal-RT	Board → Opal-RT	V_1, I_1, temperature measurements
Digital input ← Opal-RT	Opal-RT → Board	PWM gate signals for Q1, Q2, Q3, Q4

A.2.10 Dead-Time Conduction Loss

To prevent shoot-through, complementary PWM with an appropriate dead-time is applied to the switch pairs (Q_1, Q_2), (Q_3, Q_4), (Q_5, Q_6), and (Q_7, Q_8). The DAB converter operates at a switching frequency of 50 kHz, corresponding to a switching period of 20 μs.

The primary H-bridge employs normalised initial phases of 0 and 0.5, while the secondary H-bridge uses initial phases of 0.2 and 0.7, resulting in a 180° phase shift between the legs of each bridge and a controllable phase shift between the primary and secondary bridges for power transfer. During each dead-time interval, the series-inductor current is commutated through the MOSFET body diodes, introducing additional conduction losses due to the diode forward-voltage drop. For a single H-bridge, the dead-time conduction loss can be estimated as:

$$P_{dead} = 4V_f I_{L_s} t_d f_s \tag{A.7}$$

where V_f is the body-diode forward voltage, I_{L_s} is the series-inductor current, t_d is the dead-time duration, and f_s is the switching frequency. The dead-time loss increases

proportionally with V_f, I_{L_s}, t_d, and f_s. Therefore, the dead-time should be carefully selected to balance switching safety, efficiency, and ZVS performance. The summary of the components used in the first H-bridge is presented in Table A.4.

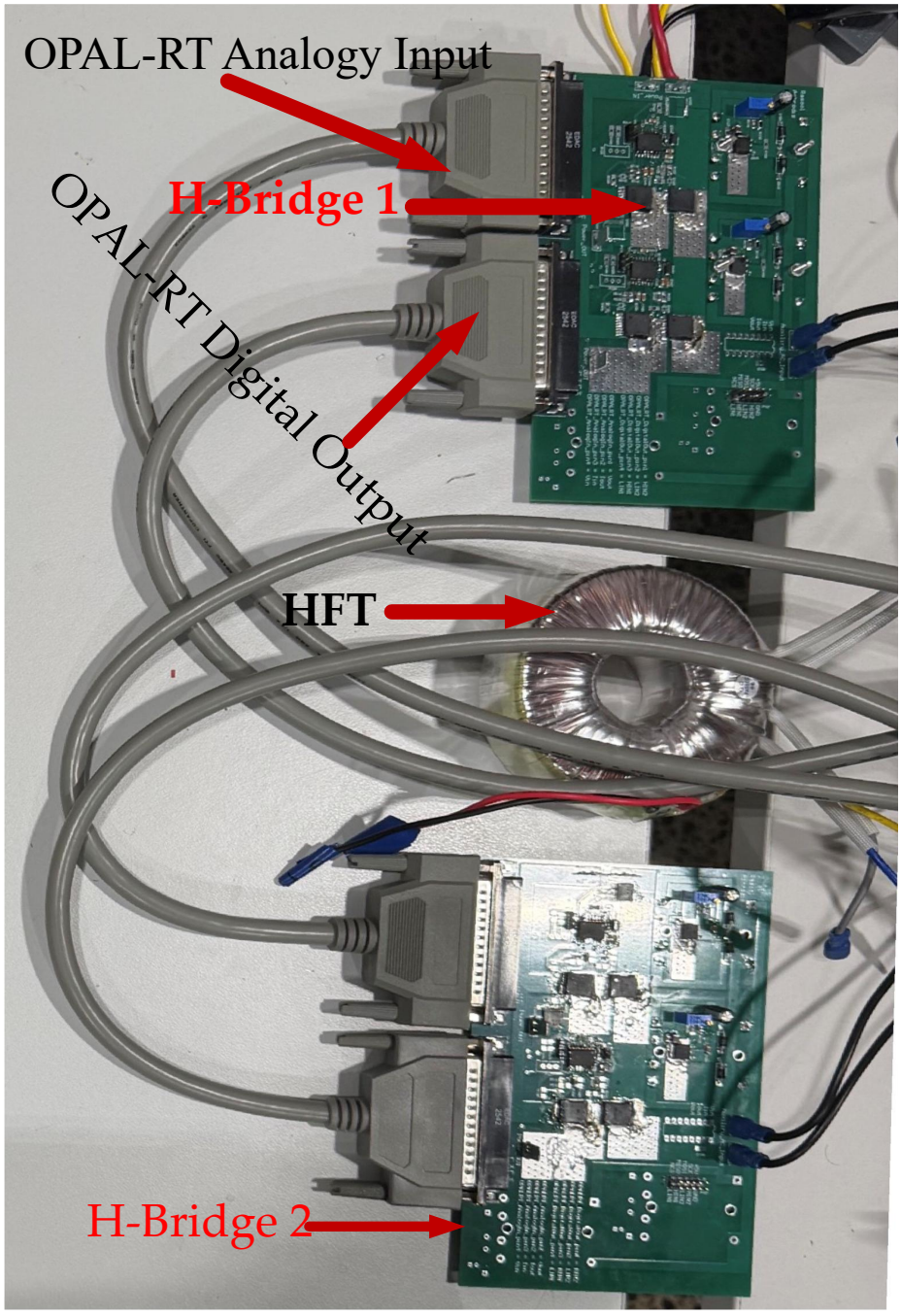


Figure A.2: Top view of the assembled DAB converter PCB.

Table A.4: Primary H-bridge components and their functions.

Component	Quantity	Primary Function
Input power terminals	2 (+ and −)	DC bus connection; carries full converter current
Bulk filter capacitors	2–4	Low-frequency ripple suppression; DC bus energy storage
Ceramic decoupling caps	8–16	High-frequency bypass; reduces switching-induced EMI
Power MOSFETs (Q1–Q4)	4	Main switching devices; generate HF AC from DC bus
Gate driver ICs	2	Signal amplification; bootstrap high-side drive; propagation matching
Dead-Time controller ICs	2	Shoot-through prevention; ZVS dead-time insertion
Gate resistors R_g	4–8	Switching speed control; EMI vs. loss trade-off
Bootstrap caps + diodes	2+2	Floating high-side gate supply for top MOSFETs
Snubber circuits	4	Overvoltage protection; dv/dt limiting
Voltage sensor circuits	2 sets	Isolated V_1 measurement; feedback to Opal-RT controller
External ADC	1	Digitisation of sensor signals for Opal-RT
AC auxiliary PSU + regulators	1 set	Control-side power supply; ± 15 V, $+5$ V, $+3.3$ V rails
OPAL-RT interface connectors	2	PWM in, analog measurements out

A.2.11 Power Switching Stage and Gate Driver Circuit

The power switching stage consists of four IRFP4768PBF N-channel MOSFETs arranged in a full-bridge configuration to enable bidirectional power transfer and high-frequency operation of the DAB converter. The bridge is interfaced with the high-frequency transformer (HFT) to provide galvanic isolation and controlled energy transfer. The MOSFETs are driven by two IR2101 half-bridge gate-driver ICs, which generate the required high-side and low-side gate signals through a bootstrap-based drive circuit.

This arrangement ensures reliable switching performance, proper electrical isolation, and accurate PWM control of the converter.

A.2.12 Current Sensing Subsystem

The current sensing subsystem employs Kelvin-connected shunt resistors and INA241-A3IDR current-sense amplifiers to accurately measure the input and output currents of the converter. These measurements are used for control, protection, and performance monitoring.

A.2.13 Voltage Sensing and Isolation

Voltage sensing is achieved using AMC1311BDWV isolation amplifiers, which provide galvanically isolated measurements of the converter voltages. This arrangement enhances safety, reduces noise coupling, and ensures reliable voltage feedback for the control system.

A.2.14 Analog-to-Digital Conversion Interface

A 12-bit AD7328BRUZ analog-to-digital converter (ADC) digitises the current and voltage feedback signals and transfers them to the controller through a serial peripheral interface (SPI). This enables accurate real-time data acquisition for monitoring and control purposes.

A.2.15 Linear Regulation

Linear regulators (LR12K4-G) are used to generate stable and low-noise supply voltages for the gate drivers and sensing circuits. Their use ensures minimal voltage ripple and electromagnetic interference, thereby improving the accuracy and reliability of the

converter control and measurement systems.

A.2.16 Isolated DC–DC Conversion

Galvanically isolated auxiliary supplies are generated using DC–DC converter modules (SPB09C-24), which are shown in Fig. A.2. These modules accept a wide input voltage range (36–75 V) and deliver isolated 24 V outputs. The isolated supplies power the isolation amplifiers, the high-side sensing circuits and the signal-conditioning stages. This architecture eliminates ground loops and enhances electromagnetic compatibility, particularly under high-frequency switching conditions.

A.2.17 Mitigation of High-Frequency Damped Oscillations

In practical DAB converters, high-frequency damped oscillations may arise from the resonance between transformer leakage inductance, printed circuit board (PCB) stray inductances, and the parasitic capacitances of semiconductor devices during switching transitions. These oscillations can cause voltage overshoots, waveform distortion, and increased EMI. To mitigate these effects, input capacitors were placed close to the power switches to minimise commutation-loop inductance, while RC snubber circuits were employed to dissipate the energy stored in parasitic elements and suppress voltage ringing, as shown in Fig. A.3.

A.3 Open-Loop Tests of the Prototype

The prototype was tested in open loop with the platform shown in Fig. A.4: the OPAL-RT simulator generated the gate signals with dead time and a fixed phase shift between the bridges, and the voltages and the series-inductor current were recorded with an oscilloscope.

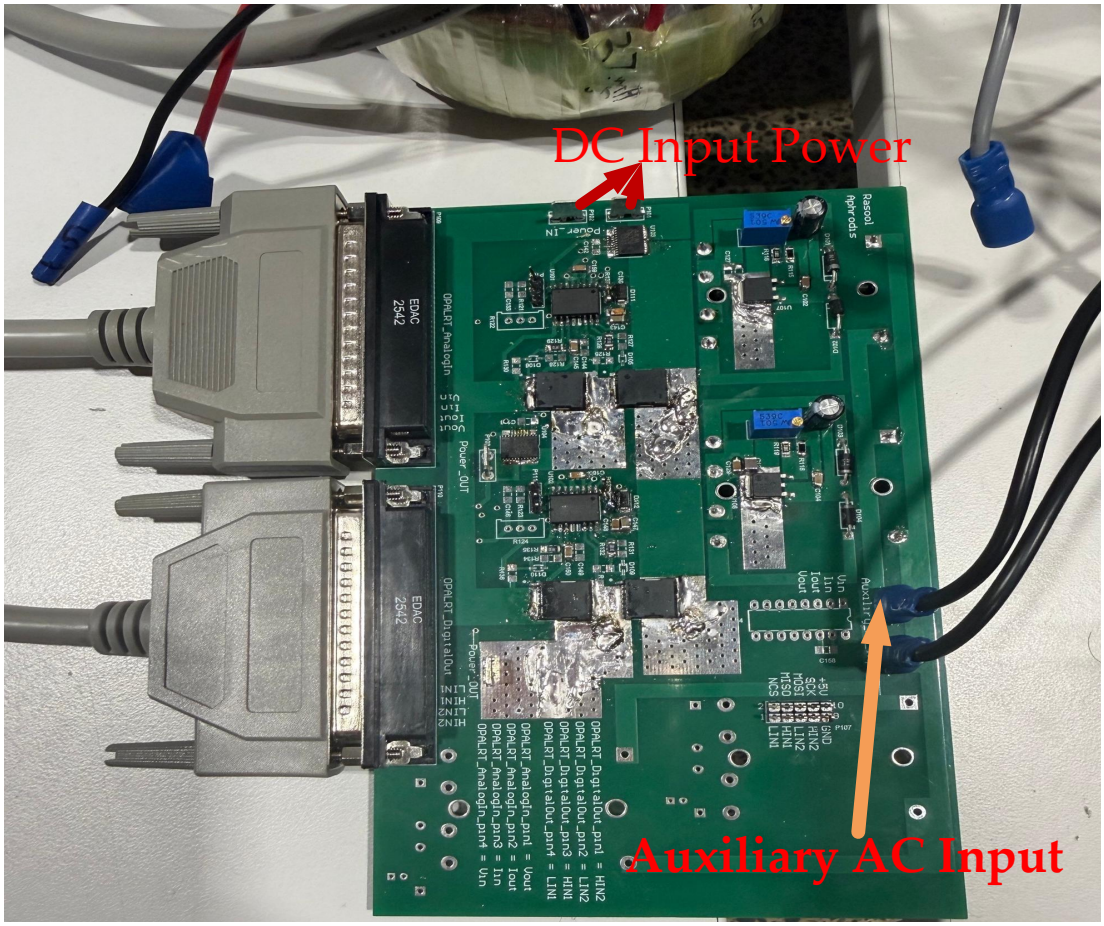


Figure A.3: H–bridge of the DAB converter PCB.

The experimental results show a switching frequency of approximately 20 kHz (T_s = 50 μs), primary and secondary voltages of about 50 V, a peak series-inductor current of approximately 5 A, and a bridge-voltage phase shift of 25 μs ($180°$), as shown in Fig. A.5.

Fig. A.6 shows the experimental complementary PWM signals of the DAB converter generated by the OPAL-RT controller. CH1–CH2 and CH3–CH4 represent the primary and secondary H-bridge gate signals, respectively.

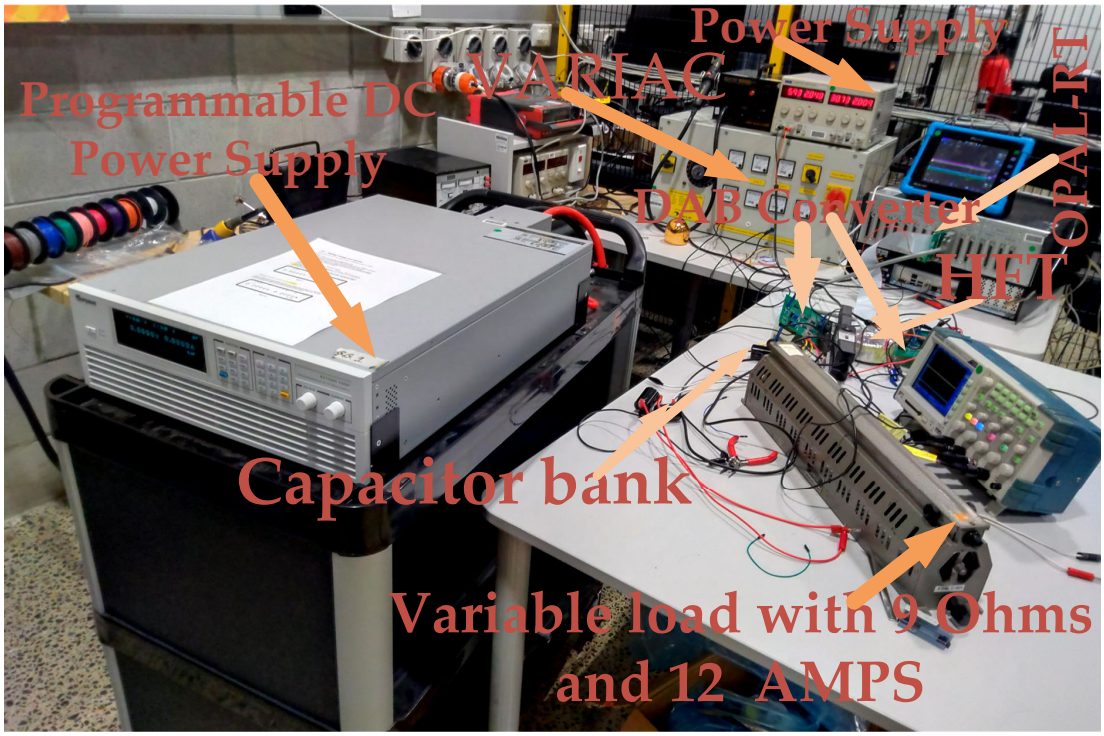


Figure A.4: DAB prototype connected to the OPAL-RT OP5700.

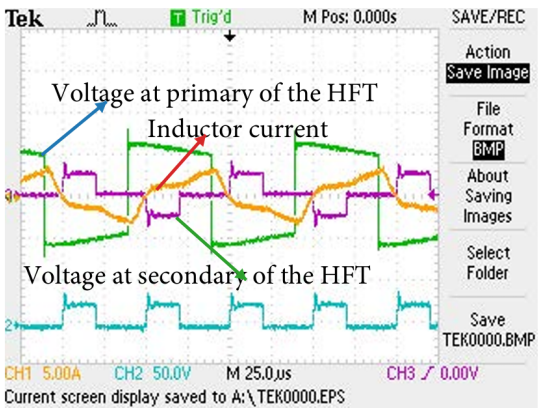


Figure A.5: Voltages at the HFT side with inductor current.

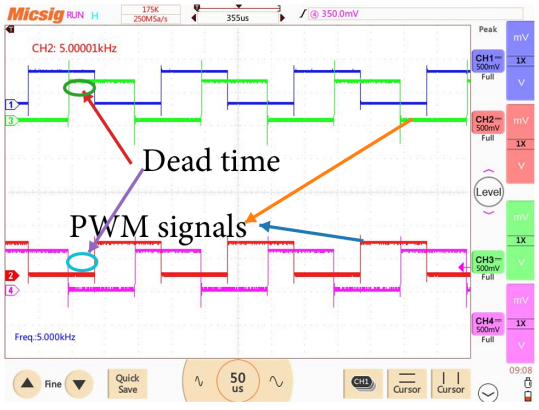


Figure A.6: Switching sequence with PWM signals.

A.4 Summary

This appendix presented the laboratory DAB prototype: the power stage, sensing circuits, gate drivers and OPAL-RT interface. The open-loop tests at about 50 V confirmed correct switching with dead time and power transfer through the phase shift between

the bridges. The closed-loop controllers of this thesis were not run on the prototype; this is listed as future work in Chapter 6.