RECONFIGURABLE MIXER DESIGN FOR SOFTWARE-DEFINED RADIOS

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DOCTOR OF PHILOSOPHY

Shilpa Mehta
School of Engineering, Computer and Mathematical Sciences

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Attestation of Authorship

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for the qualification of any other degree or diploma of a university or other institution of higher learning.

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Signature of candidate

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Abstract

The flourish of wireless communications brings along an ever-increasing number of wireless standards. This necessitates software-defined radio (SDR) to implement most transceiver components in the software domain. Ideally, an SDR receiver architecture should achieve a wide frequency dynamic range, low power consumption, high image rejection ratio (IRR), acceptable third-order intercept point (IIP3), and good conversion gain (CG) while maintaining a low noise figure (NF). However, the existing architectures cannot maintain good trade-offs among these performance parameters and doesn't have wide tuning range. Despite the rapid development of SDRs, it is challenging to realize several components in the software, including antenna, low noise amplifier (LNA), and mixers. This thesis focuses on the design and analysis of reconfigurable downconversion mixers.

The first objective of this thesis was to develop a wideband reconfigurable mixer that attained high CG, low NF, and IRR while maintaining a good trade-off among other performance parameters. To achieve this, we proposed a 0.9-13.5 GHz I/Q, inductively-peaked g_m-boosting Gilbert mixer. For the entire band of operation, the mixer attained a good return loss, $|S_{11}|$ of <- 10 dB, CG of 22 dB, NF of 2.5 dB, maximum IRR of 30.2 dB, and an IIP3 of -3.28 dBm, respectively. Additionally, the proposed mixer showed good reliability performance; however, it covered a large die area and attained poor linearity. Thus, a 1.8-5 GHz current bleeding, current mirror balanced mixer was proposed to overcome these problems. The proposed mixer achieved a maximum CG of 18.32 dB, an IIP3 of -5.89 dBm, and a NF of 1.19 dB at 5 GHz. Additionally, the mixer consumed only 10 mW of DC power and covered a 0.32 mm^2 area. However, this design also attained poor IIP3. Thus, a low-power, active inductor-based CMOS

down-conversion mixer was proposed. For 0.9-7 GHz, the mixer consumed 12.52 mW and achieved a $|S_{11}|$ of -27.69 dB and a maximum CG of 30.35 dB at the operating frequency. Additionally, the mixer was highly reliable and achieved an excellent IIP3 of 47.4 dBm and a NF of 3.5 dB. The next objective was to check the feasibility of the proposed mixer within the receiver architecture. Thus, we proposed a 0.9-20 GHz, highly reconfigurable I/Q receiver architecture that covered a design area of 4 mm^2 and consumed 320 mW of power from a 1.2V supply. The receiver attained an excellent IIP3 of 32 dBm with a NF of 5 dB and a maximum CG of 22.9 dB at 20 GHz.

To further improve the overall performance of our proposed reconfigurable mixers and receivers, we considered evolutionary algorithms (EAs) such as particle swarm optimization (PSO). Upon applying PSO, significant improvement in terms of CG, NF, IIP3, and IRR was achieved compared to the simulated results. Altogether, proposed mixer designs and reconfigurable receiver architecture contribute significantly to the development of SDRs, which will facilitate the deployment of pervasive Internet of Things (IoT) beyond the fifth generation (B5G) or the sixth generation (6G) of wireless communications.

Publications

C1: **Shilpa Mehta**, Xue Jun Li, "A Reconfigurable Mixer for 1.8-5GHz Software-Defined Radios," in Proc. of *2020 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications*, Suzhou, China, pp. 1–3, 29-31 July 2020.

C2: **Shilpa Mehta**, Xue Jun Li, "A Low Noise Image-Rejection Gilbert Mixer for Software Defined Radios," in Proc. of *2020 IEEE International Conference on Electronics, Computing and Communication Technologies*, Bangalore, India, pp. 1-6, 2-4 July 2020.

C3: **Shilpa Mehta**, Xue Jun Li, "A 0.9-20 GHz Image Rejection Receiver for Software-Defined Radios," in Proc. of *2021 Fourth IEEE International Conference on Electrical, Computer and Communication Technologies*, Erode, Tamil Nadu, India, pp. 1-6, 15-17 September 2021.

C4: **Shilpa Mehta**, Xue Jun Li, "A High Linearity Reconfigurable Mixer for Software-Defined Radios," in Proc. of *2021 Cross Strait Radio Science and Wireless Technology Conference*, Shenzhen, Guangdong, PRC, pp. 40-42, 11-13 October 2021.

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J1: **Shilpa Mehta**, Xue Jun Li, Massimo Donelli "Design and Analysis of a Reconfigurable Gilbert Mixer for Software-Defined Radios," *Sensors*, vol. 21, no. 8, pp. 1-25, 2021.

J2: **Shilpa Mehta**, Xue Jun Li, Massimo Donelli, "Recent Advancement in the Design of Mixers for Software Defined Radios," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 32, no. 3, pp. 1-20, 2022.

J3: **Shilpa Mehta**, Xue Jun Li, "Design and Analysis of A 0.9-20GHz Reconfigurable Receiver for Software-Defined Radios," *Under Review, Journal of King Saud University - Engineering Sciences*, 2021.

J4: **Shilpa Mehta**, Xue Jun Li, Massimo Donelli "Design and Analysis of A Double Balanced Mixer for Software-Defined Radios," *Under Review, International Journal of Circuit Theory and Applications*, 2021.

J5: **Shilpa Mehta**, Xue Jun Li, Massimo Donelli, "Performance Analysis of a Reconfigurable Mixer using Particle Swarm Optimization," *Under Review, International Journal of RF and Microwave Computer-Aided Engineering*, 2022.

B1: **Shilpa Mehta**, Xue Jun Li, Surjeet Dalal, "Convergence in Artificial Intelligence and Internet of Things in Software Defined Radios," *Under Review, Reshaping Intelligent Business and Industry: Convergence of AI and IoT at the Cutting Edge, Wiley-Scrivener Publishing*, 2021.

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Glossary and Notations

Glossary

ADC	Analog to Digital Converter
ASIC	Analog Semiconductor Integrated Circuit
ADS	Advanced Design System
AMPS	Advanced Mobile Phone System
AI	Active Inductor
ADE	Analog Design Environment
BPF	Bandpass filter
BW	Bandwidth
CDMA	Code Division Multiple Access
CG	Common Gate
CMOS	Complementary Metal-Oxide Semiconductor
CG	Conversion Gain
CL	Conversion Loss
CS	Common Source
CR	Current Reuse
CP1	1dB Compression Point
CCS	Cascode Common Source
CPU	Central Processing Unit
dB	Decibels
DAI	Differential Active Inductor

DDC	Digital Downconversion
DC	Direct Current
DSP	Digital Signal Processing
DAC	Digital to Analog Converter
DBIMN	Dual Band Impedance Matching Network
EM	Electromagnetic
EA	Evolutionary Algorithm
FET	Field Effect Transistor
FPGA	Field Programmable Gate Array
GPP	General Purpose Processor
GPRS	General Packet Radio Service
GHz	Giga Hertz
GSM	Global System for Mobile Communication
GPU	Graphics Processing Unit
HDR	Hardware Defined Radio
HP	High Performance
Hz	Hertz
HRR	Harmonic Rejection Ratio
HSDPA	High Speed Downlink Packet Access
I/Q	In-Phase Quadrature
IIP3	3^{rd}-order Input Intercept Point
IC	Integrated Circuit
IF	Intermediate Frequency
IFTT	Impedance and Frequency Transformation Technique
IMN	Input Matching Network
IRR	Image Rejection Ratio
IRL	Input Return Loss
IF	Intermediate Frequency

JFET	Junction Field Effect Transistor
KCL	Kirchoff Current Law
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Lowpass Filter
MUT	Mixer Under Test
MGTR	Multi Gated Transistor
MN	Matching Network
MOPSO	Multi Objective Particle Swarm Optimization
mmWave	Millimeter Wave
mW	Milliwatt
NF	Noise Figure
NFET	N-Type Field-Effect Transistor
NMOS	N-Type Metal-Oxide Semiconductor
ORL	Output Return Loss
OpAmp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PFET	P-Type Field-Effect Transistor
PSO	Particle Swarm Optimization
Q**-Factor**	Quality Factor
RF	Radio Frequency
SiP	System in Package
SDR	Software Defined Radio
Si-Ge	Silicon-Germanium
SoC	System on Chip
SMC	Scalar Mixer Calibration
SNR	Signal-to-Noise Ratio

SoC	System-on-Chip
SOLT	Short Open Load Thru
TCA	Transconductance Array
TIA	Transimpedance Biquad Amplifier
USRP	Universal Software Radio Peripheral
UHD	Universal Software Radio Peripheral Hardware Driver
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
VCR	Voltage Controlled Resistor
WPAN	Wireless Personal Area Network

Notations

G_m	Transconductance
Γ_{out}	Output Reflection Coefficient
Γ	Semi Empirical Constant
k	Boltzmann Constant
λ	Wavelength
M	Mutual Inductance
NF	Noise Figure
ω	Angular Frequency in radians/s
Ω	Ohms
ϕ	Phase Shift
θ	Angle
A_v	Voltage Gain
AV_0	Open Loop Voltage Gain
AV_f	Closed Loop Voltage Gain
C	Capacitor
C_{gs}	Gate-Source Capacitance
C_{gd}	Gate-Drain Capacitance
C_{db}	Drain-Body Capacitance
C_{ds}	Drain-Source Capacitance
c_i	Acceleration Coefficient
f	Frequency
F	Noise Factor
f_0	Operating Frequency
g_m	Transconductance
h	Height of Substrate
I_d	Drain Current

I_{IF}	IF Output Current
K	Conduction Parameter
L	Inductor
P_{DC}	DC Power Dissipation
P_{in}	Input RF Power
P_{out}	Output RF Power
s_i^k	Position of agent
S_{11}	Input Return Loss
S_{21}	Transmission Coefficient
S_{12}	Reverse Transmission Coefficient
S_{21}	Output Return Loss
V_{DD}	Supply Voltage
V_{DS}	Drain Source Voltage
V_{GS}	Gate Source Voltage
V_{in}	RF Input Voltage
V_n^2	Power Spectral Density
V_{out}	RF Output Voltage
V_{TH}	Threshold Voltage
v_i^k	Velocity of agent
w	Weighting Function
Y	Admittance
Z_{in}	Input Impedance
Z_L	Load Impedance
Z_{out}	Output Impedance
Z_P	Parallel Impedance

Chapter 1

Introduction

1.1 Background

Wireless communications may be traced back to the early 1860s when Maxwell theoretically predicted and demonstrated the existence of electromagnetic waves. In 1887, Hertz experimentally proved this concept. Marconi conducted the first wireless transmission on May 13, 1897, across the Bristol Channel: it simply read, "Are you ready?". This historical experiment demonstrated the concept of wireless communication. Since then, several other radio systems came into existence that could operate within a wide range [1, 2, 3, 4, 5]. During the early 1950s, radio systems were used to operate in the analog domain, where analog components and circuits were employed for modulation and filtering purposes. Besides, designing and implementing a reliable communication system was considered a tedious task, which requires skillful analog circuit designer experts, making it difficult for mass production. With technological advancements, it became feasible to enable mass production of the systems. Additionally, this approach was cost-effective and highly flexible. This led to the development of the first digital radio primarily dependent on non-programmable designs. Further advances in this domain resulted in the development of programmable components, making it easier to perform signal processing operations different from conventional radio systems.

The first prototype of digital radio was demonstrated in 1980 [6]. A wireless network was

established in the United States during the same year and subsequently became popular in other countries as well. When the Advanced Mobile Phone System (AMPS) standard emerged, this signified the beginning of the first generation of cellular communications. During this, separate frequencies or channels were utilized for each and every conversation. Thus, considerable bandwidth was the requirement for a large number of users. However, the first mobile phone released in this generation was bulky, required more power for frequency selection, and had low battery life. To address these issues, several other standards emerged like Global System for Mobile Communications (GSM), code division multiple access (CDMA), general packet radio service (GPRS), and high-speed downlink packet access (HSDPA), which served as the foundation for subsequent standards. They expanded wireless coverage to include medical, civil, and military applications [7, 8].

With the advancement in integrated circuit (IC) technology, it became feasible to design miniaturized devices with improved functionality. System-in-Package (SiP) and System-on-Chip (SoC) are significant packaging trends. SiP approach assembles different technology-based circuits within a single package. This approach can provide high integration flexibility, lower development costs, and rapid availability on the market. Besides, it is possible to use suitable technologies for different blocks present in the system. With the rise in the number of high-frequency interconnects, it becomes difficult to utilize this approach, as the system becomes increasingly complicated. For example, GSM mobile phones were becoming smaller as compared to AMPS phones due to the decrease in radio frequency (RF) component count, which lowers the device's form factor. SoC integrates the whole system on a chip that can be fabricated using only one technology. The rapid evolution of complementary metal-oxide-semiconductor (CMOS) technology and the downscaling of CMOS bring deep sub-micron processes. Each new CMOS technology necessitates a re-design and optimization of analog circuits. Similarly, technology scaling will lower the supply voltage, resulting in the headroom of the biasing voltage, and mature circuit designs may fail to fulfill the desired specifications. Nevertheless, CMOS technology is highly preferred as it can provide an ultra-high level of integration, miniaturized design, while maintaining low manufacturing costs for large-scale production. Therefore, IC

designers thrive on overcoming the limitations of technology and designing circuits that meet the specifications [9]. Due to the current trend in the wireless communication sector, it is necessary to have a single piece of equipment that can reconfigurably support multiple standards, is cost-effective, and has good user flexibility with wide tuning range. This necessitates the concept of SDR.

1.2 Software Defined Radios

Wireless standards are rapidly evolving, with each standard defining its own frequency spectrum, bandwidth modulation, and other physical layer specifications. As a result, a radio system must comply with a single set of wireless standards. Traditional radios, or hardware-defined radios (HDRs), are more expensive because they require specific hardware to accommodate a variety of wireless standards. For example, the progression of cellular radio from the first generation (1G) to the fifth generation (5G) allows smartphones to provide high data rate multimedia services due to device miniaturization and advancements in battery life. However, it is challenging for HDRs to switch from one standard to another. For example, second-generation (2G) or third-generation (3G) devices cannot be quickly reconfigured to support fourth-generation (4G) cellular communications. Thus, it increases the overall expense of the hardware due to rapid technological and standards development. As a result, it is desirable to create reconfigurable radio systems that function in accordance with multiple standards [8]. SDR is a novel technology developed to provide customized and reconfigurable radio systems that can support multiple services with the help of software [10]. Additionally, SDRs are capable of operating in numerous bands and standards. The advantages of SDRs included: (1) They can adapt and implement a variety of physical radio protocols. (2) They require a single hardware module with separate software installed for each radio protocol. (3) They make it easy for developers to modify the code rather than developing and replacing existing hardware modules. (4) They are simple and have a wide tuning range as compared to traditional HDRs (5) They are cost-effective, as in many radio systems it is cheaper to mass produce a radio chip that can perform demodulations

and RF processing simultaneously. On the other hand, when there is a strict requirement for prototyping or small design production, SDRs are considered perfect solutions [11].

1.2.1 Why SDR?

Wireless communications have sparked a lot of attention in recent years due to their potential to offer access to real-time information throughout the world. Modern radio systems have their own protocols and are based on current wireless communication developments. HDRs include specific components such as modulators / demodulators, coding / decoding to realize a particular protocol. In this case, all signal processing is carried out on the hardware. SDRs replace traditional radio components with their software counterparts, which allows the radio to be quickly customized, developed, and updated for multiple systems that operate within a wide tuning range to support more standards and future communication standards. Generally, an SDR consists of two major parts (1) an analogue front-end that takes care of frequency downconversion accompanied by an analogue to digital (ADC), and (2) digital signal processing components for handling processing operations. As a result, most processes are carried out within the digital domain. These can operate on various processing platforms, such as field-programmable gate arrays (FPGAs), graphics processing units (GPUs), and digital signal processors (DSP). Moreover, General-Purpose Processors (GPP) or a mixture of any of the above-mentioned platforms can be helpful for processing.

FPGAs have high computational capability and power efficiency, but due to their inflexibility, upgrade is difficult. Likewise, GPUs also suffer from the same problem. DSPs can overcome the upgrade problem, but are not the best fit for computationally intensive tasks and may rapidly degrade performance. Finally, due to the high level of reconfigurability, GPPs are commonly used for SDR implementations and prototypes. Unfortunately, as GPPs are not designed for mathematical computations, they may be inefficient in terms of power consumption.

The usual data flow in an SDR system is shown in Figure 1.1. The software domain handles the baseband signal processing on both transmission and reception ends in this scenario. To develop a perfect SDR, ADC and digital-to-analogue (DAC) blocks must be pushed deeper inside the RF

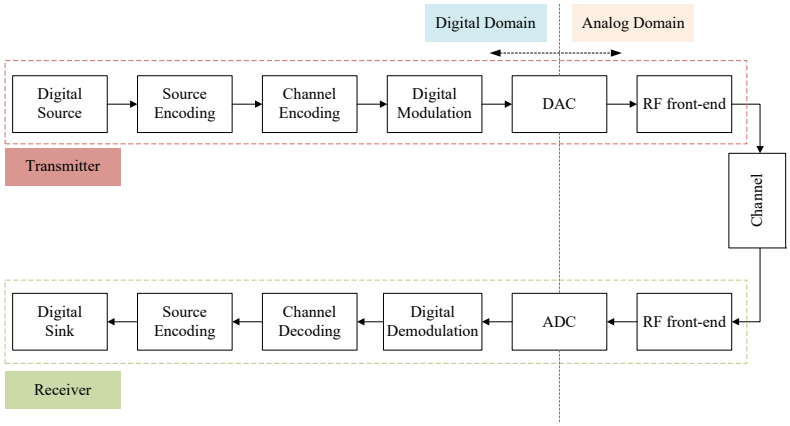


Figure 1.1: Software-Defined Radio platform

block, which will improve the programmability of RF front-ends such as mixers and low-noise amplifiers (LNAs), and antennas. The possibility of reconfigurability comes from the fact that various frequency bands, air interfacing protocols, and capabilities can be easily reconfigured by updating its software rather than completely replacing the hardware [6].

1.2.2 Challenges of SDR

The primary goal of SDR is to offer a reconfigurable platform with high interoperability. It is capable of handling several wireless communication services within a single package. Smart antennas, programmable RF modules, high-performance ADC / DAC, DSP technology, and interconnect technologies are the critical building blocks of practical SDRs. However, high-resolution, high-sampling-rate ADC converters are not quite common, especially for battery-operated SDRs. As high resolution leads to voltage resolution and sampling frequency problems. This is mainly due to the fact that the sampling rate and bits of resolution have trade-off issues. As high-resolution ADC run at low sampling frequencies, reverse process takes place during high sampling frequencies. Several attempts have been made by researchers to develop ADCs with high sampling rates and high resolution, which in turn lead to high power consumption. Additionally, clock and frequency generation circuits are common sources of power consumption. This is mainly due to the fact that a separate clock is required for each wireless standard within SDR. Moreover, current SDRs require several antennas for wideband coverage, as conventional

antenna design approaches restrict the antenna's applicability and performance. Thus, a single wideband antenna will be more effective and cost-efficient than multiple narrowband antennas. Thus, in this domain, the main focus is to determine the array processing blocks and techniques to improve antenna performance. Array processing and beamforming approaches are beneficial if the implementation cost is not important. Ideally, an SDR features a self-adapting, self-aligning, and self-healing antenna that is capable of providing high flexibility according to the desired specifications. Likewise, a group of RF modules is required to cover a wide frequency range. Reconfigurable RF modules are becoming increasingly popular as a result of various advances in synthesizers and high-performance semiconductor technology.

Another solution is to make use of micro-electromechanical system (MEMS) technology that has enabled the development of high-performance RF devices with a high degree of circuit integration, including switches. This technology enhances the performance and versatility of various RF components, such as voltage control oscillators (VCOs). Bandpass filters are another critical transceiver block that provides effective channel utilization and excellent sensitivity. These filters are expensive and least versatile blocks as part of RF modules. Implementing them in SDR must be electrically configurable or stacked to create a filter bank. Because of their complicated mechanical geometry and unique materials, MEMS devices have distinct working mechanisms and biased approaches. Thus, they require specialized methods and equipment for measuring mechanical reactions on the microscale and nanoscale and are impractical for high-volume deployment. [12]. Therefore, CMOS technology is one of the best alternatives, with a mature process and excellent integration capabilities. With the advancements in CMOS technology and a deep understanding of RF, circuit design enables easy implementation of all essential RF components and the development of fully integrated transceivers. With the proliferation of wireless protocols, it is necessary to develop reconfigurable systems with adjustable components to enable hardware sharing among different blocks [13].

1.2.3 SDR development systems

SDRs are promising candidates to implement most of the radio components in the software domain, leading to a compact radio size. Ideally, an SDR should follow the traditional transceiver architecture. However, existing SDR architectures vary significantly from one system to another. These architectures are developed using commercial or open-source software and hardware. In particular, SDR development is possible using (a) commercial software development for various hardware platforms, (b) a standardized hardware platform, (c) compilers that allow the same code to run on various hardware platforms.

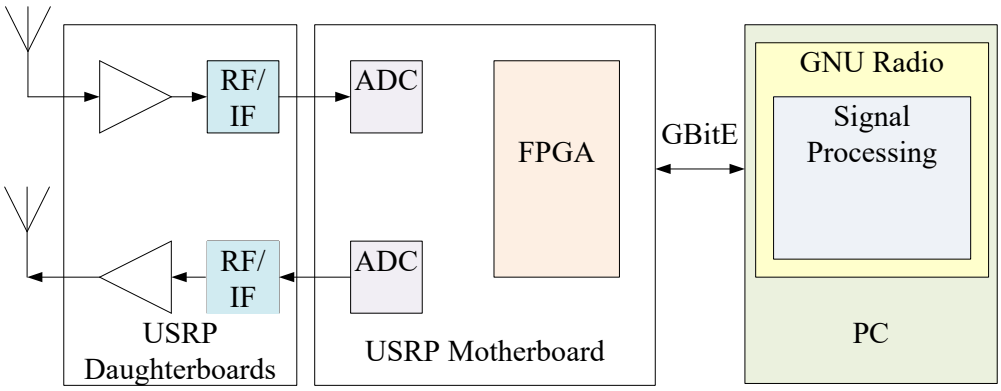


Figure 1.2: USRP architecture

GNU radio is a popular open source software platform for implementing SDRs. This is highly compatible with the Universal Software Radio Peripheral (USRP) platform, which interacts with USRP Hardware Driver (UHD) to communicate with USRP boards. Additionally, GNU Radio has high compatibility with various other hardware front-ends. This radio contains in-built signal processing blocks useful for modulation / demodulation, filtering, I/O operations, and communication with USRP boards. It is also possible to develop specific blocks for advanced functionality features. The newly developed blocks and flow graphs can be easily viewed and used by researchers and radio developers. Furthermore, a software application can allow the radio to exchange data with the connected USRP platform.

As shown in Figure 1.3, another reconfigurable hardware interface for the computation and radio (RHINO) architecture was proposed to support SDR applications using the FPGA platform

[14]. The architecture adopts a Xilinx Spartan-6 FPGA linked to an ARM3517 ARM central processing unit (CPU). FPGAs are well known for solving intensive computational algorithms, and the CPU is responsible for managing the data flow in FPGAs. USRP is the most popular FPGA-based SDR front-end hardware module, which helps users create their own SDRs. The hardware contains an antenna, RF front-end, ADC/DAC, and FPGA. Each USRP model includes a basic motherboard and a removable daughterboard. The daughterboard is used to perform the RF front-end functions, which can be easily changed for transmission and reception at different frequencies. Existing daughterboards support several radio protocols. An ADC is utilized for the ADC via a daughterboard. However, most of the digital processing is done by the host CPU. The UHD connects the USRP device to the host computer. The hardware unit is also compatible with advanced operating systems. As all USRP boards share UHD, the software developed for one device will function with the others. Therefore, developers do not have to worry about USRP models when designing radios using the USRP platform. As a result, an increasing number of researchers are turning to the USRP to create new radio protocols.

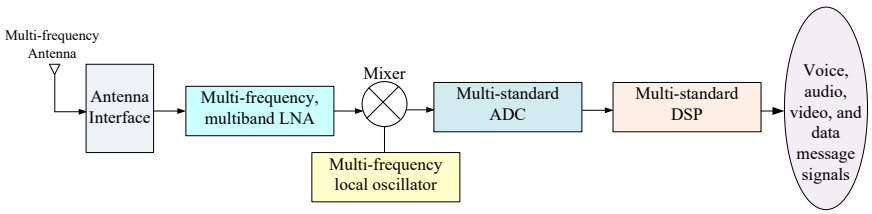


Figure 1.3: SDR receiver architecture

Likewise, in [14], another SDR receiver architecture has been discussed, as shown in Figure 1.3. The receiver requires a reconfigurable front end (LNA, mixer, and antenna), and it is challenging to develop such RF circuits. As shown in Figure 1.4, this is mainly due to numerous trade-offs that exist in designing RF circuits. As a result, SDR hardware must be modified to maximize performance and satisfy the minimum requirements. To overcome this problem, various architectures have been proposed in [15, 16, 17, 18, 19]. One of the architectures discussed in [20], follows the dynamic partition reconfiguration technology which has been deployed on FPGA which makes it flexible to handle multiple standards on the single software. The proposed architecture covered a small area and consumed less power. However, the proposed

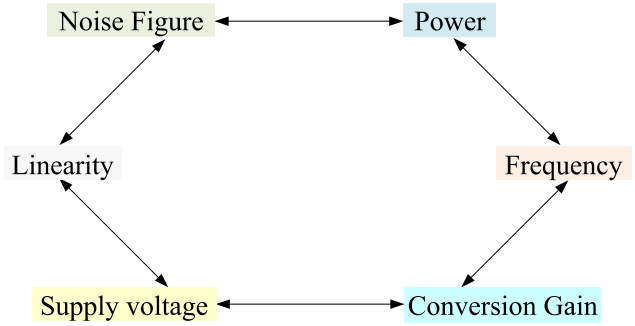


Figure 1.4: SDR design tradeoffs

architecture is not compatible with the implementation of data links and MAC layers. As a result, the increasing popularity of SDR presents many difficulties in the design of multi-frequency and multi-bandwidth RF front-ends.

The mixer is a crucial block in the SDR receiver architecture, useful for frequency downconversion. The mixer's performance has an impact on the receiver's overall performance. For example, the conversion gain (CG) of the mixer depends on the impedance matching and the provided LO level when proposing any mixer. Consequently, the mixer's NF significantly impacts the receiver's overall performance. To obtain low NF, tunable filters or noise-cancelling circuits are required. This may affect the overall power consumption and design area. Thus, the higher the power consumption, the shorter the battery life of compact devices. Furthermore, parasitics must be handled carefully to maintain the proper input impedance, which affects the noise figure (NF) and the CG. Likewise, off-chip filters can be added to enhance linearity. Besides, image rejection ratio (IRR) is an important parameter that determines how effectively a mixer rejects image signals. Image rejection circuits such as complex filters can be used to achieve high IRR at the expense of high-cost and bulky circuits. Therefore, it is vital to consider these design trade-offs when designing a high-performance mixer.

The performance of analog circuits operating in a narrowband can be easily improved by design optimization tools such as Cadence Virtuoso, Advanced Design Systems (ADS), etc. while considering downscaling technical aspects into account. However, it is difficult to resolve design issues when a wideband mixer has multiple optimization objectives. To overcome this problem, evolutionary algorithms (EAs) such as particle swarm optimization (PSO) can be used to solve

nonlinear multi-objective design problems with multiple constraints. With EAs, a set of feasible design solutions can be obtained, from which several insights and trade-offs among the circuit performance objectives can be deduced.

1.3 Research Questions

This thesis addresses the following research questions.

- Question 1: How to design and analyze a g_m-boosted Gilbert mixer for SDR applications that attains high IRR and CG while maintaining good balance among other performance parameters?
- Question 2: How to develop and analyze a balanced, reconfigurable, current-bleeding mixer for low-noise performance at the expense of IIP3?
- Question 3: How to design and analyze an active inductor-based reconfigurable balanced mixer for high linearity performance?
- Question 4: How to design and analyze a high-performance, wideband reconfigurable receiver for SDR applications?
- Question 5: How to investigate the implementation of PSO in mixers and receiver architecture for performance evaluation and comparison with previously obtained results?

1.4 Objectives

This research aims to develop and analyze novel wideband reconfigurable multiband mixer circuits for SDRs. SDR transceivers desire mixers that can achieve a high CG and consume less power. CMOS process technologies are widely used to develop current transceivers because of their ability to minimize power consumption. Nevertheless, the CG performance is degraded as a result of additional circuitry requirements. Thus, it is desirable to develop and analyze a

low-power mixer that attains high CG without significantly increasing the design complexity. As we know, the flexibility of SDR transceivers can be enhanced by improving the operating sensitivity range, reducing interference, and increasing the tunable bandwidth. Thus, low NF and high IRR must be achieved by reconfigurable design by using appropriate filter designs. The proposed design should be compact and cost-effective to prolong the battery life of mobile devices.

This research proposes and analyses reconfigurable mixers for SDR receivers, while attempting to address the above-mentioned design challenges. Additionally, it also covers the design and analysis of high-performance SDR receiver architecture. The performances of the proposed structures have been further improved using PSO.

1.5 Thesis Organisation

This thesis studies and investigates challenging problems related to SDR, including reconfigurable mixers and receiver architectures. The thesis is organized into eight chapters.

Chapter 1 outlines our rationale for undertaking this challenging research project, as well as introducing key points and summarizes our contributions to the SDR domain.

Chapter 2 presents the literature review, which revisits the basic SDR receiver architectures. The selection of mixer topologies highly influences the overall performance of the receivers. Thus, this chapter also provides a detailed survey on mixer design, focusing on wideband and multiband topologies. Based on the study, design challenges and effective techniques have been identified and subsequently incorporated into the proposed solutions.

Chapter 3 presents the design of a 0.9-13.5 GHz I/Q reconfigurable mixer. The proposed design achieves low NF, higher CG and reasonable IRR compared to similar existing works at the expense of IIP3, power and design area.

Chapter 4 presents a low power, low area 1.8-5 GHz band mixer. The proposed mixer achieves an improved NF and reasonable CG compared to the previous design at the expense of IIP3.

Chapter 5 presents a 0.9-7 GHz continuously tunable, high-linearity reconfigurable mixer. The

proposed mixer also achieves higher CG and reasonable NF than the previously proposed designs. The design consumes high power and covers a similar design area compared to the previous design discussed in Chapter 4.

Chapter 6 presents an image-rejection receiver design operating within a band of 0.9-20 GHz, based on the mixer proposed in Chapter 5 that attains an excellent IIP3 and high CG performance within the entire band of operation. The proposed receiver architecture maintains similar IIP3 and CG performance with reasonable NF. However, this design also covers more area and consumes higher power than previously proposed designs due to the complexity of reconfigurable building blocks such as mixers, LNAs, and filter circuits within the circuitry.

Chapter 7 presents the implementation of the optimization technique on all proposed circuits from previous Chapters (Chapter 3 - 6) to maintain the high performance in terms of all parameters simultaneously. This chapter covers an overview of the optimization process, various techniques, and functions that are helpful in solving optimization problems. PSO is adopted to optimize specifications while maintaining the operating conditions of the active devices present within the circuitry. The optimized performance parameters have been compared with the simulated results. Based on the comparison, it has been found that PSO has significantly improved the overall performance of a design in terms of CG, NF, IIP3 and IRR.

Chapter 8 concludes the thesis and provides recommendations for future research.

Chapter 2

Literature Review

Recent advancements in wireless communications and ICs have driven circuit design to evolve rapidly. The first step is to select the appropriate architecture to design a mixer. The next step is to understand the crucial parameters and optimize them. For reconfigurable mixers, it is desirable to select an architecture that can support multiple standards simultaneously. Additionally, the mixer architecture must be adaptable to process scaling and take advantage of the benefits offered by CMOS processes. Selecting the proper architecture can be a difficult, time-consuming, and challenging process. Thus, it is desired to understand the existing receiver architectures and their challenges. This chapter starts with an overview of different receiver architectures and the requirements for SDR receivers. Then, it will discuss about mixers, including the necessity of mixers, their classification, topology selection based on the applications, and prospective development.

2.1 SDR Receiver Systems

This section covers a set of receiver architectures, along with their advantages and disadvantages. A deep understanding of these architectures can help to select the best candidate for SDRs.

2.1.1 Superheterodyne Receivers

As illustrated in Figure 2.1, a superheterodyne receiver was introduced by Edwin Armstrong in 1918. Antennas convert electromagnetic waves into voltage signals, followed by band-pass filters (BPFs). Ceramic filters are commonly used as BPF filters, as they have good bandpass performance with excellent image filtering. After band selection, the signal amplification is done by a low noise amplifier (LNA). The structure also includes a single downconversion mixer with the LNA output and the LO signal. Thus, the obtained signal frequency shifts down to intermediate frequency (IF), and upon mixing it returns the sum and difference of these signals, referred to as IF signals. However, difference signals are considered undesired for most applications that can be rejected using a bandpass filter, followed by the mixing stage.
Image frequency rejection is one of the significant problems in receiver architectures. Figure 2.2 shows the downconversion with and without the use of image rejection filters.

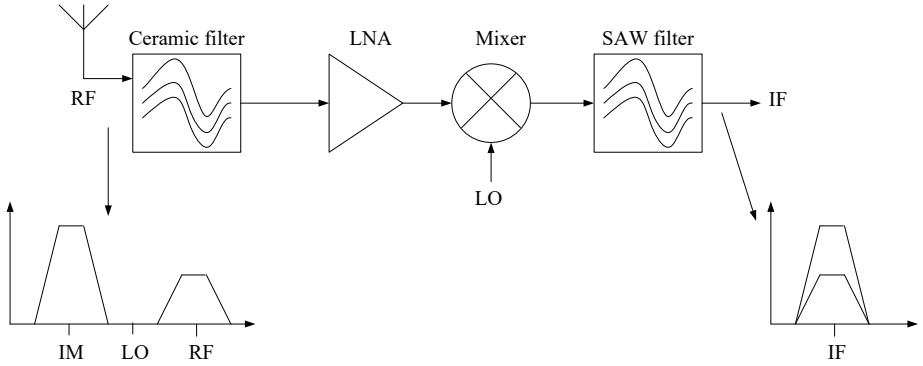


Figure 2.1: Single downconversion receiver architecture

Channel selection is another problem. The channel bandwidth is relatively small compared to the IF. Thus, it is desirable to use surface acoustic wave (SAW) filters for selecting analog channels. Nevertheless, these filters are not widely used due to their high cost and incompatibility with monolithic integration. The superheterodyne architecture addresses this problem by performing an image signal filtering process before entering the mixing stage. For example, in the case of dual sideband communication, since both RF signals carry the same information, IF band spectrum overlapping will occur, which does not create any problem. However, it becomes problematic in the case of sideband applications, as unwanted image signal rejection becomes

predominant. Similarly, the trade-off between an antenna and channel filtering enforces the optimal IF frequency, which drives the design of single conversion superheterodyne receivers [21].

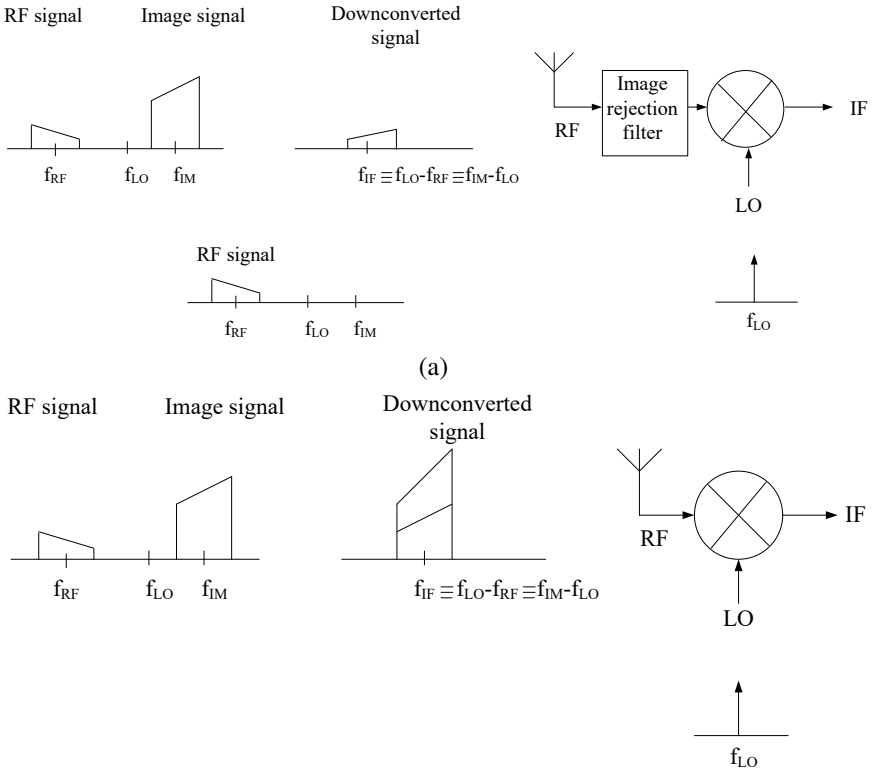


Figure 2.2: Downconversion process (a) with image rejection (b) without image rejection

2.1.2 Dual conversion Superheterodyne Receivers

For single conversion superheterodyne receivers, choosing low IF affects the antenna filter specifications regardless of any change in the channel filters. On the contrary, a high IF restricts the channel filtering process and relaxes the filter standards. In either case, for most wireless applications, strict antenna filter specifications require ceramic filters to behave like an image rejection filter, and IF filtering necessitates the use of SAW filters for analog channel selection. Figure 2.3 shows the dual conversion superheterodyne receiver architecture. The receiver utilizes dual IFs for easy image filtering and channel selection purposes. The primary goal of this architecture is to upconvert RF to high IF by relaxing the image filter specifications. The

down-conversion process results in low IF, which simplifies channel selection. Nonetheless, there is a need for antenna and image filters in most applications that desire the implementation of ceramic filters. Thus, it is difficult for the superheterodyne receivers to overcome the image rejection problem monolithically.

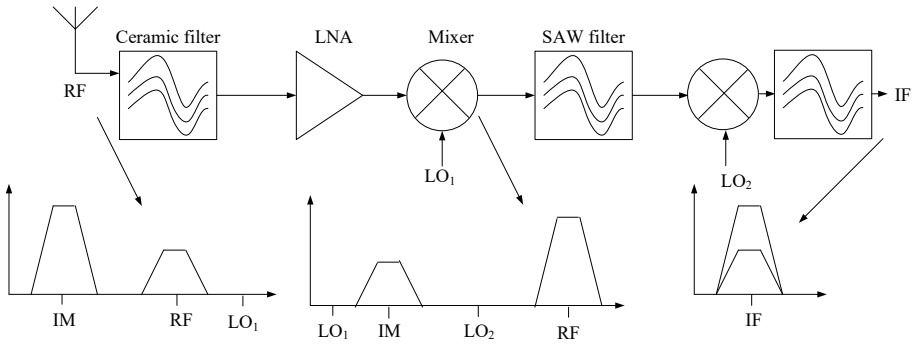


Figure 2.3: Dual downconversion receiver architecture

2.1.3 Image Rejection Receivers

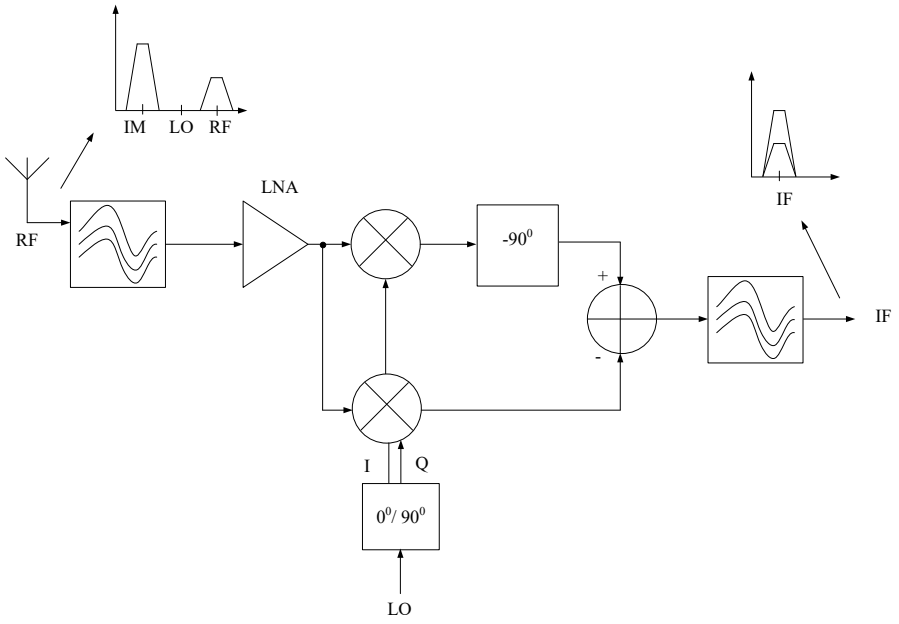


Figure 2.4: Image rejection receiver

Superheterodyne receivers were tuned to address the image rejection problem rather than RF performance. An image rejection receiver, as shown in Figure 2.4 consists of sophisticated mixer

circuitry that suppresses the undesired signal, eliminates the lock-on structure and enables the system designers to maximize the performance of the RF system. The complex mixer circuitry contains two mixers sharing the common RF input, whereas the LO port is taken care of by the quadrature signals. Thus, introducing a 90-degree delay line within one of the signal paths makes it possible to show in-and out-of-phase signals, where the image signal is in-phase, and the desired signal will be delayed by 180 degrees. As a result, the difference between the paths results in cancellation of the image signal and the addition of the desirable signal. This eliminates the use of ceramic filters within the architecture; however, the main requirement is to consider the quadrature accuracy in terms of both gain and phase of LO/IF paths for image rejection purposes. For example, the undesired signal can be eliminated if both LO signals have a 90-degree phase delay.

It is challenging to develop perfect wideband quadrature phase shifters. Thus, it is desired to use the weaver receiver architecture as shown in Figure 2.5. This architecture employs additional mixer and quadrature LO signals to eliminate the 90-degree phase shifter within the circuitry. Thus, for both image rejection techniques, the baseband processing gets relaxed in the presence of low IF, IF filtering specifications. To further reduce image rejection, polyphase filters can be employed within the architecture.

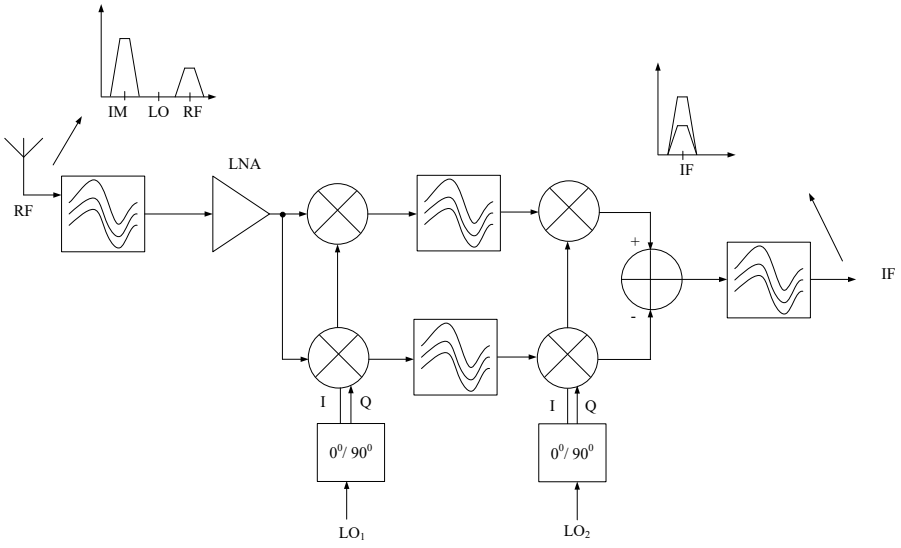


Figure 2.5: Weaver receiver

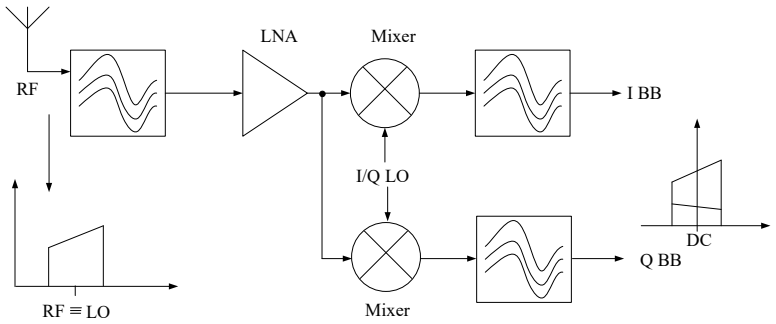


Figure 2.6: Quadrature receiver architecture

2.1.4 Direct conversion Receiver architecture

The aforementioned receiver architectures suffer from the image rejection problem. Figure 2.6 shows the block representation of the direct conversion receiver architecture. This architecture can also be referred to as the homodyne or zero-IF architecture. Thus, the image signal will have an amplitude comparable to that of the desired signal, which in turn relaxes the image rejection specifications. Therefore, this architecture is well suited for monolithic integration and maintaining a suitable reconfiguration. However, the direct conversion receiver still has some drawbacks, such as DC offset and 1/f noise, which in turn affects the NF of the receiver because a direct signal to baseband conversion occurs in this case. Additionally, the output can be possibly overloaded even with small DC offset values. Such a problem can't be resolved by frequent AC coupling. Even-order distortion is another major problem in direct conversion receiver architecture, as it generates signal-dependent DC offsets. Handling the dynamic offset desires a differential receiver architecture. Likewise, self-mixing is another challenging problem in direct conversion receiver architectures. Thus, good RF-LO port isolation is desired to overcome this problem.

2.1.5 Low-IF Receiver Architecture

Although direct-conversion receivers may overcome the image rejection problem, they suffer from DC offset, flicker noise, and self-mixing problems. Thus, another receiver architecture was proposed to overcome these problems. Figure 2.7 shows the block representation of the low IF

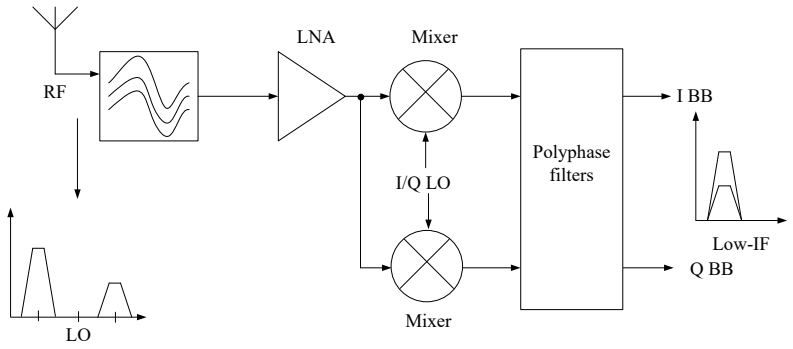


Figure 2.7: Low-IF receiver architecture

receivers, which resolved the problems faced by the direct conversion receiver but alleviated the image rejection problem. This, in turn, desires an active polyphase filter at the mixer output [22].

SDR receivers should accommodate multiple standards with a flexible architecture, with the consideration of single-chip integration, power consumption, and chip size. Conversely, from the area and IF selection perspectives, superheterodyne receivers are inconvenient because they desire image rejection filters, which are not suitable for monolithic integration. On the other hand, low-IF architectures can be useful in overcoming the image rejection problem. Likewise, the power consumption constraints can be overcome using direct conversion receiver architectures, but they suffer from DC offset and flicker noise problems. This will also impact the dynamic linear behaviour of the receiver. Thus, different techniques can be employed to overcome this problem, such as offset and intermodulation (IM) cancellation circuitry, current bleeding, and cross-coupling post-distortion approaches. Still, it degrades the receiver's performance in terms of other parameters. Another major problem with the direct downconversion receiver architecture is noise performance, which can be improved using the image rejection architecture [23, 24, 25]. Thus, different architectures can be used based on the desired specifications. For example, in [26], a direct conversion receiver has been proposed for the application in the G band. The proposed structure contains a cascaded single-stage distributed amplifier that consumes low DC, LO power, and attains reasonable NF and IIP3. Furthermore, the design covered a large bandwidth and a small chip area.

Conventional receivers first employ an LNA and then a mixer. With the rise in the frequency up to f_{max} of the technology, the frequency downconversion occurs as an upfront, resulting in a mixer first receiver structure [27, 28, 29, 30, 31, 32, 33]. It is challenging to design these receivers as they desire highly accurate active and passive components, resulting in complicated architectures. Likewise, LO chain realization is done using a VCO or frequency multipliers. Frequency multipliers are more effective than VCOs, particularly when a wide tuning range and low phase noise performance are expected [34]. Based on this idea, a receiver architecture is proposed as discussed in [35]. It has been reported that mixer-based reconfigurable receiver architectures can select or reject signals based on their properties while operating in various domains, such as frequency, spatial, or code domains.

The mixer-first acoustic filtering superheterodyne receiver is an alternative receiver architecture as reported in [33]. The architecture employs a highly tunable passive mixer-first frontend with high-selectivity acoustic filters while maintaining good tradeoffs among various performance parameters and frequency-tuning problems in acoustics. The architecture suffers from problems such as power handling issues, high NF, etc. Therefore, to overcome these problems, advanced receiver architectures are required that use advanced CMOS process technologies to improve power handling and minimize NF. For example, a quadrature RF-to-baseband-current-reuse receiver architecture can be adopted to overcome the power handling problem. The design not only attains high CG and IRR, but also maintains a small die area [36]. The proposed design suffers from poor NF. Thus, to further improve the NF, another receiver architecture was proposed in [37]. The receiver employed a novel capacitive stacking approach within the mixer, resulting in a high CG. Similarly, the architecture also employed a step-up transformer to improve IIP3 performance and reduce power consumption.

The following sections will focus on the most important building blocks of the receiver architecture, such as mixers.

Figure 2.8: Mixers conversion (a) Upconversion (b) Downconversion

2.2 Mixer Fundamentals

Mixers are one of the important components of transceiver circuits that are responsible for downconversion or upconversion processes. Figure 2.8 depicts these operations. During the mixing process, the output signal frequency is expressed in the form of a sum or difference of the input frequency signals [38, 39, 40, 41].

It is desirable to have LO input polarity switching to maintain low NF and high linearity. However, such mixers separate RF signals into in-phase and out-of-phase components. Moreover, the LO signal will be capable of selecting these signals alternatively. These mixers should ideally maintain low noise and high linearity [42, 41]. Furthermore, they should be unaffected by LO intermodulation products. Nevertheless, typical mixers will have drawbacks such as high NF, restricted CG, and poor linearity [43, 41].

2.3 Mixer Topologies

Figure 2.9 illustrates the classification of mixers into passive mixers and active mixers. Generally, passive mixers are responsible for introducing signal attenuation. Additionally, the mixing is accomplished with the help of passive switches. Furthermore, these mixers are quite popular as they are capable of consuming zero power while maintaining high IIP3 and good NF while degrading port isolation. Nevertheless, the major problem with passive mixers is the strict LO power requirements [38, 41].

Active mixers are commonly used because of their ability to maintain high performance in terms of CG, port isolation, NF, and low LO power requirements. Nevertheless, they struggle to

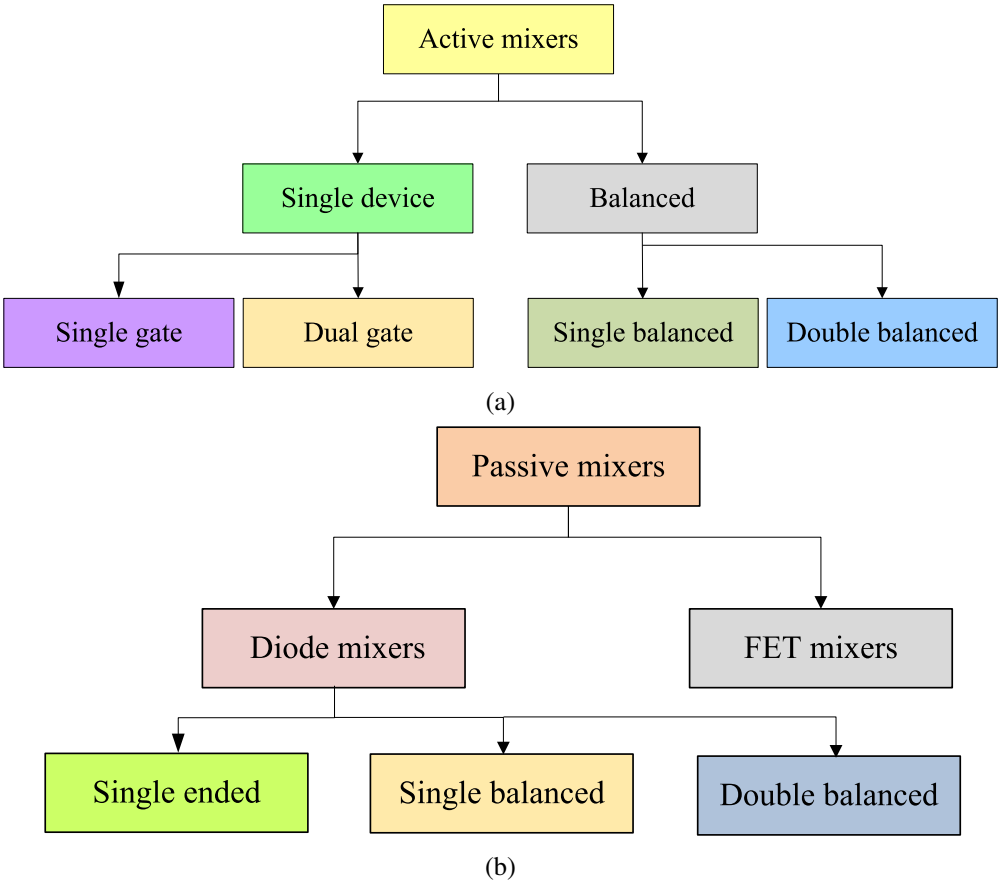


Figure 2.9: Mixers classification (a) Active mixers (b) Passive mixers

achieve high linearity and require additional circuitry.

2.3.1 Passive Mixers

Field-effect transistors (FETs) or non-linear diodes are used to implement a passive mixer[41].

2.3.1.1 Passive Diode Mixers

Passive diode mixers employ non-linear diodes and filters[41]. Figure 2.10 shows the classification of passive diode mixers.

Figure 2.10 (a) depicts a single-ended mixer that is easier to construct and is independent of the DC power supply. However, additional filtering elements are desirable to improve port isolation [38, 41].

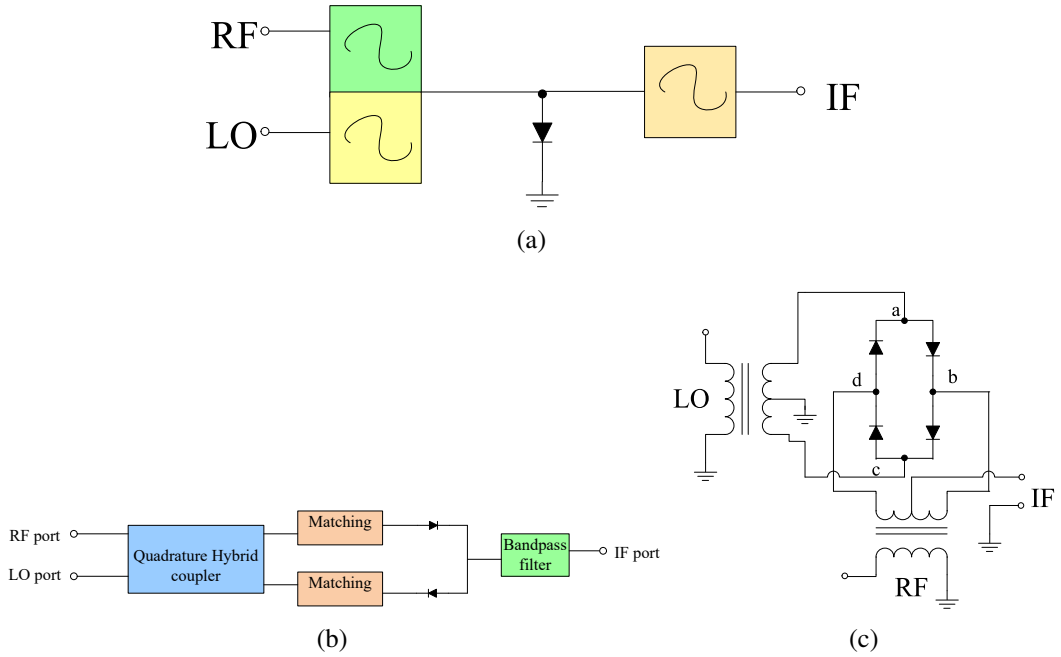


Figure 2.10: Passive mixers (a) Single ended mixer (b) Single balanced mixer (c) Double balanced mixer

Single-balanced mixers contain two devices, developed using single-device mixers coupled with 180-degree or 90-degree couplers. Matching networks are desirable within the circuitry if a 90-degree coupler is utilized, which in turn lowers the port isolation. The 180-degree couplers offer excellent port isolation, but poor matching. Figure 2.10 (b) depicts a single balanced mixer as discussed in [44, 41]. The structure employs a 90-degree hybrid coupler, Schottky diodes, and band-matching circuits. The LO input signal is shared between two Schottky diodes. Likewise, the Schottky diode divides the RF input signal equally with some phase difference. After the mixing operation, the obtained outputs are combined at the IF end. Therefore, bandpass filters select the desired frequency component at the output end. Balanced mixers show good port isolation compared to single-ended mixers at the expense of LO input power [41].

Figure 2.10 (c) depicts a double-balanced mixer that contains differential inputs and outputs. The LO signal's behaviour determines the switching operation of the mixer. The alternate pair of diodes gets turned on and off during this operation. Moreover, nodes 'a' and 'c' act as virtual ground for RF. Besides, the points 'b' and 'd' correspond to the balanced RF signal. Such mixers not only operate within a wide band, but also achieve good linearity at the expense of a high NF

[45, 41].

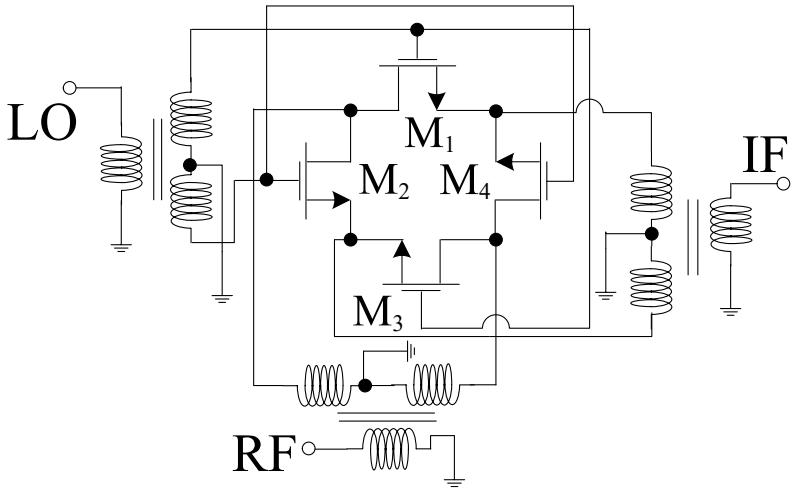


Figure 2.11: Passive FET quad mixer

2.3.1.2 Passive FET Mixers

Figure 2.11 shows the schematic of a passive FET mixer that employs FETs that act like switches. The drain source resistance within the passive mixer acts as a voltage-controlled resistor (VCR), where the channel resistance varies with the gate source voltage. During positive half-cycles, the alternate FETs get turned on and off. Thus, switched-on FETs link the IF balun's secondary winding to the RF balun. The reverse process occurs during the negative half-cycle [46, 41]. Passive FET mixers show high performance in terms of linearity compared to diode mixers with similar conversion gains. As a result, a comparative study of passive mixers is provided in Table 2.1 that assists in choosing the best mixer topology. As per Table 2.1, high linearity can be maintained within mixers while using a double-balanced passive diode mixer or a passive FET mixer topology. Similarly, single-ended mixers are commonly used due to their compact architecture, and double balanced passive mixers can be used for wideband operation [38, 41].

2.3.2 Active Mixers

Active mixers are classified into single-device active mixers, and balanced active mixers [41].

Table 2.1: Passive Mixers Comparison

Category	Passive diode mixers			
	Single ended mixer	Single balanced mixer	Double balanced mixer	Passive FET mixer
Benefits	High frequency band operation Simple High input linearity with low noise Low LO drive in case of integrated LO buffers	Poor response rejection and intermodulation products Good port isolation AM noise rejection in LO	Wideband operation High linearity, good NF Good port isolation Improved spurious products suppression	High linearity No flicker noise induction
Drawbacks	Low port isolation Poor 2nd-order distortion Off-chip diplexers are required for RF-IF port separation Injection filter for AM noise attenuation	high LO drive level requirement Well matched diodes for good NF	High LO drive level requirement Minimum two baluns are required Pad attenuators for bandwidth improvement Improper matching results in high CL	DC bias requirement for diode switching correction Discrete components based mixers require optimization for high performance

2.3.2.1 Single Device Active Mixers

Figure 2.12 shows the further classification of single device mixers into single-gate mixers and dual-gate mixers.

(a) A single-gate mixer uses a single transistor to impart RF and LO input signals via gates. Thus, diplexers are desirable for differentiating input signals [38, 41].

(b) Dual-gate mixers employ dual-gated transistors to pass RF and LO signals through distinct gate terminals, which results in excellent port isolation while maintaining high IIP3 [38, 41].

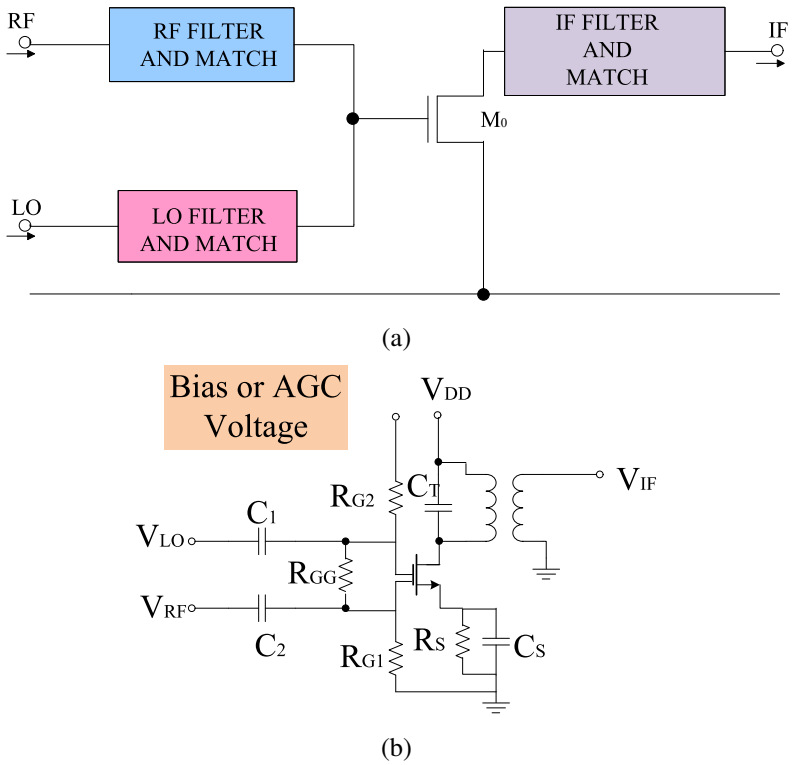


Figure 2.12: Single device active mixers (a) Single gated mixer (b) Dual gate mixer

2.3.2.2 Balanced Mixers

Balanced mixers are categorized into single, balanced, and double balanced (Gilbert) mixers [41].

Figure 2.13 (a) shows the single balanced mixer that contains single-ended RF and differential input LO signals, resulting in differential IF output signals. These mixers maintain high CG, NF, and port isolation performance. Additionally, they cover a small chip size while consuming low power when compared to double-balanced mixers [47, 41].

Figure 2.13 (b) shows the Gilbert mixer that adopts differential inputs and outputs. These mixers are developed by combining dual single balanced mixers that provide high IIP3, better port isolation, while maintaining good CG [38, 41]. RF stage transistors are responsible for RF input voltage to current conversion and further amplification. Likewise, LO transistors are responsible for the switching operation.

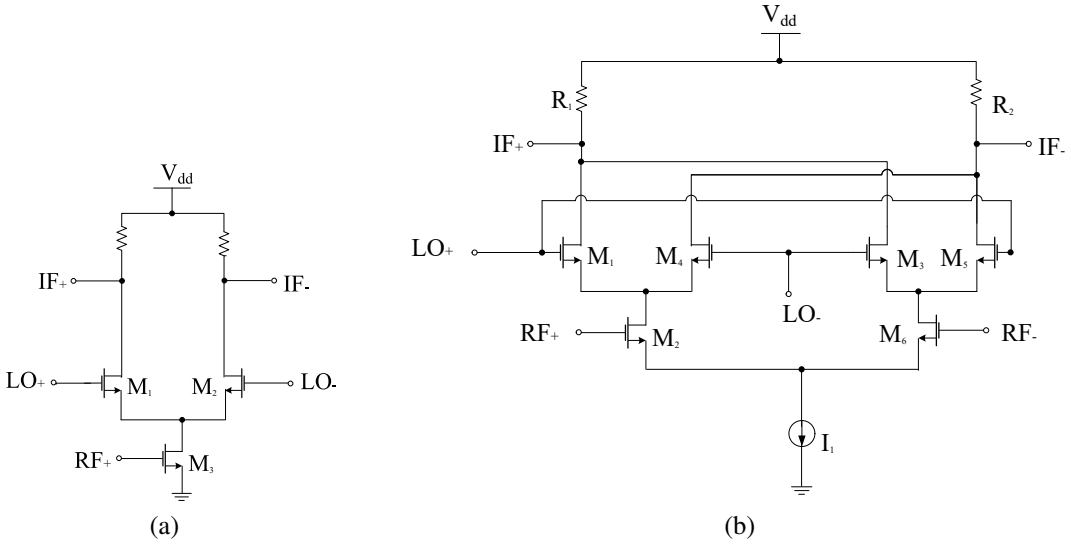


Figure 2.13: Active balanced mixers (a) single balanced mixer (b) double balanced mixer

2.4 Mixer Performance Metrics

Mixers are critical components of wireless communication systems, especially within superheterodyne receivers [48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 41]. As a result, performance metrics

must be carefully selected to evaluate the mixer performance. However, there exist trade-offs among different performance parameters. Based on the literature study, high CG mixers have been found to suffer from high NF problems, while high IIP3 mixers sacrifice CG and power consumption [47, 41].

Port isolation is another critical performance metric. To accomplish port isolation, mixer balance and hybrid junctions can be used. Therefore, it is necessary to maximize isolation to obtain the desired output signal [58, 41].

Image rejection is another vital aspect. This is because the undesired image signal may result in spurious output signals and may consume high power [59, 41].

Besides, for proper impedance matching, filters are required, which in turn avoids distortion on the receiver side [60, 41].

Mixer's performance can be determined using vector network analyzers (VNAs) with calibration advancements that also include scalar mixer calibration (SMC) and vector mixer calibration (VMC). The frequency offset produced by the mixer is important for SMC to occur. For measurement purposes, VNA provides RF/IF inputs for upconversion or downconversion at the output terminal. The variation in output frequency with the input frequency makes it desirable to set the output port in frequency offset mode. SMC utilizes Short-Open-Load-Thru (SOLT) calibration, for successful calibration at all desirable frequencies. For SOLT calibration measurements, it is important to enable the frequency offset mode to attain accurate results. However, this approach is time-consuming. Thus, disabling frequency offset modes can quickly generate results at the expense of interpolation, especially when actual measurements occur. Along with the mixer-under-test (MUT), VMC must include additional calibrated mixer and filter circuits. Additionally, VMC calibration is highly desirable for phase and group measurements [61, 41].

With recent technological advances, SDR mixers have evolved that are highly reconfigurable within the entire band of operation concurrently or discretely [62, 41]. Table 2.2 summarizes the important mixer specifications for various SDR applications. These mixers must have the ability to fulfill the desired specifications for all supported bands [63, 41] while maintaining a

Table 2.2: SDR reconfigurable mixer specifications

Parameters	Typical values
Conversion Gain	>10dB
Noise Figure	<5dB
Linearity	$\geq$ 0dBm
Reverse Isolation	<-30dB
Image Rejection ratio	>20dB
Return Loss	<-10dB
Area	<2mm^2
Bandwidth	>500MHz
Frequency Reconfiguration	Multiple bands

reasonable circuit area, power consumption compared to narrowband mixers.

2.5 SDR Design Techniques

Figure 2.14 depicts the classification of SDR mixers that are categorized into wideband and multiband mixers. Attenuating interfering signals is a difficult task for wideband mixers [64, 41]. Thus, multiband mixers are necessary for SDR applications. Several mixers can be used in parallel for multiband operations, each operating at different bands. Nevertheless, this process is not feasible, as per current industry requirements as they consume high power and cover a large chip area. As a result, it is preferable to have a single mixer that meets the desired specifications within frequency bands without degrading overall performance [41].

2.5.1 Wideband Mixers

The wideband mixer maintains a flat gain response and requires tuning circuits for good frequency reconfiguration throughout a wideband. Some of the most widely used wideband mixer topologies include cross-coupled common gate [65, 41], inductive peaking [66, 67, 68, 41], bulk cross-coupling and current bleeding [69, 41] and current reuse with current mirror approach [70, 41].

Figure 2.15 shows a Gilbert mixer with a cross-coupled common gate transconductance stage.

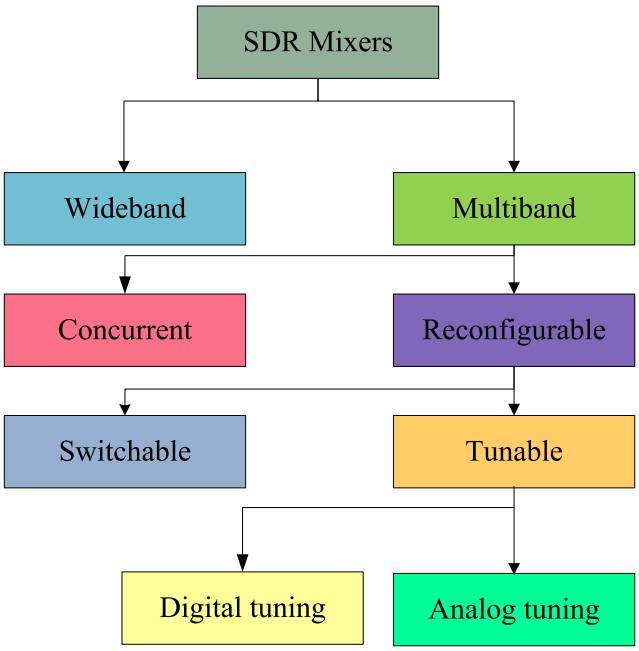


Figure 2.14: Classification of SDR Mixers

The proposed design maintains a flat CG and offers high impedance matching while consuming low power. Unfortunately, it suffers from high NF and low IIP3. To overcome these issues, it is necessary to use an inductive peaking technique, responsible for balancing the CG at higher frequencies while improving the bandwidth [66, 71, 41]. Likewise, in [68, 41], an inductive peaking topology-based mixer has been proposed to provide wideband impedance matching as shown in Figure 2.16. The inductors are present at the transconductance stage to resonate with the parasitic capacitors, resulting in a flat CG. Additionally, the load stage contains significant resistance and transistors, acting as diode loads to maintain the virtual AC ground at the transistor gate terminals, resulting in high voltage headroom. Furthermore, a resistive double balanced structure is shown in Figure 2.17 to maintain a high IIP3 and good CG [67, 41]. The design proposed novel on-chip baluns to satisfy circuit conversion requirements. Additionally, the design employed inductors for input matching purposes. Similarly, optimal gate and source inductive feedback techniques are expected to be utilized to maintain high gain within a wideband.

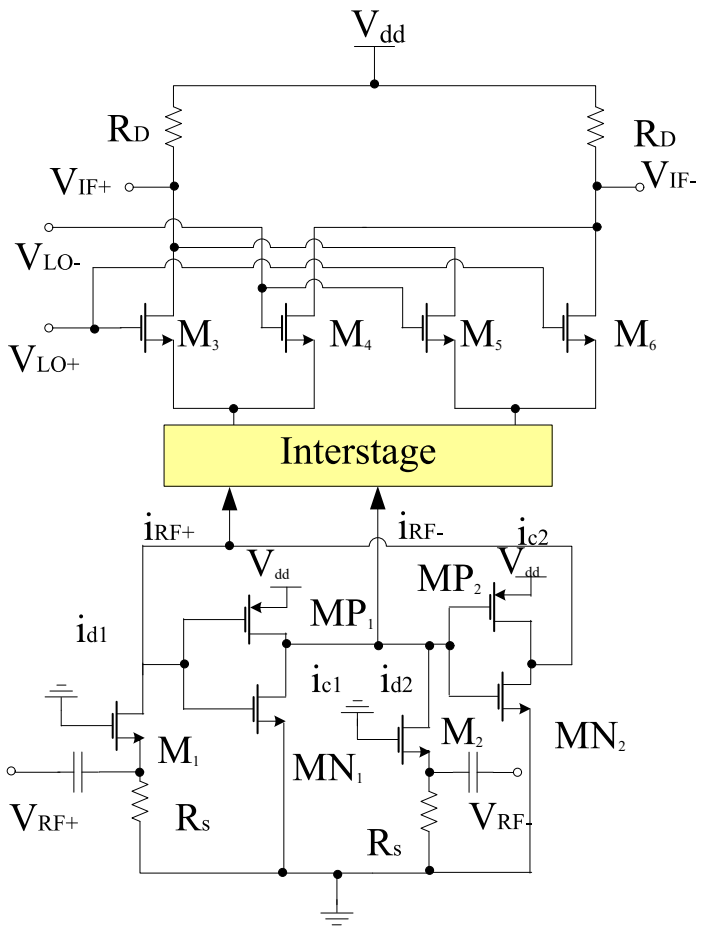


Figure 2.15: Cross-coupled mixer

2.5.1.1 Active Wideband Mixers

Gilbert mixer maintains a high CG and good port isolation [72, 73, 74, 75, 76, 77, 41]. Based on this, Adiseno et al. proposed a Gilbert mixer that achieves a flat CG at the expense of high NF and low IIP3 [78, 41]. Thus, to maintain high CG and high IIP3, the best known solution is to employ a resistive topology. The proposed technique is well suited for direct receiver architectures [79, 41]. Alternatively, derivative superposition and noise cancellation approaches can be used for mixer circuitry [80, 41]. Furthermore, the design employed auxiliary transistors to maintain high-linearity enhancement within the circuitry. Likewise, a multi-gated transistor (MGTR) topology has been employed within the design for thermal noise cancellation within the input transistors. The proposed design maintains high CG, good IIP3, and low NF [41]. Active mixers maintain an excellent trade-off between CG and NF. In practice, current reuse

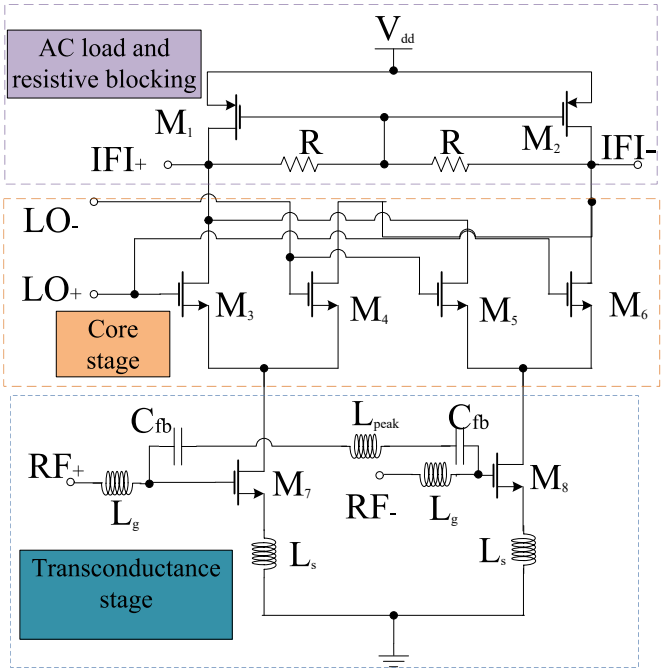


Figure 2.16: Wideband mixer

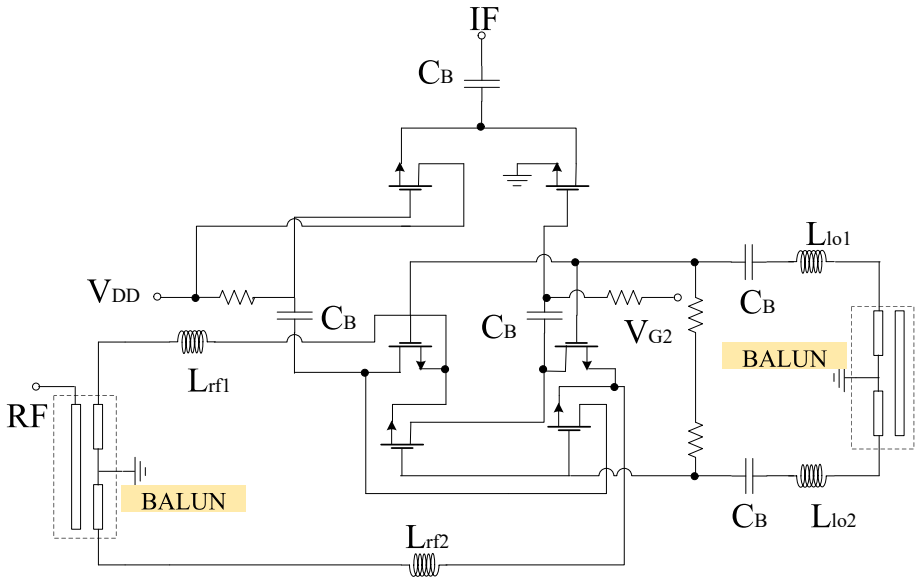


Figure 2.17: Wideband CMOS mixer

and current mirror techniques have been employed by Ma et al. within mixer circuitry, resulting in high performance in terms of CG, IIP2 with degraded NF [70, 41]. Likewise, in [81, 41], Gladson et al. proposed an improved Gilbert mixer that employs the current bleeding approach, as shown in Figure 2.18. The proposed design also considered the body effect of the transistors

present within the circuitry. This resulted in high IIP3, low NF at the expense of CG. The design also covered a small design area while consuming less power. This makes it suitable for various 5G applications.

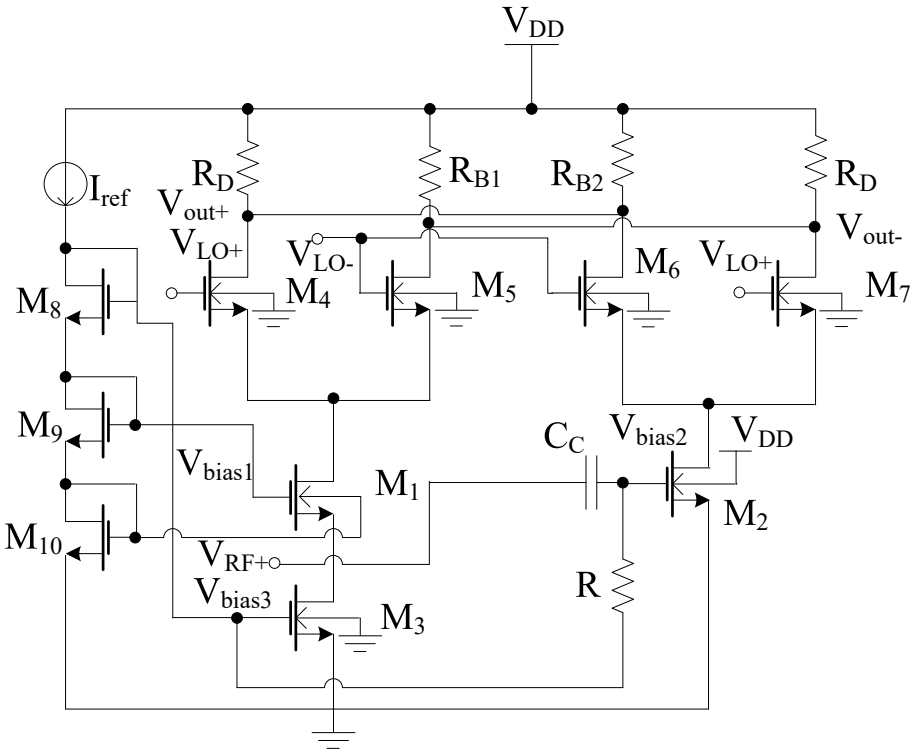


Figure 2.18: RF current bleeding mixer

To further improve performance within the downconversion mixer, the MGTR technique can be utilized as shown in Figure 2.19. The proposed design improved not only IIP3 but also CG while occupying a small chip area [82, 41].

Additionally, it is challenging to maintain large bandwidth and high CG. Thus, the most ideal solution is to employ the Blixer circuitry proposed by Blaakmeer et al. in [83, 41]. The circuitry combines LNA, Balun, and I/Q mixer. The proposed design is not only compact but also consumes low power.

2.5.1.2 Passive Wideband Mixers

Passive mixers are well known for providing low-voltage operation due to their ability to provide high IIP3 [84, 85, 86, 87, 41]. A noise-cancelling receiver with an 8-phase passive mixer was

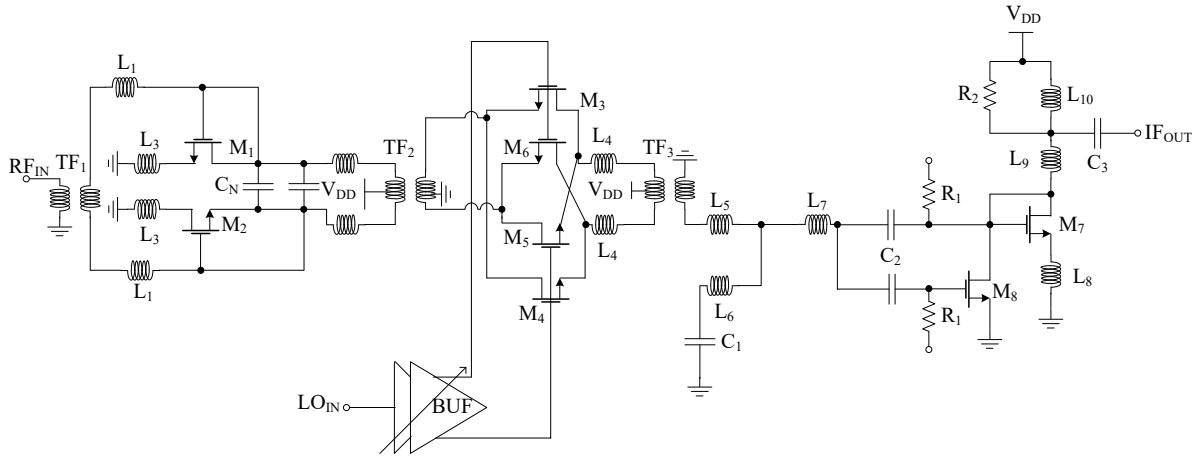


Figure 2.19: High linearity downconversion mixer

proposed in [88]. Thus, by jointly employing passive mixers and high-gain baseband operational amplifiers, it became possible to suppress the voltage swing prior to any baseband filtering. Furthermore, the fixed transimpedance amplifier output helps to obtain the desired I / Q signal components and cancel the undesired signal components [41].

2.5.1.3 Dual Topology Mixer

Active mixers maintain high CG, whereas passive mixers can obtain high IIP3. Therefore, to maintain high CG and IIP3, it is expected to develop mixers with features of active and passive mixer topologies in a single design [89, 41]. Based on this idea, a mixer is proposed that contains an active transconductance stage and a passive LO stage that employ the current mirror technique [70, 41] and maintains good performance.

Dual topology SDR mixers require a compact topology that maintains high performance within a wideband without consuming high power. Existing mixer designs that employ on-chip inductors cover a large chip area, maintain a low-quality factor, and are highly susceptible to electromagnetic interference, making them unsuitable for SDR applications. Likewise, for SDR mixers to operate within a wide band, it is necessary to take care of the parasitic capacitances associated with CMOS transistors, when the proposed architectures are highly complicated. Although it is possible to tune the parasitic capacitances with on-chip inductors, off-chip

inductors are preferable as they cover a low chip area and maintain good performance [90, 41].

2.5.2 Multiband Mixers

Multiband mixers can simultaneously support various bands while using continuous or discrete tuning approaches [91, 41]. In general, they can be classified as concurrent mixers and reconfigurable mixers.

2.5.2.1 Concurrent Mixers

Concurrent mixers operate on various frequency bands in a concurrent manner. Nevertheless, to develop miniaturized and low-cost designs, it is expected to pay attention to the power consumption, as mixers and LNAs are the primary sources of power consumption within the receiver circuit. Thus, a single mixer operating at multiple bands will be suitable, as design complexity is another significant concern [92, 93, 41]. Likewise, novel mixers were proposed in [93] that operate within dual bands, and capacitive tuning plays a vital role within the circuitry, especially for multi-band operation. Additionally, the design obtained a high image rejection ratio (IRR). The mixer switching is an alternative approach, as discussed in [94, 41], useful for dual-band concurrent operation. Based on this idea, in [95], Abdelrheem et al. proposed a mixer that employed a dual-band impedance matching network for concurrent narrow-band matching. The design also employed a resistive degeneration approach for overall performance improvement, resulting in a compact mixer design. Figure 2.20 shows the Q_1, Q_2 transistors forming an RF stage and Q_3–Q_6 transistors represent the core stage. Additionally, Figure 2.21 (a) depicts the return loss performance of the design, which is reasonable within the entire band and maintained a high CG within the dual bands. Based on the design, it was found that the transconductance is large for frequencies smaller than the unity gain frequency f_T. Thus, it becomes easier for a mixer to operate at multiple frequencies [95, 41].

The design area is critical when proposing any mixer design. Using on-chip filters instead of off-chip filters is crucial for developing high-performance, cost-effective mixers. In [96], a mixer was proposed that not only employed on-chip baluns but also LC series-parallel resonators; the

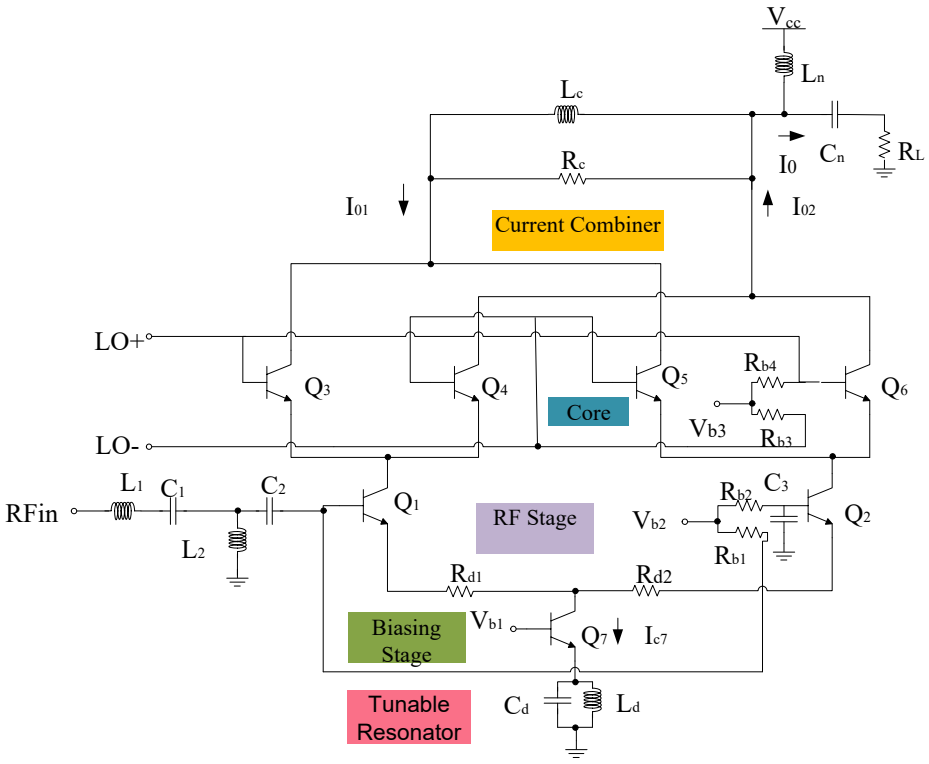
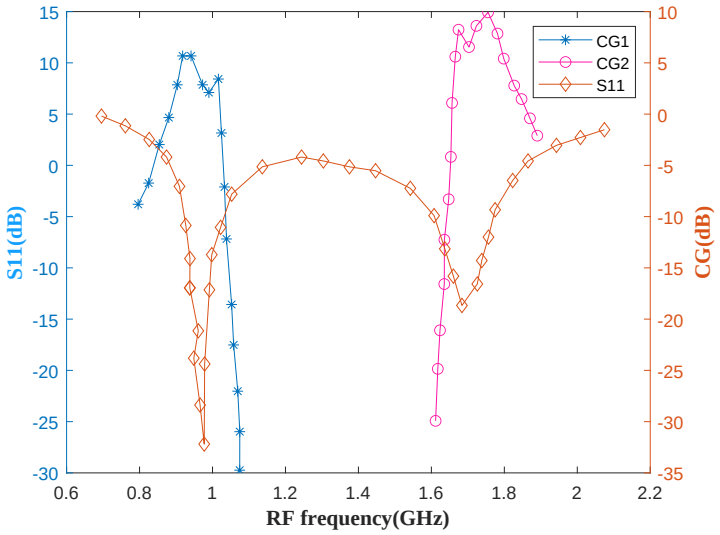


Figure 2.20: Dual-band Mixer

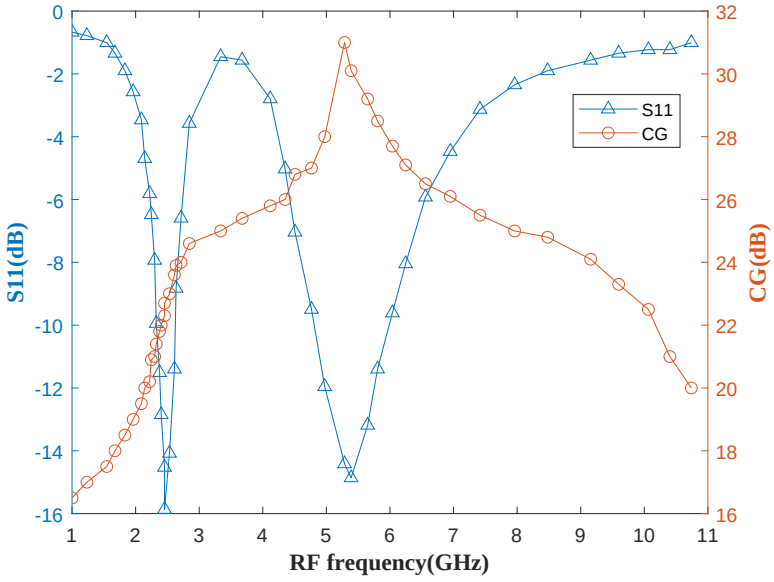
prominent role of the resonator is to maintain dual-band operation. Additionally, the proposed mixer consumed low power with degraded CG and NF [41]. Furthermore, in [10], a novel concurrent dual-band receiver was proposed. The proposed design adopted current reuse and a common gate stage with component stacking approaches, resulting in a high CG, low NF, and low power consumption. Figure 2.22 depicts the receiver architecture that proposed a novel parallel-series combination matching network to show the concurrent matching within the structure. The proposed design maintained a good return loss and CG within the dual bands, as shown in Figure 2.21 (b).

2.5.2.2 Reconfigurable Mixers

High-performance reconfigurable mixers must be developed to support multiple bands. One of the best solutions is to integrate various mixers in parallel, each operating within a different band. However, they are only feasible for low-frequency band operations. This gave rise to switchable mixers and tunable mixers [41].



(a)



(b)

Figure 2.21: (a) Performance plots for dual-band mixer (b) Performance plots for concurrent dual-band receiver

2.5.2.2.1 Switchable Mixers

Switchable mixers use switches to maintain good reconfiguration within various bands. The discrete switch helps to maintain good reconfiguration using toggling operation, resulting in high return loss within the desirable bands. Gilbert topology-based switchable mixer is shown

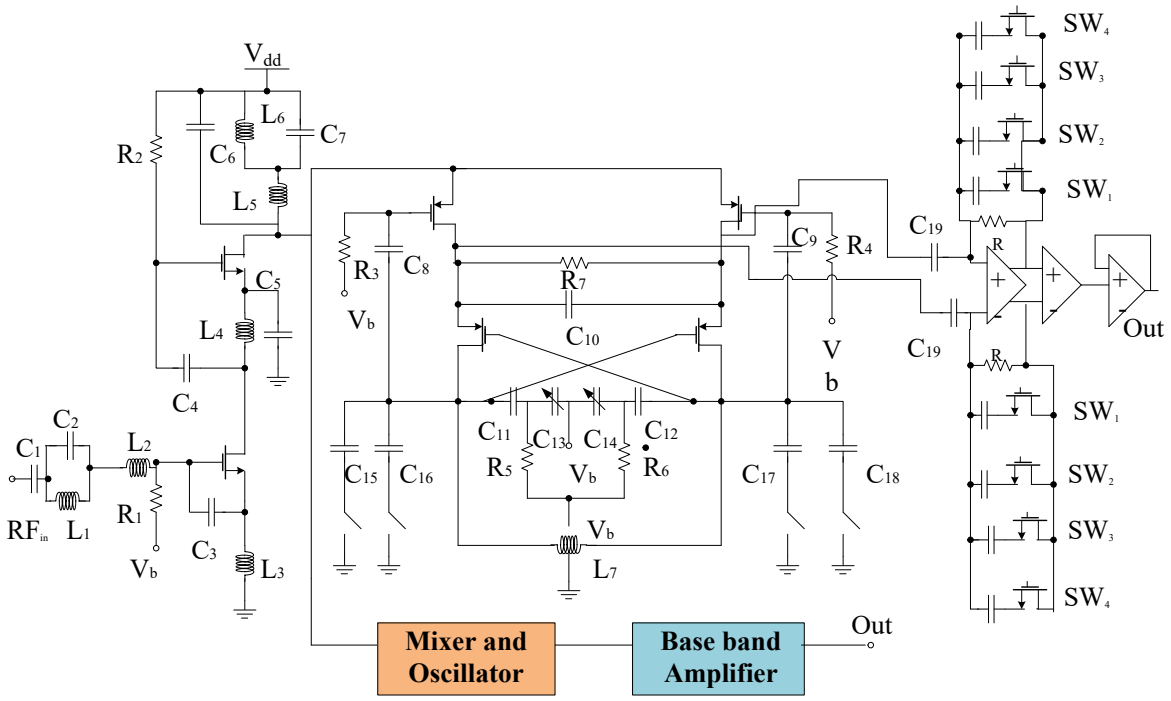


Figure 2.22: Concurrent dual-band receiver

in Figure 2.23. The parasitic capacitor within the switching stage has a considerable impact on the dynamic range that is tuned with a variety of inductors. Additionally, the switches present within the circuitry are responsible for switching operation. The proposed design achieved high performance in terms of CG, NF, and IIP3 while consuming a large chip size [41]. Similarly, in [97, 41], a current-driven passive mixer was proposed to use a switchable transconductance array (TCA) to maintain reasonable flicker noise and IIP3. Additionally, the buffer section utilizes the Tow-Thomas transimpedance biquad amplifier (TIA) that acts as a filter to maintain high gain while operating within a wideband. The mixer design shown in Figure 2.24 makes use of the passive mixer topology that maintains high linearity and low flicker noise. Additionally, the design also employed a DAC for DC offset calibration purposes.

2.5.2.2.2 Tunable Mixers

Tunable mixers can continuously or discretely tune at different frequencies within the entire band of operation. Generally, digitally tunable SDR receivers utilize multiband mixers for broadband frequency operation [98, 41]. Based on this idea, a digital receiver architecture was proposed in

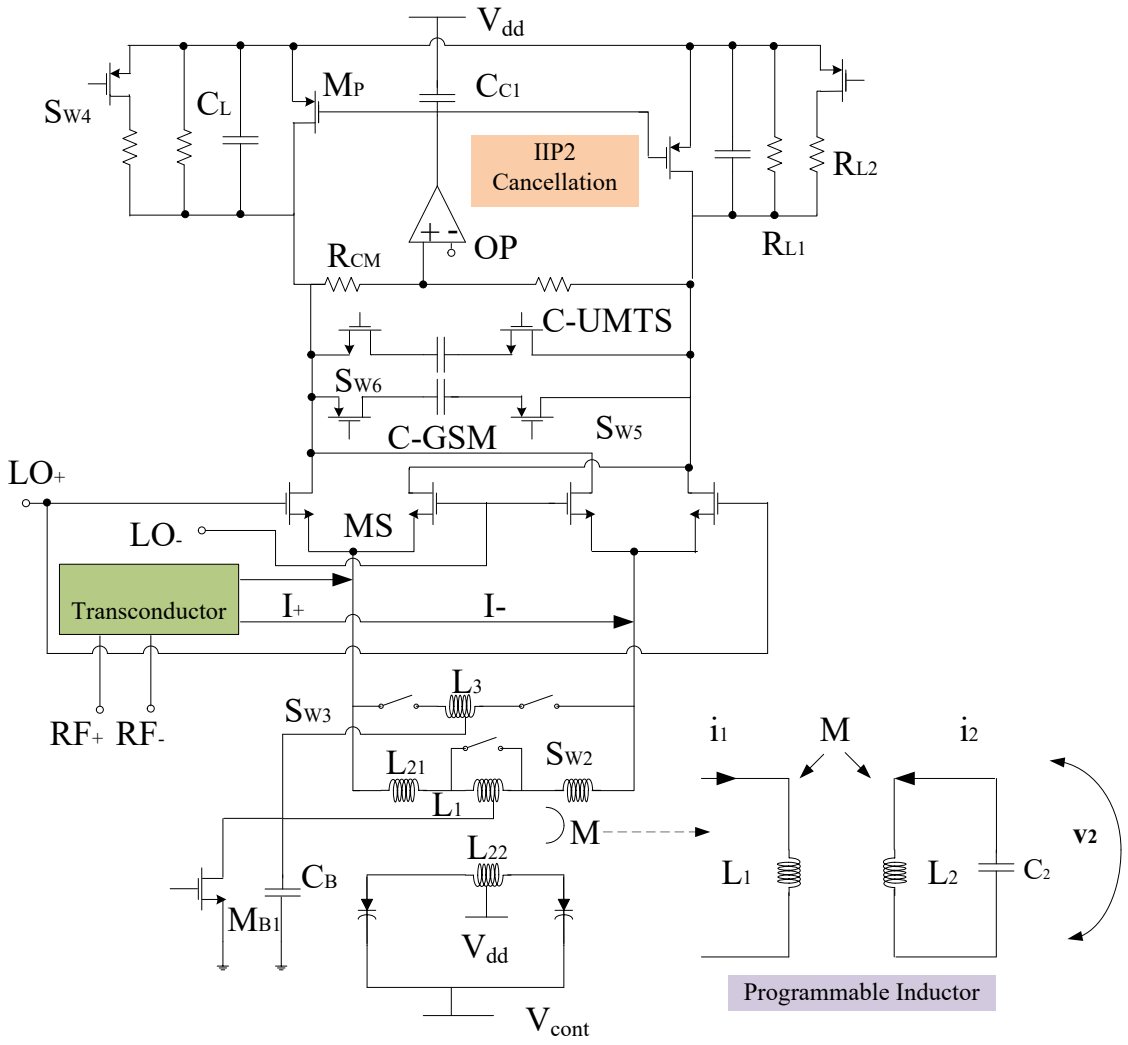


Figure 2.23: Reconfigurable mixer

[99] to satisfy the ADC sampling and perform an FPGA-based digital down-conversion process. Likewise, in [100, 41], the main focus was on frequency tuning algorithms that utilized a platform containing USRP and RFX2400 daughterboards for lossless signal processing [101, 102, 41]. Besides, SDR receivers desire reconfigurable RF frontends for operating within a wideband. Therefore, during the selective filtering process, SNR degradation is possible due to the amplification of out-of-band blockers and interference. Some of the SDR architectures discussed in the literature depend on the voltage-mode passive mixer, especially for suppressing out-of-band blockers. Similarly, to suppress harmonic interference, the harmonic rejection mixer is the best solution [41].

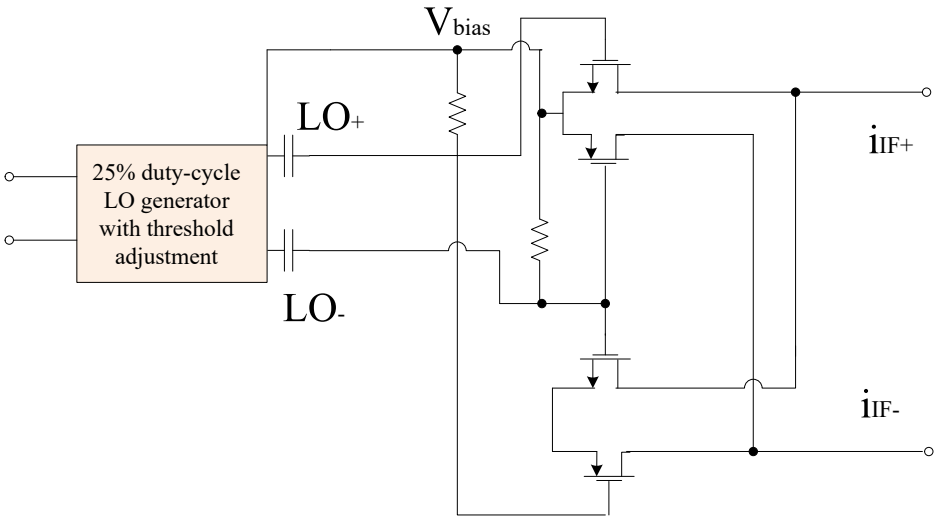


Figure 2.24: The current-driven passive mixer

Various techniques have been discussed in the literature that show high harmonic rejection ratio (HRR) performance while sacrificing CG and phase mismatch. The harmonic rejection approach is one of them that consumes high power due to its complex circuitry and large die area [103, 41]. Thus, a mixer circuit proposed in [104, 41], is useful for maintaining good IRR and other performance parameters, which employ low IF SDR architecture. It uses digital calibration for the desired band. Additionally, the design operates in three modes. Starting with the current-mode mixer, which is responsible for maintaining low NF. Likewise, a voltage passive mixer is employed for high-linearity performance that is responsible for rejecting out-of-band interference. Finally, the harmonic rejection passage was accountable for the vector gain calibration. Nevertheless, the design shows degraded performance [104, 41]. Thus, it is expected to use continuous tuning instead of discrete tuning, as it is less affected by process variations.

2.5.2.3 Active Multiband Mixers

Several active multiband mixers have been reported in the literature that maintain high performance. For example, in [105, 41], different mixers were discussed that utilized current bleeding and charge injection approaches [105, 41]. Nevertheless, the proposed structures were not efficient and suffered from poor CG [89, 41]. Similarly, in [52, 41], the mixer was presented

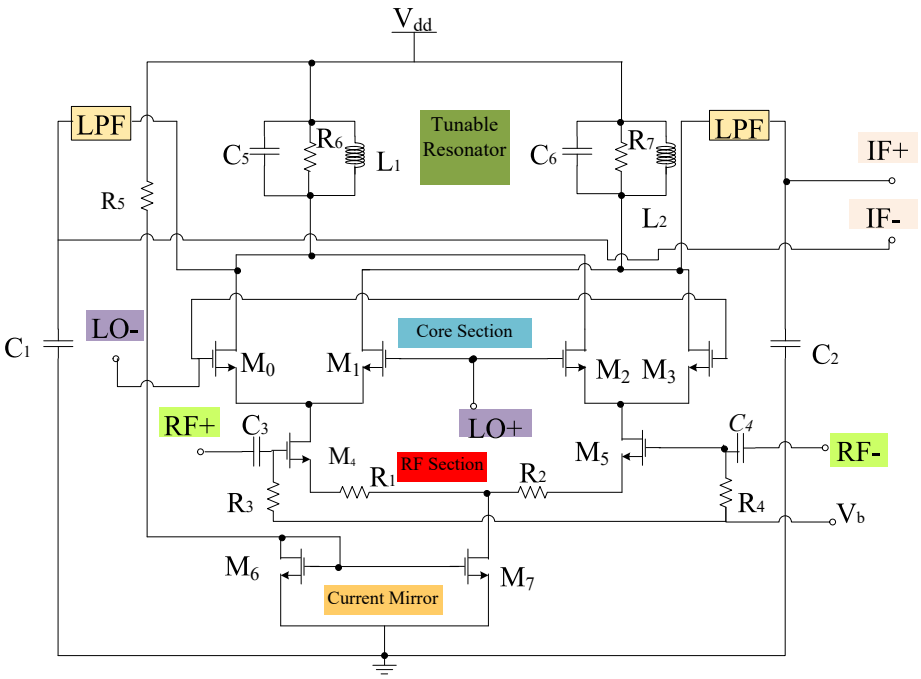


Figure 2.25: Tunable Gilbert Mixer

that employed a Tow-Thomas topology that acts as a filter, resulting in high CG, low NF, and high IIP3. Furthermore, Chen et al. adopted current reused G_m stage, source degeneration, and multi-gated transistor approaches in mixer circuitry [84, 41]. The proposed design achieved high IIP3 by sacrificing other parameters such as CG and NF. Similarly, in [106, 41], a mixer was proposed with an improved complimented common gate pair as the RF stage, a transformer for chip area reduction and PMOS with inductive peaking. This resulted in improved NF, CG and bandwidth performance with degraded IIP3. Additionally, RLC tunable resonators as mentioned in [107, 41] are useful for maintaining high performance, as shown in Figure 2.25. The resonance frequency of the tunable resonator is expressed as

$$f_r = 1/(2\pi\sqrt{LC}) \tag{2.1}$$

As can be seen from Figure 2.26, the design achieved low NF and good CG.

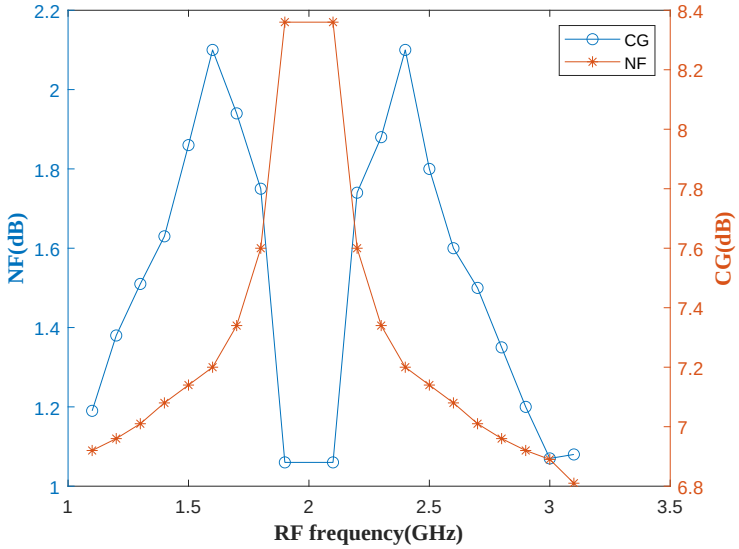


Figure 2.26: Performance plots for tunable mixer

2.5.2.4 Passive Multiband Mixers

In [108, 41], it has been discussed that power amplifier (PAs) based passive mixers are responsible for maintaining low NF. The proposed design showed high reconfigurability at the expense of power consumption. Likewise, a transceiver was proposed in [109, 41], which contained a passive mixer. The design achieved low phase noise and high port isolation compared to the existing similar works. Additionally, the design covers a small chip size and maintains a good CG.

It is well known that both inductor-based and inductorless designs can cover a large chip area depending on the design specifications. A passive multiband inductorless I/Q mixer was proposed in [110, 41], employing an operational amplifier-based output section with a passive core stage [110, 41]. The overall performance showed that the design attained high CG, high IIP3 and good NF at the expense of the chip area.

2.5.2.5 Dual-mode Multiband Mixers

Passive mixers attain high linearity while consuming low power. However, some of the significant drawbacks of these mixers are high conversion loss and considerable LO power. Meanwhile,

active mixers are well known to maintain improved CG while sacrificing linearity and NF [111]. In [112, 41], a dual-mode mixer was proposed that employed an active balun with a ring mixer to alternate switching between different modes. As per the design, there is a possibility to control the conversion gain by varying the control voltage. The active balun was developed using a DC-coupled differential pair to eliminate off-chip IF balun. The design operates in dual CG modes while maintaining good trade-offs with IIP3 in both modes.

2.6 Impedance Matching Techniques

Traditional mixers utilize off-chip surface mount components for more accessible employment of various impedance matching techniques, such as stubs or quarter-wave transformers. In addition to this, it is possible to characterize before implementation. Furthermore, off-chip components achieve higher quality factors compared to on-chip components. Nonetheless, they are uncommon due to their difficult integration approach to the circuits. Advanced integrated circuit technologies allow designers to utilize on-chip components. Unfortunately, due to their limited size and band of operation, they are not commonly used [113, 41].

Lumped element, transformer-based, or microstrip line matching are commonly used impedance matching techniques that utilize on-chip components. The performance of these techniques may vary with different applications [52, 114, 115, 116, 117, 118, 119, 120, 41].

2.6.1 Lumped Elements Matching

Lumped element matching is a commonly used technique among various multiband mixers designed for SDRs. The electrostatic technique is responsible for the frequency tuning that can occur when the resonator capacitance employing electrostatic, piezoelectric, or thermal micro-actuators are varied [121, 41]. In [96], a matching network was proposed for a mixer design operating within a wideband to compensate for the parasitic capacitance effects at the receiving end. The design also employed a peaking inductor for the low-band mixing stage for extending the IF port 3-dB bandwidth. The discussed approach maintained good matching within 6-18GHz

bands of operation. Similarly, a work was discussed in [122, 41] that shows concurrent matching at 2.45GHz and 5.25GHz, using a parallel network to resonate with the desired frequencies. The concurrent multi-band gain and high image rejection ratio can be achieved only when the drain load network has excellent impedance at both concurrent frequencies. This can be achieved by a combination of series and parallel LC tank networks. In [123, 41], a tunable differential active inductor tuned with parasitic capacitance was proposed for a mixer. In addition to this, the differential inductor design employed a variable feedback resistor, which shows the reconfiguration behaviour within the mixer.

2.6.2 Transformer Based Matching

Transformer matching is another commonly used technique in multi-band front-ends, of which multi-tap transformers are the most effective solution. The design showed good flexibility, but the quality factor was degraded [124, 41]. In [125], a transformer was employed at the output end for signal conversion and wideband matching purposes. The coupling capacitors were also employed within the design for amplitude and phase matching purposes. Similarly, in [126, 41], the proposed design utilized an on-chip resonating transformer to maintain a high current gain. The proposed design covered a small die size and maintained better port isolation. In addition to this, in [127, 41], a single balanced transformer-based mixer topology is discussed that achieves high port isolation while covering a small die size.

2.6.3 Microstrip Line Matching

Microstrip line-based matching is one of the excellent approaches used for reconfigurable multiband mixers. Based on this approach, in [128, 41], T-shaped transmission lines and Marchand balun were employed to improve the overall bandwidth of the design. The proposed structure maintained reasonable chip size and excellent port isolation. Similarly, in [129, 41], a thin film microstrip line was employed for matching purposes. In addition to this, the design also maintained high port isolation. Another work proposed in [130, 41], utilized π-shaped

series transmission line-based networks in both transconductance and core stages of the mixer circuitry while operating within a wideband.

2.7 Comparative Study

Table 2.3 summarizes various SDR based mixers. Each mixer topology shows a wideband operation. From Table 2.3, it has been found that various circuits have been developed and tested within 180 nm CMOS technology. Switching played an important role in maintaining excellent performance within circuitry [131, 132, 41] and multi-gated transistor techniques [133, 41]. In Table 2.3, the minimum NF is around 1.5 dB and the highest IIP3 mixer attained is 12.5 dBm. From the literature study, it has been noticed that the reconfigurable mixers attain higher linearity than the concurrent mixers. The overall power dissipation increases with increasing CG, but at the expense of IIP3. Additionally, the overall mixer design area is determined by the complexity of the design.

2.8 Design Challenges and Techniques

Multiband mixers are complicated, bulky, and necessitates several passive components. This in turn consumes high power and covers a large chip area [146, 49, 41]. Thus, it is necessary to have a proper mixer design to obtain the performance parameters effectively [159, 146, 136, 41]. As a result, various approaches have been discussed in existing works taking into account the reconfigurability and wideband tuning of mixers [160, 41]. This section describes various problems encountered while developing mixer circuits, as well as the approaches that can be used to overcome these problems.

2.8.1 Image Rejection

When the wanted and undesirable signals traverse at the same instant at the input port, it degrades the overall performance of the mixer circuit. It is critical to discard these undesirable signals. In

Table 2.3: Comparison Summary

Ref	Freq(GHz)	Category	Results				
			CG/CL(dB)	NF(dB)	IIP3(dBm)	Area(mm^2)	P_{diss}(mW)
[134]	57-66	Wideband	>5.6	<10.91	>12.4	0.22	18
[50]	5-6	Wideband	9	11	2	0.8	4.2
[135]	0.5-6.5	Wideband	10	13	9.5	0.015	4.5
[136]	1-6	Wideband	10-13	12-18	-4.5	Nil	Nil
[137]	3.1-10.6	Wideband	12	4-5.7	-14	0.928	4.6
[138]	0.7-2.3	Wideband	21	10.6	9	0.19	9.9
[139]	20-32	Wideband	3	10.5-13	>0.5	0.19	18
[133]	0.045-2.5	Wideband	5.8-8.6	7.4-9.1	0.6-7.2	0.093	16.38
[140]	91-95	Wideband	7.5-9.2	Nil	Nil	2.72	Nil
[141]	57-66	Wideband	-2.7-5.4	Nil	-14.75	0.4	1.4
[142]	57-67	Wideband	6.95	14.4	>-9.4	0.35	16
[143]	0.1-40	Wideband	16	3.8	-9	1.89	415
[144]	16-53	Wideband	-0.5±2	Nil	19-21	0.34	5.9
[70]	0.01-2	Reconfigurable	17.5	11.1	-0.9	0.071	4.6
[64]	0.15-1	Reconfigurable	48	3.2	-7	0.72	64
[145]	57-64	Reconfigurable	23	9	Nil	Nil	319
[132]	4-10	Reconfigurable	15.5-17.5,13.5	4-5.2	12.5	Nil	8.3
[146]	0.401-0.457	Reconfigurable	29-31	<5.2	>-19.5	0.6	0.37
[147]	54-64	Reconfigurable	16.21.5	11.2	-5-0	0.67/0.06	5.25-4.25
[148]	1.4-3.6	Reconfigurable	12.3	16.9	4.8	4.6	Nil
[149]	1.5-4.5	Reconfigurable	12-16.4	8.2-12	-11	0.919	0.28
[150]	0.1-5	Reconfigurable	68-84	2.3-6.5	-3-10	2	59-115
[151]	0.1-2.4	Reconfigurable	40-70	-4+/-1	Nil	2.5	37-70
[152]	2-3	Reconfigurable	33	11	-16	0.1	2.5
[131]	1-2	Reconfigurable	29.4-92.6,15.8-20.1	4.9,14.8	0.9	Nil	46.4,67.3
[153]	0.6-5/0.1-0.6	Reconfigurable	35.4/27	9/12.6	-7.1/5.5	12.48/6.3	0.49
[154]	3-11	Reconfigurable	8.8-17.1	12.8-16.5	-10-0	0.77	3.45
[96]	6-18	Concurrent	31	12	-11	Nil	137.6
[155]	0.3-1.4	Concurrent	42	2.5-3.9	Nil	0.48	Nil
[78]	0.8-1,1.8-2	Concurrent	19.3-20,19.2-20.2	1.85-1.95,1.55-1.85	-3,-4.5	Nil	67.5
[156]	2.3,5.2	Concurrent	15.6,11.3	12.1,16	-6.7,-1.1	Nil	7.52
[157]	3.1-4.8,6.3-7.9	Concurrent	12.5–16.5,14.5–16	7.5-12.5	-4.1,-5.2	1.02	75.6
[158]	2.4/5.2	Concurrent	11.2/11.6	4.6/4.3	6.7/5.5	0.52	8.4

recent research, it has been found that RF sampling can be an alternative to downconverter, with a special focus on discrete architecture instead of continuous architecture [41]. However, samplers affect the performance of the wideband SDRs. In [161, 41], the charge sampling technique demonstrates the inverse conversion gain and frequency relations. Thus, voltage samplers can be used to overcome this problem, resulting in wideband noise folding that necessitates prefiltering in both cases. Unfortunately, it is difficult to implement this technique and is also responsible for increasing the overall cost of the receiver. This in turn increases the complexity of the overall design [162, 41]. As a result, the optimal approach is to develop a compact and reliable rejection mixer while maintaining the high performance of the circuitry [163, 164, 165, 166, 41]. Based on this idea, an image rejection mixer was proposed that employed a balanced mixer and orthogonal bridge [164, 41]. The proposed design obtained a high image rejection ratio at the

expense of conversion loss.

2.8.2 Conversion Gain-Linearity Balance

Advanced architectures are designed using various CMOS processes due to their potential to maintain cost-effective and low power within circuits [167, 41]. Unfortunately, since CMOS-based transistors show poor transconductance, the CG gets automatically degraded, which necessitates additional amplifiers [159, 41]. Additionally, cascode current bleeding and g_m-boosting techniques can be used to enhance the overall CG performance. These techniques guarantee a low chip area design at the expense of IIP3 [159, 168, 169, 41], which depicts the good gain and linearity trade-off. Another mixer design was proposed by Na et al., employing a current mirror approach. The proposed design achieved low NF, high CG with degraded IIP3 [170, 41].

2.8.3 Power Consumption

The advancements in mobile gadgets have experienced a high circuit integration capability. This would not have been possible without any downscaling, which in turn improves the overall performance. The latest research is centered on SoCs that make use of CMOS technology. However, this technology has issues in maintaining low power consumption while fulfilling the recent trends of SDRs for contemporary wireless communications [171, 41]. CMOS wideband mixers are commonly developed architectures that consume low power [172, 173, 41]. However, it degrades other performance metrics [152, 174, 85, 168, 41]. In addition to this, cross-coupled PMOS transistors, inductive peaking, and current bleeding approaches can be alternatively used to maintain high CG, low power utilization with degraded linearity [175, 41]. Cascode common source is another effective approach while consuming low power [176, 41]. Designers proposed various other structures that guarantee less power consumption with degraded performance [174, 176, 168, 90, 177, 85, 178, 41].

2.8.4 Noise Performance

Various techniques can be found in the literature that focus on providing low NF for mixer circuits. The best approach is to utilize filters. In [107, 41], a wideband tunable Gilbert mixer was discussed. The proposed mixer achieved a moderate NF while covering a large chip size. Similarly, in [62, 41], a dynamic current injection mixer was proposed to maintain moderate NF. Likewise, Gladson et al. discussed a mixer that operates in dual modes, i.e., high gain and high linearity, while showing CG and IIP3 in alternate modes [90, 41]. Thus, it has been found that the individual structure is ineffective in operating simultaneously within both modes.

2.9 Summary

This chapter discusses some of the important receiver architectures and the challenges faced by different architectures. This helps to select the best architecture based on the specifications. Upon selecting the receiver architecture, the next task is to develop the front-ends. This thesis focuses mainly on mixer design. Thus, based on the study, it has been found that different techniques can be used to design multiband mixers for SDRs. Current bleeding [159, 179, 180, 181], active balun [112], current mirror [182], gain boosting [168], current reuse [174] and current injection [135], double linearization [183] are some of the commonly used techniques while designing mixers. Nevertheless, each approach discussed has its own set of advantages and disadvantages. It is important to maintain trade-offs, obtain high performance, and minimize drawbacks. Various techniques and design topologies have been proposed to address the problem, such as balanced LNA-mixer structures [78], passive inductor-based tunable resonators [107], dual matching networks [95], programmable notches [176], discrete-time mixing [161] and current-reuse source degeneration MGTR [84] to solve noise, power consumption, gain-linearity trade-offs, and linearity problems with multiband mixers. However, all these problems cannot be solved simultaneously as they may result in complex circuitry and desire a high chip area. This shows that there is a research gap in the literature and more research must be done to overcome design challenges. Therefore, after careful literature study, we aim to present some challenges

that are addressed in our research reported in this thesis.

This thesis aims to develop and analyse reconfigurable mixers for SDRs instead of concurrent mixers due to their inability to maintain good trade-offs among various performance parameters. The proposed reconfigurable mixers are active in nature and cover a wide tuning range while maintaining high performance within the entire band of operation. These mixers followed different design topologies and employed the best possible techniques to achieve high performance within a wide frequency tunable range. The proposed mixers and receiver architecture are briefly explained as mentioned below:

The first proposed mixer used Gilbert mixer topology and employed g_m-boosting technique for maintaining good CG. However,this technique does not guarantee good IIP3 which clearly illustrates the gain-linearity trade-off. The design also included separate LOI/LOQ stages and reconfigurable filters for image rejection and impedance matching purposes. The second proposed mixer utilized a balanced structure to maintain a small chip area. Moreover, it employed current mirror and current bleeding approaches, which can maintain good CG and low NF while utilizing low power at the expense of IIP3. Furthermore, the third mixer is mainly focused on overcoming the problem of IIP3 in active mixers. The mixer was balanced in nature and utilized an active inductor circuitry that maintained a good balance among IIP3 and the area. To further maintain good performance in terms of CG, the design also utilized current mirror approach.

The wideband reconfigurable receiver architecture is also a part of this thesis, which also attained high performance within the entire band of operation. The proposed architecture was developed to maintain good IRR, IIP3, which utilized I/Q active inductor-based mixers, filters, reconfigurable LNAs, and IF amplifiers. The upcoming chapters will provide a detailed discussion on the proposed mixers and receiver architecture.

PSO is one of the simple, powerful, and most effective solutions for improving the overall performance of the RF circuits. Thus, it has been implemented on all proposed mixers and receiver architecture that significantly improve performance in terms of all the parameters compared to the unoptimised results.

Chapter 3

Design and Analysis of a Reconfigurable Gilbert Mixer for Software Defined Radios

3.1 Introduction

A mixer is considered one of the essential blocks of SDR receivers. Among the existing mixer topologies, the Gilbert cell is the most common due to its ability to provide broadband performance without affecting other parameters [184]. For SDRs, a wideband mixer is essential, which lowers the design complexity and overall cost [133]. SDR mixers must have the ability to provide linear operation and maintain good design stability. Additionally, the design must be able to attain good performance in terms of IIP3, NF, CG, IRR, dynamic range and filtering, [185, 186, 187, 188, 189, 104]. Additionally, the mixer design should have low complexity and power consumption to enhance the battery lifespan [190]. However, based on a literature study [191, 192, 193, 194, 195, 196], a limited number of SDR mixers can be found that can maintain high performance in terms of various parameters simultaneously. Thus, this chapter discusses an image-rejected Gilbert mixer operating in the 0.9 GHz - 13.5 GHz band. The mixer has been developed using 8HP CMOS process technology. The proposed mixer employs g_m-boosting circuitry to maintain a high CG. Additionally, for tuning purposes, the 9^{th} order tunable resonator has been developed for proper tuning within the mixer [197]. This chapter focuses on

the design and analysis of the reconfigurable mixer. The mixer's reliability performance has also been analyzed using Relxpert software and is compared with the simulation results to validate the circuitry.

3.2 Motivation

Figure 3.1 depicts the merged LNA and mixer circuitry [196, 197]. The merged circuitry consists of g_m-boosting circuitry and current bleeding circuitry to maintain good design performance. Additionally, LNA sections can also contain additional capacitors and inductors. Moreover, current peaking circuitry is necessary for the design to operate within a wideband [196, 197]. Furthermore, as shown in Figure 3.2, the small-signal model helps to determine the circuit impedance at the input and output [196, 197].

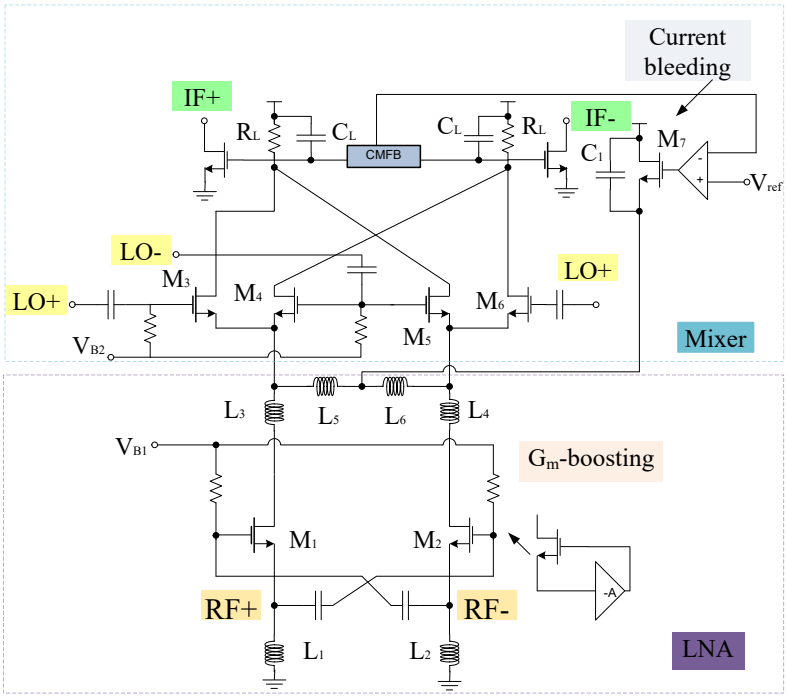


Figure 3.1: Integrated architecture

The input impedance, Z_{in} can be defined as [196, 197]

$$Z_{\text{in}} = \frac{sL_1}{1 + (G_{\text{m1}} + sC_{\text{gs1}})sL_1} \tag{3.1}$$

where C_{gs1} denotes the gate to the source capacitance.

G_m-boosting is responsible for improving the overall transconductance of the circuitry, which in turn improves the overall gain. It is indicated by the factor (-A) as shown in Figure 3.1. Upon analysing the circuitry, g_m is defined as [196, 197]

$$G_{m1} = \frac{r_{01} + Z_L}{1 + 2g_{m1}r_{01}} \tag{3.2}$$

where g_{m1} denotes transconductance, r_{01} refers to the transistor impedance, and Z_L denotes the refers to the load impedance of transistor M_1. Likewise, the output impedance, Z_L can be expressed as [196, 197]:

$$Z_L = \frac{1}{sC_1}||[sL_3 + (\frac{1}{sC_2})||sL_5||(\frac{1}{g_{m3}}||\frac{1}{g_{m4}})] \tag{3.3}$$

where C_1, C_2 correspond to the interstage parasitic capacitances. g_{m3}, g_{m4} refer to the transistor transconductance. On the basis of the input network circuitry it has been found that the resonant frequency depends on C_{gs1} and L_1. Thus, the resonant frequency of the real input impedance, Z_{in} can be expressed as [196, 197]

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_{gs1}}} \tag{3.4}$$

Therefore, tunable resonators must be employed within the circuitry to achieve the tunable frequency, f_0 and the input impedance [196, 197]. As a result, the total chip area and power consumption will be increased at the expense of NF.

Based on the proposed mixer in [196, 197], this chapter proposed an active Gilbert mixer with a tunable resonator. Thus, to achieve the good return loss, S_{11}, the input impedance must be reconfigured. The g_m-boosting technique is used to further enhance circuit performance.

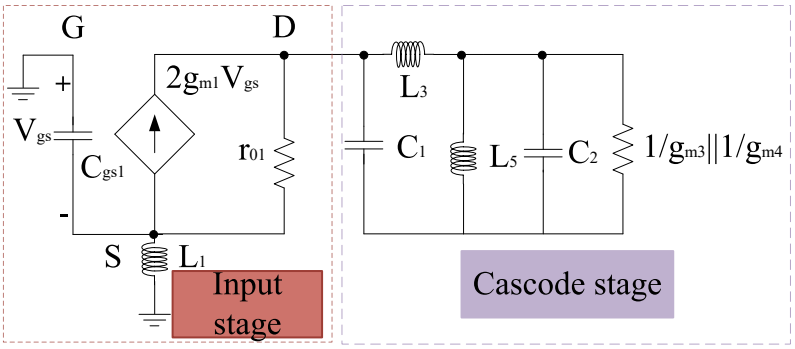


Figure 3.2: Small signal model

3.3 Proposed Mixer Topology

Figure 3.3 shows the block diagram of the proposed mixer with different stages. Starting from the bottom, Stage I indicates the transconductance stage that follows a common source configuration. Stage II refers to the core stage, categorized into local oscillator in-phase (LOI) and local oscillator out-of-phase (LOQ) stages, where the input signals are in a 90-degree phase shift from each other. Likewise, coupling capacitors are used for coupling transconductance and core stages, respectively [197]. Stage III refers to the g_m-boosting stage. Finally, stage IV discusses the filters, i.e., the first-order filter to avoid power supply leakage and the 9^{th} order tunable filter for impedance matching at RF and IF stages [197]. For a detailed understanding of the proposed circuit topology, the design and analysis of all stages are discussed below.

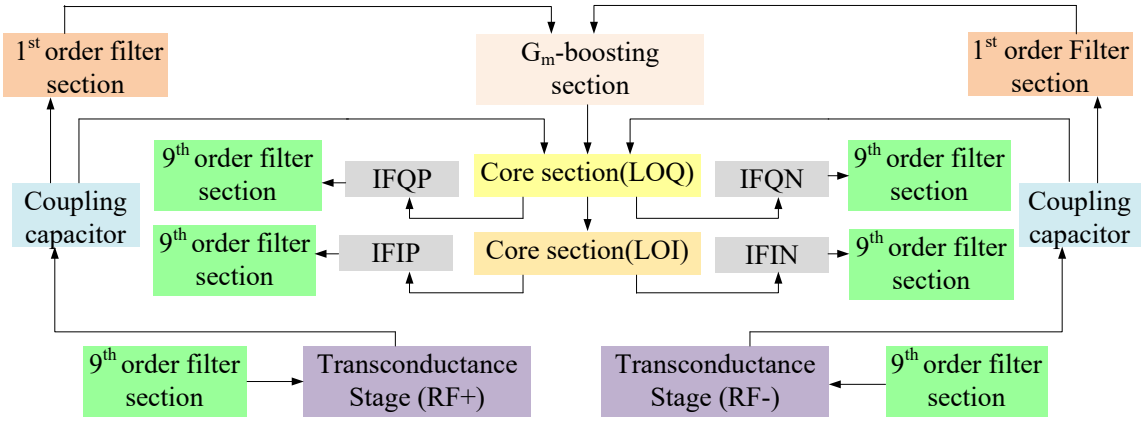


Figure 3.3: Proposed mixer architecture

3.3.1 Tranconductance stage

Figure 3.4 shows the complete circuit diagram of the proposed mixer. The transconductance stage follows the common source configuration, shown in the RF+ and RF- stages. Both the RF + and RF- stages contain different resistors arranged in a shunt configuration with the RF + stage that consists of input resistors R_1, R_2, and R_3. Similarly, RF- consists of input resistors R_5, R_6, and R_7, respectively. R_1 and R_5 resistors are responsible for the overall input resistance of each stage and can alter the input voltage and hence the overall gain performance. R_4 and R_8 refer to the load resistors opted while keeping the desired drain current I_D [197, 198, 185]. Filters are also present at the input end of these stages for impedance-matching purposes. The W / L ratio of the transistors is chosen in such a way as to satisfy the operating conditions of the core stage. The input, output impedance, and gain expression of the RF stages can be obtained with the help of the equivalent small signal model, as shown in Figure 3.5. The small signal model does not include the filter section, whose detailed analysis is discussed in the filter section [197, 185, 198]. Therefore, for the RF + stage, R_{in} is the internal resistance, R_G refers to the gate resistance, which is the parallel combination of R_1, R_2, and R_3 respectively. The input impedance and the output impedance for the RF + stage are expressed by Z_{in} and Z_{out}, respectively, as mentioned below [197]:

$$Z_{\text{in}} = R_{\text{G}} = R_1||R_2||R_3 \tag{3.5}$$

$$Z_{\text{out}} = R_1||\frac{1}{jwC_1} = \frac{R_1}{(R_1)(jwC_1)+1} = \frac{R_1}{(R_1)(sC_1)+1} \tag{3.6}$$

where $R_1 = r_{ds_{14}} = R_4$, $sC_1 = sC_{db14} + sC_3$. Similarly, the input and output impedances of the RF stage can be expressed as [197]

$$Z_{\text{in}} = R_{\text{G}} = R_5||R_6||R_7 \tag{3.7}$$

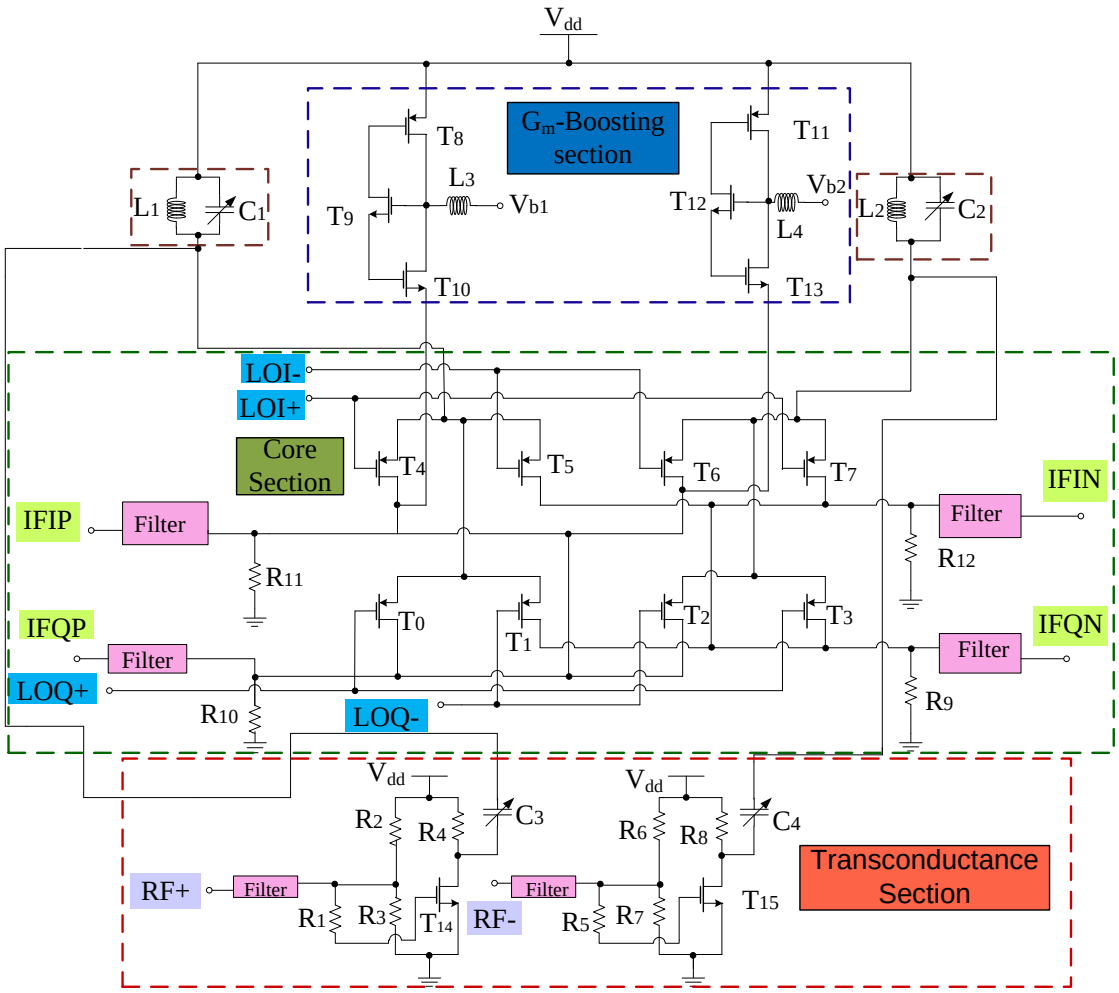


Figure 3.4: Proposed mixer

Output impedance of the RF- stage

$$Z_{out} = R_2 || \frac{1}{jwC_2} = \frac{R_2}{(R_2)(jwC_2)+1} = \frac{R_1}{(R_2)(sC_2)+1} \tag{3.8}$$

where $R_2 = r_{ds_{15}} = R_8$, $sC_2 = sC_{db15} + sC_4$. Therefore, to obtain the frequency response of the small signal circuit, a nodal analysis can be done. The first term should be the node at which the currents are added. If node voltages are multiplied, then it refers to all admittances being connected to a node. The next terms with negative signs are actually neighbouring node voltages, and each of these terms uses a multiplication operation on the connecting admittance. The final terms refer to current sources having a positive sign that is considered only if current sources are

flowing out of that node [199, 197]. Based on this, we have

$$V_1(G_G + sC_{gs14} + sC_{gd14}) - V_{in}G_G - V_{out}sC_{gd14} = 0 \tag{3.9}$$

$$V_{out}(G_1 + sC_1 + sC_{gd14}) - V_1 sC_{gd14} + g_{m14}V_{gs14} = 0 \tag{3.10}$$

As $V_1 = V_{gs}$, then from equation(3.10), we get;

$$V_1 = \frac{V_{out}(G_1 + sC_1 + sC_{gd14})}{-g_{m14} + sC_{gd14}} \tag{3.11}$$

By substituting (3.11) into (3.9), we get [197];

$$V_{out}[G_1G_G + s[G_1(C_{gs14} + C_{gd14}) + G_G(C_{gd14} + C_1) + g_{m1}C_{gd14}] + s^2[(C_{gs14} + C_{gd14}) (C_1 + C_{gd14}) - C^2{}_{gd14}]] = V_{in}G_G(-g_{m14} + sC_{gd14}) \tag{3.12}$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m14}(1 - s\frac{C_{gd14}}{g_{m14}})R_1}{1 + sa + s^2b} \tag{3.13}$$

$$a = R_G[C_{gs14} + C_{gd14}(1 + g_{m14}R_1)] + R_1(C_{gd14} + C_1) \tag{3.14}$$

R_{in} is ignored, and G_G, G_1 are converted and simplified to R_G, R_1, we get [197];

$$b = R_G R_1(C_{gd14}C_{gs14} + C_{gs14}C_1 + C_{gd14}C_1) \tag{3.15}$$

If s=0, the low frequency gain is obtained as mentioned below [197]:

$$A_v = -g_{m14}R_1 \tag{3.16}$$

When the poles are real [197] and

$$w_{p1} << w_{p2} \tag{3.17}$$

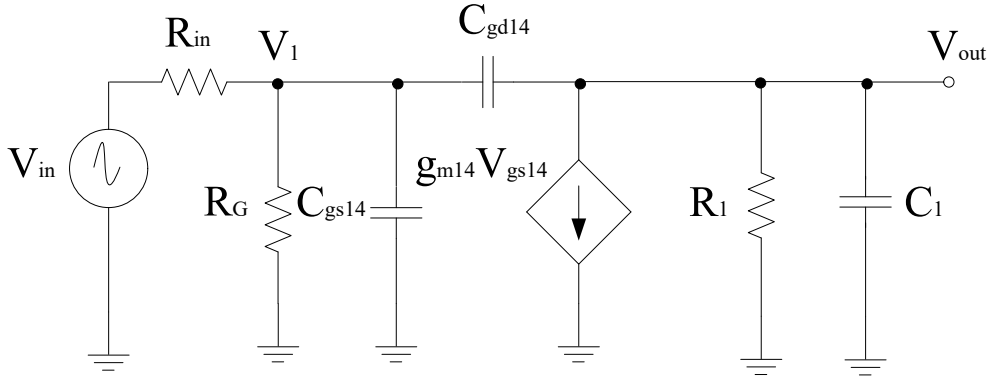


Figure 3.5: Small signal model for the transconductance stage

The denominator of equation (3.13) is expressed as [197]

$$D(s) = (1 + \frac{s}{w_{\text{p1}}})(1 + \frac{s}{w_{\text{p2}}}) = 1 + \frac{s}{w_{\text{p1}}} + \frac{s^2}{w_{\text{p1}} w_{\text{p2}}} \tag{3.18}$$

Comparing equation (3.15) with equation (3.19), we get;

$$w_{\text{p1}} = \frac{1}{a} \tag{3.19}$$

$$w_{\text{p2}} = \frac{1}{b w_{\text{p1}}} \tag{3.20}$$

The simplified gain for the RF- stage can be represented as [197]

$$A_{\text{v}} = -g_{\text{m15}} R_2 \tag{3.21}$$

3.3.2 Core stages

The image signal is an unwanted input signal to the mixer. Its frequency will be above or below the local oscillator (LO) frequency by an amount equal to the IF frequency. For example, if f_{R1}, refers to the frequency of the desired input signal, then f_{R2} will be its image. Therefore, both image and actual input signals mix with the LO and will down-convert to the same frequency. This is quite problematic for the mixer, as both downconverted products will interfere with each other as they exit the IF port together [197, 198]. Thus, it is desirable to have separate LO stages

where the outputs will be obtained at different IF stages. On the basis of this phenomenon, two core stages have been used for the proposed mixer, whose output will be obtained at different IF stages. The switching stages controlled by LO inputs are classified as in-phase (I) and quadrature-phase (Q) stages for image rejection purposes. Both these LO stages contain p-type field-effect transistors (PFETs) for flicker noise reduction purposes; the transistors T_0-T_3,T_4-T_7 are part of the LOQ and LOI stages, respectively [197]. Alternate transistors at each stage will form a differential pair and operate alternatively by applying the LO pulse. Therefore, differential outputs will be obtained, and the current switch can be seen between outputs. Additionally, the output current is directly proportional to the input current and the signal applied at the gate terminals. To determine the output voltage, the current flowing through the load resistor must be considered along with the load resistor itself. The proposed design utilizes coupling capacitors for RF and LO stage coupling. The small signal model is shown in Figure 3.6, which is useful to obtain the output voltage with respect to the current obtained from the RF stage. The model uses Kirchoff's current law (KCL) for analysis [198, 41, 185]. Thus, the output current is expressed as

$$i_{\text{IF}} = i_1 + i_2 \tag{3.22}$$

$$i_{\text{IF}} = \frac{V_{\text{IF}}}{R_{10}} + \frac{V_{\text{IF}}}{R_{11}} \tag{3.23}$$

$$i_{\text{IF}} = V_{\text{IF}}(\frac{1}{R_{10}} + \frac{1}{R_{11}}) \tag{3.24}$$

$$i_{\text{IF}} = V_{\text{IF}}(\frac{R_{10} + R_{11}}{R_{10}R_{11}}) \tag{3.25}$$

$$\frac{V_{\text{IF}}}{i_{\text{IF}}} = \frac{R_{10}R_{11}}{R_{10} + R_{11}} \tag{3.26}$$

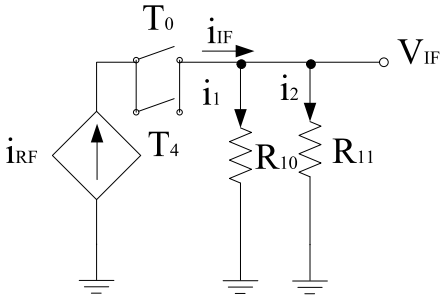


Figure 3.6: Small signal model for core stage

3.3.3 G_m-boosting section

The proposed mixer employs g_m-boosting circuit to improve the overall transconductance within the mixer, which in turn improves the overall CG [200]. The proposed g_m-boosting circuits employ peaking inductors at the gate terminals of the transistors. These inductors resonate with the parasitic capacitances and avoid current leakage. The design also employs P-type FETs (T_8 and T_{11}) connected to V_{dd} [197]. However, (T_9-T_{12}) are N-type FETs. The circuitry also follows the stacking structure, where transistors T_9 and T_{12} act as an amplifier that helps improve g_m and overall gain by a factor of (-A). Transistors T_{10} and T_{13} deliver the current to the connecting stages. All transistors present within the circuitry operate in the saturation region. The drain current will start flowing in the core stages; the current obtained from this stage will bleed into the transconductance stage [197]. This current will be reused by transistors T_{14} and T_{15}, respectively. The equivalent circuit for the g_m-boosting stage is shown in Figure 3.7. When the

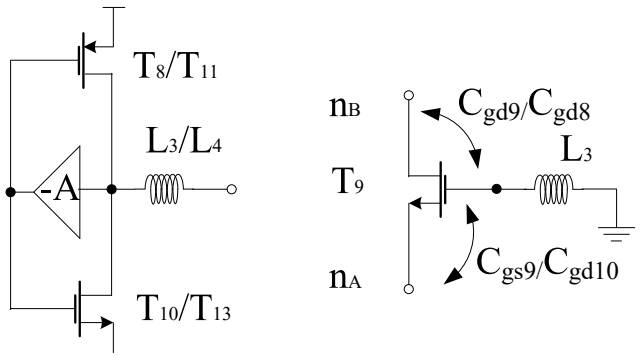


Figure 3.7: G_m design

transistors T_8, T_{10}, T_{11}, and T_{13} operate in the saturation region, the current flowing through that

stage is expressed as [197] :

$$i_{\text{GM+}} = I_{\text{D8}} + I_{\text{D10}} - (1 + A) g_{\text{m8}} g_{\text{m10}} v_{\text{RF}} \tag{3.27}$$

Likewise, for the other section

$$i_{\text{GM-}} = I_{\text{D11}} + I_{\text{D13}} - (1 + A) g_{\text{m11}} g_{\text{m13}} v_{\text{RF}} \tag{3.28}$$

As LO switches are considered ideal, the output current will be positive during the positive half of the LO pulse. The current obtained will be negative during the negative half-cycle. The total current due to the half-LOI stage is represented as [197]:

$$i_0 = I_{\text{D4}} - I_{\text{D5}} = I_{\text{D11}} + I_{\text{D13}} - (1 + A) g_{\text{m11}} g_{\text{m13}} v_{\text{RF}} \tag{3.29}$$

This current is transferred to the LOQ stage, and then the current within this stage will be due to LOI and the stage itself [197].

$$i_1 = i_0 + I_{\text{D0}} - I_{\text{D1}} \tag{3.30}$$

The coupling capacitors connect the LO stages to the RF stage. Thus, the overall boosting can be observed in terms of CG, where the g_m stage is acting in parallel with the load at the IF end [197]. In addition to this, the g_m-boosting inductors, L_3 or L_4 present within the design are responsible for the gain improvement. The design analysis of the g_m-boosting stage is explained according to the positive feedback theory, whose model is shown in Figure **7**. To use this principle, the T_9 signal paths are taken into account and the output impedance has been ignored for simplicity [197]. Therefore, due to the presence of L_3 or L_4 a non-zero impedance can be observed at the gate terminal of T_9. Likewise, the feedforward and feedback paths are considered using parasitic capacitances such as the gate source capacitance (C_{gs}) and the gate drain capacitance (C_{gd}), respectively. Therefore, the gate source voltage of T_9 becomes $V_{g,T9}$ when considering new signal paths. The next step is to calculate the open-loop voltage gain according to the voltage-voltage feedback [197]. Based on the model, the voltage at the drain

terminal is expressed as

$$V_{\text{nB}} = -g_{\text{m9}} V_{\text{gs9}} Z_{\text{nB}} = g_{\text{m9}}(V_{\text{nA}} - \alpha V_{\text{nA}}) Z_{\text{nB}} \tag{3.31}$$

where V_{gs9}, g_{m9} and Z_{nB} refer to the gate-to-source voltage of T_9, transconductance of T_9 and the output impedance at node nB that includes duplicate, respectively [197]. where

$$Z_{\text{nB}} = Z^{'}_{\text{nB}} || (sL_3 + \frac{1}{sC_{\text{gd9}}}) \tag{3.32}$$

$$Z^{'}_{\text{nB}} = \frac{1}{sC_{\text{gd9}}} || \frac{1}{sC_{\text{gd8}}} || (\frac{1}{g_{\text{mLOI}} + g_{\text{mLOQ}}}) \tag{3.33}$$

where $Z^{'}_{nB}$, α, C_{gd9} and C_{gd8} refer to the output impedance excluding duplicate, the voltage ratio from source to gate, the parasitic capacitances for T_8 and T_9, respectively [197]. Thus, the open-loop gain is represented as [197]

$$A_0 = (1 - \alpha) g_{\text{m9}} Z_{\text{nB}} \tag{3.34}$$

where

$$\alpha = \frac{sL_3 || \frac{1}{sC_{\text{gd9}}} || \frac{1}{sC_{\text{gd8}}}}{(\frac{1}{sC_{\text{gs9}}} || \frac{1}{sC_{\text{gd10}}}) + sL_3 || \frac{1}{sC_{\text{gd9}}}} \tag{3.35}$$

Finally, the voltage gain (AV_0) without the feedback inductor and the closed-loop voltage gain (AV_f) can be expressed as [197]

$$A_{\text{v0}} = \frac{V_{\text{nB}}}{V_{\text{nA}}}|_{(\text{w/o})L_3} = g_{\text{m9}} Z_{\text{nB}}|_{(\text{w/o})L_3} \tag{3.36}$$

$$A_{\text{vf}} = \frac{V_{\text{nB}}}{V_{\text{nA}}}|_{(\text{w})L_3} = \frac{A_0}{1 + \beta A_0} \tag{3.37}$$

where

$$Z_{\text{nB}}|_{(\text{w/o})L_3} = Z^{'}_{\text{nB}} || \frac{1}{sC_{\text{gd9}}} \tag{3.38}$$

$$\beta = \frac{sL_3}{(\frac{1}{sC_{\text{gd9}}}||\frac{1}{sC_{\text{gd9}})} + sL_3} \tag{3.39}$$

where β is the feedback factor from the drain to the gate. Therefore, it has been verified from the above equations that the gain has been boosted in the presence of the inductor [197].

3.3.4 Filter section

The proposed mixer includes reconfigurable filters in the input-output ports, responsible for impedance matching at various frequency bands. Additionally, the filters are also present near the LO stage, which prevents signal leakage from the power supply. The current literature study shows that transmission lines, transformer-dependent programmable or spiral inductors, and dual-behaviour resonator topology [201, 202, 203, 204, 198, 185, 197] are some of the techniques commonly used to develop filters. Nevertheless, the filters created using these techniques are on-chip and have limited band coverage. Thus, it is helpful to employ off-chip filters. These filters also suffer from problems such as complex integration and high cost. Therefore, the researchers must propose novel image rejection mixers with reconfigurable filters. This chapter proposes a 9$^{\text{th}}$-order bandpass perfectly tunable filters that are present at the RF and IF stages of the mixer, as shown in Figure 3.8. Besides, Figure 3.9 shows the circuitry of the first-order bandpass filter present at the source terminals of the LOI stage transistors at one end and the power supply at the other end to avoid leakage from the power supply. The input and output impedance of the 9$^{\text{th}}$-order filter sections that can be expressed as a combination of series and parallel LC sections within the design. The filter order depends on the number of LC pairs [197, 198, 185]. The input impedance, Z_{in} is expressed as [197]:

$$\begin{aligned} Z_{\text{in}} = [[[[[[(sL_1||\frac{1}{sC_1} + sL_2||\frac{1}{sC_2})||\frac{1}{sC_3}] + sL_3||\frac{1}{sC_4}] \\ ||sC_5] + sL_4||\frac{1}{sC_6}]||\frac{1}{sC_7}] + sL_5||\frac{1}{sC_8}]||sL_6||\frac{1}{sC_9}] \end{aligned} \tag{3.40}$$

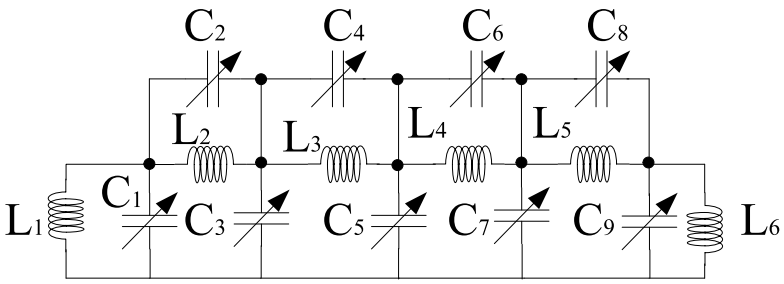


Figure 3.8: 9th order Filter

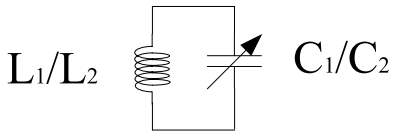


Figure 3.9: 1st order filter

$$Z_{\text{in}} = (Y + F)||G \tag{3.41}$$

$$Y = (X + D)||E \tag{3.42}$$

$$X = (A + B)||C \tag{3.43}$$

$$A = (sL_1||\frac{1}{sC_1} + sL_2||\frac{1}{sC_2})||\frac{1}{sC_3} \tag{3.44}$$

$$B = sL_3||\frac{1}{sC_4} = \frac{sL_3}{s^2L_3C_4 + 1} \tag{3.45}$$

$$C = \frac{1}{sC_5} \tag{3.46}$$

$$D = sL_4||\frac{1}{sC_6} = \frac{sL_4}{s^2L_4C_6 + 1} \tag{3.47}$$

$$E = \frac{1}{sC_7} \tag{3.48}$$

$$F = sL_5 || \frac{1}{sC_8} = \frac{sL_5}{s^2 L_5 C_8 + 1} \tag{3.49}$$

$$G = sL_6 || \frac{1}{sC_9} = \frac{sL_6}{s^2 L_6 C_9 + 1} \tag{3.50}$$

For simplicity, different letters have been defined to represent the LC combinations. The output impedance, Z_{out} is expressed as [197]:

$$Z_{\text{out}} = sL_6 || \frac{1}{sC_9} \tag{3.51}$$

Likewise, the 1st order impedance depends on the parallel combination of L and C [197].

$$Z_{\text{P}} = Z_{\text{L}} || Z_{\text{C}} = \frac{Z_{\text{L}} Z_{\text{C}}}{Z_{\text{L}} + Z_{\text{C}}} \tag{3.52}$$

The resonant frequency at which the impedance, Z_P will be real can be defined as [197]

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3.53}$$

or

$$\frac{1}{2\pi\sqrt{L_2 C_2}} \tag{3.54}$$

where Z_P refers to the parallel circuit impedance. The resonant frequency varies depending on the selected filter circuit within the design [197].

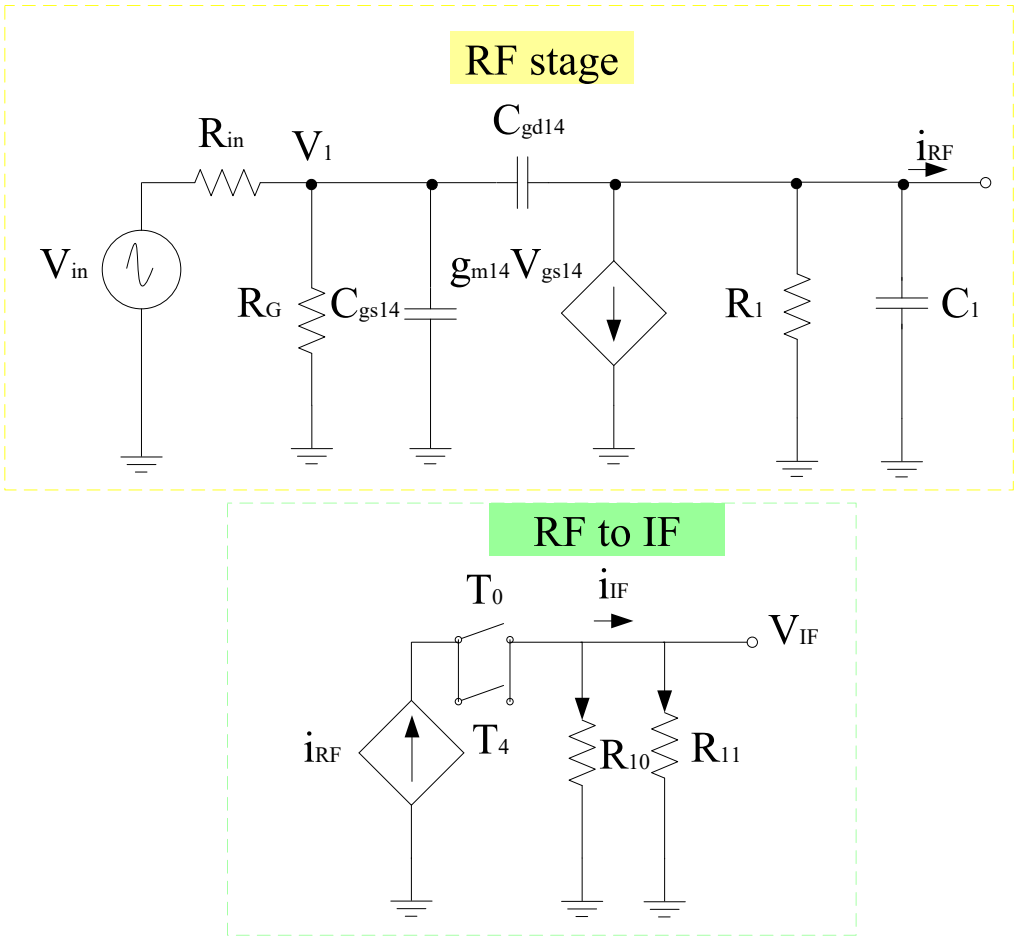


Figure 3.10: Small signal model for a complete circuit

3.4 Mixer Design Analysis

Figure 3.4 shows the complete mixer architecture. Several necessary steps are involved in the design. The initial step is to determine the band of operation. The next step is to choose the design topology and filters for a successful reconfiguration. The proposed design utilizes the Gilbert topology, which is responsible for improving the overall CG, NF. To further enhance design performance, g_m-boosting with inductive peaking is employed. The design is structured to provide good image rejection without affecting the performance of the design [197].

3.4.1 Conversion Gain

Figure 3.10 shows the complete small signal model used to obtain the overall CG within the design [198, 197]. The CG, A_v is represented by the expression below [197]:

$$A_v = \frac{V_{IF}(s_{IF})}{i_{IF}(s_{IF})} \frac{i_{IF}(s_{IF})}{i_{RF}(s_{RF})} \frac{i_{RF}(s_{RF})}{V_{gs14}(s_{RF})} \frac{V_{gs14}(s_{RF})}{V_{in}(s_{RF})} \tag{3.55}$$

where all expressions in equation (3.55) are obtained using the small signal model except $i_{IF}(s_{IF})/i_{RF}(s_{RF})$ which can be obtained using Fourier series analysis by approximating the LO signal like a square wave [197].

$$\frac{V_{gs14}(s_{RF})}{V_{in}(s_{RF})} = \frac{1}{(1 + \frac{R_{in}}{R_G}) + sC_{gs14}R_{in}} \tag{3.56}$$

$$\frac{V_{IF}(s_{IF})}{i_{IF}(s_{IF})} = \frac{R_{10}R_{11}}{R_{10} + R_{11}} \tag{3.57}$$

$$\frac{i_{IF}(s_{IF})}{i_{RF}(s_{RF})} = \frac{2}{\pi} \tag{3.58}$$

For determining $i_{RF}(s_{RF})/V_{gs14}(s_{RF})$ ratio, KCL is applied and we obtain the expression as mentioned below [197]:

$$V_{gs14}(s_{RF})[s(C_{gs14} + C_{gd14}] = g_{m14}V_{gs14} + i_{RF}(s_{RF})[\frac{1}{R_1} + sC_1] \tag{3.59}$$

Rearranging (3.59), we get [197]

$$V_{gs14}(s_{RF})[sC_{gs14} + sC_{gd14} - g_{m14}] = i_{RF}(s_{RF})(\frac{1}{R_1} + sC_1) \tag{3.60}$$

$$\frac{i_{RF}(s_{RF})}{V_{gs14}(s_{RF})} = \frac{sC_{gs14} + sC_{gd14} - g_{m14}}{\frac{1}{R_1} + sC_1} \tag{3.61}$$

By substituting (3.56)-(3.61) into (3.55), the overall CG can be obtained.

3.4.2 Noise Figure

Figure 3.11 shows the noise model for the proposed circuit. All passive elements are considered ideal in the circuitry, and the analysis is done based on the thermal noise of resistors and transistors, respectively. Thus, the overall power spectral density of each stage is obtained [205, 199, 197].

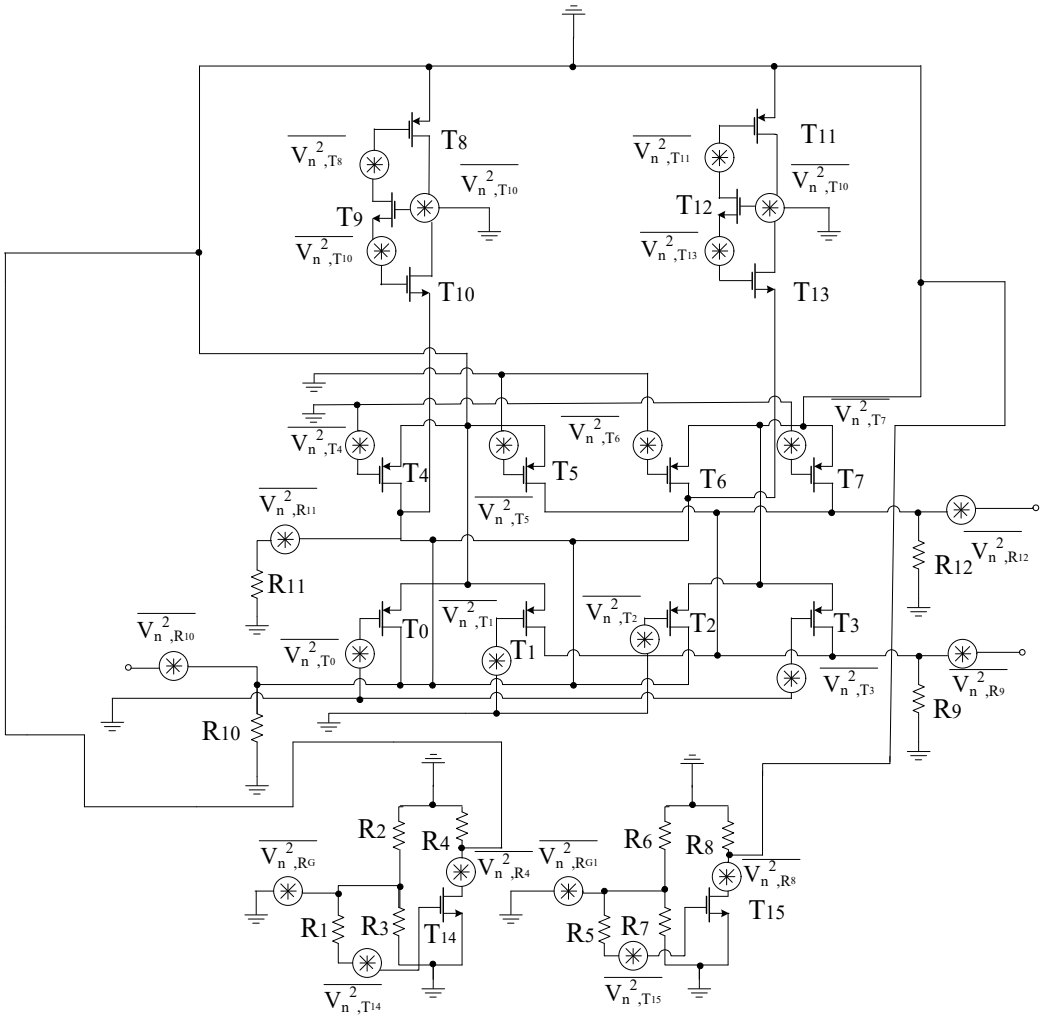


Figure 3.11: Proposed mixer noise model

Equation (3.62) defines the power spectral density, which is the combination of the power spectral density obtained from all stages present within the design [197].

$$\overline{V^2}_{\text{n}} = \overline{V^2}_{\text{n,RF}} + \overline{V^2}_{\text{n,LOI}} + \overline{V^2}_{\text{n,LOQ}} + \overline{V^2}_{\text{n,GM}} \tag{3.62}$$

The power spectral density for all stages is obtained based on the resistors and transistors present within each stage. Thus, the power spectral density for the RF+ stage is expressed as [197]

$$\overline{V^2_{\text{n,RF+}}} = \overline{V^2_{\text{n,R}_1}}+\overline{V^2_{\text{n,R}_2}}+\overline{V^2_{\text{n,R}_3}}+\overline{V^2_{\text{n,R}_4}}+\overline{V^2_{\text{n,T}_{14}}} = \frac{4kT\gamma}{g_{\text{m14}}}+4kTR_3+4kTR_2+4kTR_4+4kTR_1 \tag{3.63}$$

Likewise, the power spectral density for RF- stage is defined below

$$\overline{V^2_{\text{n,RF-}}} = \overline{V^2_{\text{n,R}_5}}+\overline{V^2_{\text{n,R}_6}}+\overline{V^2_{\text{n,R}_7}}+\overline{V^2_{\text{n,R}_8}}+\overline{V^2_{\text{n,T}_{15}}} = \frac{4kT\gamma}{g_{\text{m15}}}+4kTR_5+4kTR_6+4kTR_7+4kTR_8 \tag{3.64}$$

Besides, the power spectral densities for LOI and LOQ stages are expressed as

$$\overline{V^2_{\text{n,LOI}}} = \overline{V^2_{\text{n,T}_4}} + \overline{V^2_{\text{n,T}_5}} + \overline{V^2_{\text{n,T}_6}} + \overline{V^2_{\text{n,T}_7}} + \overline{V^2_{\text{n,R}_{11}}} + \overline{V^2_{\text{n,R}_{12}}} \tag{3.65}$$

$$\overline{V^2_{\text{n,LOI}}} = 4kTR_{11} + 4kTR_{12} + \frac{4kT\gamma}{g_{\text{m4}}} + \frac{4kT\gamma}{g_{\text{m5}}} + \frac{4kT\gamma}{g_{\text{m6}}} + \frac{4kT\gamma}{g_{\text{m7}}} \tag{3.66}$$

$$\overline{V^2_{\text{n,LOQ}}} = \overline{V^2_{\text{n,T}_0}} + \overline{V^2_{\text{n,T}_1}} + \overline{V^2_{\text{n,T}_2}} + \overline{V^2_{\text{n,T}_3}} + \overline{V^2_{\text{n,R}_9}} + \overline{V^2_{\text{n,R}_{10}}} \tag{3.67}$$

$$\overline{V^2_{\text{n,LOQ}}} = 4kTR_9 + 4kTR_{10} + \frac{4kT\gamma}{g_{\text{m0}}} + \frac{4kT\gamma}{g_{\text{m1}}} + \frac{4kT\gamma}{g_{\text{m2}}} + \frac{4kT\gamma}{g_{\text{m3}}} \tag{3.68}$$

$$\overline{V^2_{\text{n,GM}}} = \overline{V^2_{\text{n,GM+}}} + \overline{V^2_{\text{n,GM-}}} \tag{3.69}$$

Finally, the power spectral densities for the GM stages are expressed as [197]

$$\overline{V^2_{\text{n,GM+}}} = \overline{V^2_{\text{n,T}_8}} + \overline{V^2_{\text{n,T}_9}} + \overline{V^2_{\text{n,T}_{10}}} = \frac{4kT\gamma}{g_{\text{m9}}} + \frac{4kT\gamma}{g_{\text{m8}}} + \frac{4kT\gamma}{g_{\text{m10}}} \tag{3.70}$$

$$\overline{V^2_{\text{n,GM-}}} = \overline{V^2_{\text{n,T}_{11}}} + \overline{V^2_{\text{n,T}_{12}}} + \overline{V^2_{\text{n,T}_{13}}} = \frac{4kT\gamma}{g_{\text{m11}}} + \frac{4kT\gamma}{g_{\text{m12}}} + \frac{4kT\gamma}{g_{\text{m13}}} \tag{3.71}$$

Hence, the noise figure of the proposed mixer is expressed as

$$NF = 1 + \frac{\overline{V^2_{\text{n}}}}{{A_{\text{v}}}^2} \tag{3.72}$$

Furthermore, to analyze the high-frequency noise in the proposed mixer, the thermal noise due to resistors, the thermal noise due to the drain, and the FET gate are considered [206]. The noise contributions due to the RF, LOI, LOQ, and output stages are considered for the proposed mixer. The noise contribution is obtained by considering Figure 3.11.

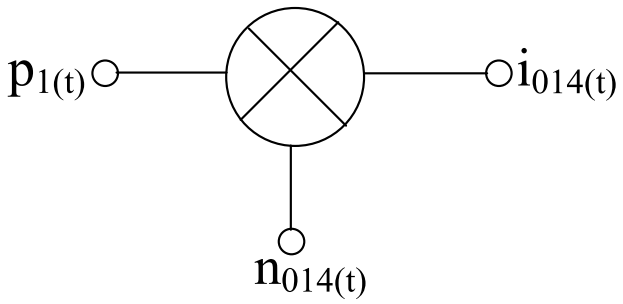


Figure 3.12: Mixer operation for noise calculation

The single-sideband NF is considered over the double sideband NF as [197]

$$NF_{\text{SSB}} = \frac{\int_0^\infty < S^0{}_{\text{n014}}(\omega,t) > d\omega}{|g_{\text{c}}(\omega)|^2}\frac{1}{4kTR_{\text{G}}}$$
$$= \frac{< S^0{}_{\text{n014}}(\omega,t) > + S^0{}_{\text{n01}}(\omega,t) + S^0{}_{\text{n45}}(\omega,t) + < S^0{}_{\text{nLO}}(\omega,t) > + (4kTR_{10} + 4kTR_{11}||G_{\text{M}})}{|g_{\text{c}}(\omega)|^2} \tag{3.73}$$

The above expression is defined for a single balanced mixer as derived in A.1. Similarly, for the double-balanced mixer, NF can also be defined, which is almost twice that obtained for a single balanced mixer [197].

3.5 Results and Discussion

The proposed mixer is designed and simulated in SiGe 8HP process technology. To further enhance transconductance within the RF stage, g_m-boosting technique has been used in the proposed design, resulting in high CG. Figure 3.13 shows the pre-and post-layout simulation results to depict the conversion gain performance of the proposed mixer. As illustrated in

Figure 3.13, the CGmin and CGmax values are quite similar for both simulations. Nevertheless, the variation can be observed at other frequencies within a band considering parasitic effects. The pre-layout CG at the center frequency, 7GHz, is 18.39 dB, and after the layout, it degrades to 17.7 dB. The CG degrades after the final layout due to the parasitic effects of passive components within the circuitry. In particular, the quality factors of the inductors within the circuitry are responsible for the gain performance degradation. Moreover, the parasitic resistance within the inductors can also lower the voltage gain within the circuitry [197]. Figure 3.14 depicts the NF

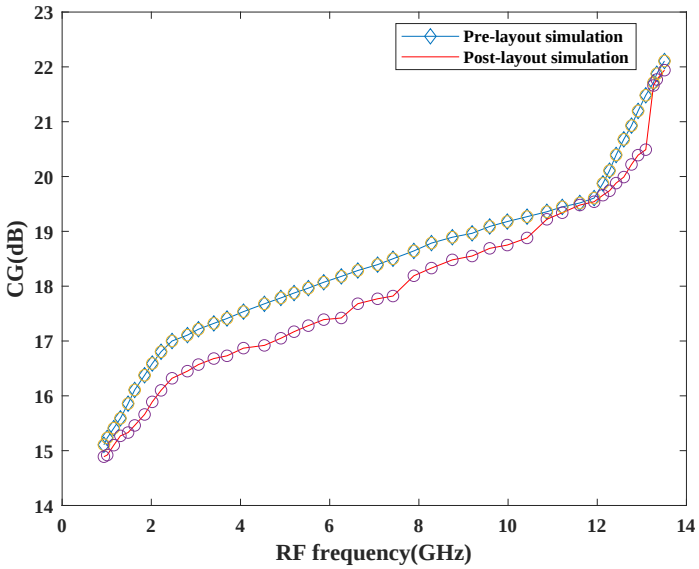


Figure 3.13: CG performance plot

of the mixer concerning the frequency. Based on the simulation results, it has been found that the NF is less than 3 dB before pre-layout simulation and raised by 0.8 dB upon post-layout simulation at the maximum frequency. The performance has also been affected by the parasitic effects of passive components. Additionally, performance gets affected by the variation in the number of resistive components, transistors, and conversion gain of the design. The proposed mixer attains good NF with a variation of ± 1 dB across the entire frequency [197]. The linearity performance of the mixer has been shown in Figure 3.15 and Figure 3.16, respectively. The mixer design is considered linear if it shows proportional behaviour within the input and output. This proportionality behaviour can be observed using third-order input intercept points (IIP3) and 1dB compression point (CP1). The actual behaviour of the mixer is well depicted in terms of

pre-and post-layout simulation results. As per the simulation results, it has been found that the design attained moderate linearity behaviour when observed at different frequencies in a band where IP3 is 10dBm higher than CP1. The image rejection ratio is another important parameter while designing the mixer, as depicted in Figure 3.17. When desired and image signals enter the input together, it degrades the overall performance of the circuitry and wastes power. Thus, to overcome this problem, the image signal must be rejected. The proposed mixer attains a good IRR of 28.91 dB at 10.46 GHz upon performing pre-and post-layout simulations. The maximum IRR is around 30 dB, within the normal specified IRR range of 20-40 dB. Figure 3.18 depicts the return loss performance with respect to frequency. Based on the simulation results, it has been found that the $|S_{11}|$ is below 10 dB at each centered frequency for the entire tuning band, which is as low as -22.42 dB at 11.91 GHz and 13.22 GHz, respectively [197]. Figure 3.19 depicts the layout of the proposed mixer. The circuitry is designed and simulated in 8HP process technology covering around 1.98 mm^2 area. The layout contains 48 pads, among which 14 pads are used to show power supply, biasing voltages, and various input and output ports. The design circuitry contains different sections, as discussed in detail in Section 3. The filter section is composed of spiral inductors and capacitors. Inductors are utilized to provide accurate inductance values and are capable of achieving the maximum Q at the desired operating frequency. Additionally, variable capacitors, i.e., varactors, are used to attain the tuning capacitance [197, 198].

Table 3.1 summarizes the proposed mixer's performance and compares the circuitry with recent works that attain low NF and high CG. As per Table 3.1, the minimum NF is around 2.5 dB and the maximum S_{11} is -20 dB. With the rise in CG, the IP3 gets degraded due to the CG-IIP3 trade-off. Furthermore, the maximum IRR is 36 dB. The overall area of the proposed mixer is higher than the other reported designs. However, the design achieves high performance in terms of CG, NF, IRR, and S_{11} simultaneously at the expense of IIP3, which is the best among all reported works in the literature [198, 185, 197]. To further improve the performance of the proposed mixer, PSO has been implemented on the mixer as discussed in Chapter 7, Section 7.7.1. The optimized results are obtained and compared with the simulated results. Based on the observation, it has been found that performance of the proposed mixer has significantly

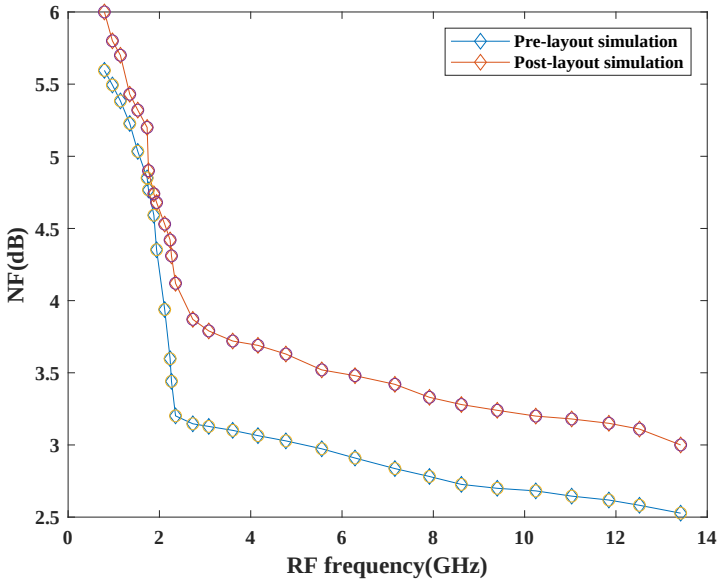


Figure 3.14: NF performance plot

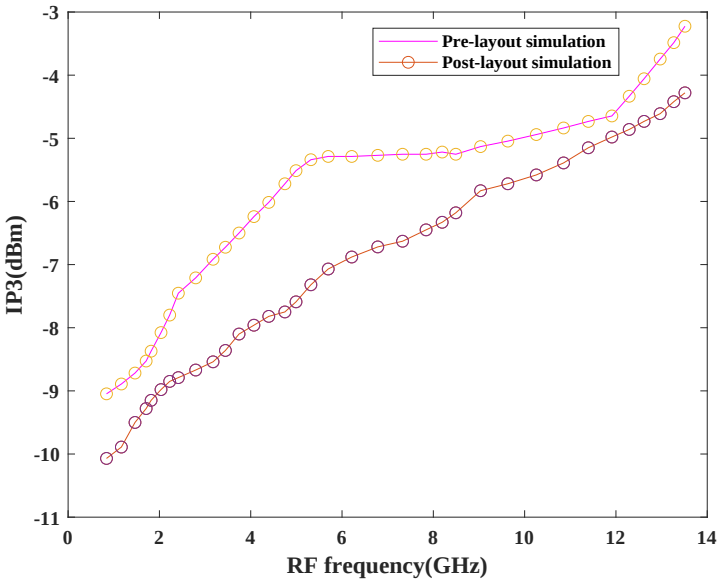


Figure 3.15: IP3 performance plot

improved.

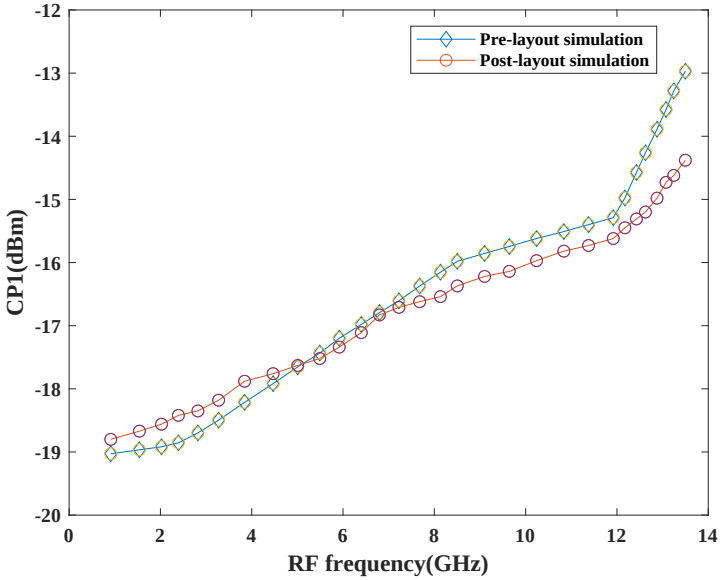


Figure 3.16: CP1 performance plot

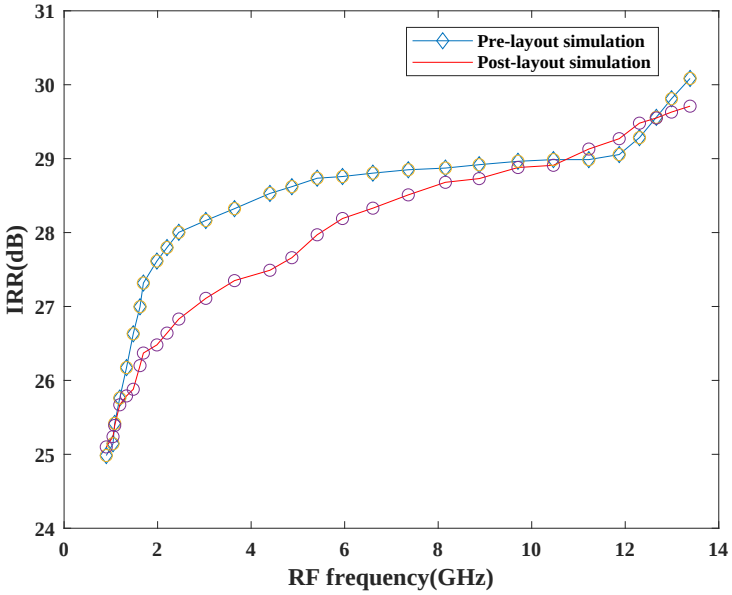


Figure 3.17: IRR performance plot

3.6 Reliability Analysis

Reliability analysis was the least prevalent among traditional designs because of the limitations of the process and the design guide. However, in recent years, it is essential to consider

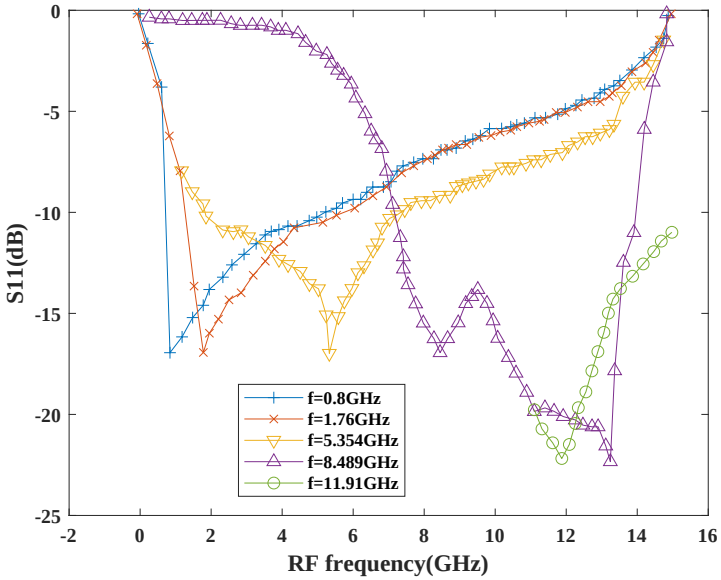


Figure 3.18: S_{11} performance plot

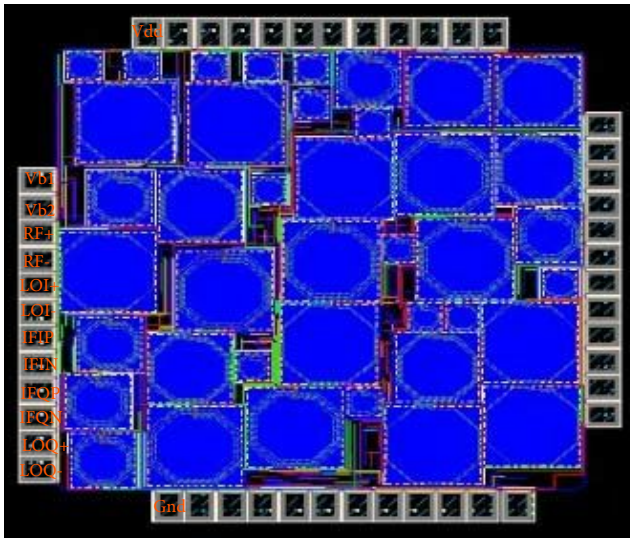


Figure 3.19: Designed Mixer Layout

design reliability due to time, budget, scaling, and demanding profile constraints. The Cadence-RelXpert tool can help simulate FET devices to determine their degradation performance due to stress time and biases. RelXpert output refers to a "corner in time" that moves towards slow corners while simulating from a typical corner. This process helps designers analyze the degradation in circuit behavior during the initial design flow stage [215, 197, 41, 198]. Degradation performance has been evaluated with respect to critical parameters such as CG, CP1, IP3, NF, and IRR ratio. Figure 3.20 depicts the mixer's IRR and NF performance with 5

Table 3.1: Performance Comparison Summary

Ref.	Tech.	Area (mm^2)	Freq.(GHz)	S_{21}(dB)	NF(dB)	IRR (dB)	IIP_3 (dBm)	S_{11}(dB)
This work	SiGe 8HP	1.8	0.9-13.5	15.1-22.1	2.5-5.6	24.9-30.2	-3.28-9.05	-17.14-22.7
[201]	0.25 um	Nil	0.9	5	8	30	1	-15
[84]	0.065 um	0.19	0.9,1.8-2.5	9.2-13	13.6-18.3	Nil	≥ 10.8	Nil
[207]	0.18 um	Nil	2.42-2.48	10.73	Nil	Nil	-7.31	Nil
[208]	0.18 um	Nil	2.4	9.3	7.4	Nil	8	Nil
[117]	0.18 um	Nil	2.4	17	11	Nil	1	Nil
[192]	0.18 um	Nil	2.44	18.6	7.15	Nil	-8.1	Nil
[209]	0.18 um	<1	3.1-10.6	≥ 10	10	Nil	4	-25
[200]	0.18 um	1.4	5.1	18	13.2	Nil	-5.85	-14.5
[203]	SiGe	0.9	5.1-5.8	14	6.8	36	-5.5	-11
[168]	0.13 um	0.85	7.2-8.4	23.8	4.3	30	-10.5	Nil
[210]	0.18 um	0.11	1.8-2.4	23-26	16-20	Nil	-2	Nil
[211]	0.18 um	0.61	0.5-7.5	5.7	15	Nil	-5.7	Nil
[212]	0.18 um	1.14	3-5	19.8-20.6	7.7-8.7	Nil	>-6	-10.5-15.2
[116]	0.065 um	0.21	1-10.5	10-14.5	6.5-10	Nil	Nil	-20
[213]	0.13 um	0.31	1-5.5	17.5	3.9	Nil	0.84	<-8.8
[89]	0.09 um	0.57	80-110	4.1-11.6	15.8-18.1	Nil	3	-8.7-22
[214]	0.065 um	0.5	17-43	-0.1$\pm$1.5	12.4	Nil	3.4	Nil
[170]	0.13 um	0.13	0.87-3.7	13.5-14	2.9-6.5	Nil	-10-13	Nil

years of aging. Based on the observation, it has been found that NF degradation is more than the IRR.

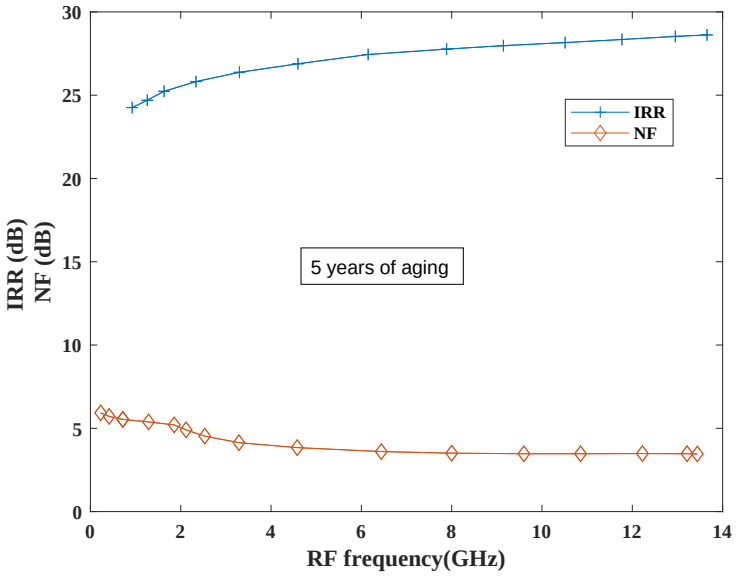


Figure 3.20: IRR and NF reliability performance

Figure 3.21 depicts the linearity plots for the proposed mixer circuit. The post-layout simulation results show that the linearity gets degraded compared to pre-layout simulation results. Thus, it is expected to have degraded linearity after five years of degradation, well depicted from the linearity performance plots. Likewise, the CG performance of the mixer can be seen from Figure 3.22. The gain shows negligible degradation after 5 years of aging. Thus, the proposed

mixer is reliable for future SDR applications [197].

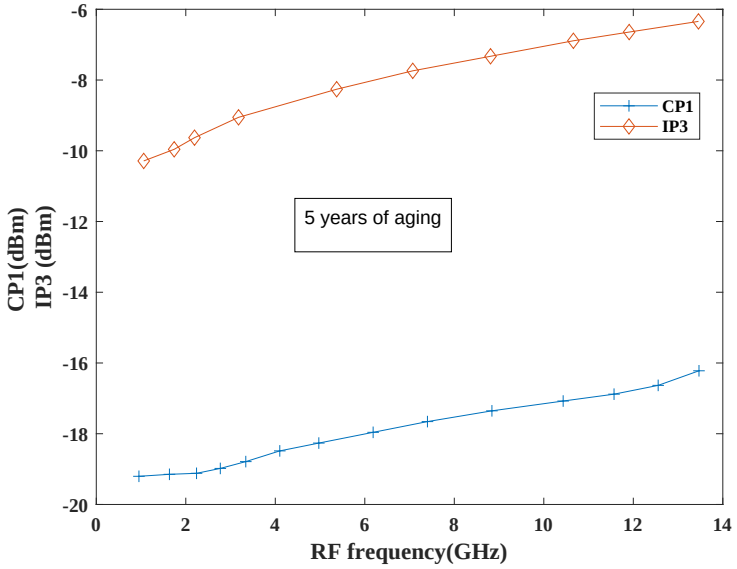


Figure 3.21: CP1 and IP3 reliability performance

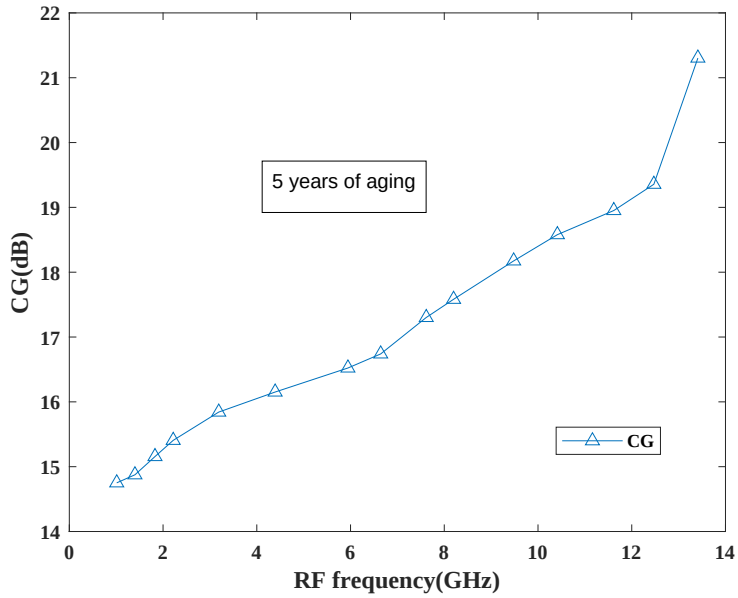


Figure 3.22: CG degradation performance

3.7 Summary

This chapter proposes a novel reconfigurable I/Q Gilbert mixer. The proposed design is developed using SiGe 8HP process technology. Different filters have been included within the

circuitry where the 9^{th}-order tunable LC filters present at the RF and IF ports are responsible for maintaining excellent port matching and NF improvement. Likewise, 1^{st}-order tunable filter is accountable for leakage avoidance via the power supply. The employment of G_m-boosting technique helped in maintaining good transconductance within the circuitry. Additionally, the peaking inductors help compensate for the gain reduction at high frequencies while extending the overall bandwidth, resulting in high gain. The simulation results depict that the design achieves a good CG, an excellent NF, and a reasonable IRR. However, IIP3, area, and power dissipation are the limitations of the current design. Thus, another mixer is proposed in the next chapter that overcomes the problem of power consumption while maintaining a good CG and low NF.

Chapter 4

Design and Analysis of a Double Balanced Mixer for Software Defined Radios

4.1 Introduction

Gilbert mixers are commonly used among SDR receivers due to their ability to provide high performance, broadband operation, and large band covering capability [184, 216, 134, 217, 80, 218, 97, 114, 11, 8, 150, 176], these mixers are not convenient for higher frequency bands due to the presence of parasitic capacitance at different nodes that behaves like a low-pass filter (LPF) [197]. Thus, the best solution to this problem is to push the cut-off frequency of LPF to the higher frequency that results in low CG and high NF [219]. Besides, this design also consumes high power due to the requirement of a large number of transistors. To overcome these issues, the folding structure can be used. This structure requires fewer transistors, but consumes high power due to the partial sharing of bias current between RF and LO stages. Additionally, different techniques have to be employed to enhance the mixer's performance, according to the design requirements, which makes the design more complex. Thus, employing a current bleeding technique within a mixer is the best option to enhance the CG and NF performance [220].

Several mixers have been reported based on this approach in [221, 133, 138, 222, 114, 174,

223, 224] that utilized current bleeding and inductive degeneration techniques. The inductive degeneration is responsible for lowering the flicker noise, hence enhancing the IIP3 and NF. The employment of current bleeding results in high CG. Similarly, in [220], a double-balanced mixer is proposed that employs current-bleeding, forward-body bias and inductive gate bias approaches. The overall performance shows that the design achieves high CG port isolation at the expense of IIP3.

Based on the literature study, it has been found that to attain low NF; the current bleeding approach must be employed. Besides, to enhance the g_m, the inductors can be employed at the gate of the current bleeding transistors. Additionally, a current mirror technique can be useful for controlling the current within the circuitry. Thus, as per the above-discussed approaches, a double-balanced current bleeding mixer is proposed in this Chapter [185, 198]. This mixer also contains an inductor at the gate that resonates with the parasitic capacitance. The overall performance shows that the design attains high CG and low NF while maintaining a small chip area. Besides, the proposed design consumes low power, and the overall current of the mixer is controlled using the current mirror technique.

4.2 Proposed Mixer

Figure 4.1 depicts the proposed mixer circuitry. The complete design is divided into four different sections. The current mirror section controls the current flow within the mixer circuitry. The mixer section is responsible for the downconversion operation. The current bleeding and filter sections enhance the overall performance of the circuit by introducing the external current and impedance matching within the design. The detailed analysis of the different sections is discussed as follows.

4.2.1 Current Mirror

In general, current mirror circuits contain two main transistors. These circuits can mirror the current flowing from one transistor to another transistor within the circuitry. The mirrored current

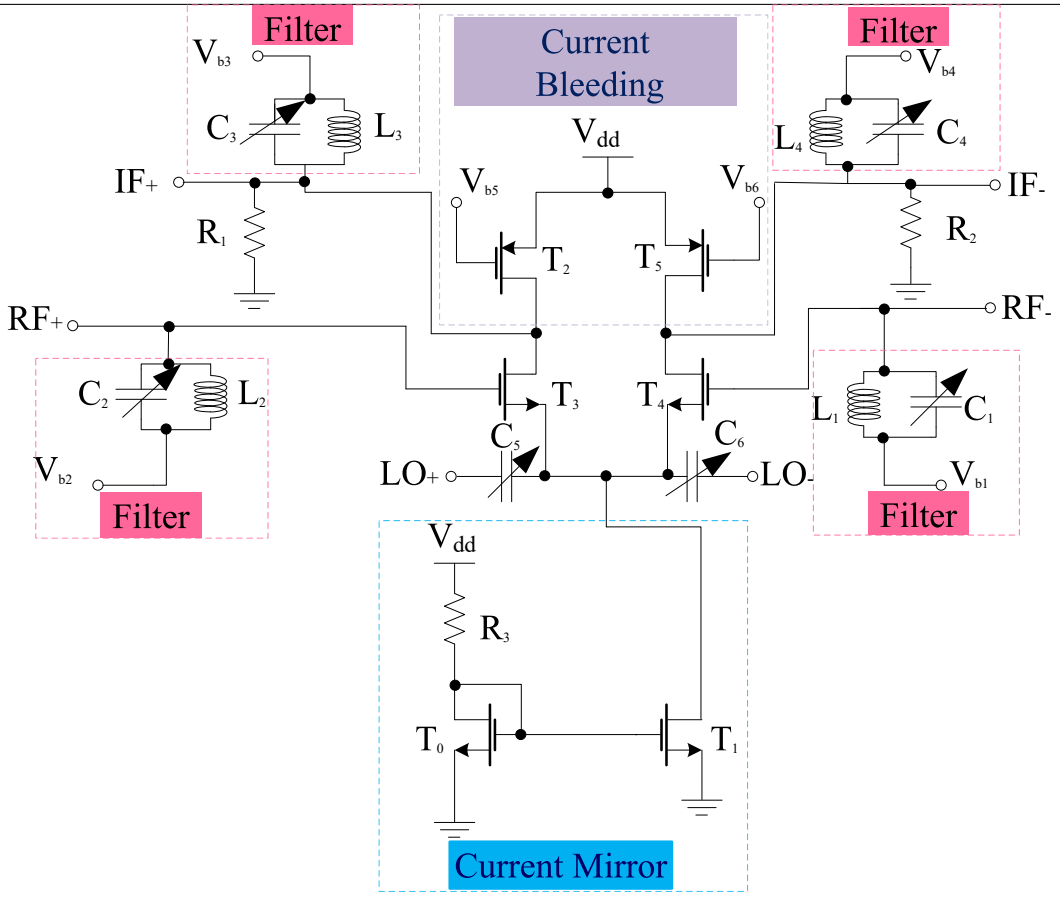


Figure 4.1: Proposed Mixer

can be constant or vary depending on actual circuit requirements [225, 226]. The proposed mixer uses a current mirror circuit with three transistors (T_0, T_1 and T_6), where transistors T_0 and T_1 operate in the saturation region and T_6 acts as resistor. For T_1 to operate in saturation condition, the output voltage should be higher than the saturation voltage. T_1 will remain in this operating region until the saturation voltage is lower than the output voltage. Therefore, the input current flowing through the transistor, T_0 can control the current that flows through the transistor, T_1. As the current flowing via the gate of the transistors, T_0 and T_1 is zero, the input current must flow within the drain of the transistor, T_0 [227]. Let I_P denote the current flowing through T_0 developed using T_6, which can be expressed as [139, 120]

$$I_R = K_{n0}(V_{GS0} - V_{TN0})^2 = K_{n6}(V_{GS6} - V_{TN6})^2 \tag{4.1}$$

When T_6 and T_0 are identical, then

$$V_{GS0} = \frac{\sqrt{\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_0}}}{1+\sqrt{\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_0}}}.(V_{dd}) + \frac{1-\sqrt{\frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_6}}}{1+\sqrt{\frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_6}}}.V_{TN} = V_{GS1} \tag{4.2}$$

Hence, the load current, I_L can be expressed as

$$I_L = I_{D1} = \left(\frac{W_1}{L_5}\right)(\frac{1}{2}\mu_n C_{ox})(V_{GS1} - V_{TN})^2 \tag{4.3}$$

Hence, the current mirror circuit has flexibility as the width to length (W / L) ratio can be decided as per the requirement [185, 198, 197]. Figure 4.2 depicts the small signal model for the half current mirror circuit. By applying KCL to the half current mirror circuit by considering

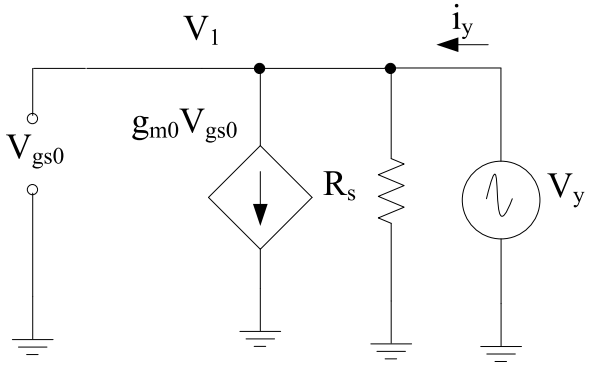


Figure 4.2: Small signal model for half current mirror circuit

only the transistor T_0, we get

$$i_x = \frac{V_x}{R_s} + gm_{m0}V_x \tag{4.4}$$

$$\frac{V_x}{i_x} = R_s||\frac{1}{g_{m0}} \approx \frac{1}{g_{m0}} \tag{4.5}$$

where $R_s = r_{ds0} \parallel r_{06}$ As per equation (5), the complete small signal model can be drawn including parasitic capacitances as shown in Figure 4.3. The voltage V_1 can be expressed as

$$V_1 = i_1(\frac{1}{g_{m0} + sC_A + sC_B}) \tag{4.6}$$

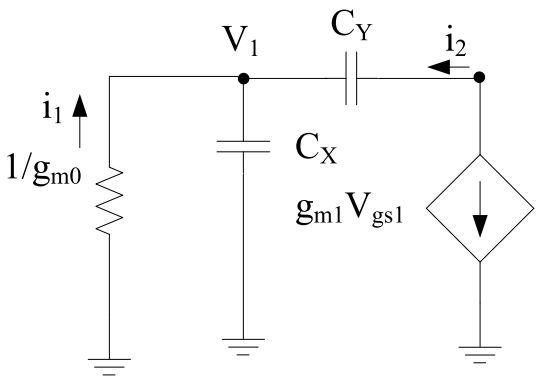


Figure 4.3: Complete small signal model for current mirror circuit

where C_X= C_{gs0}+C_{gs1}+C_{db0}+C_{gs6} , C_Y=C_{gd1}. Likewise,

$$i_2 = g_{m1} - V_1 s C_B \tag{4.7}$$

By substituting V_1 into equation (4.6), we obtain the transfer function, A_I as

$$A_I = \frac{i_2}{i_1} = \frac{g_{m1} - sC_B}{g_{m0} + sC_X + sC_Y} \tag{4.8}$$

4.2.2 Mixer Design

The proposed double balanced mixer design consists of two NFETs (T_3,T_4), each acting as an individual mixer. The mixer uses a common source configuration. The structure is modelled in such a way that RF inputs are provided through the gate terminals of (T_3,T_4), and LO signals are imparted via the source terminals for high RF-LO isolation. IF+/IF- are the outputs that can be obtained with respect to the drain terminals of these transistors [185]. Resistors, R_1 and R_2 are the load resistors being connected at the output terminals [185, 198]. RF and IF stages also employ first-order filters for impedance matching purposes, as discussed in detail in the filter section. Besides, the design also employs current bleeding circuitry acting like a load for the main transistors as discussed in the current bleeding stage [185].

4.2.3 Current Bleeding

The current bleeding technique is generally used to improve the overall performance of a mixer [51, 228, 229, 230]. It is possible to achieve high IIP3 and CG if a large current passes through the RF stage but at the expense of power consumption. Besides, a large current flow within the core stage may lead to a voltage headroom problem in the presence of resistive loads. Additionally, the high current flow within the core stage desires a large LO drive voltage which cannot be attained at higher LO frequencies.

In addition to this, to determine the performance of NF, flicker noise must be considered [185]. Flicker noise can be direct or indirect, where the direct flicker noise is due to the current flow within the LO, while the indirect flicker noise is due to the parasitic capacitance at the LO transistor source terminal. The indirect flicker noise is lower than the direct flicker noise. Therefore, the direct flicker noise must be lowered. Several techniques have been proposed, among which the most widely used approaches are static and dynamic current bleeding [180, 231, 185, 198]. The static current bleeding approach is commonly used to reduce the current of the LO switching stage, resulting in low flicker noise and high load resistance. This will enhance the overall CG. However, direct flicker noise still affects the CG. Besides, dynamic current bleeding is more beneficial in comparison to the static current bleeding approach, as it employs a PFET that provides low flicker noise. However, there is still a current flow that affects the load resistor, and hence the CG performance [185, 180, 231].

Gilbert mixer is the most commonly used topology. With the current bleeding technique, the load resistance will enhance the CG. The main contributor of flicker noise within this mixer is the core stage, as the noise contributed from the RF stage is transferred to the core stage. In [221, 185], Gilbert mixer has been discussed with the current bleeding inductive degeneration approach. This lowers the design core stage current and flicker noise. Furthermore, the load resistance will improve the performance of CG and NF.

Based on the above discussed techniques, a new current bleeding technique is proposed using PFETs, (T_2,T_5) respectively [185]. The employment of current bleeding transistors will enhance the current within the mixer in such a way that (T_3, T_4) operates in the saturation region. These

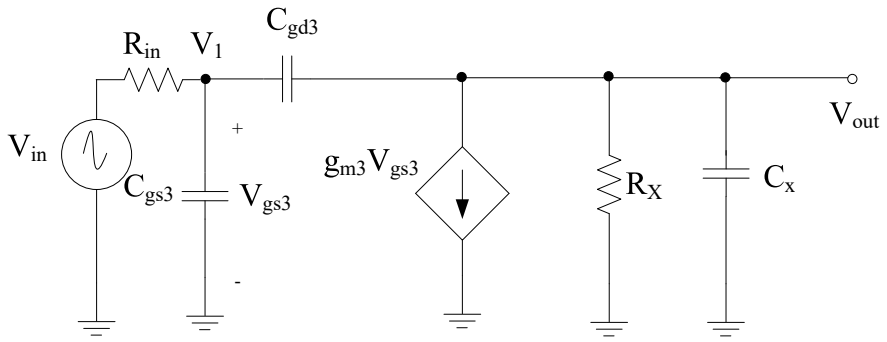


Figure 4.4: Small signal model for mixer and current bleeding stage

transistors will bleed the current in the two single mixers as such transistors provide low flicker noise. This is possible by connecting the drain terminals of these transistors to the source of the mixer transistors (T_3, T_4), instead of the gate terminals that form a cross-coupled structure [185]. This allows the drain current to enter the IF ports, leading to a high current within the mixer, especially in the RF ports [185]. The rise in current at RF ports will improve the transconductance and hence the overall CG. Additionally, the overall NF will improve with an improvement in CG. The voltage headroom problem also resolves with the current bleeding approach [185]. For better understanding, we propose a small signal model that consists of a mixer and a current bleeding stage only, as shown in Figure 4.4. On the basis of the small signal model, the input impedance of the RF + stage

$$Z_{\text{in+}} = \infty \tag{4.9}$$

The output impedance for the RF+ stage can be expressed as

$$Z_{\text{out+}} = R_{\text{x}} = R_1||r_{02}||r_{03} \tag{4.10}$$

Besides, C_x=C_{ds2}+ C_{ds3}. Thus, to obtain the frequency response of the small signal circuit, nodal analysis can be performed [199, 197, 41].

$$V_1(G_{\text{in}} + sC_{\text{gs3}} + sC_{\text{gd3}}) - V_{\text{in}}G_{\text{in}} - V_{\text{out}}sC_{\text{gd3}} = 0 \tag{4.11}$$

$$V_{\text{out}}(G_{\text{x}} + sC_{\text{x}} + sC_{\text{gd3}}) - V_1 sC_{\text{gd3}} + g_{\text{m3}}V_{\text{gs3}} = 0 \tag{4.12}$$

As $V_1 = V_{\text{gs3}}$, then from equation(4.12), we get;

$$V_1 = \frac{V_{\text{out}}(G_{\text{x}} + sC_{\text{x}} + sC_{\text{gd3}})}{-g_{\text{m3}} + sC_{\text{gd3}}} \tag{4.13}$$

By substituting (4.13) into (4.11), we obtain

$$\begin{aligned} &V_{\text{out}}[G_{\text{x}}G_{\text{in}} + s[G_{\text{x}}(C_{\text{gs3}} + C_{\text{gd3}}) + G_{\text{in}}(C_{\text{gd3}} + C_{\text{x}}) + g_{\text{m3}}C_{\text{gd3}}] + \\ &s^2[(C_{\text{gs3}} + C_{\text{gd3}})(C_{\text{x}} + C_{\text{gd3}}) - C^2{}_{\text{gd3}}]] = -V_{\text{in}}G_{\text{in}}(g_{\text{m3}} - sC_{\text{gd3}}) \end{aligned} \tag{4.14}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_{\text{m3}}(1 - s\frac{C_{\text{gd3}}}{g_{\text{m3}}})R_{\text{x}}}{1 + sa + s^2 b} \tag{4.15}$$

$$a = R_{\text{x}}(C_{\text{gd3}} + C_{\text{x}}) + R_{\text{in}}[C_{\text{gd3}}(1 + g_{\text{m3}}R_{\text{x}}) + C_{\text{gs3}}] \tag{4.16}$$

Upon simplification and converting G_x, G_{in} to R_x, R_{in}, we get;

$$b = R_{\text{in}}R_{\text{x}}(C_{\text{gd3}}C_{\text{gs3}} + C_{\text{gs3}}C_{\text{x}} + C_{\text{gd3}}C_{\text{x}}) \tag{4.17}$$

If s=0, the low frequency gain will be

$$A_{\text{v}} = -g_{\text{m3}}R_{\text{x}} \tag{4.18}$$

When the poles are real in equation (4.15) and

$$w_{\text{p1}} << w_{\text{p2}} \tag{4.19}$$

The denominator of equation (4.15) is expressed as

$$D(s) = (1 + \frac{s}{w_{\text{p1}}})(1 + \frac{s}{w_{\text{p2}}}) = 1 + \frac{s}{w_{\text{p1}}} + \frac{s^2}{w_{\text{p1}}w_{\text{p2}}} \tag{4.20}$$

Upon comparison of equation (4.15) with equation (4.20), we obtain

$$w_{\mathrm{p1}} = \frac{1}{a} \tag{4.21}$$

$$w_{\mathrm{p2}} = \frac{1}{bw_{\mathrm{p1}}} \tag{4.22}$$

Likewise, the gain can be obtained for the RF stage as well, which can be expressed as:

$$A_{\mathrm{v}} = -g_{\mathrm{m4}}R_{\mathrm{y}} \tag{4.23}$$

Furthermore, the transistor T_2 also includes the g_m-boosting inductor L_{16} that is responsible for the present gain improvement. Based on the design, the analysis is discussed according to the positive feedback theory [197]. Based on the design principle, the signal paths for T_2 must be considered. Besides, the output impedance must be ignored for simplicity. Therefore, due to the presence of L_{16} or L_{17} a non-zero impedance must be observed at the gate terminal of T_2. Additionally, the feedforward and feedback paths must be considered using parasitic capacitances. Therefore, the gate source voltage of T_2 is represented as $V_{\mathrm{g,T2}}$ when considering new signal paths [197]. Then, the open-loop voltage gain has to be analyzed depending on the voltage-voltage feedback configuration. Thus, the voltage at the drain terminal is expressed as [197]

$$V_{\mathrm{nP}} = -g_{\mathrm{m2}}V_{\mathrm{gs2}}Z_{\mathrm{nP}} = g_{\mathrm{m2}}(V_{\mathrm{nQ}} - \alpha V_{\mathrm{nQ}})Z_{\mathrm{nP}} \tag{4.24}$$

where V_{gs2}, g_{m2} and Z_{nP} refers to the gate-to-source voltage of T_2, transconductance of T_2 and output impedance at node nQ including duplicate, respectively. where [197]

$$Z_{\mathrm{nP}} = Z^{'}{}_{\mathrm{nP}} || (sL_{16} + \frac{1}{sC_{\mathrm{gd2}}}) \tag{4.25}$$

$$Z^{'}{}_{\mathrm{nP}} = \frac{1}{sC_{\mathrm{gd9}}} || \frac{1}{sC_{\mathrm{gd8}}} || (\frac{1}{g_{\mathrm{mLOI}} + g_{\mathrm{mLOQ}}}) \tag{4.26}$$

where $Z^{'}{}_{\mathrm{nB}}$, α, C_{gd9} and C_{gd8} refer to the output impedance excluding duplicate, the voltage ratio

from source to gate, parasitic capacitances for T_8 and T_9, respectively [197]. Thus, the open-loop gain is represented as [197]

$$A_0 = (1-\alpha) g_{m9} Z_{nB} \tag{4.27}$$

where

$$\alpha = \frac{sL_3 || \frac{1}{sC_{gd9}} || \frac{1}{sC_{gd8}}}{(\frac{1}{sC_{gs9}} || \frac{1}{sC_{gd10}}) + sL_3 || \frac{1}{sC_{gd9}}} \tag{4.28}$$

Finally, the voltage gain (A_{V0}) without the feedback inductor and the closed-loop voltage gain (A_{Vf}) can be expressed as [197]

$$A_{v0} = \frac{V_{nB}}{V_{nA}}|_{(w/o)L_3} = g_{m9} Z_{nB}|_{(w/o)L_3} \tag{4.29}$$

$$A_{vf} = \frac{V_{nB}}{V_{nA}}|_{(w)L_3} = \frac{A_0}{1+\beta A_0} \tag{4.30}$$

where

$$Z_{nB}|_{(w/o)L_3} = Z^{'}{}_{nB} || \frac{1}{sC_{gd9}} \tag{4.31}$$

$$\beta = \frac{sL_3}{(\frac{1}{sC_{gd9}} || \frac{1}{sC_{gd9)}} + sL_3} \tag{4.32}$$

where β is the feedback factor from drain to gate Hence, it has been verified from the above equations that the gain has been boosted in the presence of the inductor [197, 185, 232].

4.2.4 Filter

In general, the main role of filters is to match the impedance of the input and output stages at the desired frequencies within a band. Transmission lines and transformer-based programmable spiral inductors are commonly used. These filters cover a large chip size and operate within a limited band. An alternative is to use off-chip filters. However, these filters show difficult integration within a circuit. Therefore, the best way is to develop a small on-chip filter. We use a 4^{th}-order filter with passive components, i.e., varactor and inductor. The order of the filter depends on the number of LC pairs. The impedance of the filter depends on the parallel

combination of L and C. Thus, the input impedance is expressed as [197]

$$Z_{\text{in}} = [(sL_4||\frac{1}{sC_4}) + (sL_5||\frac{1}{sC_6}||sL_7)]||(\frac{1}{sC_5}||sL_6) \tag{4.33}$$

The output impedance of the filter circuit is given by

$$Z_{\text{out}} = \frac{1}{sC_5}||sL_6 \tag{4.34}$$

4.3 Performance Analysis

This section is aimed to assess the mixer performance in terms of conversion gain and noise figure.

4.3.1 Conversion Gain

Figure 4.5 depicts the small-signal model for the proposed mixer circuit. The current bleeding and current mirror terms are simply represented as resistors (r_{01}, r_{02}), respectively. Besides, the inductor present at the input to the transistor, T_2 is ignored for simplicity. Therefore, the circuit behaves like a common source amplifier that degenerates from the source.

Based on the circuit, the controlled current source determines the current through r_{01} and V_1 can be expressed as:

$$V_1 = (g_{m3}V_{gs3})r_{01} = g_{m3}r_{01}(V_{\text{in}} - V_1) \tag{4.35}$$

$$V_1(1 + g_{m3}r_{01}) = g_{m3}r_{01}V_{\text{in}} \tag{4.36}$$

$$A_1 = \frac{V_1}{V_{\text{in}}} = \frac{g_{m3}r_{01}}{1 + g_{m3}r_{01}} \tag{4.37}$$

Once V_1 is obtained, the output voltage can be expressed as

$$V_{\text{out}} = -R_D(g_{m3}V_{gs3}) = -g_{m3}R_D(V_{\text{in}} - V_1) \tag{4.38}$$

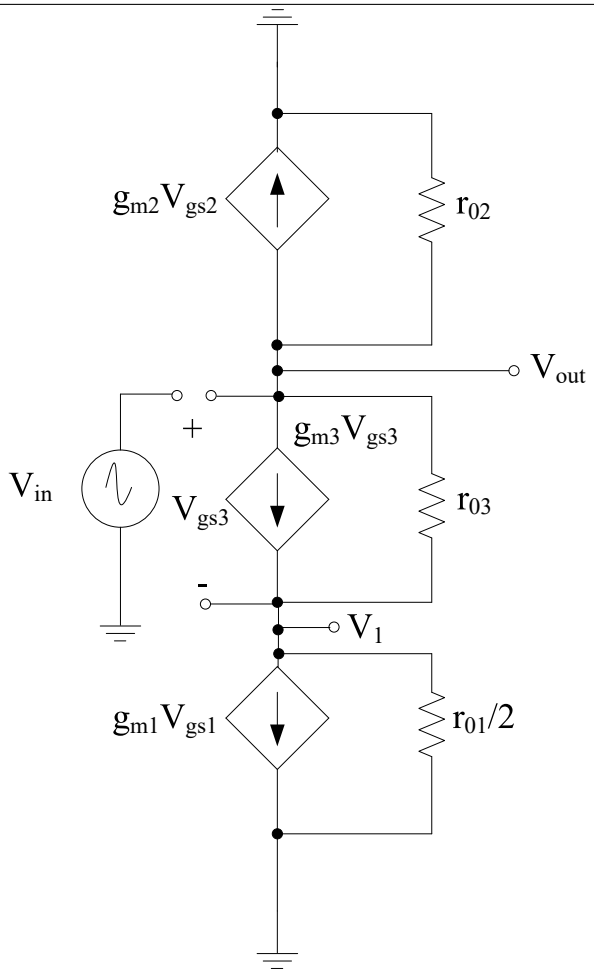


Figure 4.5: Complete small signal model for circuit

where $R_D = R_1 \parallel r_{02}$. Substituting V_1 from (4.31) into (4.32), we get

$$V_{out} = -\frac{g_{m3}R_D}{1 + g_{m3}r_{01}}V_{in} \tag{4.39}$$

$$A_0 = \frac{V_{out}}{V_{in}} = -\frac{g_{m3}R_D}{1 + g_{m3}r_{01}} \tag{4.40}$$

To examine the impact of parasitic capacitors present in C_{gd3} and C_{gs3}, Miller's theorem can be used, which relates the equivalent capacitance to the gain between the nodes to which the capacitor is tied to. Assuming C_{in}, C_1 and C_0 are present at the gate, source and drain terminals of the transistor, T_3. Thus, these capacitance's can be expressed by Miller's theorem as

$$C_{in} = C_{gs3}(1 - A_1) + C_{gd3}(1 - A_0) \tag{4.41}$$

$$C_0 = C_{\text{gd3}}(1 - \frac{1}{A_0}) \tag{4.42}$$

$$C_1 = C_{\text{gs3}}(1 - \frac{1}{A_1}) \tag{4.43}$$

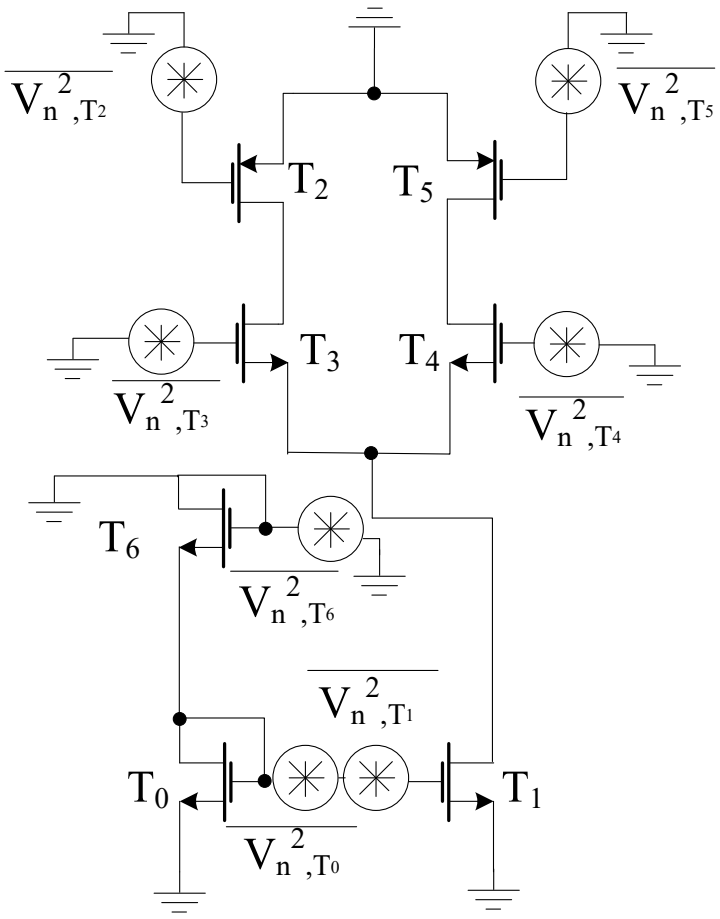


Figure 4.6: Noise model for proposed mixer

4.3.2 Noise Figure

Figure 4.6 shows the complete noise model for the proposed mixer. Within the circuit, all passive components are assumed to be ideal. As thermal noise is the key noise source, the power spectral density of each stage is obtained based on this source [205, 197]. Hence, the proposed design only consists of resistors and transistors, respectively.

Equation (4.44) refers to the overall power spectral density of the proposed mixer, which is the combination of the power spectral density obtained from all stages present within the design

[232, 197].

$$\overline{V^2{}_{\mathrm{n}}} = \overline{V^2{}_{\mathrm{n,CM}}} + \overline{V^2{}_{\mathrm{n,CB}}} + \overline{V^2{}_{\mathrm{n,M}}} + \overline{V^2{}_{\mathrm{n,L}}} \tag{4.44}$$

The power spectral density for all stages is obtained based on the resistors and transistors present within each stage [197]. The power spectral density of the current mirror stage is expressed as [197]

$$\overline{V^2{}_{\mathrm{n,CM}}} = \overline{V^2{}_{\mathrm{n,R_3}}} + \overline{V^2{}_{\mathrm{n,T_0}}} + \overline{V^2{}_{\mathrm{n,T_1}}} = \frac{4kT\gamma}{g_{\mathrm{m0}}} + 4kTR_3 + \frac{4kT\gamma}{g_{\mathrm{m1}}} \tag{4.45}$$

Likewise, the power spectral density of the mixer section is given by [197]

$$\overline{V^2{}_{\mathrm{n,M}}} = \overline{V^2{}_{\mathrm{n,T_3}}} + \overline{V^2{}_{\mathrm{n,T_4}}} = \frac{4kT\gamma}{g_{\mathrm{m3}}} + \frac{4kT\gamma}{g_{\mathrm{m4}}} \tag{4.46}$$

Similarly, the power spectral density of the current bleeding section is represented as [197]

$$\overline{V^2{}_{\mathrm{n,CB}}} = \overline{V^2{}_{\mathrm{n,T_2}}} + \overline{V^2{}_{\mathrm{n,T_5}}} = \frac{4kT\gamma}{g_{\mathrm{m2}}} + \frac{4kT\gamma}{g_{\mathrm{m5}}} \tag{4.47}$$

Finally, the power spectral density of the load section is defined as [197]

$$\overline{V^2{}_{\mathrm{n,L}}} = \overline{V^2{}_{\mathrm{n,R_1}}} + \overline{V^2{}_{\mathrm{n,R_2}}} = 4kTR_1 + 4kTR_2 \tag{4.48}$$

Therefore, the noise figure of the proposed mixer is given by

$$NF = 1 + \frac{\overline{V^2{}_{\mathrm{n}}}}{A_{\mathrm{v}}{}^2} \tag{4.49}$$

where $A_{\mathrm{v}}{}^2$, $\overline{V^2{}_{\mathrm{n}}}$ refers to the overall gain obtained within the previous section, overall power spectral density as per equation (4.44) [232, 197].

4.4 Results and Discussion

The proposed double-balanced mixer is designed and simulated in the SiGe 8HP CMOS process technology. To boost the overall performance of the design, current bleeding and current mirror

Table 4.1: Performance Comparison

Ref	Freq(GHz)	PT(μm)	CG (dB)	NF(dB)	IIP3(dBm)	S_{11}(dB)	P_{diss}(mW)
This work	1.8-5	8HP	13.13-19.26	1.15-1.87	-5.88	>-10	10
[198]	1.8-5	8HP	12.9-18.32	1.19-1.89	-5.89	>-10	10
[233]	1.8-5	HEMT	5-10	<2	28	Nil	Nil
[167]	5.1	0.09	16	8.39	-1.93	Nil	8.19
[74]	3.43	0.18	8.05	11.3-15	-10.8	-22.9	Nil
[234]	2.4	0.18	15.7	10.7	-9	Nil	18
[51]	3.5	0.15	5.1	11.6	1.5	Nil	39.6
[235]	3.1-4.8	0.35	12-13.5	<8.8	>0	>-4	18
[3]	2.4	0.13	7.5	15	1	Nil	0.572
[186]	2.4/5.2	0.18	16.1/13.07	27.2/30.3	-3.1/-2.8	Nil	0.93
[236]	0.86-0.87	0.13	17	7.5	-4.1	-19.5	6
[85]	2.4	0.11	19	14.2	-7	Nil	3
[116]	1-10.5	0.65	14.5	6.5	15	-30	14.4

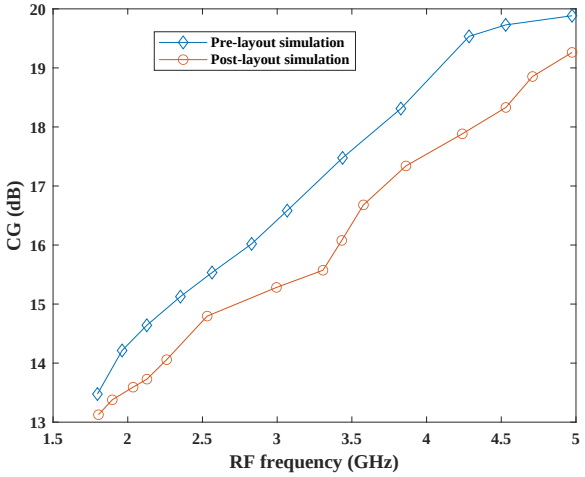


Figure 4.7: Simulated CG over RF input frequency

techniques are employed, resulting in high CG, low NF at the expense of linearity. The pre/post-layout simulation results for CG of the proposed double-balanced mixer are shown in Figure 4.7. The pre-and post-layout curves show the variation in CG, which is ± 0.5 dB due to the imperfect resonance of the parasitic components with the parasitic effect and current leakage.

In general, the quality factor of the inductor, Q affects the design performance. Figure 4.8 depicts the NF of the proposed mixer. As per the simulation results, NF is less than 2 dB within the entire band. The post-layout results show degradation in the results due to the parasitic effect of passive components as it affected the CG. Figure 4.9 shows the input return loss of the circuit.

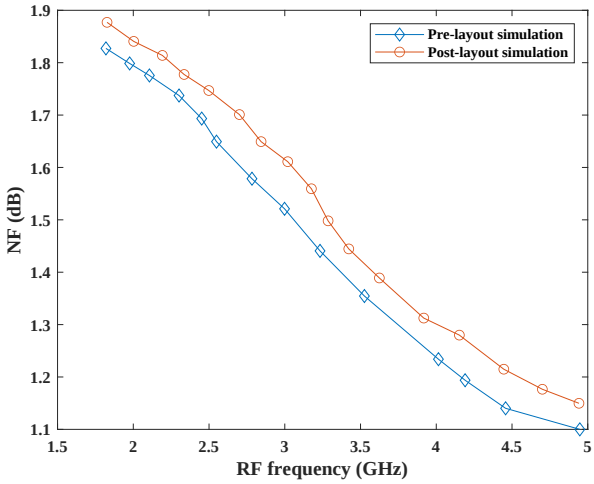


Figure 4.8: Simulated NF over RF input frequency

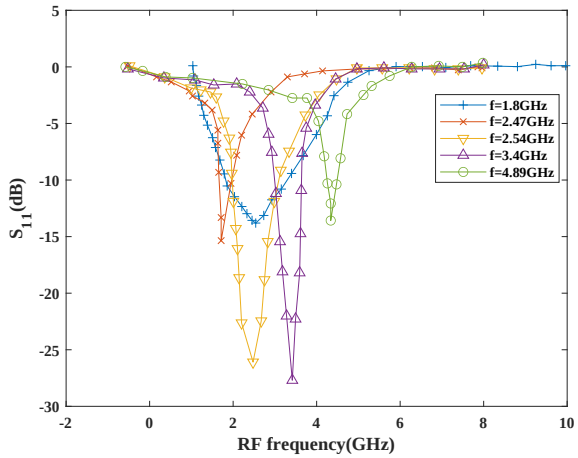


Figure 4.9: Simulated S_{11} over RF input frequency

Upon observation, it has been found that $|S_{11}|$ <-10 dB within the entire band of operation. Linearity of the mixer is represented in terms of IIP3 as shown in Figure 4.10, respectively. The difference in pre-and post-layout results is depicted in the curves. As per the curves, the mixer shows nonlinear behaviour. Besides, the post-layout simulated IIP3 results are depicted in Figure 4.11.

Figure 4.12 shows the mixer layout with a die size of 1.2 mm^2 including the pads and guard ring. The layout contains 48 pads, among which 14 pads are used to show power supply, biasing voltages and various input and output ports. The proposed mixer is modelled in SiGe 8HP process technology. As per the design, there are four pairs of on-chip spiral inductors. These

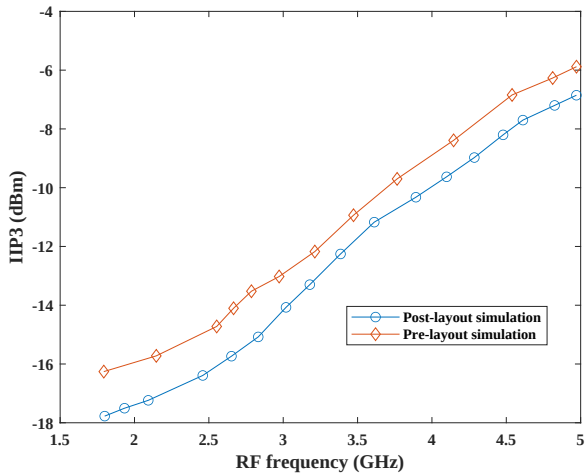


Figure 4.10: Simulated IIP3

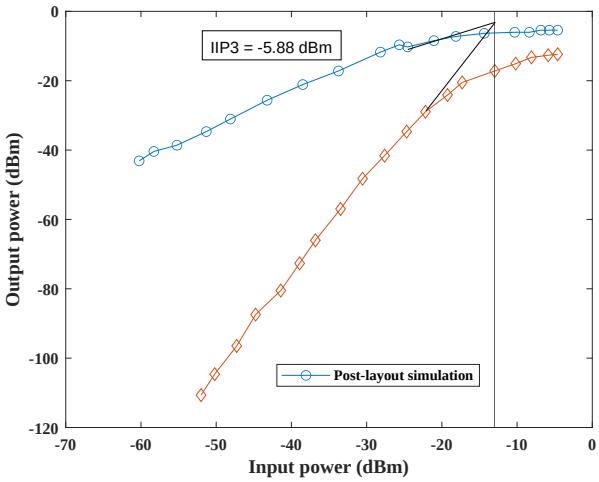


Figure 4.11: Post-layout IIP3 results

inductors are highly accurate, have high Q at the desired band. Table 4.1 summarizes the proposed mixer's performance compared to recent mixer designs that maintain small chip area, attains high CG and low NF. It is noted that they follow different mixer topologies. Additionally, the proposed mixer shows the best performance in terms of NF compared to the other works. The proposed mixer shows attractive performance in terms of CG and return loss. Besides, it also covers a small chip area while consuming low power, which makes it well suited for software-defined radios.

To further improve the performance of the proposed mixer, PSO has been implemented on the mixer as discussed in Chapter 7, Section 7.7.2. The optimized results are obtained and compared

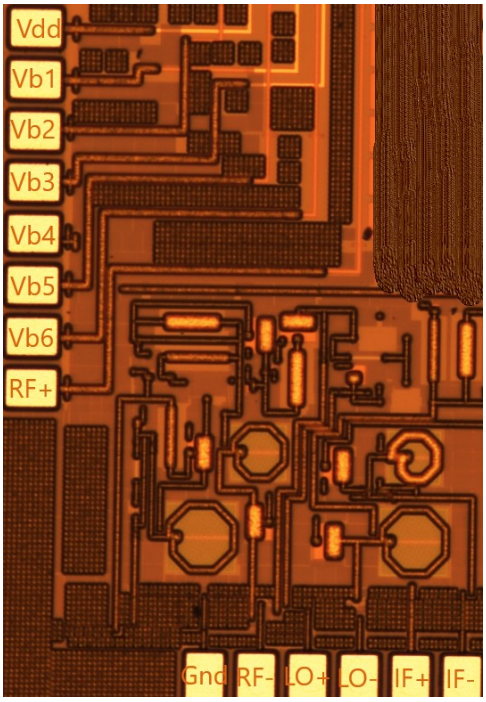


Figure 4.12: Layout of the proposed mixer

with the simulated results. Based on the observation, it has been found that performance of the proposed mixer has significantly improved.

4.5 Summary

In this Chapter, a novel double-balanced mixer design suitable for software-defined radio has been demonstrated, which features an improved conversion gain and noise figure. Current bleeding along with the current mirror technique is employed as an effective technique to lower the signal leakage and improve the overall conversion gain. The noise figure has been improved by tuning with the external capacitance at the RF and the IF port of the mixer. Additionally, the proposed design achieved low power dissipation and covered a small chip area at the expense of linearity. Thus, to improve the linearity performance, another reconfigurable mixer is proposed by making use of active inductors in the next Chapter.

Chapter 5

Design and Analysis of a High Linearity Mixer for Software Defined Radios

5.1 Introduction

As per the literature, a limited number of SDR mixers are available till date, which shows high performance and good reconfigurability. Besides, it is desirable for the designers to opt for the appropriate CMOS technology process while keeping in mind the desired specifications to attain the desired outcomes. Since the last decade, the scaling up of CMOS technology has played a significant role in the electronics industry, leading to rapid integration. Nowadays, transistors are 20 times faster and consume around 1% area of those transistors constructed 20 years ago [237]. Emerging CMOS technologies have shown a reduction in the power supply voltage due to the rapid scaling process. The technology scaling process has demonstrated significant improvement in the noise performance of RF receivers. Besides, this has also enhanced the cut-off frequency (f_T) of the transistors. Nevertheless, the linearity and intrinsic DC gain performance have been degraded. Therefore, it is crucial to use linearization approaches to comprehend the high linearity receivers [238]. Many different approaches have been presented in the literature, significantly to enhance the linearity performance within the mixer. One of the most popular techniques is resistive degeneration. Yet, due to the presence of a degenerated resistor, the NF performance is

degraded, and the power consumption is increased as the overall transconductance is lowered [239]. Another linearity enhancement technique is derivative superposition, which employs an auxiliary transistor [80, 240]. The main aim of employing the auxiliary transistor (biased in the weak inversion region) is to suppress the $g_m{}''$ of the main transistor. In [241], inductors are included within the switching stage to enhance the linearity and NF performance. Besides, the design uses the PMOS switching stage to improve the overall flicker noise performance compared to the conventional Gilbert cell mixer. Finally, in [123], a novel mixer circuitry is proposed based on the conventional Gilbert mixer, which employs a differential active inductor (DAI) circuit, cross-coupled current injection technique, and cross-coupled current bleeding techniques for improving the flicker noise and conversion gain performance of the mixer. The active inductor circuitry resonates with the parasitic components. Hence lowers the leakage current containing harmonic components and generates flicker noise.

Based on the above-discussed approaches, a novel double-balanced mixer is proposed. The current mirror and DAI circuits are adopted to achieve the mixer's high performance. The improved folded DAI circuit is employed instead of the passive inductors for perfect tuning of the parasitic capacitance, leading to enhanced NF performance. Besides, a triple transistor current mirror circuit is used instead of a conventional current mirror circuit for current controlling purposes. The proposed mixer design attained excellent IIP3, high CG, reasonable NF while covering a small area.

5.2 Proposed Mixer

Figure 5.1 proposed mixer is divided into the current mirror, mixer, and active inductor sections, respectively.

5.2.1 Current mirror

Current mirror circuits are composed of two main transistors, which can mirror the current flowing from one transistor to another. The copied current can be constant or varying depending

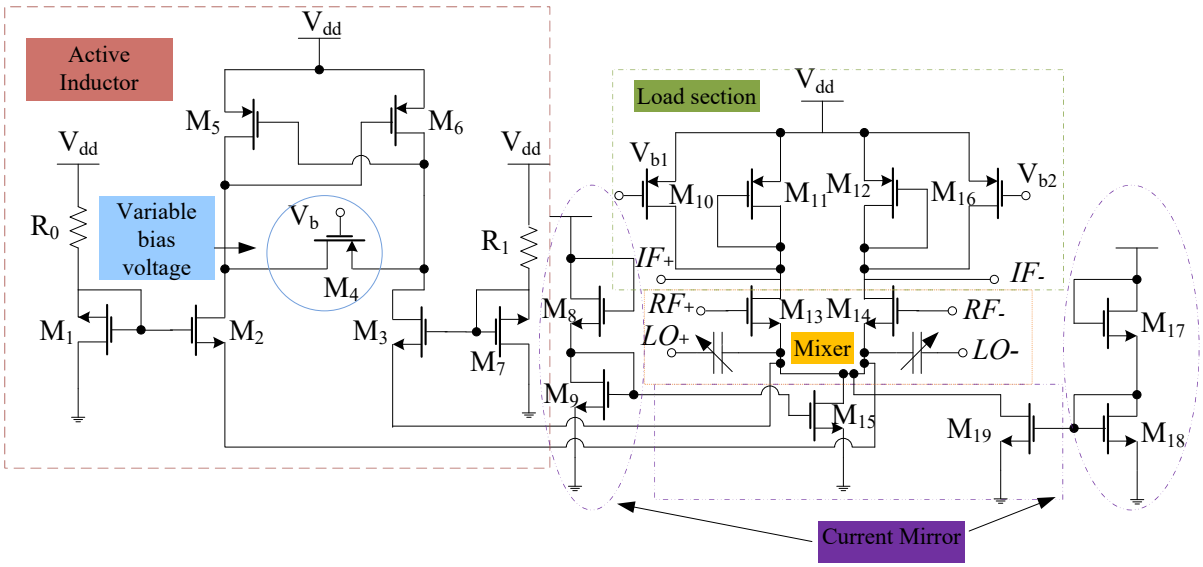


Figure 5.1: Mixer schematic

on the requirements of the circuit [227, 232]. Based on this technique, the proposed mixer uses a current mirror circuit that contains three transistors (M_8, M_9 and M_{15}), where M_8 functions as a resistor. The transistors (M_9 and M_{15}) are operating in the saturation region [197]. The transistor, M_{15} will remain in saturation until the output voltage is higher than the saturation voltage. Consequently, the input current flowing through the transistor, M_9 can control the current flowing through the transistor, M_{15}.Likewise, the effect for current mirror circuit containing transistors M_{17}-M_{19} can be determined. However, it is not shown due to symmetrical circuitry containing transistors, M_8, M_9 and M_{15}, respectively. To show the symmetry within the circuitry, M_{17}-M_{19} transistors are also included within the design. Based on the circuit, M_8 and M_9 are in series and let I_R denote the current flowing through M_9 developed using M_8, which can be expressed as

$$I_{\mathrm{R}} = K_{\mathrm{n9}}(V_{\mathrm{GS9}} - V_{\mathrm{TN9}})^2 = K_{\mathrm{n8}}(V_{\mathrm{GS8}} - V_{\mathrm{TN8}})^2 \tag{5.1}$$

If M_8 and M_9 are identical, then

$$V_{\mathrm{GS9}} = \sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}.(V_{\mathrm{GS8}}) + \left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}\right) V_{\mathrm{TN}} \tag{5.2}$$

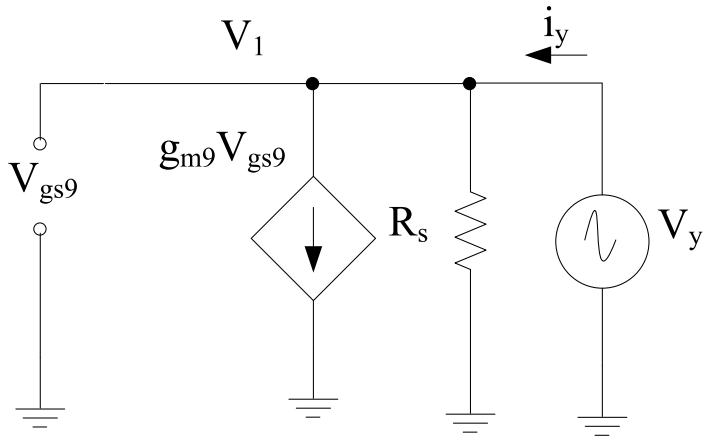


Figure 5.2: Small signal model for the half current mirror circuitry

Besides,

$$V_{\text{GS8}} + V_{\text{GS9}} = V_{\text{dd}} - 0 = V_{\text{dd}} \tag{5.3}$$

Thus,

$$V_{\text{GS9}} = \frac{\sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}}{1+\sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}}.(V_{\text{dd}}) + \frac{1-\sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}}{1+\sqrt{\frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_9}}}.V_{\text{TN}} = V_{\text{GS15}} \tag{5.4}$$

Finally, the load current, I_0 can be expressed as

$$I_0 = I_{\text{D15}} = \left(\frac{W_{15}}{L_{15}}\right)(\frac{1}{2}\mu_{\text{n}}C_{\text{ox}})(V_{\text{GS15}} - V_{\text{TN}})^2 \tag{5.5}$$

Thus, it is quite flexible to develop such current sources as the width-to-length (W/L) ratio can be decided as per the requirement. Figure 5.2 shows the small signal model for the half current mirror circuit. By applying Kirchoff's current law (KCL) to the half current mirror circuit and considering only the transistor M_9, we obtain

$$i_{\text{y}} = \frac{V_{\text{y}}}{R_{\text{s}}} + gm_{\text{m9}}V_{\text{y}} \tag{5.6}$$

where $R_s = r_{ds9} \parallel r_{08}$

$$\frac{V_{\text{y}}}{i_{\text{y}}} = R_{\text{s}}||\frac{1}{g_{\text{m9}}} \approx \frac{1}{g_{\text{m9}}} \tag{5.7}$$

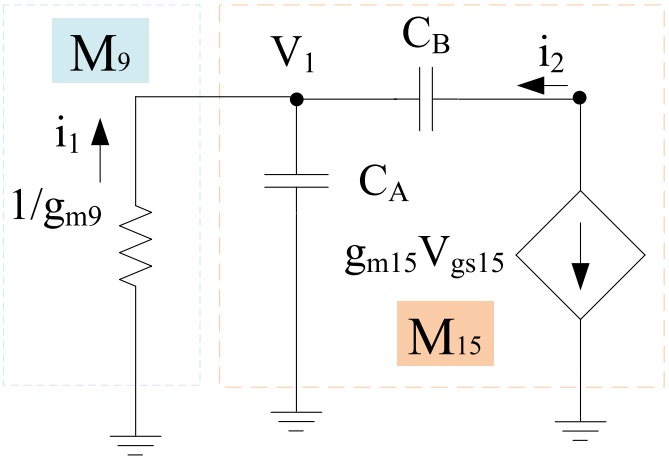


Figure 5.3: Complete small signal model for current mirror circuit

As per equation (5.7), the complete small signal model can be drawn including the parasitic capacitance as shown in Figure 5.3. As per the complete small-signal model shown in Figure 5.3, the voltage V_1 can be expressed as

$$V_1 = i_1\left(\frac{1}{g_{m9} + sC_A + sC_B}\right) \tag{5.8}$$

Where $C_A = C_{gs9}+C_{gs8}+C_{gs15}+C_{db9}$, $C_B = C_{gd15}$. Likewise,

$$i_2 = g_{m9} - V_1 sC_B \tag{5.9}$$

By substituting V_1 into equation (5.8), we obtain the transfer function, A_I which can be represented as

$$A_I = \frac{i_2}{i_1} = \frac{g_{m15} - sC_B}{g_{m9} + sC_A + sC_B} \tag{5.10}$$

5.2.2 Mixer

The proposed double-balanced mixer design consists of two n-type field-effect transistors (NFETs) (M_{13}, M_{14}), each acting as an individual mixer [232, 185]. The mixer uses a common source configuration. As per the design, RF inputs are provided through the gate terminals of transistors (M_{13}, M_{14}), and LO signals are imparted through the source terminals for high RF-LO

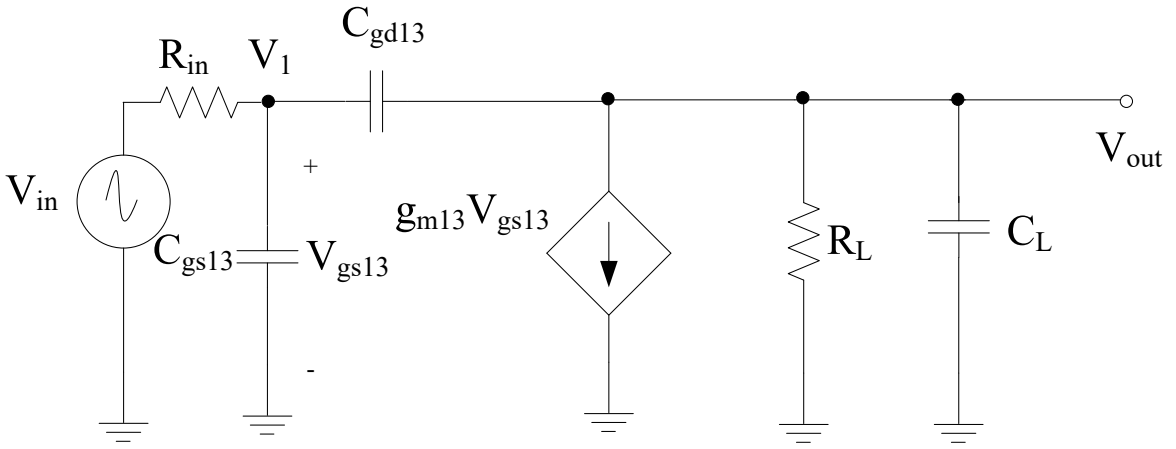


Figure 5.4: Small signal model for mixer and load stage

isolation. IF+/IF- are the outputs that can be obtained using drain terminals of these transistors. Due to the presence of two transistors, the design resembles a fully balanced [232, 185]. Besides, PFET diode loads (M_{11}, M_{12}) are employed within the design instead of load resistors because of the fabrication difficulties of resistors as they normally have tightly controlled values of physical size. Moreover, higher drain resistors are needed for high gain requirements, which shows the lower DC biasing voltage as required at the output port. This will have a high risk on transistor operating conditions, i.e., switching from saturation to triode region. Moreover, transistors M_{10} and M_{16} are used within the load stage to enhance the overall performance of the circuit [185]. To understand the behaviour of the mixer, a joint small signal model for the mixer and load stage is developed as shown in Figure 5.4. As per the model, the input and output impedance of RF+ and RF- stages can be obtained. Thus, the input impedance of the RF+ and RF- stage is expressed as

$$Z_{\text{in+}} = \infty \tag{5.11}$$

$$Z_{\text{in-}} = \infty \tag{5.12}$$

The output impedance of RF+ stage is expressed as

$$Z_{\text{out+}} = R_{\text{L}} = r_{013}||r_{010}||r_{011}||\frac{1}{g_{\text{m11}}} \tag{5.13}$$

Likewise, the output impedance of RF- stage

$$Z_{\text{out-}} = R_{\text{M}} = r_{014}||r_{016}||r_{012}||\frac{1}{g_{\text{m12}}} \tag{5.14}$$

As per the circuit, $C_L = C_{ds13} + C_{ds11} + C_{ds10}$. Thus, to obtain the frequency response of the small signal circuit, nodal analysis can be performed [199, 197].

$$V_1(G_{\text{in}} + sC_{\text{gs13}} + sC_{\text{gd13}}) - V_{\text{in}}G_{\text{in}} - V_{\text{out}}sC_{\text{gd13}} = 0 \tag{5.15}$$

$$V_{\text{out}}(G_{\text{L}} + sC_{\text{L}} + sC_{\text{gd13}}) - V_1 sC_{\text{gd13}} + g_{\text{m13}}V_{\text{gs13}} = 0 \tag{5.16}$$

As $V_1 = V_{gs13}$, then from equation (5.16), we get;

$$V_1 = \frac{V_{\text{out}}(G_{\text{L}} + sC_{\text{L}} + sC_{\text{gd13}})}{-g_{\text{m13}} + sC_{\text{gd13}}} \tag{5.17}$$

By substituting (5.17) in (5.15), we get

$$\begin{aligned} &V_{\text{out}}\{G_{\text{L}}G_{\text{in}} + s[G_{\text{L}}(C_{\text{gs13}} + C_{\text{gd13}}) + G_{\text{in}}(C_{\text{gd13}} + C_{\text{L}}) + g_{\text{m13}}C_{\text{gd13}}] + \\ &s^2[(C_{\text{gs13}} + C_{\text{gd13}})(C_{\text{L}} + C_{\text{gd13}}) - C^2{}_{\text{gd13}}]\} = -V_{\text{in}}G_{\text{in}}(g_{\text{m13}} - sC_{\text{gd13}}) \end{aligned} \tag{5.18}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_{\text{m13}}(1 - s\frac{C_{\text{gd13}}}{g_{\text{m13}}})R_{\text{L}}}{1 + sa + s^2 b} \tag{5.19}$$

$$a = R_{\text{L}}(C_{\text{gd13}} + C_{\text{L}}) + R_{\text{in}}[C_{\text{gd13}}(1 + g_{\text{m13}}R_{\text{L}}) + C_{\text{gs13}}] \tag{5.20}$$

Upon simplification and converting G_L, G_{in} to R_L, R_{in}, we get;

$$b = R_{\text{in}}R_{\text{L}}(C_{\text{gd13}}C_{\text{gs13}} + C_{\text{gs13}}C_{\text{L}} + C_{\text{gd13}}C_{\text{L}}) \tag{5.21}$$

If s=0, the low frequency gain is obtained as mentioned [197]:

$$A_{\text{v}} = -g_{\text{m13}}R_{\text{L}} \tag{5.22}$$

When the poles of equation (5.19) are real and

$$\omega_{\text{p1}} << \omega_{\text{p2}} \tag{5.23}$$

The denominator of equation (5.19) becomes

$$D(s) = (1 + \frac{s}{\omega_{\text{p1}}})(1 + \frac{s}{\omega_{\text{p2}}}) = 1 + \frac{s}{\omega_{\text{p1}}} + \frac{s^2}{\omega_{\text{p1}}\omega_{\text{p2}}} \tag{5.24}$$

Comparing equation (5.19) with equation (5.24), we get;

$$\omega_{\text{p1}} = \frac{1}{a} \tag{5.25}$$

$$\omega_{\text{p2}} = \frac{1}{b\omega_{\text{p1}}} \tag{5.26}$$

Similarly, for RF- stage, the simplified gain can be expressed as:

$$A_{\text{v}} = -g_{\text{m14}} R_{\text{M}} \tag{5.27}$$

5.2.3 Differential Active Inductor

Inductors are passive electronic components that can suppress the rapid variation in the current. Bond wires, spirals, multi-level spirals, and solenoids are some of the passive inductors available within CMOS process technologies. These inductors can be opted depending on the application. Spiral inductors are most commonly used in high-speed signal processing and data communication applications. These inductors exhibit degraded performance due to their spiral layout structure, which demands a large silicon area, leading to low-quality factors, low self-resonant frequency. Thus, active inductors are employed within the circuits. These inductors are developed using active devices, especially MOSFETs, operational amplifiers (Op-Amps), operational transconductance amplifiers (OTAs), and resistors [242]. The resistors are customarily used as feedback elements to enhance the performance of the inductors, which will further improve the

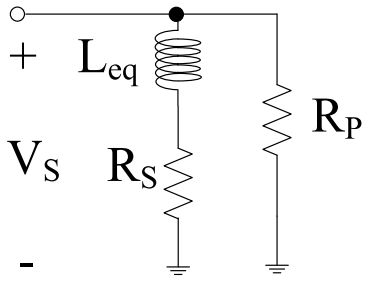


Figure 5.5: RL circuit of an active inductor circuit

overall performance of the circuit within which active inductors are employed. Alternatively, these inductors can follow the gyrator-C topology that contains two transconductors arranged in a feedback manner. Within particular DC biasing conditions and signal swing restrictions, the active network (combination of active devices) behaves like an inductor within a specified frequency band [243]. These inductors show high tunability and quality factor, which makes them convenient for differential RF front-ends like low-noise amplifiers and mixers.

In [123], a DAI circuit is used within the mixer circuitry, responsible for tuning out the parasitic capacitors, which in turn lowers the flicker noise while maintaining good conversion gain and linearity. Different active inductor topologies have been proposed in [244, 245, 246]. The proposed mixer uses a folded differential active inductor with a current mirror approach based on the AI discussed in [123, 197]. The design consists of transistor pairs (M_2-M_3, M_5-M_6) are arranged in feedback manner and operate in saturation region. M_4 behaves like a voltage-controlled resistor, which is biased in the triode region. The biasing voltage of M_4 is varied to show the tunability behaviour of the inductor. The cross-coupled transistors are balanced with the other transistors. The current in the active inductor is controlled using a current mirror approach, which mirrors the current from M_1 and M_7 to M_2 and M_3 transistors, respectively. The proposed AI resonates with the capacitor and parasitic capacitance. RL equivalent circuit of the active inductor is shown in Figure 5.5. The parameters of the equivalent circuit are expressed as

$$R_{\mathrm{P}} = \frac{1}{g_{\mathrm{m5}}} \tag{5.28}$$

$$L_{eq} = \frac{C_A(g_B + g_{m4}) + C_B(g_A + g_{m4})}{{g_{m2}}^2(g_{m5} - g_{m4} + g_{m3})} \tag{5.29}$$

$$Q = (g_A + g_{m4})(g_B + g_{m4}) - \omega^2 C_A C_B + (g_{m5} - g_{m4} + g_{m2})(g_{m4} - g_{m6} + g_{m3}) \tag{5.30}$$

Therefore,

$$R_s = \frac{Q}{{g_{m2}}^2(g_{m5} - g_{m4} + g_{m3})} \tag{5.31}$$

5.3 Performance Analysis

5.3.1 Conversion Gain

Figure 5.6 shows the complete small-signal model for the proposed mixer circuit for CG analysis. The load and current mirror sections are simply represented as resistors (r_{010}, r_{015}), whereas, the diode load is represented by r_{011} and $1/g_{m011}$, respectively. Besides, the active inductor is represented using the RL model of the inductor. Thus, the circuit behaves like a source-degeneration-based common source amplifier. Based on the circuit, the controlled current source determines the current through R_S and V_1 can be expressed as:

$$V_1 = (g_{m13}V_{gs13})R_S = g_{m13}R_S(V_{in} - V_1) \tag{5.32}$$

$$V_1(1 + g_{m13}R_S) = g_{m13}R_S V_{in} \tag{5.33}$$

$$A_1 = \frac{V_1}{V_{in}} = \frac{g_{m13}R_S}{1 + g_{m13}R_S} \tag{5.34}$$

Once V_1 is obtained, the output voltage can be defined as:

$$V_{out} = -R_D(g_{m13}V_{gs13}) = -g_{m13}R_D(V_{in} - V_1) \tag{5.35}$$

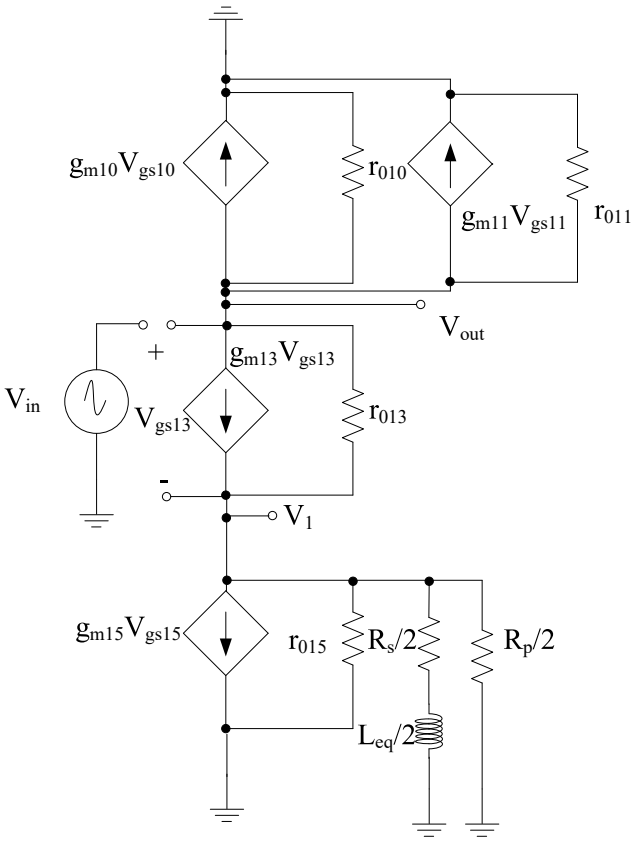


Figure 5.6: Complete small signal model for half circuit

where $R_D = r_{010} \parallel r_{011} \parallel \frac{1}{g_{m11}}$.

Substituting V_1 from (5.32) to (5.33), we get

$$V_{out} = -\frac{g_{m13}R_D}{1 + g_{m13}R_S}V_{in} \tag{5.36}$$

where $R_s = \frac{r_{015}}{2} \parallel (\frac{R_{011}}{2} + jX_{Leq/2}) \parallel \frac{R_P}{2}$

$$A_0 = \frac{V_{out}}{V_{in}} = -\frac{g_{m13}R_D}{1 + g_{m13}R_S} \tag{5.37}$$

To determine the impact of parasitic capacitors present at C_{gd13} and C_{gs13}, Miller's theorem can be used, which relates the equivalent capacitance to the gain between the nodes that the capacitor is tied to. Assuming C_{in}, C_1 and C_0 are present at the gate, source and drain terminals of the

transistor, M_3. Thus, these capacitances can be expressed by Miller's theorem as

$$C_{\text{in}} = C_{\text{gs13}}(1 - A_1) + C_{\text{gd13}}(1 - A_0) \tag{5.38}$$

$$C_0 = C_{\text{gd13}}(1 - \frac{1}{A_0}) \tag{5.39}$$

$$C_1 = C_{\text{gs13}}(1 - \frac{1}{A_1}) \tag{5.40}$$

5.3.2 Noise Figure

The noise model of the proposed mixer is shown in Figure 5.7. The model contains only transistors and resistors, and all passive elements are considered ideal. Besides, the noise figure is obtained by considering only thermal noise and based on which the power spectral density of each stage is obtained [205, 197].

Equation (5.41) defines the power spectral density, which is the combination of the power spectral density obtained from all stages present within the design.

$$\overline{V^2{}_{\text{n}}} = \overline{V^2{}_{\text{n,M}}} + \overline{V^2{}_{\text{n,L}}} + \overline{V^2{}_{\text{n,CM}}} + \overline{V^2{}_{\text{n,AI}}} \tag{5.41}$$

The power spectral density for all stages is obtained based on the resistors and transistors present within each stage. The power spectral density of the mixer stage is represented as

$$\overline{V^2{}_{\text{n,M}}} = \overline{V^2{}_{\text{n,M}_{13}}} + \overline{V^2{}_{\text{n,M}_{14}}} = \frac{4kT\gamma}{g_{\text{m13}}} + \frac{4kT\gamma}{g_{\text{m14}}} \tag{5.42}$$

Likewise, the power spectral density of the load stage is

$$\overline{V^2{}_{\text{n,L}}} = \overline{V^2{}_{\text{n,M}_{10}}} + \overline{V^2{}_{\text{n,M}_{11}}} = \frac{4kT\gamma}{g_{\text{m10}}} + \frac{4kT\gamma}{g_{\text{m11}}} \tag{5.43}$$

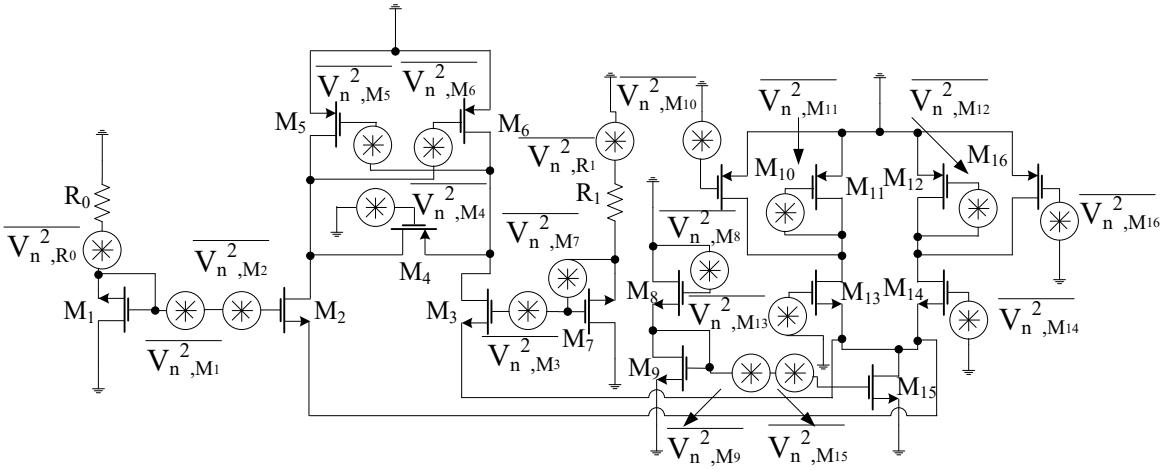


Figure 5.7: Noise model of proposed mixer

Besides, the power spectral density of the current mirror stage is given as

$$\overline{V^2_{\text{n,CM}}} = \overline{V^2_{\text{n,M}_8}} + \overline{V^2_{\text{n,M}_9}} + \overline{V^2_{\text{n,M}_{15}}} = \frac{4kT\gamma}{g_{\text{m8}}} + \frac{4kT\gamma}{g_{\text{m9}}} + \frac{4kT\gamma}{g_{\text{m15}}} \tag{5.44}$$

Finally, the power spectral density of the active inductor stage is

$$\overline{V^2_{\text{n,AI}}} = 4kTR_0 + \frac{4kT\gamma}{g_{\text{m1}}} + \frac{4kT\gamma}{g_{\text{m2}}} + \frac{4kT\gamma}{g_{\text{m4}}} + \frac{4kT\gamma}{g_{\text{m5}}} \tag{5.45}$$

Hence, the noise figure is given by

$$NF = 1 + \frac{\overline{V^2_{\text{n}}}}{{A_{\text{v}}}^2} \tag{5.46}$$

5.3.3 Linearity

It is essential to determine the nonlinear behaviour of the mixer circuit. Based on the literature study, we found that resonant circuits can enhance linearity performance. As per the conventional Gilbert mixers, harmonic generation is possible, especially due to the RF stage because the LO stage behaves like a switch and the load stage contains passive components. Thus, LO and load

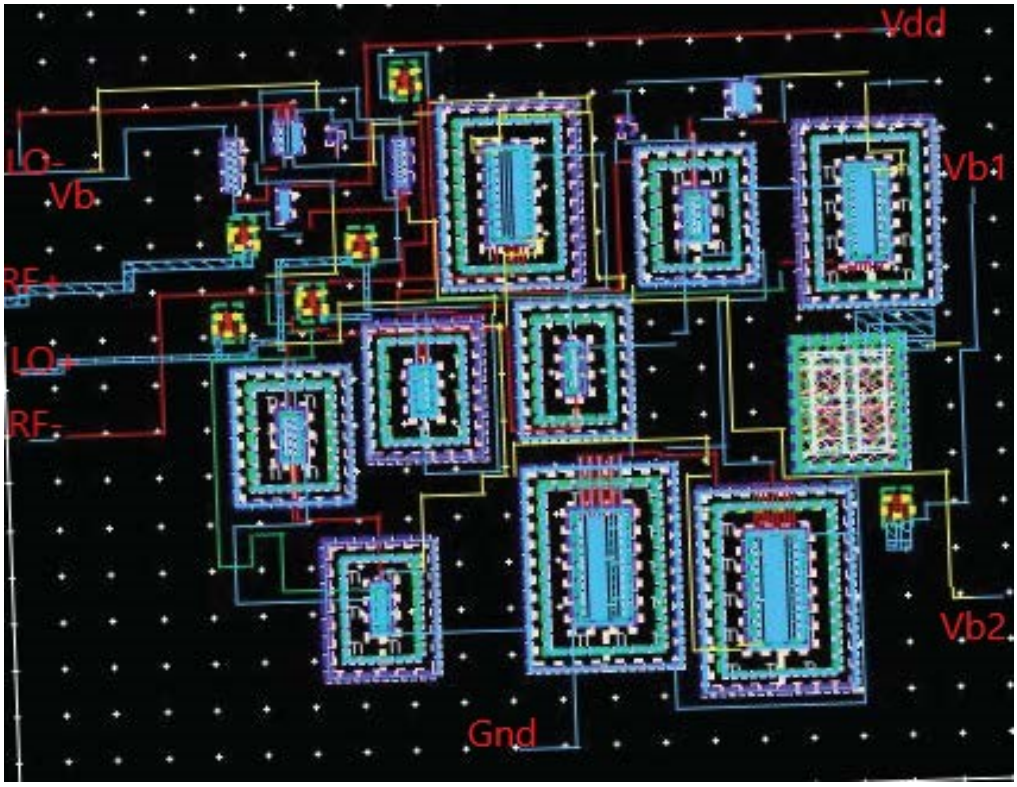
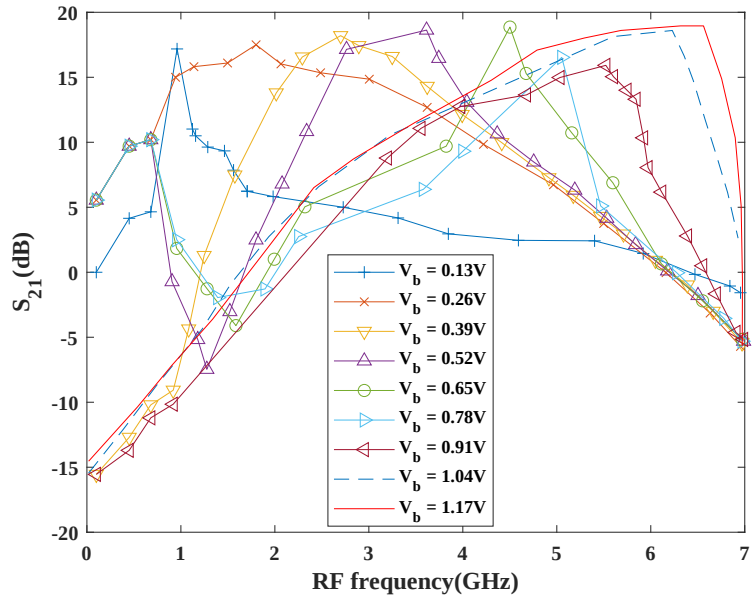


Figure 5.8: Mixer layout

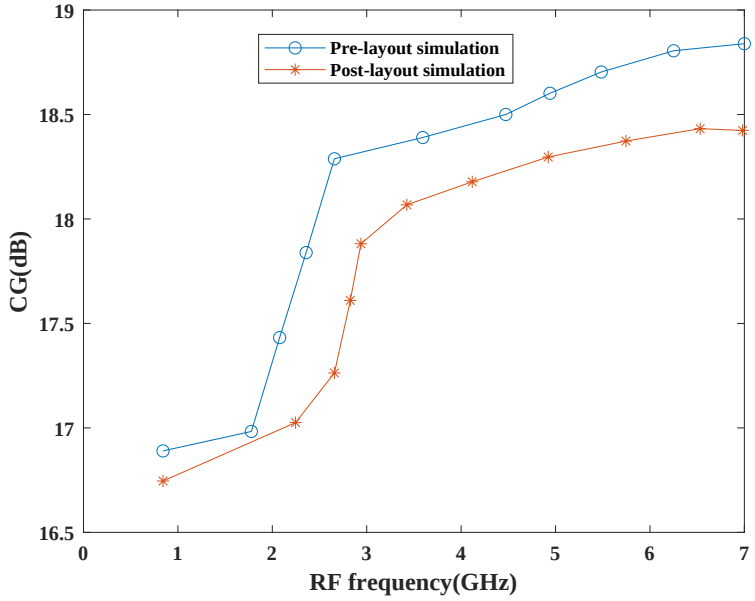
stages do not produce distortions [247]. Within the transconductance stage, the main source of harmonics are transconductance (g_m), output conductance (g_{ds}) and gate-source capacitance (C_{gs}), where g_m is the most predominant one [240]. Thus, the equivalent drain current of the transconductance stage is represented as a function of g_m and v_{gs}

$$i_{ds} = g_m(v_g - v_s) + g_m{}'(v_g - v_s)^2 + g_m{}''(v_g - v_s)^3 + ... \tag{5.47}$$

where g_m, $g_m{}'$ and $g_m{}''$ coefficients represent transconductance, 2nd and 3rd order nonlinearity of transistor transconductance, respectively. Additionally, v_g and v_s refers to the gate and source voltages of the transistor. Besides, the switching stage transistors are responsible for providing parasitic components which results in linearity degradation. Based on the above discussion, it has been found that the harmonics of the mixer depend on all transistors present within the design and parasitic component effects. In the proposed design, a single transistor is operating as a mixer, thus the effect of parasitic and g_m are equally important for the main mixer transistors



(a)



(b)

Figure 5.9: S_{21} plots (a) S_{21} at different biasing voltages (b) Pre and post layout S_{21}

i.e., M_{13} and M_{14}. Besides, load stage also contains transistors instead of passive components and the parasitics obtained using M_{13} and M_{14} are balanced using the resonating active inductor circuit. Additionally, the circuit also includes current mirror circuits with resistive loads where the parasitic effect can be considered. Thus, drain current i_{13} is expressed as

$$i_{13} = g_{m13}(-v_1) + g_{m13}{}'(-v_1{}^2) + g_{m13}{}''(-v_1{}^3) \tag{5.48}$$

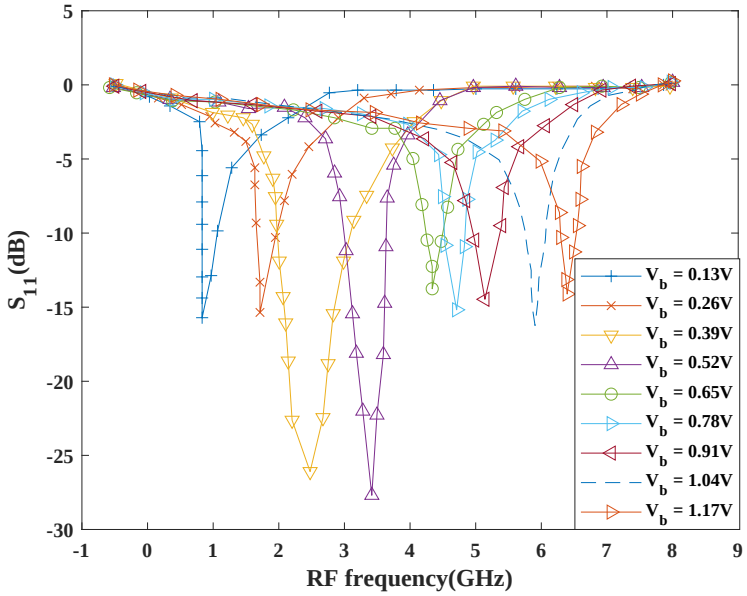


Figure 5.10: Return loss at different biasing voltages

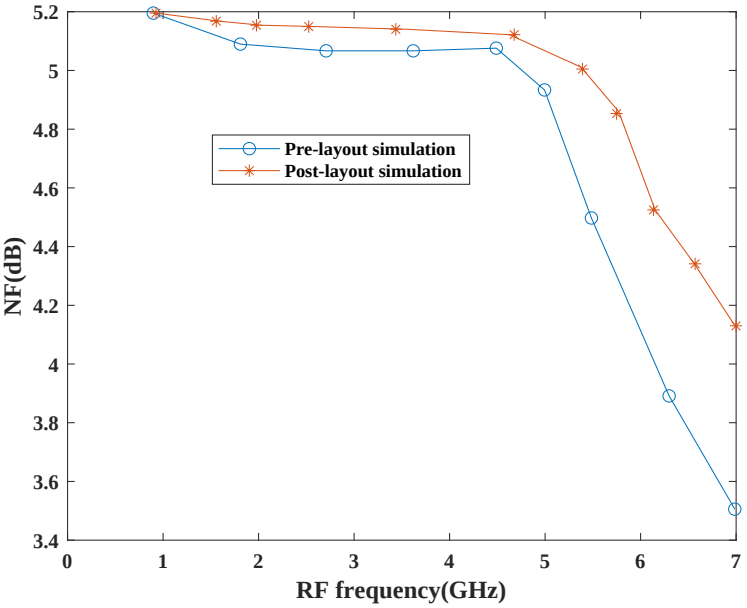


Figure 5.11: Pre and post layout NF

Based on the model depicted in Figure 5.1, the total current flow through the half-mixer circuit is expressed in equation (5.48). Besides, the parasitic capacitance at node V_1 is denoted by C_P which is balanced by the active inductor circuitry.

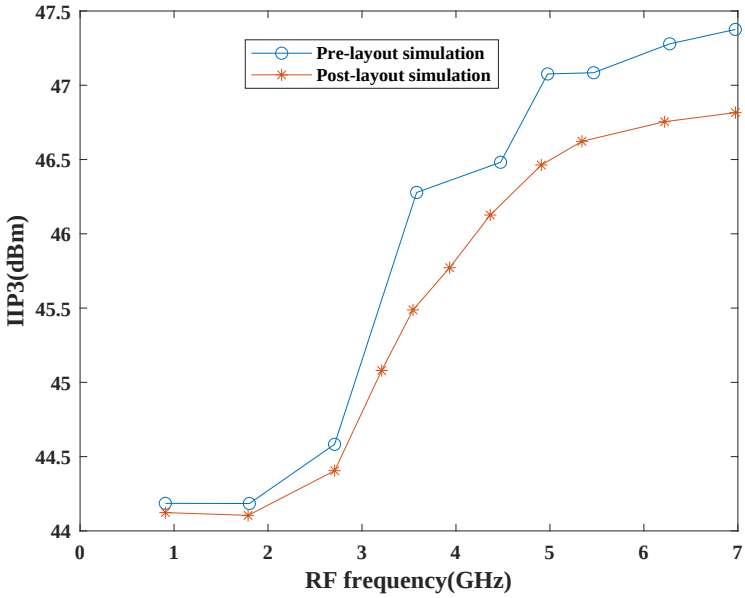


Figure 5.12: Pre and post layout IIP3

As per equation (5.48), the transconductance, G_m of the half mixer is expressed as

$$G_m = g_{m13} \tag{5.49}$$

Besides, to enhance the linearity, the coefficient of v_1^3 must be 0.

5.4 Results and Discussions

The proposed mixer is designed and simulated using Cadence with 0.13 μm CMOS Silterra process. The pre-and post-layout CG results of the proposed mixer are illustrated in Figure 5.9. The proposed mixer shows a good CG within the entire band while maintaining the highest gain of 18.75 dB during the pre-layout simulation and degrades by 0.3 dB after the post-layout simulation. Figure 5.10 depicts the return loss plot with respect to frequency. As per the simulation results, $|S_{11}|$ is below 10 dB within the entire band. The pre-and post-layout simulation results of NF are shown in Figure 5.11. With the employment of different techniques such as active inductor and current mirror approaches, the design obtains good NF. The minimum achievable NF is 3.5 dB at 7 GHz during pre-layout simulation. This NF raised by 0.6 dB after

Table 5.1: Performance Comparison Summary

References	Technology	Supply	RF(GHz)	NF(dB)	S_{21}(dB)	IIP3(dBm)
This work	0.13um	1.2	0.9-7	3.5-5.19	15.2-18.75	44.2-47.4
[48]	HEMT	1.2	1.8-5	<2	5-10	28
[123]	0.18um	2.4	2.4	11.2	23.7	-6
[248]	0.18um	1.8	1-10	16.7	6-3	0.15-2
[74]	0.18um	1.8	3.43	11.3-15	8.05	-10.8
[80]	0.09um	1.1	0.5-3.1	6.7	15	9.3
[135]	0.13um	1.2	0.5-6.5	13	10	9.52
[249]	0.18um	1.8	2.4	4.55	14.5	12.5
[238]	0.09um	1.2	2.4	11.4	12	19.6
[240]	0.09um	1	1-5	8.6	11.1	9.9
[250]	0.18um	1.5	2.4	14.87	3.3	5.46
[251]	0.18um	1.8	2.4	15	20.3	20.3
[252]	0.18um	1.8	2.1	14	15	15

post-layout simulations due to parasitic effects and the obtained CG. Likewise, IIP3 simulation results of the proposed mixer are depicted in Figure 5.12. The proposed mixer attains a maximum IIP3 of 47.4 dBm during pre-layout simulations, which is best among the reported works due to the presence of folded active inductor DAI circuit that perfectly resonates with the capacitances. IIP3 has not degraded much after post-layout simulations. Figure 5.8 depicts the layout of the double-balanced mixer developed in Silterra 130nm process technology. The design covers <1 mm^2 area as shown in Figure 5.8 while consuming only 12.52 mW power. Thus, due to the mixer's high performance, it is well suited for software-defined radios.

Table 5.1 compares the proposed mixer with several reported works developed within different CMOS technologies that attain high CG. However, the IIP3 performance is not comparable to the proposed mixer due to design topology and design technique used by the proposed mixer, indicating the effectiveness of the proposed folded active inductor technique.

To further improve the performance of the proposed mixer, PSO has been implemented on the mixer as discussed in Chapter 7, Section 7.7.3. The optimized results are obtained and compared with the simulated results. Based on the observation, it has been found that performance of the proposed mixer has significantly improved.

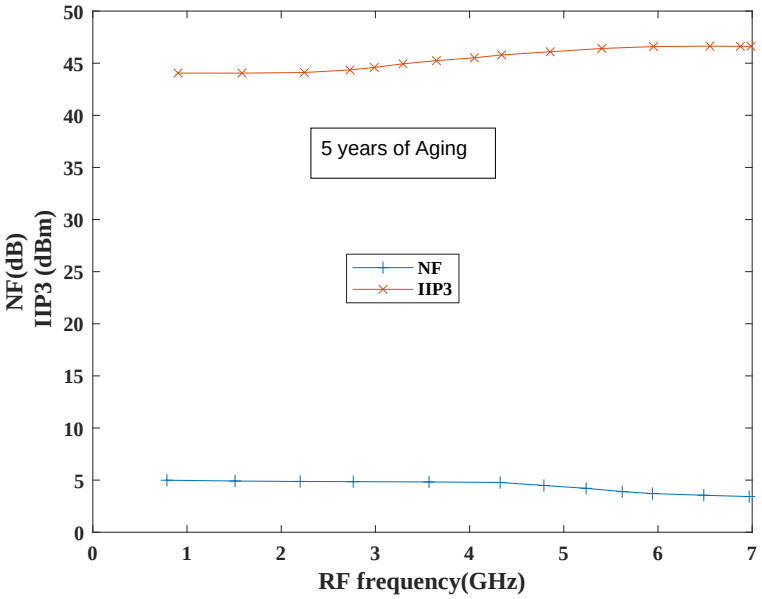


Figure 5.13: Reliability plots for NF and IIP3

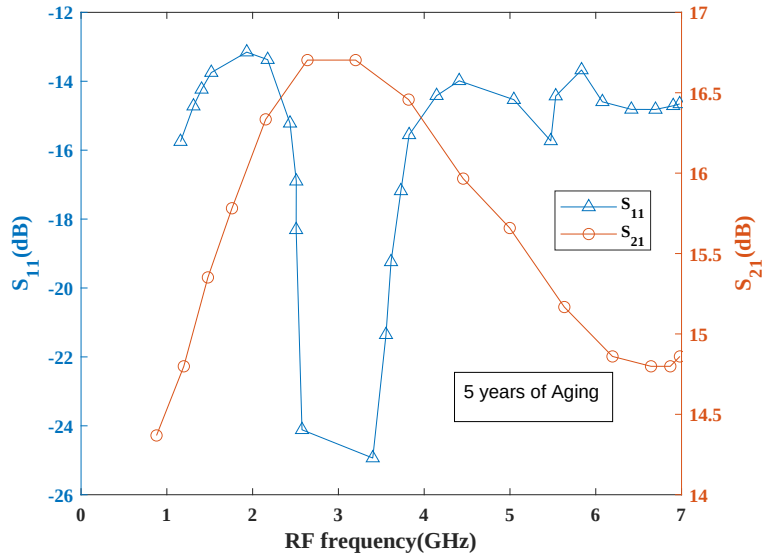


Figure 5.14: Reliability plots for S_{11} and S_{21}

5.5 Reliability performance

A recent study shows that design reliability is vital due to limited timeline, budget, scaling, and demanding profile constraints. Reliability testing can be done using the RelXpert tool developed by Cadence [197]. RelXpert tool has the capability to simulate PFET and NFET devices to determine the device degradation performance. This process is very convenient for analyzing

the degradation in circuit behaviour, especially during the initial design flow stages [215, 232]. Based on this approach, the degradation performance has been evaluated for the proposed mixer in terms of various performance parameters such as NF, CG, IIP3, and S_{11}, respectively. The NF and IIP3 degradation behaviour of the proposed mixer can be observed from Figure 5.13. As per the plot, it has been observed that NF and IIP3 reach 3.421 dB and 46.62 dBm after 5 years of aging. However, the current simulation results show around 5.1 dB and 47.4 dBm, respectively. Return loss and gain degradation performance curves are depicted in Figure 5.14. Based on the observation, it has been found that $|S_{11}|$ still remains below 10 dB after 5 years of aging and shows less degradation. The maximum gain attained after 5 years of aging is 14.8 dB. As a result, the proposed mixer is suitable for future SDR applications.

5.6 Summary

A highly linear mixer with an improved gain is demonstrated in this Chapter. The use of an active inductor at the source terminal of the main mixing transistors is the mechanism used to maintain high linearity while improving the gain. Simulation results showed a conversion gain of 30.35 dB and an IIP3 of 47.2 dBm. The proposed mixer also attained a reasonable noise figure while consuming small power with a small chip area. Based on the obtained performance in terms of different parameters, it is desirable to check the behaviour of the mixer in the receiver architectures. Thus, a high-performance SDR receiver will be presented in Chapter 6.

Chapter 6

Design and Analysis of High Performance Receiver for Software Defined Radios

6.1 Introduction

Wireless communication plays a vital role in our day-to-day life. Thus, with the advancement in the number of wireless standards, it is desired to develop a radio that has the capability to handle several wireless standards. Conventional radios cannot handle multiple wireless standards because of their hardware dependency problems. SDRs, on the other hand, have good flexibility to reconfigure their operations [197].

Earlier SDR receiver systems were implemented using FPGAs [20]. Thus, signal processing was carried out in the digital domain. As a result, it became possible to have extensive accessibility of software-controlled features of SDR. However, it consumes high power, making it inconvenient for wide deployment. Thus, to overcome this problem, discrete-time and mixed-signal systems became significant. These systems require additional blocks such as LNAs and mixers before ADC blocks. Furthermore, these methods provide good reconfigurability while consuming less power. As a result, LNAs and mixers are considered as the critical blocks of SDR as they amplify and then downconvert the RF band to IF with respect to the input bandwidth, easing the ADC requirements in the following stage [253]. Moreover, they should maintain a low NF, high

CG, and good linearity while occupying a small die area for offering optimum SDR receiver performance [254, 197, 41].

Generally, SDRs are often developed with customizable front-ends that have the ability to handle wideband transmissions and tune their operating frequencies in such a way that it lowers interference. Additionally, it is highly desirable to maintain a small chip size with low power consumption and cost to maximize battery life and resource conservation. It is also essential to analyze existing receiver structures and identify critical problems within them before proposing any new receiver design [190]. Superheterodyne receivers are among the most common receiver architectures because of their high performance. However, they suffer from various problems such as difficulty in deploying on-chip filters and narrow-band applicability. Thus, developing a single chip solution within this architecture is challenging. The alternative solution is to employ off-chip filters; however, it will raise the overall cost of the receiver. For example, the superheterodyne receiver in [255], employed in-built filters for interference and image rejection purposes that achieve high IIP3, low NF, and reasonable CG at the expense of the design area, which in turn enhances the overall cost of the circuitry. Thus, to overcome this problem, homodyne receivers can be used as they perform direct RF to IF conversion and can eliminate the unnecessary filters [2]. Based on this idea, a receiver architecture was presented in [256] that consumed less power due to the common transconductance stage shared by both mixers and LNA. This improved the amplification of both RF and IF signals. Additionally, the design also employed complex filters for the selection of the desired channel. The proposed receiver attained high CG, consumed less power, and covered a small chip size while degrading NF. Likewise, a dual-conversion transmitter / receiver design with stacked passive components was proposed in [257] to maintain a low die area. Furthermore, the design utilized non-invasive baseband filtering to provide high sensitivity with minimal power consumption. The proposed design achieved excellent CG at the cost of NF [254, 197].

Image rejection is another major challenge for receiver architectures. This problem can be overcome by using wideband receivers such as double-conversion and low-IF designs that have the features of heterodyne and direct-conversion systems. However, these receivers attain limited

IRR due to signal mismatch and limited quality factor of on-chip inductors. Several architectures have been reported in the literature [216, 258, 7, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 128, 279, 280, 281, 282, 283, 104], aiming to achieve high image rejection for different applications. Kim and Lee presented a front-end receiver with a high-IF and double quadrature architecture to generate sufficient IR at high-frequency [284]. The design adopted a three-stage polyphase RC network; however, the in-band loss was substantially increased. As high parasitic capacitances predominate at the mixing stage, their placement near the mixer's input may further increase the losses. To solve this issue, two spiral inductors were connected at the output of the polyphase filter before connecting it to the mixer stage. The inductors would tune out the mixing stage's total input parasitic capacitance, which will enhance the polyphase filter's output loading. The proposed receiver attained high IR and consumed less power at the expense of IIP3. Moreover, the receiver attained moderate CG and high NF of >5 dB. Similarly, in [285], a reconfigurable receiver architecture was proposed to use a dual-mode resonator-based reconfigurable filter, which can tune at the centre frequency and the desired bandwidth of the filter using MEMS switches. The receiver attained high IR, covering a small area at the expense of NF and IIP3 [254].

The aforementioned issues with the existing design motivate us to propose a 0.9-20 GHz reconfigurable receiver with a reasonable trade-off among CG, NF, IIP3, and IRR. We present a novel receiver architecture that employs a reconfigurable LNA, active inductor-based I/Q mixers, and IF amplifiers. For tuning purposes at the LNA stage, 8^{th}-order tunable filter has been employed, which is developed using varactors and inductors. Furthermore, the receiver also employs a polyphase filter for selecting the desired output signal before final amplification. The proposed receiver attains high CG, low NF while maintaining high IR and high IIP3 [254].

6.2 Receiver Architecture

The block diagram of 0.9-20 GHz RF front-end receiver is shown in Figure 6.1. The receiver adopts an image rejection architecture where the LNA initially amplifies the incoming RF signals

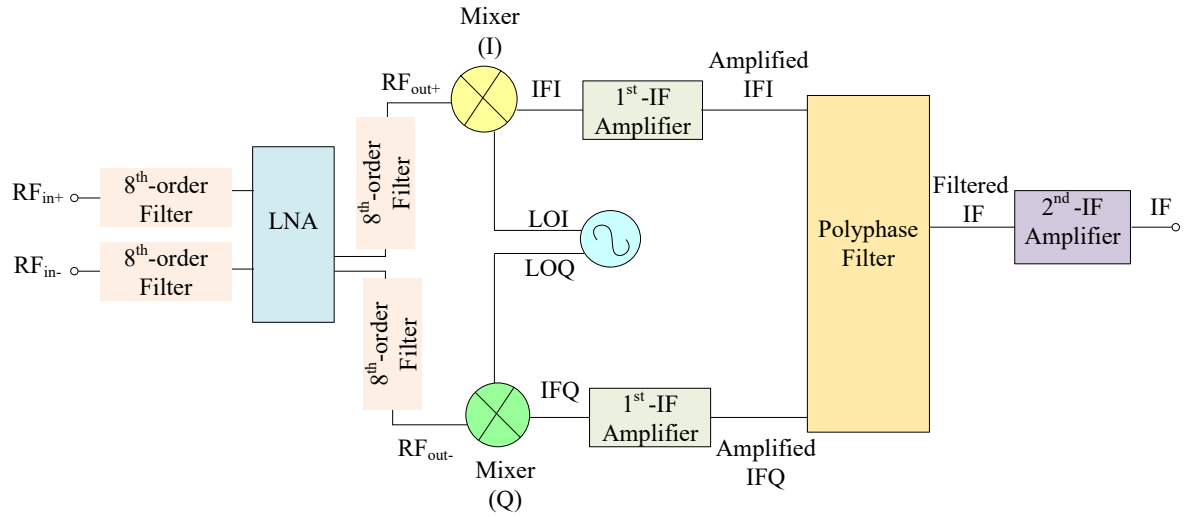


Figure 6.1: Block diagram of an image rejection receiver

and then is converted to in-phase and out-of-phase RF signals by 8th-order tunable filter. Upon mixing, RF signals are down-converted and then further amplified by the 1st-IF amplifier. The primary purpose of the IF polyphase filter is to allow desired IF signals and reject image signals. The 2nd-IF amplifier makes up for the polyphase filter's insertion loss and removes the undesired signals obtained from the mixers. An external LO signal of 1 GHz is provided to the mixer circuitry.

6.3 Circuit Implementation

6.3.1 Low Noise Amplifier

Cascode topology is commonly used for designing LNA structures [286, 287]. Based on the design observation, it has been found that limiting the voltage across the input drive transistor will lower the impact of the short channel effects. It is also very helpful in case there is need to apply higher voltage to the circuit without effecting the common-source transistor [199]. Thus, the proposed receiver architecture used cascode topology-based LNA. Additionally, as shown in Figure 6.2, the LNA design can also include source-degenerated inductors (L_1, L_2), at the source terminals of the main transistors (M_3, M_4) to enhance the CG and NF performance. Hence, for maximum power transfer perfect tuning is required. Thus, 8th-order reconfigurable filters are

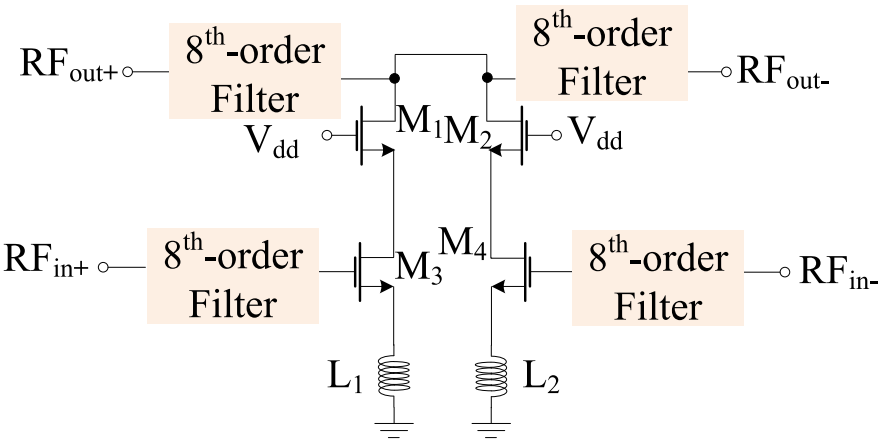


Figure 6.2: LNA circuit

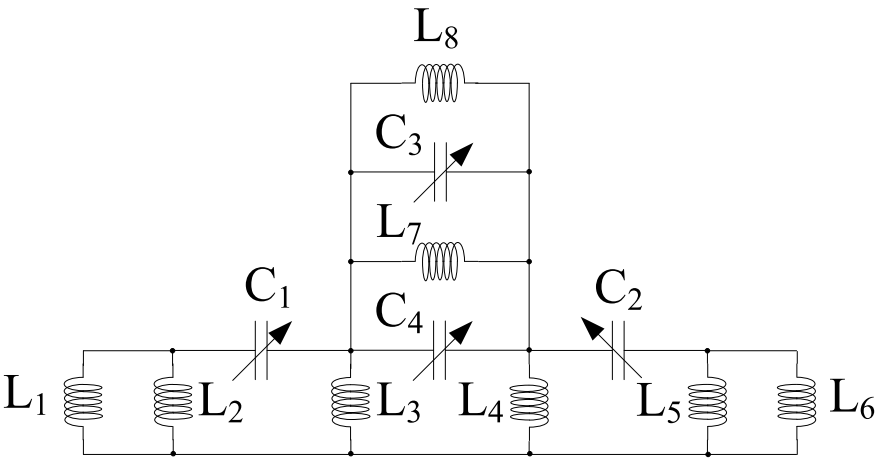


Figure 6.3: Schematic of the LNA filter

employed at the input and output terminals of LNA [284, 288, 289, 290, 291, 292], as shown in Figure 6.3. Based on the filter design, the input impedance of the filter section can be expressed as [254]

$$Z_{\text{in}} = \{[(A+B)||C]+D\}\,||(E||F) \tag{6.1}$$

where

$$A = sL_1||sL_2 \tag{6.2}$$

$$B = \frac{1}{sC_1} \tag{6.3}$$

$$C = sL_3 \tag{6.4}$$

$$D = \frac{1}{sC_4}||sL_7||\frac{1}{sC_3}||sL_8 \tag{6.5}$$

$$E = sL_4 + \frac{1}{sC_2} \tag{6.6}$$

$$F = sL_5||sL_6 \tag{6.7}$$

Likewise, the output impedance is expressed as

$$Z_{\text{out}} = F = sL_5||sL_6 \tag{6.8}$$

6.3.2 Mixer

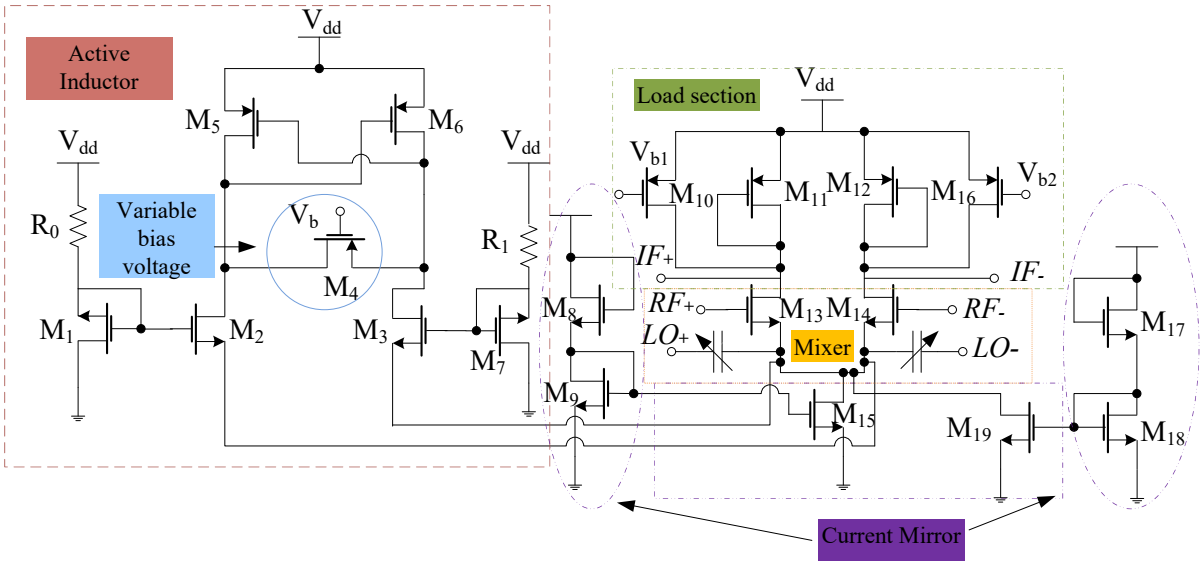


Figure 6.4: Schematic diagram of an active inductor based mixer

A novel double-balanced mixer design is proposed for the receiver circuitry that comprises of two NFETs (M_{13}, M_{14}), each of which acts as an individual mixer as shown in Figure 6.4. The proposed mixer follows a common source configuration. Additionally, for maintaining high RF-LO isolation, RF inputs are imparted via the gate terminals of transistors (M_{13}, M_{14}), whereas LO signals are provided through the source terminals. Likewise, the outputs denoted by IF+/IF- are obtained via drain terminals of these transistors. The proposed design resembles a fully balanced mixer because of the presence of two transistors, acting as a single mixer.

The design also employs PFET diode loads (M_{11}, M_{12}) instead of load resistors due to the manufacturing challenges of resistors that have tightly controlled physical size values. Another major problem is that large drain resistors must maintain high gain, which demands low DC biasing voltage at the output port. This significantly affects the transistor operating conditions, such as transitioning from saturation to triode region. Furthermore, the load stage also employs transistors, M_{10} and M_{16} for improving the overall performance of the circuit [185]. Likewise, the effect for current mirror circuit containing transistors M_{17}-M_{19} can be determined. However, it is not shown due to symmetrical circuitry containing transistors, M_8, M_9 and M_{15}, respectively. To show the symmetry within the circuitry, M_{17}-M_{19} transistors are also included within the design. The current mirror circuit is also a part of the mixer design that contains three transistors (M_8, M_9 and M_{15}), respectively, where M_8 behaves like a resistor. The transistors (M_9 and M_{15}) are operating in the saturation region. The transistor, M_{15} will remain in saturation condition until the output voltage is higher than the saturation voltage. Consequently, the input current flowing through the transistor, M_9 can control the current flowing through the transistor, M_{15} [185, 232, 226, 41].

Based on the active inductor (AI) design described in [123], the proposed mixer employs a folded differential active inductor with a current mirror approach. The design is made up of transistor pairs (M_2-M_3, M_5-M_6) that are organized in feedback and operate in the saturation region. Transistor, M_4 operates as a voltage-controlled resistor within the triode region. The biasing voltage of the transistor, M_4 is adjusted to demonstrate the inductor's tunability behaviour. The cross-coupled transistors are balanced with the other transistors. Moreover, current mirror approach is used within the design to regulate the current in the AI, which reflects the current from (M_1, M_7) to (M_2, M_3) transistors, respectively. The proposed AI resonates with capacitors and parasitic capacitances. AI can be simplified as RL equivalent circuit as shown in Figure 6.5, and the circuit parameters are expressed as

$$R_{\mathrm{P}} = \frac{1}{g_{\mathrm{m5}}} \tag{6.9}$$

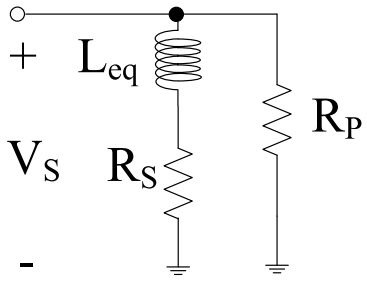


Figure 6.5: RL circuit of an active inductor

$$L_{\text{eq}} = \frac{C_{\text{A}}(g_{\text{B}} + g_{\text{m4}}) + C_{\text{B}}(g_{\text{A}} + g_{\text{m4}})}{{g_{\text{m2}}}^2(g_{\text{m5}} - g_{\text{m4}} + g_{\text{m3}})} \tag{6.10}$$

$$Q = (g_{\text{A}} + g_{\text{m4}})(g_{\text{B}} + g_{\text{m4}}) - \omega^2 C_{\text{A}} C_{\text{B}} + (g_{\text{m5}} - g_{\text{m4}} + g_{\text{m2}})(g_{\text{m4}} - g_{\text{m6}} + g_{\text{m3}}) \tag{6.11}$$

Therefore,

$$R_{\text{s}} = \frac{Q}{{g_{\text{m2}}}^2(g_{\text{m5}} - g_{\text{m4}} + g_{\text{m3}})} \tag{6.12}$$

6.3.3 IF Amplifiers

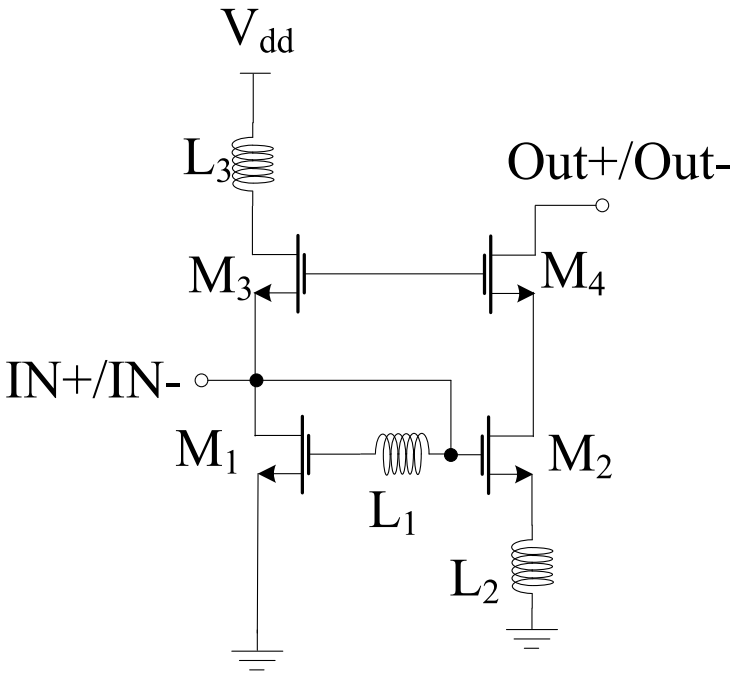


Figure 6.6: Schematic of 1st-IF Amplifier

Figure 6.6 depicts the schematic of the 1st-IF amplifier that employs a small inductor (L_1) at

the gate of the diode-connected transistors (M_1, M_2) that shows similar performance to that of active inductors. The design also contains inductors (L_2, L_3) that are present at the source and drain terminals of transistors (M_2, M_3), respectively, responsible for resonating with the parasitic capacitances of the design. This design attains high input impedance, which subsequently lowers the attenuation of the previous mixing stages. Furthermore, the overall linearity of the receiver is improved [284]. Likewise, the receiver also employs 2nd-IF amplifier containing the current mirror transistors (M_5, M_8), as shown in Figure 6.7. These transistors copies the current to the other transistors (M_6, M_7), which in turn gets transferred to the main transistors (M_2, M_3). Additionally, the design also employs the inductors (L_1-L_4), responsible for resonating with the parasitic capacitance. This amplifier enhances the performance of the filtered signal that is obtained from the filter stage.

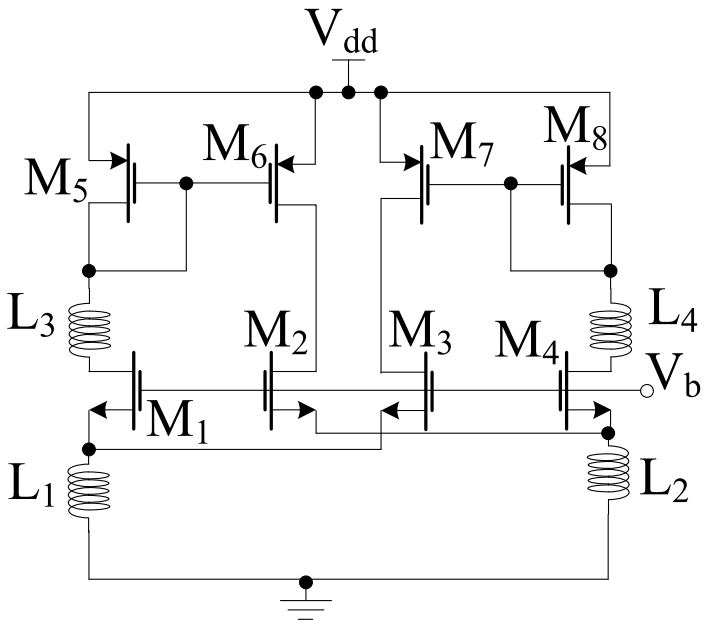


Figure 6.7: Schematic of 2nd-IF Amplifier

6.3.4 Polyphase Filter

RC polyphase filters are critical components of wireless transceivers' analogue front-end circuitry. These filters are responsible for generating in-phase (I) and quadrature-phase (Q) signals and for rejecting images. The receiver design employs a cascaded RF polyphase filter as shown

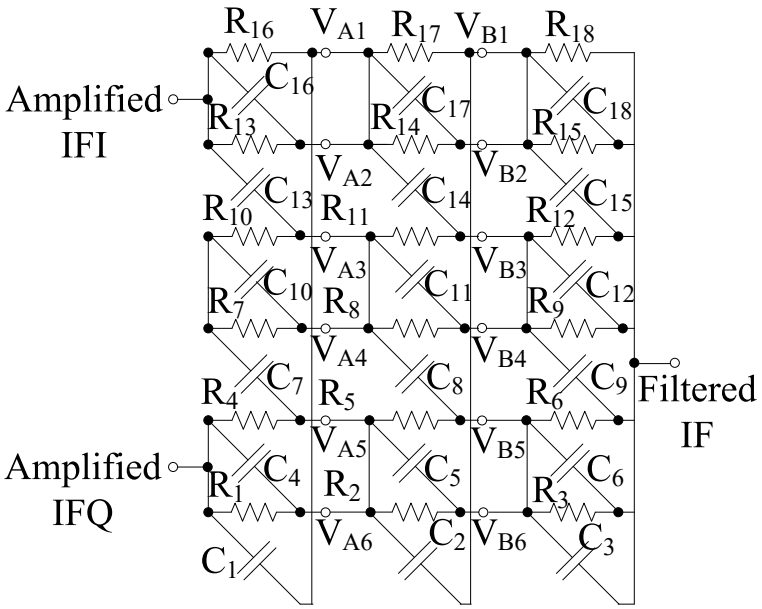


Figure 6.8: Schematic of polyphase filter

in Figure 6.8. Thus, the number of stages within the polyphase filter depends on the desired bandwidth and IRR. The proposed receiver makes use of the three-phase multi-stage filter to meet these criteria. The main function of this filter is to reject undesirable image signals and transfer the desired signal to the 2nd-IF amplifier stage for further amplification purposes. For analyzing the design, impedances of the capacitor C_A-C_C are denoted by Z_A-Z_C. Likewise, on the sub-branches, the resistance distances of all nodes are determined from the input loop to the output loop. The input voltages $V_{1,2}$ are the notations of 2 input sources from V_{in1} to V_{in2}. Thus, on applying the superposition principle at each loop, the voltages can be obtained using nodal equations as represented below

$$V_{\mathrm{Ai}} Y_{\mathrm{A}} = \frac{V_{\mathrm{in1,2}}}{R_{\mathrm{A}}} + \frac{V_{\mathrm{in2,1}}}{Z_{\mathrm{CA}}} \tag{6.13}$$

where V_{Ai} refers to the voltages at nodes 1,2,3,4,5 and 6 while moving in the clockwise direction (V_{A1} - V_{A6}), C_A= C_1= C_4= C_7= C_{10}= C_{13}= C_{16} and R_A= R_1= R_4= R_7= R_{10}= R_{13}= R_{16}.

$$V_{\mathrm{Bi}} Y_{\mathrm{B}} = \frac{V_{\mathrm{Ai}}}{R_{\mathrm{B}}} + \frac{V_{\mathrm{Ay}}}{Z_{\mathrm{CB}}} \tag{6.14}$$

where V_{Bi} refers to the voltages at nodes 1,2,3,4,5 and 6 while moving in the clockwise direction (V_{B1} - V_{B6}), V_{Ay} refers to the voltages at nodes 1,2,3,4,5 and 6 while moving in the anticlockwise direction (V_{A6} - V_{A1}), C_B= C_2= C_5= C_8= C_{11}= C_{14}= C_{17} and R_B= R_2= R_5= R_8= R_{11}= R_{14}= R_{17}.

$$V_{\text{outi}} Y_{\text{C}} = \frac{V_{\text{Bi}}}{R_{\text{C}}} + \frac{V_{\text{By}}}{Z_{\text{CC}}} \tag{6.15}$$

where V_{outi} V_{Bi} refers to the voltages at nodes 1,2,3,4,5 and 6 while moving in the clockwise direction (V_{out1} - V_{out6}), C_C= C_3= C_6= C_9= C_{12}= C_{15}= C_{18} and R_C= R_3= R_6= R_9= R_{12}= R_{15}= R_{18}. Here, Y_A, Y_B and Y_C refers to the admittances looking in respective nodes excluding R_k and Z_k (k = A,B,C)

$$Y_{\text{A}} = \frac{1}{R_{\text{A}}} + \frac{1}{Z_{\text{A}}} + \frac{1}{R_{\text{B}} + \frac{1}{\frac{1}{Z_{\text{CB}}} + \frac{1}{R_{\text{C}} + \frac{1}{\frac{1}{Z_{\text{CC}}}}} + \frac{1}{Z_{\text{CC}} + \frac{1}{R_{\text{C}}}}}} + \frac{1}{Z_{\text{CB}} + \frac{1}{\frac{1}{R_{\text{B}}} + \frac{1}{R_{\text{C}} + \frac{1}{\frac{1}{Z_{\text{CC}}}}} + \frac{1}{Z_{\text{CC}} + \frac{1}{R_{\text{C}}}}}} \tag{6.16}$$

$$Y_{\text{B}} = \frac{1}{R_{\text{B}}} + \frac{1}{Z_{\text{CB}}} + \frac{1}{R_{\text{C}} + \frac{1}{\frac{1}{Z_{\text{CC}}}}} + \frac{1}{Z_{\text{CC}} + \frac{1}{\frac{1}{R_{\text{C}}}}} \tag{6.17}$$

$$Y_{\text{C}} = \frac{1}{R_{\text{C}}} + \frac{1}{Z_{\text{CC}}} \tag{6.18}$$

6.4 Performance Analysis

6.4.1 Conversion Gain

The overall CG of the receiver depends on the gain obtained from various stages of the complete circuitry. Thus, this section discusses the overall CG obtained by analyzing the small-signal models of different stages.

6.4.1.1 LNA Stage Gain

LNA's small-signal model for CG analysis is shown in Figure 6.9. The circuit follows the cascode topology, which combines a common source and a common gate configuration [199].

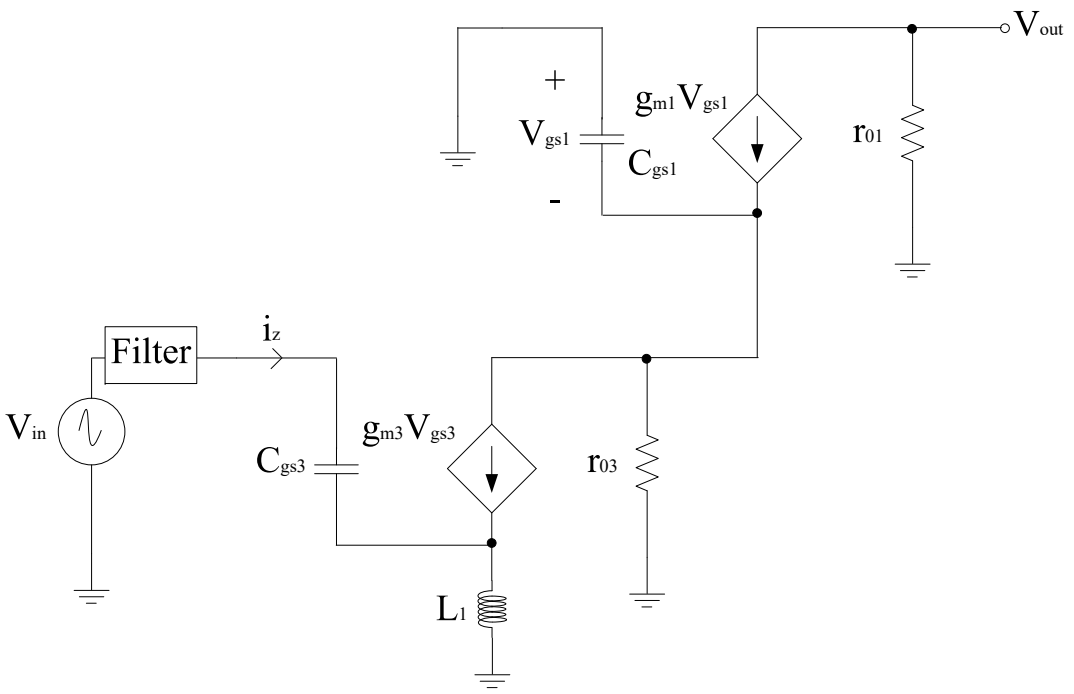


Figure 6.9: Small signal model for half LNA circuit

Besides, V_{gs1} = 0, and V_{gs3} is represented as

$$V_{\text{gs3}} = i_{\text{z}} \cdot \frac{1}{j\omega C_{\text{gs3}}} \tag{6.19}$$

Input impedance, Z_{in} is expressed as

$$Z_{\text{in}} = \frac{g_{\text{m3}} L_1}{C_{\text{gs3}}} + j[\omega(F + L_1) - \frac{1}{\omega C_{\text{gs3}}}] \tag{6.20}$$

Likewise, the output impedance, R_0 is defined as

$$R_0 = r_{03} + r_{01} + g_{\text{m1}} r_{03} r_{01} \approx g_{\text{m1}} r_{03} r_{01} \tag{6.21}$$

Overall gain, A_v is defined as

$$A_{\text{v, LNA}} = \frac{V_{\text{out}}}{V_{\text{in}}} = G_{\text{m}} R_0 = -g_{\text{m3}} g_{\text{m1}} r_{03} r_{01} \tag{6.22}$$

where, G_m = -g_{m3}, due to the common source configuration

6.4.1.2 Mixer Stage Gain

The complete small-signal model of the proposed mixer circuit for CG analysis is shown in Figure 6.10. The load and current mirror sections are simply represented as resistors (r_{010}, r_{015}), whereas, the diode load is represented by r_{011} and $1/g_{m011}$, respectively. Additionally, the active inductor section can be represented as the RL model of the inductor. Thus, the overall circuit behaves like a source-degenerated common source amplifier [205].

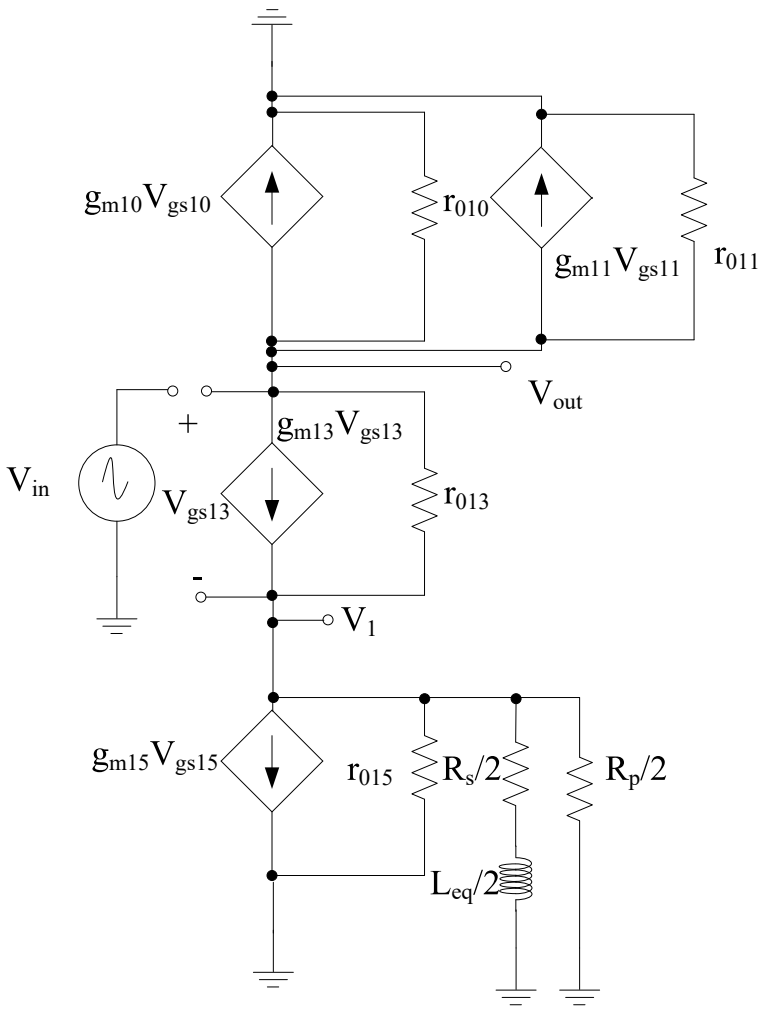


Figure 6.10: Complete small signal model for half mixer circuit

Based on the circuit, the controlled current source is responsible for determining the current through R_S. Thus, V_1 can be expressed as:

$$V_1 = (g_{m13}V_{gs13})R_S = g_{m13}R_S(V_{in} - V_1) \tag{6.23}$$

$$V_1(1 + g_{m13}R_S) = g_{m13}R_S V_{in} \tag{6.24}$$

$$A_1 = \frac{V_1}{V_{in}} = \frac{g_{m13}R_S}{1 + g_{m13}R_S} \tag{6.25}$$

Once V_1 is obtained, the output voltage can be defined as:

$$V_{out} = -R_D(g_{m13}V_{gs13}) = -g_{m13}R_D(V_{in} - V_1) \tag{6.26}$$

where $R_D = r_{010} \parallel r_{011} \parallel \frac{1}{g_{m11}}$

Substituting V_1 from (6.23) to (6.24), we obtain

$$V_{out} = -\frac{g_{m13}R_D}{1 + g_{m13}R_S}V_{in} \tag{6.27}$$

where $R_s = \frac{r_{015}}{2} \parallel (\frac{R_{011}}{2} + jX_{Leq/2}) \parallel \frac{R_P}{2}$

$$A_{v,MIXER} = \frac{V_{out}}{V_{in}} = -\frac{g_{m13}R_D}{1 + g_{m13}R_S} \tag{6.28}$$

Miller's theorem is useful for determining the impact of parasitic capacitors present at C_{gd13} and C_{gs13}. This theorem relates the equivalent capacitance to the gain between the nodes that the capacitor is tied to. Assuming capacitances (C_{in}, C_1 and C_0) are present at the gate, source, and drain terminals of the transistor M_3, which can be expressed by Miller's theorem as

$$C_{in} = C_{gs13}(1 - A_1) + C_{gd13}(1 - A_0) \tag{6.29}$$

$$C_0 = C_{gd13}(1 - \frac{1}{A_0}) \tag{6.30}$$

$$C_1 = C_{gs13}(1 - \frac{1}{A_1}) \tag{6.31}$$

6.4.1.3 First-IF Amplifier Gain

The small signal model of 1st-IF Amplifier is shown in Figure 6.11. For analysis, the channel length modulation and body effects are ignored [199, 293]. By applying KCL at nodes (b) and

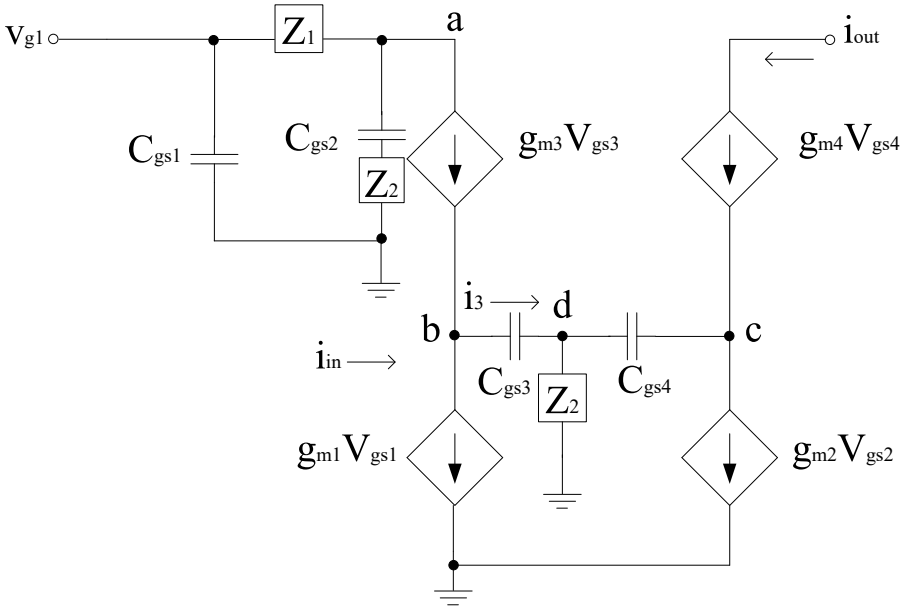


Figure 6.11: Small signal model of 1st-IF Amplifier

(c), we obtain

$$i_{\text{in}} + g_{\text{m3}} V_{\text{gs3}} = g_{\text{m1}} V_{\text{gs1}} + i_1 \tag{6.32}$$

$$g_{\text{m4}} V_{\text{gs4}} + i_1 = g_{\text{m2}} V_{\text{gs2}} \tag{6.33}$$

Upon substituting i_1 from (6.33) to (6.32), we obtain

$$i_{\text{in}} + g_{\text{m3}} V_{\text{gs3}} = g_{\text{m1}} V_{\text{gs1}} + g_{\text{m2}} V_{\text{gs2}} - g_{\text{m4}} V_{\text{gs4}} \tag{6.34}$$

Neglecting channel-length modulation effect, the output current i_{out} can be expressed as

$$i_{\text{out}} = g_{\text{m4}} V_{\text{gs4}} \tag{6.35}$$

Substituting i_{out} from (6.35) to (6.34), we obtain

$$i_{\text{in}} + g_{\text{m3}} V_{\text{gs3}} = g_{\text{m1}} V_{\text{gs1}} + g_{\text{m2}} V_{\text{gs2}} - i_{\text{out}} \tag{6.36}$$

where

$$V_{\text{gs1}} = V_{\text{gs2}}(\frac{1}{1 + sC_{\text{gs1}}Z}) \tag{6.37}$$

where Z refers to L_1. Likewise, upon applying KCL at node (c), we obtain

$$(v_{\text{s4}} - v_{\text{g4}})sC_{\text{gs4}} + g_{\text{m2}}V_{\text{gs2}} = i_{\text{out}} \tag{6.38}$$

Thus, V_{gs2} is expressed as

$$V_{\text{gs2}} = (\frac{i_{\text{out}}}{g_{\text{m2}}}) + (\frac{sC_{\text{gs4}}V_{\text{gs4}}}{g_{\text{m2}}}) \tag{6.39}$$

Substituting V_{gs4} from (6.35) to (6.39), we get

$$V_{\text{gs2}} = (\frac{i_{\text{out}}}{g_{\text{m2}}})(1 + \frac{sC_{\text{gs4}}}{g_{\text{m4}}}) \tag{6.40}$$

Substituting equation (6.40) into (6.37), we get

$$V_{\text{gs1}} = (\frac{i_{\text{out}}}{g_{\text{m2}}(1 + sC_{\text{gs1}}Z)})(1 + \frac{sC_{\text{gs4}}}{g_{\text{m4}}}) \tag{6.41}$$

Applying KCL at node (d), we obtain

$$i_1 = -V_{\text{gs3}}(sC_{\text{gs3}} + \frac{1}{sL}) = sC_{\text{gs4}}V_{\text{gs4}} \tag{6.42}$$

$$i_1 = -V_{\text{gs3}}(sC_{\text{gs3}} + \frac{1}{sL}) = i_{\text{out}} \tag{6.43}$$

$$V_{\text{gs3}} = -i_{\text{out}}(\frac{sL}{s^2C_{\text{gs3}}L + 1}) \tag{6.44}$$

Substituting (6.35), (6.37), and (6.40) into (6.34), we obtain

$$i_{\text{in}} = i_{\text{out}}[(\frac{sL}{s^2C_{\text{gs3}}L + 1}) + g_{\text{m1}}(\frac{1}{g_{\text{m2}}(1 + sC_{\text{gs1}}Z)})(1 + \frac{sC_{\text{gs4}}}{g_{\text{m4}}}) + (1 + \frac{sC_{\text{gs4}}}{g_{\text{m4}}}) - 1] \tag{6.45}$$

Thus, the overall conversion gain, $A_{I,\,IF1}$ can be expressed as

$$A_{\mathrm{I,IF1}} = \frac{i_{\mathrm{out}}}{i_{\mathrm{in}}} = \frac{1}{[(\frac{sL}{s^2 C_{\mathrm{gs3}} L+1}) + g_{\mathrm{m1}}(\frac{1}{g_{\mathrm{m2}}(1+sC_{\mathrm{gs1}}Z)})(1+\frac{sC_{\mathrm{gs4}}}{g_{\mathrm{m4}}}) + (1+\frac{sC_{\mathrm{gs4}}}{g_{\mathrm{m4}}}) - 1]} \tag{6.46}$$

6.4.1.4 Second-IF Amplifier Gain

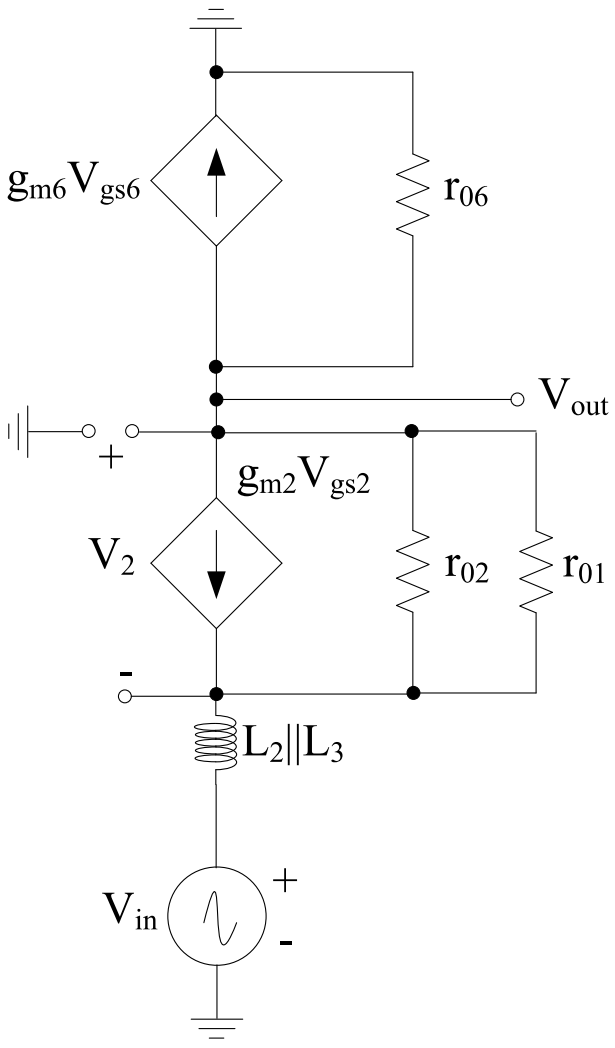


Figure 6.12: Small signal model of 2nd-IF Amplifier

The small signal model of 2nd-IF Amplifier is shown in Figure 6.12. Based on the model, the current through L is expressed as $\frac{-V_{\mathrm{out}}}{r_{06}}$ [199]:

$$V_2 - \frac{V_{\mathrm{out}}}{r_{06}} L + V_{\mathrm{in}} = 0 \tag{6.47}$$

where L= L_2|| L_3. Similarly, the current through r is expressed as $\frac{-V_{\text{out}}}{r_{06}} - g_{\text{m2}}V_{\text{gs2}}$:

$$r(\frac{-V_{\text{out}}}{r_{06}} - g_{\text{m2}}V_{\text{gs2}}) - (\frac{V_{\text{out}}}{r_{06}})sL + V_{\text{in}} = V_{\text{out}} \tag{6.48}$$

where r = r_{01}|| r_{02} and V_{gs2}=V_2. Replacing r and L in equation (6.48), we get

$$(r_{01}||r_{02})(\frac{-V_{\text{out}}}{r_{06}} - g_{\text{m2}}V_{\text{gs2}}) - (\frac{V_{\text{out}}}{r_{06}})(sL_2||sL_3) + V_{\text{in}} = V_{\text{out}} \tag{6.49}$$

Substituting V_2 from (6.47)-(6.49), we obtain

$$(r_{01}||r_{02})(\frac{-V_{\text{out}}}{r_{06}} - g_{\text{m2}}(\frac{V_{\text{out}}}{r_{06}}(sL_2||sL_3) - V_{\text{in}})) - (\frac{V_{\text{out}}}{r_{06}})(sL_2||sL_3) + V_{\text{in}} = V_{\text{out}} \tag{6.50}$$

$$\begin{aligned}(r_{01}||r_{02})(\frac{-V_{\text{out}}}{r_{06}}) - g_{\text{m2}}(r_{01}||r_{02})(\frac{V_{\text{out}}}{r_{06}})(sL_2||sL_3) + g_{\text{m2}}V_{\text{in}}(r_{01}||r_{02})- \\ \frac{-V_{\text{out}}}{r_{06}}(sL) + V_{\text{in2}}||sL_3) + V_{\text{in}} = V_{\text{out}}\end{aligned} \tag{6.51}$$

$$V_{\text{out}}[1 + \frac{r_{01}||r_{02}}{r_{06}} + \frac{r_{01}||r_{02}}{r_{06}}(sL_2||sL_3)g_{\text{m2}} + \frac{sL_2||sL_3}{r_{06}}] = V_{\text{in}}[1 + g_{\text{m2}}(r_{01}||r_{02})] \tag{6.52}$$

Overall conversion gain, $A_{\text{v,IF2}}$ is expressed as

$$A_{\text{v,IF2}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 + g_{\text{m2}}(r_{01}||r_{02})}{r_{06} + (r_{01}||r_{02}) + g_{\text{m2}}(r_{01}||r_{02})(sL_2||sL_3) + (sL_2||sL_3)} \tag{6.53}$$

6.4.2 Noise Figure

The noise models of different receiver blocks are shown in Figure 6.13. All models contain only transistors and resistors as all passive elements are considered ideal. Additionally, thermal noise is considered as the main source for obtaining the noise figure, based on which the power spectral density of each stage is obtained while considering only the resistors and transistors, respectively. Based on this idea, the power spectral density of LNA stage is expressed as [197, 232, 41]

$$\overline{V^2{}_{\text{n,LNA}}} = \overline{V^2{}_{\text{n,M}_1}} + \overline{V^2{}_{\text{n,M}_2}} + \overline{V^2{}_{\text{n,M}_3}} + \overline{V^2{}_{\text{n,M}_4}} = \frac{4kT\gamma}{g_{\text{m1}}} + \frac{4kT\gamma}{g_{\text{m2}}} + \frac{4kT\gamma}{g_{\text{m3}}} + \frac{4kT\gamma}{g_{\text{m4}}} \tag{6.54}$$

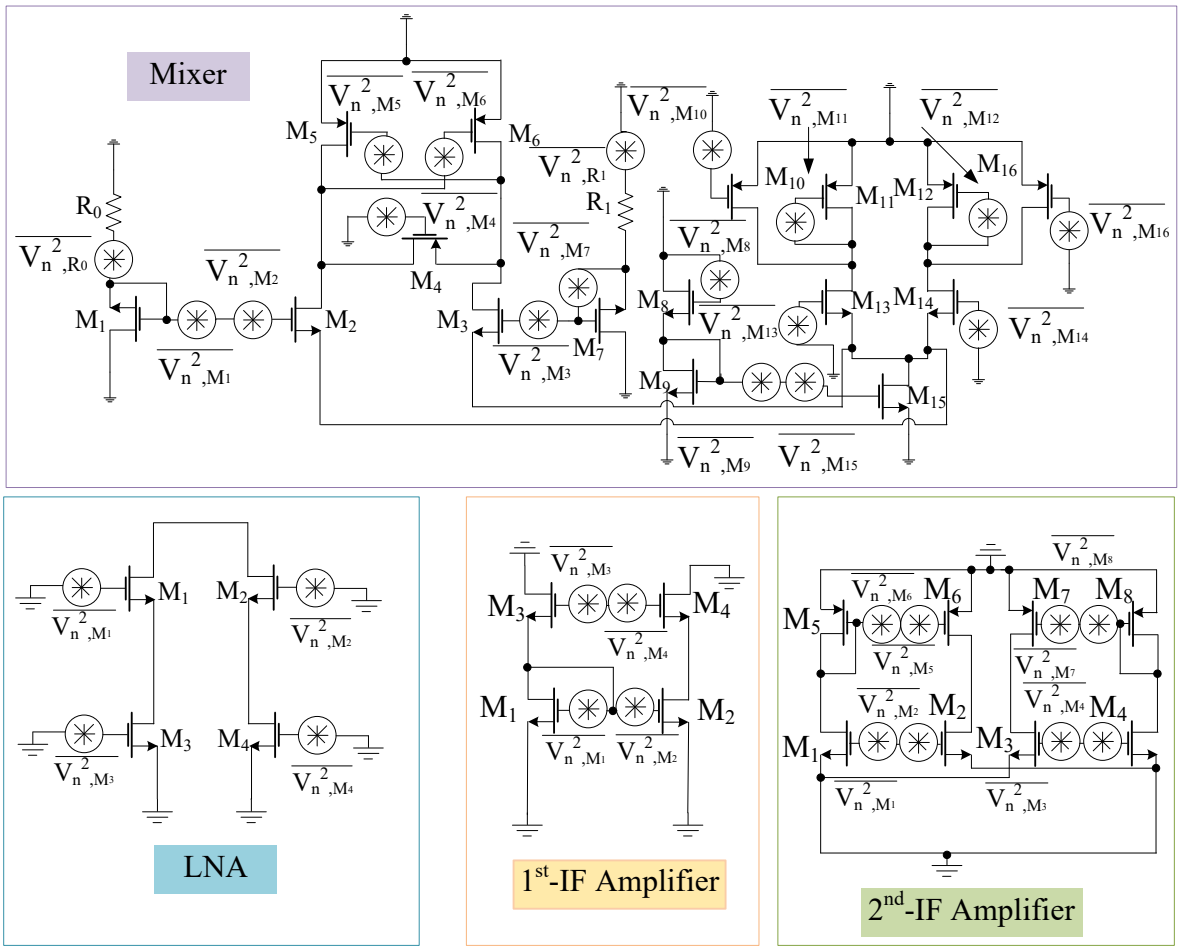


Figure 6.13: Receiver Noise Model

Likewise, the power spectral density of the mixer circuit is the combination of the power spectral density obtained from all stages present within the mixer design. Equation (6.55) represents the power spectral density of the mixer circuit, which combines the mixing stage, load stage, current mirror stage, and active inductor stage, respectively [197].

$$\overline{V^2}_{\text{n,MIXER}} = \overline{V^2}_{\text{n,M}} + \overline{V^2}_{\text{n,L}} + \overline{V^2}_{\text{n,CM}} + \overline{V^2}_{\text{n,AI}} \tag{6.55}$$

Thus, the power spectral density of the mixing stage is expressed as

$$\overline{V^2}_{\text{n,M}} = \overline{V^2}_{\text{n,M}_{13}} + \overline{V^2}_{\text{n,M}_{14}} = \frac{4kT\gamma}{g_{\text{m13}}} + \frac{4kT\gamma}{g_{\text{m14}}} \tag{6.56}$$

Likewise, the power spectral density of the load stage is defined as [197]

$$\overline{V^2{}_{\mathrm{n,L}}} = \overline{V^2{}_{\mathrm{n,M_{10}}}} + \overline{V^2{}_{\mathrm{n,M_{11}}}} = \frac{4kT\gamma}{g_{\mathrm{m10}}} + \frac{4kT\gamma}{g_{\mathrm{m11}}} \tag{6.57}$$

Besides, the power spectral density of the current mirror stage is given as [197]

$$\overline{V^2{}_{\mathrm{n,CM}}} = \overline{V^2{}_{\mathrm{n,M_8}}} + \overline{V^2{}_{\mathrm{n,M_9}}} + \overline{V^2{}_{\mathrm{n,M_{15}}}} = \frac{4kT\gamma}{g_{\mathrm{m8}}} + \frac{4kT\gamma}{g_{\mathrm{m9}}} + \frac{4kT\gamma}{g_{\mathrm{m15}}} \tag{6.58}$$

Finally, the power spectral density of the active inductor stage is

$$\overline{V^2{}_{\mathrm{n,AI}}} = 4kTR_0 + \frac{4kT\gamma}{g_{\mathrm{m1}}} + \frac{4kT\gamma}{g_{\mathrm{m2}}} + \frac{4kT\gamma}{g_{\mathrm{m4}}} + \frac{4kT\gamma}{g_{\mathrm{m5}}} \tag{6.59}$$

Similarly, the power spectral density of the 1st-IF amplifier is expressed as

$$\overline{V^2{}_{\mathrm{n,IF1}}} = \overline{V^2{}_{\mathrm{n,M_1}}} + \overline{V^2{}_{\mathrm{n,M_2}}} + \overline{V^2{}_{\mathrm{n,M_3}}} + \overline{V^2{}_{\mathrm{n,M_4}}} = \frac{4kT\gamma}{g_{\mathrm{m1}}} + \frac{4kT\gamma}{g_{\mathrm{m2}}} + \frac{4kT\gamma}{g_{\mathrm{m3}}} + \frac{4kT\gamma}{g_{\mathrm{m4}}} \tag{6.60}$$

Moreover, the power spectral density of the 2nd-IF amplifier is expressed as

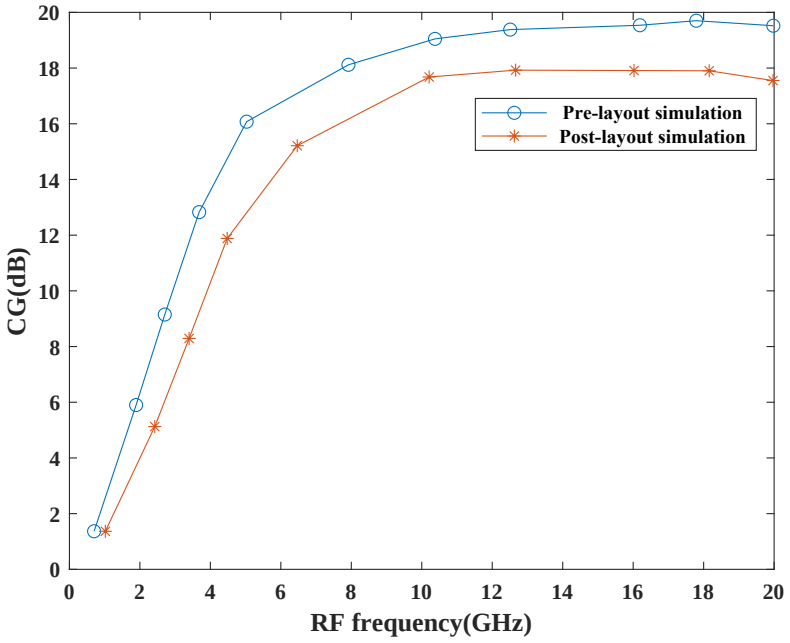
$$\overline{V^2{}_{\mathrm{n,IF2}}} = \overline{V^2{}_{\mathrm{n,M_1}}} + \overline{V^2{}_{\mathrm{n,M_2}}} + \overline{V^2{}_{\mathrm{n,M_3}}} + \overline{V^2{}_{\mathrm{n,M_4}}} + \overline{V^2{}_{\mathrm{n,M_5}}} + \overline{V^2{}_{\mathrm{n,M_6}}} + \overline{V^2{}_{\mathrm{n,M_7}}} + \overline{V^2{}_{\mathrm{n,M_8}}} = \frac{4kT\gamma}{g_{\mathrm{m1}}} + \frac{4kT\gamma}{g_{\mathrm{m2}}} + \frac{4kT\gamma}{g_{\mathrm{m3}}} + \frac{4kT\gamma}{g_{\mathrm{m4}}} + \frac{4kT\gamma}{g_{\mathrm{m5}}} + \frac{4kT\gamma}{g_{\mathrm{m6}}} + \frac{4kT\gamma}{g_{\mathrm{m7}}} + \frac{4kT\gamma}{g_{\mathrm{m8}}} \tag{6.61}$$

Hence, the overall NF of the receiver is given by

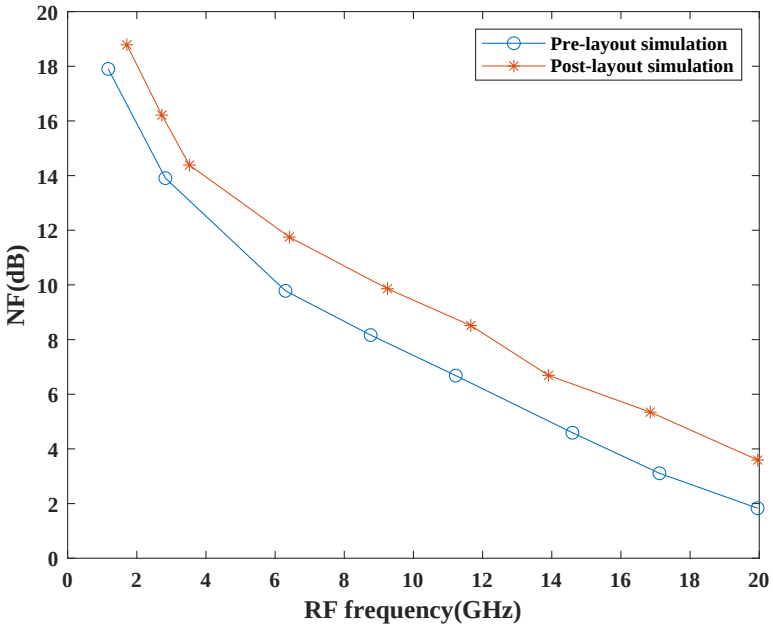
$$NF = \overline{V^2{}_{\mathrm{n,LNA}}} + \overline{V^2{}_{\mathrm{n,MIXER}}} + \overline{V^2{}_{\mathrm{n,IF1}}} + \overline{V^2{}_{\mathrm{n,IF2}}} \tag{6.62}$$

6.5 Results and Discussion

The receiver circuit has been developed using 130 nm Silterra process technology while covering an area of 4 mm^2. As discussed in previous sections, the design circuitry is divided into different sections, such as mixers, LNAs, filters, and IF amplifiers. The reconfigurable filter consists of



(a)



(b)

Figure 6.14: Performance plots (a) Pre and post layout CG (b) Pre and post layout NF

spiral inductors and capacitors. Accurate inductance values are provided by inductors, which are capable of achieving the highest Q at a desired operating frequency. In addition, to achieve tuning capacitances, variable capacitors, i.e., varactors, are used. Polyphase filters are also part of the circuit, which is developed using a combination of resistors and capacitors. Besides, the

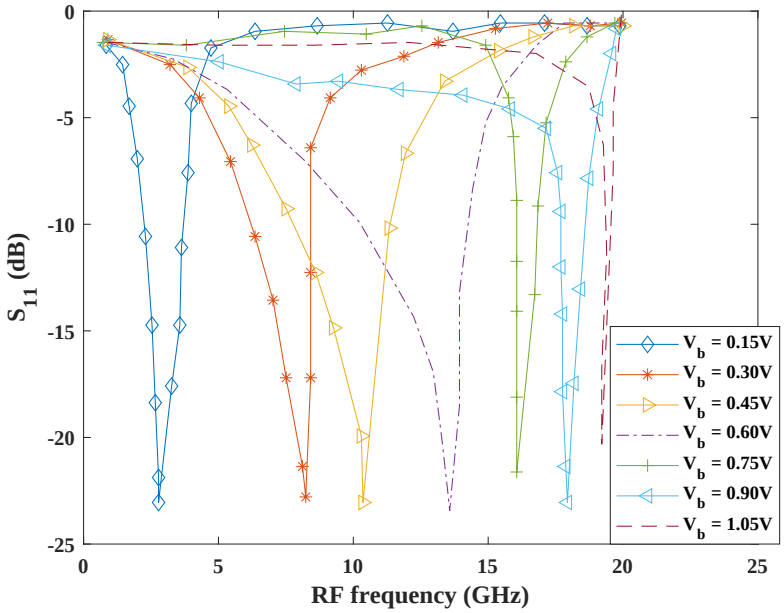


Figure 6.15: S_{11} at different bias voltages

bias voltage is responsible for tuning the circuit's behavior. Thus, for various bias voltages (V_b) ranging from 0.15 V-1.05 V, several performance metrics such as CG, NF, IIP3, S_{11} and IRR has been obtained. The main benefit of bias voltage variation is to maintain good tuning behaviour within the receiver. Figure 6.14 depicts the overall performance of the receiver in terms of various parameters such as CG and NF. Thus, based on the observation, it has been found that the design attains high CG within the entire band of operation while attaining a maximum gain of 20 dB during pre-layout simulations and degraded by 2 dB after post-layout simulation. The overall performance gets affected due to parasitic effects of the parasitic components and also due to the quality factor of inductors present within the circuitry. By varying the width-to-length (W/L) ratios of different transistors, it is possible to attain varied tuned centre frequencies and performance results. In addition to this, the receiver achieves excellent IIP3 performance during pre and post-layout simulations, as shown in Figure 6.16, while attaining a maximum IIP3 of 32 dBm during pre-simulation and 28 dB during post-layout simulations. The receiver attains high IIP3 within the entire band of operation due to the presence of active inductor circuits within the mixer circuitry. The pre and post-layout simulation results of NF of the receiver are depicted in Figure 6.14 which is <2 dB at the maximum frequency of operation during pre-layout simulation.

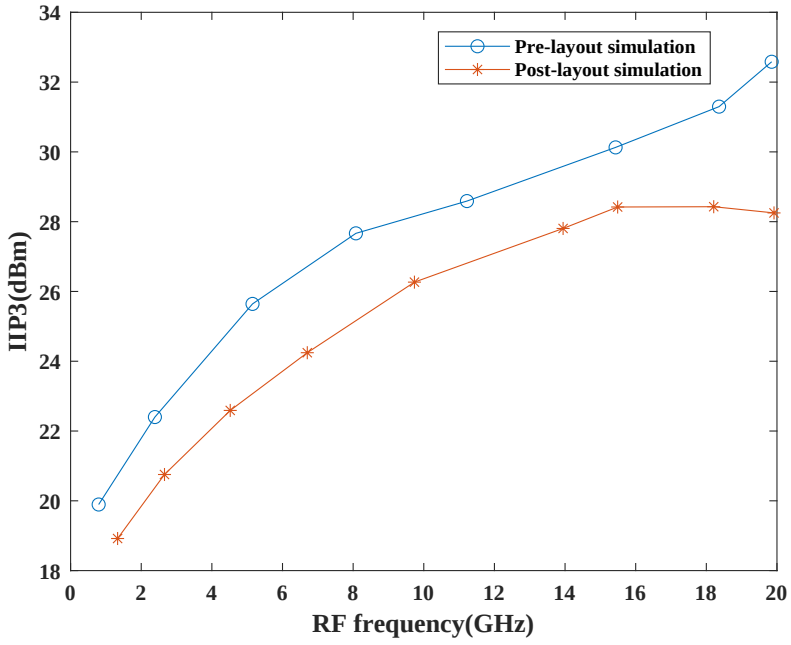
Table 6.1: Performance Comparison

Ref	Freq(GHz)	Technology(nm)	CG(dB)	NF(dB)	IIP3(dBm)	IRR(dB)	Area(mm^2)	P_{diss}(mW)
This work	0.9-20	130	22.9	<5	32	30	4	320
[256]	0.402-0.405	180	40	9.2	Nil	Nil	0.873	0.16
[216]	5	180	28	9.7	-7.8	Nil	2.2	43.9
[143]	2.4	28	60	6	-16	Nil	0.48	0.9
[294]	24.5-43.5	45	35.2	3.2-6.1	Nil	32-56	0.77	60
[261]	3-6	40	>12.8	<5.8	>15.1	Nil	Nil	64.1-69.6
[295]	0.1-0.6	40	26.4-30.1	5.8/6.5	5.8	-20.1/-15.1	>34	41.1
[296]	4	65	25	23	Nil	Nil	1.1	0.267
[297]	0.5-1.2	65	35	6.7	10	>0	0.47	29.4
[253]	0.8-4	130	>25	3.8	-3.5	>38	33	0.25

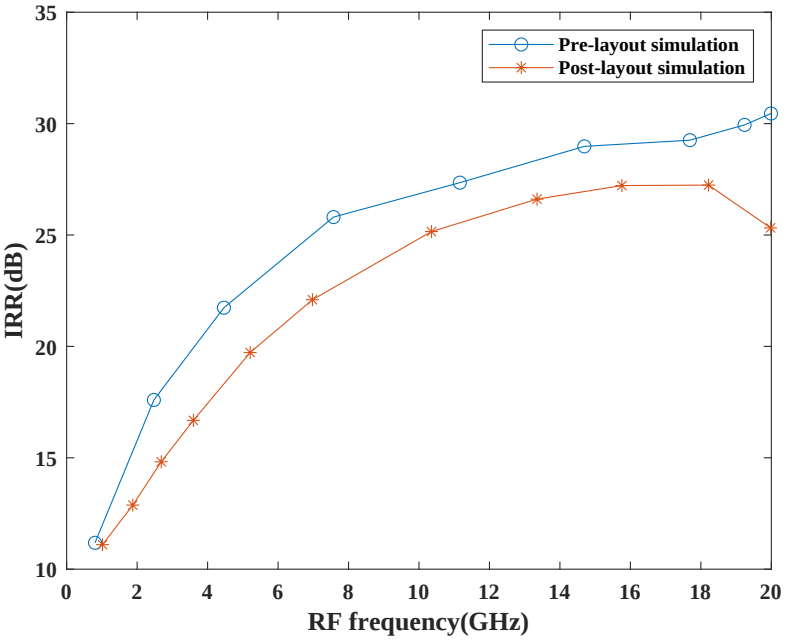
NF performance got raised by 2 dB after post-layout simulation. This is due to the parasitic effects of the parasitic components present within the receiver circuitry. Additionally, other components within the circuitry also get affected, such as resistors, transistors, and obtained CG. IRR is another critical parameter that must be considered while proposing any receiver circuits, which is obtained for the proposed receiver as depicted in Figure 6.16. The image rejection is possible by using polyphase filters within the proposed receiver. As a result, at the highest frequency of 20 GHz, the receiver achieves a high IRR of 30 dB during pre-layout simulations and 25 dB during post-layout simulations, as shown in Figure 6.16. Likewise, the return loss $|S_{11}|$ as shown in Figure 6.15 is below -10 dBm from 0.9 to 20 GHz, providing good matching in the desired band. Furthermore, the layout of the proposed receiver is shown in Figure 6.17. The design includes an LNA, a mixer, a reconfigurable filter, and IF Amplifiers, respectively. The reconfigurable filters are responsible for providing suitable reconfiguration within the desired band, i.e., 0.9-20 GHz. Additionally, the circuit also consumes high power due to the presence of a large number of inductors within the LNA filtering stage.

Table 6.1 summarizes different receiver designs, each operating in a wideband. The comparisons are done by selecting the works that attain high performance in terms of CG, NF, IRR and IIP3, respectively. From Table 6.1 it has been found that the works have been implemented in different CMOS technologies, and most of the receivers are operating within a wideband. In Table 6.1, the minimum NF is 3.8 dB, and the maximum IIP3 is 32 dBm. Furthermore, the overall design area depends on the design complexity.

To further improve the performance of the proposed mixer, PSO has been implemented on the



(a)



(b)

Figure 6.16: Performance plots (a) Pre and post layout IIP3 (b) Pre and post layout IRR

mixer as discussed in Chapter 7, Section 7.7.4. The optimized results are obtained and compared with the simulated results. Based on the observation, it has been found that performance of the proposed mixer has significantly improved.

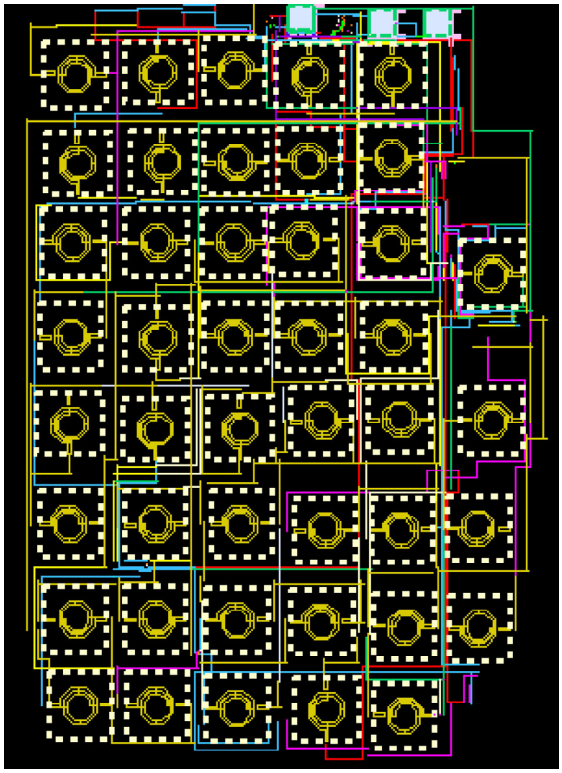


Figure 6.17: Receiver layout

6.6 Reliability Performance

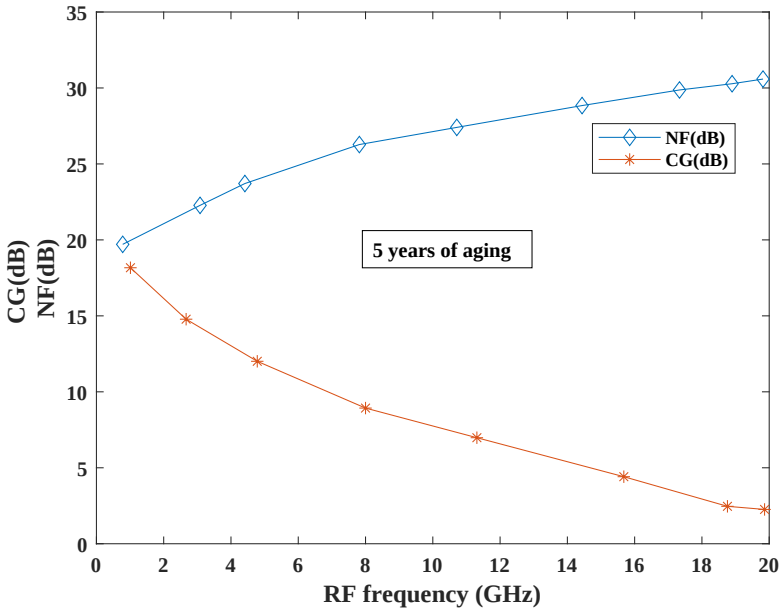


Figure 6.18: Performance degradation in terms of CG and NF

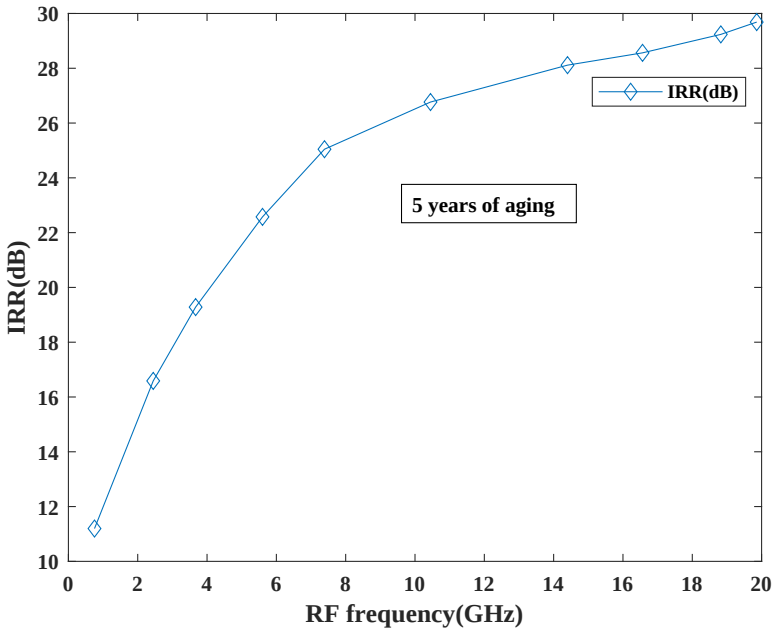


Figure 6.19: Performance degradation in terms of IRR

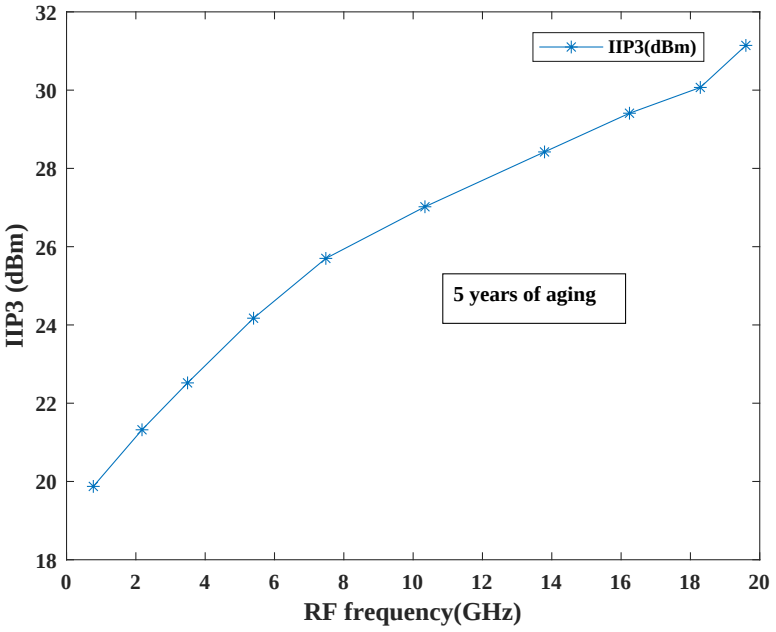


Figure 6.20: Performance degradation in terms of IIP3

Due to design procedure constraints and guidelines, traditional designs are less reliable. However, recent advancements demand reliability analysis of ongoing projects due to time, cost, size, and stringent profile constraints. The Relxpert tool created by Cadence is helpful in modelling the degradation of PFET and NFET devices where the performance is evaluated on the basis of

stress period and bias. In a typical corner simulation, the output of RelXpert may be observed as a "time coordinate", travelling in a slow corner. This technique is helpful for designers in analyzing the degradation of circuits in the early design stages. Based on this idea, the degradation performance of the proposed receiver has been evaluated in terms of CG, NF, IRR, and IIP3, respectively. The reliability performance of CG and NF can be seen from Figure 6.18. Based on the curves, it has been found that NF degradation is significantly less as it reaches 2.25 dB after 5 years of aging, and at present, this is around 1.87 dB. Similarly, CG has been degraded to 7.6 dB compared to the simulation results. Figure 6.19 depicts IRR performance after 5 years of aging. Based on the curve, it has been observed that IRR shows significantly less degradation, and the maximum IRR attained is 29.6 dB. Finally, IIP3 performance of the receiver is depicted in Figure 6.20. Based on the observation, it has been found that the IIP3 reached 31 dBm after 5 years of aging, which is still significantly less compared to the simulation results.

6.7 Summary

This chapter proposes a novel reconfigurable receiver designed and simulated in 130 nm Silterra technology. The adopted LNA follows the cascode architecture because cascode stages have the ability to attain large CG for a single-stage because of the large impedance at the output. Likewise, 8^{th}-order tunable filters are employed at the LNA stage for maintaining high-frequency reconfiguration. The polyphase filter is also a part of the receiver circuitry, responsible for choosing the desired signals. Based on the simulation results, it has been found that the proposed receiver design shows improved CG, IIP3 due to the presence of an active-inductor-based mixer stage. The current bleeding technique within the mixer stage is responsible for enhancing the overall CG and NF performance within the mixer circuitry, which in turn improves the performance within the receiver circuitry. Based on the simulation results, it has been found that with the application of a 1.2V power supply, the design attains a maximum gain of 22.9 dB. The design also attains low NF and good return loss within an entire band of operation, where the input return loss is <10 dB, and NF is <5 dB at the maximum frequency. The design

also shows a high IRR of 30 dB within the entire band. Thus, it can be concluded that the proposed reconfigurable receiver is a promising candidate for SDR applications. Although the proposed receiver architecture attains high performance in terms of various performance parameters, it is still possible to further improve the performance of these architectures by using optimization approaches. Thus, in Chapter 7, the PSO technique has been applied to all the proposed architectures discussed in this thesis, and the performance has been tested.

Chapter 7

Particle Swarm Optimization of Designs for Software Defined Radios

7.1 Introduction

The current wireless industry demands advanced receivers with reconfigurable components that can support several wireless standards. SDRs proved to be one of the promising candidates as they offer high flexibility by enabling various operations within the desired band while having a single circuitry. Earlier SDRs suffer from high power consumption problems, which necessitate the use of discrete-time and mixed-signal systems for frequency conversion purposes. Consequently, mixers become an essential component of SDR, responsible for converting RF to a smaller band at IF in comparison to the input bandwidth and relaxing ADC requirements [38, 298].

It is desirable to have reconfigurable front-ends for obtaining a compact, and cost-effective architectures [299]. However, the inadequate number of front-ends with high reconfigurability and high-performance capabilities became necessary to develop novel structures with good tuning or switching capability. Through a careful literature review, it was found that various approaches can be applied to enhance the overall performance of analogue front-ends such as g_m-boosting, inductive peaking, current bleeding, active inductor, etc as discussed in Chapter 2.

However, it is difficult to maintain high performance in terms of all performance metrics. Based on the recent study in [300], it has been found that Particle Swarm Optimization (PSO) has the capability to enhance the analogue front-ends' performance. This chapter starts with an overview of optimization, followed by optimization methods and functions. Moreover, it discusses PSO and its implementation on the proposed mixers and receiver architectures discussed in this thesis. Upon observation, it has been found that the optimized designs showed better performance compared to the unoptimized ones.

7.2 Optimization

Optimization is the process of determining the best possible solution to a particular problem under specific conditions. For example, a testing manager in a particular firm is interested in making several technical and managerial plans. The main aim of the plan will be to maximize the profit or minimize the efforts, which can be done with the help of optimization. In general, maximizing any function is mathematically equivalent to the minimization of its additive inverse. Optimization problems can be classified as linear or non-linear. When an optimization problem is chosen for the real-world scenario, and it is possible to define the objective function as a linear function of unknown variables, constraints such as linear equality, or inequalities, this is called linear optimization. However, if the objective functions and constraints are non-linear, the optimization is termed as non-linear optimization [301].

Depending on the characteristics, optimization problems can be classified into the following categories: constrained optimization, unconstrained optimization, and dynamic optimization.

7.2.1 Constrained Optimization

When optimization problems require non-negative decision variables, the problem is referred to as a constrained optimization problem [301]. The function and conditions are defined below:

$$minimize \quad f(x), x = (x_1, x_2, x_3, ...x_{\mathrm{n}}) \tag{7.1}$$

subject to

$$g_{\mathrm{m}}(x) \leq 0, m = 1, 2, ..., n_{\mathrm{g}} \tag{7.2}$$

$$h_{\mathrm{m}}(x) = 0, m = n_{\mathrm{g}} + 1, n_{\mathrm{g}} + n_{\mathrm{h}} \tag{7.3}$$

where n_g, n_h refer to inequality and equality constraints.

7.2.2 Unconstrained Optimization

When the optimization problem does not have restrictions on the values and can be easily assigned to different variables of the problem. The whole search space will be the feasible space [301]. These types of optimization problems are termed as unconstrained optimization problems as defined below:

$$minimize \quad f(x), x \in R^{\mathrm{n}} \tag{7.4}$$

where n refers to the dimension of x.

7.2.3 Dynamic Optimization

The optimization problems where objective functions change over a period of time and these changes will affect the optima position [301]. Such problems are referred to as dynamic optimization problems as mentioned below:

$$minimize \quad f(x, \varpi(t)) \tag{7.5}$$

where x = (x_1, x_2,...,x_n), ϖ(t) = (ϖ_1(t),ϖ_2(t),...,$\varpi_{n\varpi}$(t)) subject to

$$g_{\mathrm{m}}(x) \leq 0, m = 1, 2, ..., n_{\mathrm{g}} \tag{7.6}$$

$$h_{\mathrm{m}}(x) = 0, m = n_{\mathrm{g}} + 1, n_{\mathrm{g}} + n_{\mathrm{h}} \tag{7.7}$$

$\forall$x $\in$ R^n where ϖ(t) refers to the vector of time-dependent objective function control parameters,

$x^*(t)$ refers to the optimum obtained at time step t.

7.3 Optimization methods

Global or local optimization methods are useful for solving various optimization problems [301].

7.3.1 Global Optimization

Global optimization is a minimization approach that is defined by x^* in such a way that

$$f(x^*) \leq f(x) \tag{7.8}$$

where $f(x^*)$ refers to the global minimum and x^* is the global minimizer.

$\forall x \in S$, where S refers to the search space and $S = R^n$ for unconstrained problems.

7.3.2 Local Optimization

Local optimization is another minimization approach that is defined by

$$f(x^*) \leq f(x) \tag{7.9}$$

$\forall x \in L$, where L refers to the region and $L \subseteq R^n$.

7.4 Optimization Functions

Various functions are used to solve optimization problems [301]. The common optimization functions include uniform distribution function, sigmoid function, Rosebrock function, Rastigin function, De-Jong multi-sphere parametric function, and Shaffer's function.

7.4.1 Uniform Distribution Function

Uniform distribution can be denoted as a rectangular distribution. In this type of distribution, the probability of occurrence is the same for all values of x. Throwing a dice is one of the common examples of this distribution where the probability of occurrence of each number is the same at a particular instant. In general, the distribution is defined in terms of U(a,b), where a and b refer to the minima and maxima [301]. Thus, distribution functions on a interval [a,b] are given by

$$f(x) = 0 \quad for \quad x < a \tag{7.10}$$

$$f(x) = \frac{1}{b-a} \quad for \quad a \leq x \leq b \tag{7.11}$$

$$f(x) = 0 \quad for \quad x > b \tag{7.12}$$

Likewise,

$$F(x) = 0 \quad for \quad x < a \tag{7.13}$$

$$F(x) = \frac{x-a}{b-a} \quad for \quad a \leq x \leq b \tag{7.14}$$

$$F(x) = 0 \quad for \quad x > b \tag{7.15}$$

7.4.2 Sigmoid Function

Sigmoid function can also be known as logistic function [301] as

$$s(t) = \frac{1}{1+e^{-t}} \tag{7.16}$$

s(t) is a monotonically increasing function with

$$s(t) = 1 \quad if \quad t \to \infty \tag{7.17}$$

$$s(t) = \frac{1}{2} \quad t = 0 \tag{7.18}$$

$$s(t) = 0 \quad if \quad t \to -\infty \tag{7.19}$$

Due to the monotonically increasing nature of the sigmoid function, s(t) is expressed as

$$s(t) = s(t+ \in), \in > 0 \tag{7.20}$$

7.4.3 Rosenbrock Function

Rosenbrock's function standard formulation covers two design variables, which compute a single objective function. It can also be considered as a least-square optimization problem that has two residuals for minimization as the objective function and is expressed as the sum of squared terms [300]. The function is well-suited for minimization problems and is described as below:

$$f(x) = \sum_{i}^{N-1} [100(x_{\text{i+1}} - {x_{\text{i}}}^2)^2 + (1 - x_{\text{i}})^2] \tag{7.21}$$

where x = (x_1 , x_2, x_3, ...x_n) $\in R^n$.

7.4.4 Rastigin Function

Rastigin function is another optimization function which has several local minima. Although it is multimodal, the minima locations are regularly distributed [300].

$$f(x) = 10d + \sum_{i=1}^{d} [{x_{\text{i}}}^2 - 10cos(2\pi x_{\text{i}})] \tag{7.22}$$

The function is normally applied on the hypercube where $x_i \in$ [-5.12,5.12] for all i = 1,...d.

7.4.5 De-Jong multi-sphere Optimization Function

De-Jongs multi-sphere is a parametric optimization based spherical model or function that is unimodal, continuous, and convex in nature [300], where the function is defined as

$$f(x) = \sum_{i-1}^{n} {x_{\text{i}}}^2 \tag{7.23}$$

7.4.6 Shaffer's Function

Shaffer's function covers several oscillations or peaks that are difficult for hill-climbing techniques for convergence [300]. The main advantage of this function is that it is designed to have its peak at the origin with a value as 1 and the function is defined as

$$f(x) = 0.5 + \frac{sin^2(x_1^2 - x_2^2) - 0.5}{[1 + 0.01(x_1^2 + x_2^2)]^2} \tag{7.24}$$

The function is applied on the square where $x_i \in$ [-100,100], for all i = 1,2.

7.5 Particle Swarm Optimization

PSO is an evolutionary optimization technique that depends on the behaviour of several insects and animals such as bees, ants, fishes, and birds, which cooperate in a smart swarm environment [300, 302]. The realization process follows simple rules, models, and programs. The behaviour rules of different species can be simple, but swarm behaviour can be complex. As per Reynolds in [300], three vectors are considered as simple rules on boid : (a) step away from any nearest agent; (b) move towards the destination, and (c) move towards the swarm center.

Every species behaviour can be easily modeled with the help of simplified vectors. Based on this basic background of PSO, Kennedy and Eberhart in [300] proposed PSO with the help of simulations in two-dimensional space. In this algorithm, the position and velocity of of each species are expressed in terms of two vectors $\vec{v}$, $\vec{s}$, respectively. Based on the study, the modified position of the species is realized by iterating the two update equations, i.e., the velocity update equation (7.25) and position update equation (7.26) defined below.

$$v_i^{k+1} = wv_i^k + c_1 rand_1(pbest_i - s_i^k) + c_2 rand_2(gbest_i - s_i^k) \tag{7.25}$$

where v_i^k refers to the i^{th}-agent velocity at k^{th}- iteration, w is weighting function, c_1, c_2 are acceleration coefficients, rand is a random number generator between 0 and 1, s_i^k is current position of the i^{th}-agent at k^{th} iteration, $pbest_i$ is the pbest of agent i, and gbest is the global best

of the group.

Similarly, the position of each agent is expressed as:

$$s_i^{k+1} = s_i^{k} + v_i^{k+1} \tag{7.26}$$

Furthermore, the optimization of the objective function is done in this approach, where the personal best value (pbest) of all species along with their x,y positions are well known by the species themselves. Additionally, the best value within a group (gbest) is also known among all pbest values at a particular instant. Besides, the process of modification of the searching point followed by PSO is shown in Figure 7.1. The notations used in the plot are depicted in Table 7.1.

Table 7.1: PSO Terminology

PSO Notations	Explanation
s^k	current search point
s^{k+1}	modified search point
v^k	current velocity
v^{k+1}	updated velocity
v_{pbest}	personal best velocity
v_{gbest}	global best velocity

Furthermore, it is crucial to understand the steps followed by PSO to implement this algorithm on the proposed circuits discussed in Chapters 3-6. Figure 7.2 shows the flowchart of PSO. The first step is to identify the objective function, define PSO parameters, and define the population size. The next step is to randomly select the velocity and position of every particle/agent. Furthermore, pbest and gbest values are obtained based on the defined objective function. Additionally, the agent's position is updated if the agent's current position is better than the previous position, and the best agent is obtained according to the agent's previous best position. Upon completion of this process, the agent's velocity is also updated. Thus, the agent reaches a new position. The process will continue until the population meets the desired termination criteria.

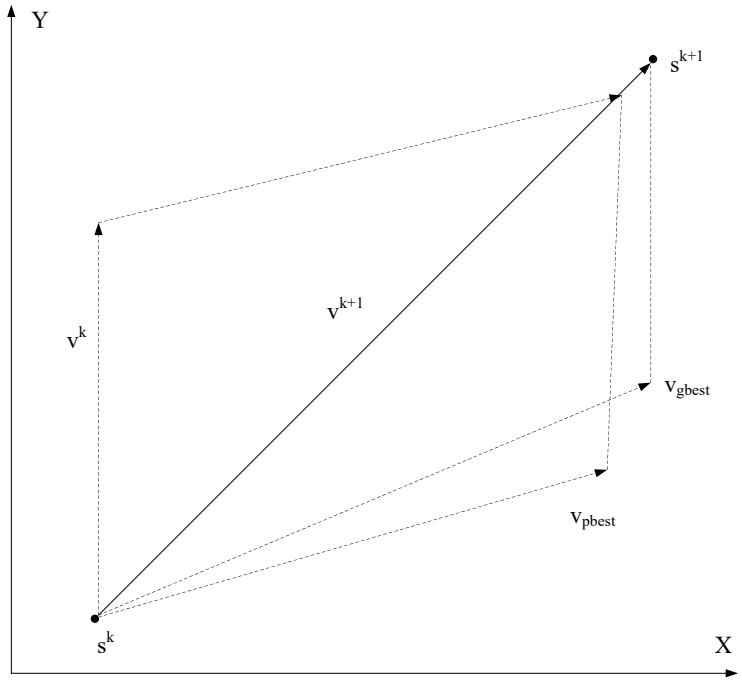


Figure 7.1: Searching point modification by PSO

7.6 Research Methods

This section outlines the methodologies adopted to conduct the systematic review, exploring the most relevant studies based on PSO. The systematic review (SR) process is beneficial in providing an overview of the research topic and identifying the appropriate research and its scope. Furthermore, the SR process identifies gaps within the existing works and determines future trends. The complete SR process involved in this study follows various steps that are enlisted below: (i) Outlining the research questions (ii) Selection of digital repositories and search strategy (iii) Defining inclusion and exclusion criteria (iv) Screening articles or reports based on the inclusion and exclusion criteria (v) Data extraction and analysis

7.6.1 Research Questions

The research questions covered by this study are mentioned below:

RQ1: How to improve the performance of the RF mixer for SDR?

RQ2: What contributions have been made in the context of PSO in the years 2017 to 2021, and

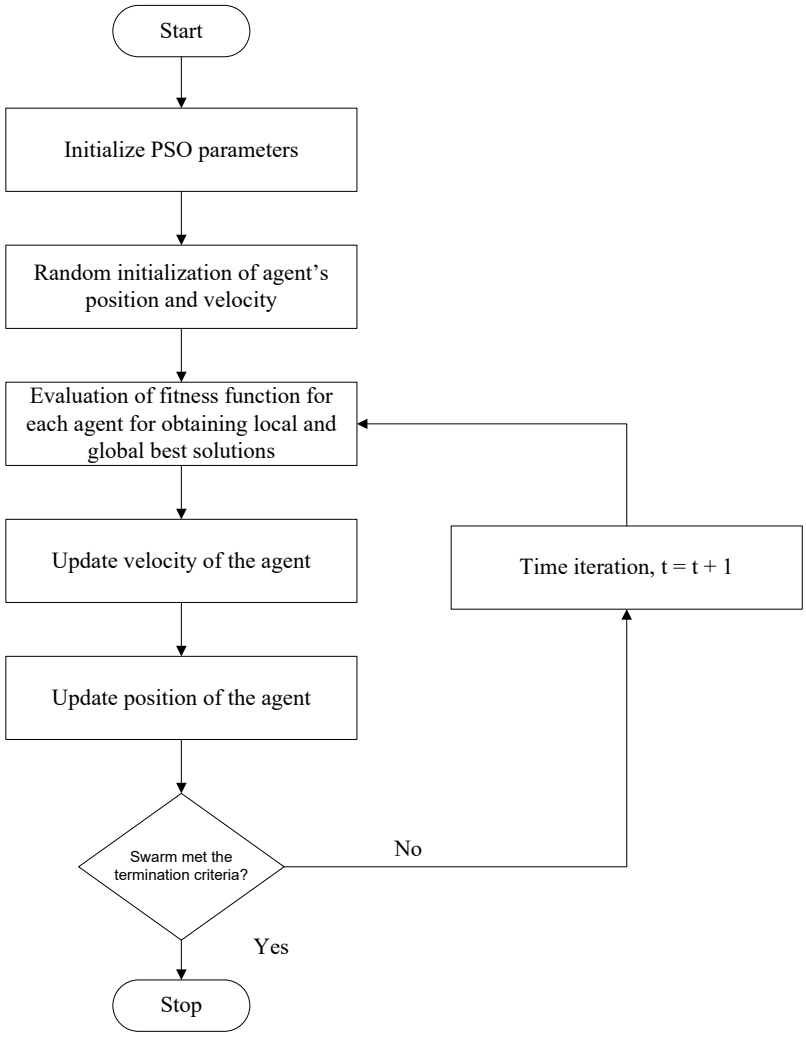


Figure 7.2: Flowchart of PSO algorithm

how many publications are available based on the PSO concerning the selected keywords?

RQ3: How can PSO be applied to mixer circuits?

RQ4: Has the performance been improved after applying the PSO to mixer circuits?

RQ1 aims to improve the performance of mixer circuits for SDR applications. This can be done by simultaneously optimizing the design parameters by applying PSO, resulting in the mixer's high performance compared to the unoptimized mixer circuits. RQ2 identifies the articles available on various repositories based on the PSO approach in response to the selected keywords. In this work, we have identified both review and research works to provide readers with conceptual and real applicable insights on how this can be beneficial in future works. We have identified various publication sources such as conference proceedings, journals, or

thesis that are relevant to the study. RQ4 aims to verify the performance of mixer circuits upon implementing PSO on them by following the process discussed by researchers within the literature as identified within our selected time period. PSO implementation has been further extended to the receiver circuit in this work. Upon observing the results, it was found that the optimized results are better than the unoptimized results. Thus, PSO is the most reliable optimization approach for SDRs.

7.6.2 Phases of the study

The systematic review is based on the Preferred Reporting Items for Systematic Reviews and Meta-Analyses (PRISMA) guidelines [303], with a slight modification to adapt the process of this study by incorporating the guidelines proposed in [304] to tailor this SR for the electronics and communication domain.

7.6.2.1 Digital Repositories Selection and Search Strategy

The search process was conducted by searching through 5 different repositories. The selected repositories are enlisted below: (i) Scopus (ii) Web of Science (iii) ACM (iv) Microsoft Academic (v) Science Direct.

The primary purpose of choosing the above-mentioned repositories is to obtain peer-reviewed works, reports, and relevant results.

Search criteria in selected repositories: The search criteria applied to the selected databases are mentioned below:

Scopus : Advanced Search option was selected in the Scopus, and articles were selected based on the "ALL" option, which shows the results if the keyword is found anywhere within the document. Boolean Operators "AND" and "OR" are applied to get the desired results. The search was conducted for the years 2017 to 2021. The subject area was restricted only to Engineering, and language was restricted to English.

Web of Science: Advanced search option was chosen in Web of Science Core Collection, where articles were selected based on the topic search, i.e., the "TS" option. The investigation was

conducted for the years 2017 to 2021. The research area was restricted to "Engineering" with "Engineering Electrical Electronic" category and language was restricted to English.

ACM Digital Library: The database was used to search the relevant articles. The articles were searched without any restrictions on the search, such as title, abstract, full text and affiliation, instead; articles were searched everywhere. Boolean Operators such as "AND" and "OR" were used to find the exact match within the desired year range. During the initial search, 106 articles were obtained. Upon applying the exclusion criteria, this list was reduced to 88 articles.

Microsoft Academic: The search option was chosen in the database by restricting the search within 2017-2021. Boolean operators "AND" and "OR" were chosen to extract the best match based on the relevant publication types. The publication category was chosen as "Engineering" with a primary focus on "Electronics Engineering".

ScienceDirect: Advanced Search was conducted in Science Direct database for the field Abstract, Title and Keyword. Boolean operators were applied and the search was conducted between 2017-2021.

Figure 7.3 depicts the systematic review process flowchart based on the PRISMA flow diagram. After applying each selection criteria, the number of shortlisted documents are shown after each corresponding step as per the selected databases. Initially, there were 7,379 publications obtained from the five databases during 2017-2021. Figure 7.4 shows the keywords chart obtained by different words used by researchers within their work. This is obtained using VOS viewer.

7.6.3 Inclusion, exclusion criteria and screening of Articles

Upon applying the exclusion criteria such as subject area, language, document type, and exact keywords, respectively, the list was reduced to 345 publications. These articles were eligible for the title and abstract review for Stage 3, which are depicted in Figure 7.5-Figure 7.9 corresponding to various databases during the year 2017-2021. The articles irrelevant to our work were removed and were shortlisted based on our defined categories with a primary focus on SDR front-ends. As a result, it was found that there were 143 relevant articles as shown in Figure 7.11-Figure 7.14.

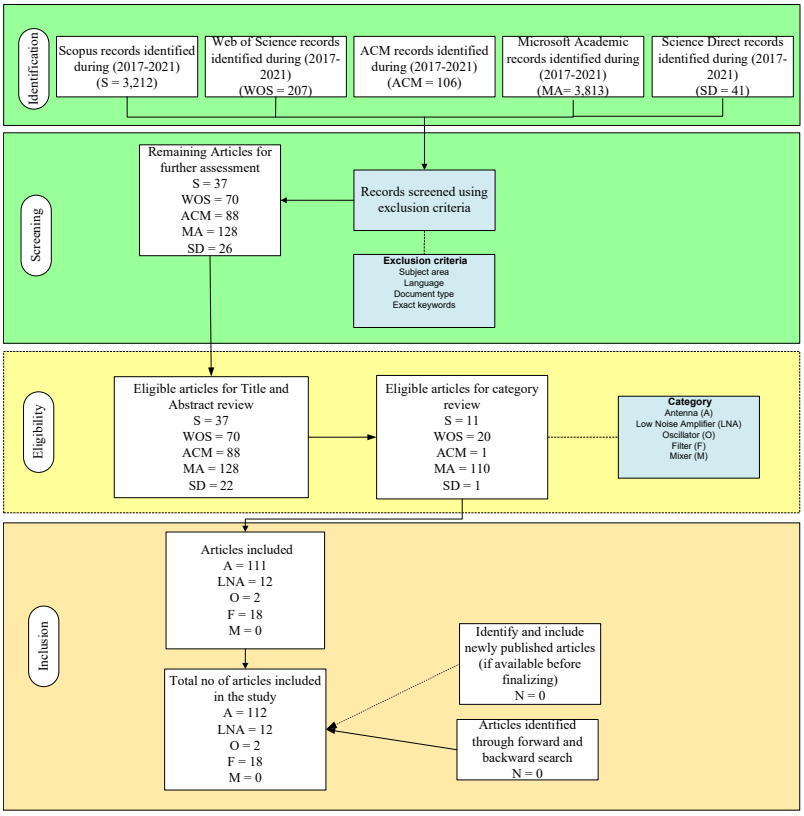


Figure 7.3: PRISMA flow diagram

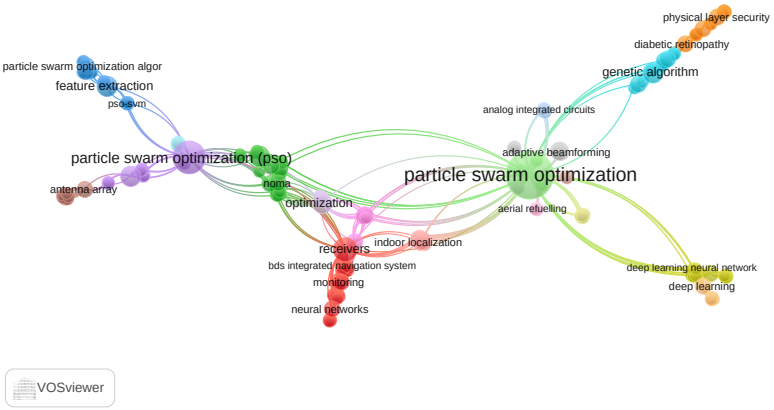


Figure 7.4: Keywords chart

Table 7.2-Table 7.19 depicts the shortlisted articles based on the category during the year 2017-2021.

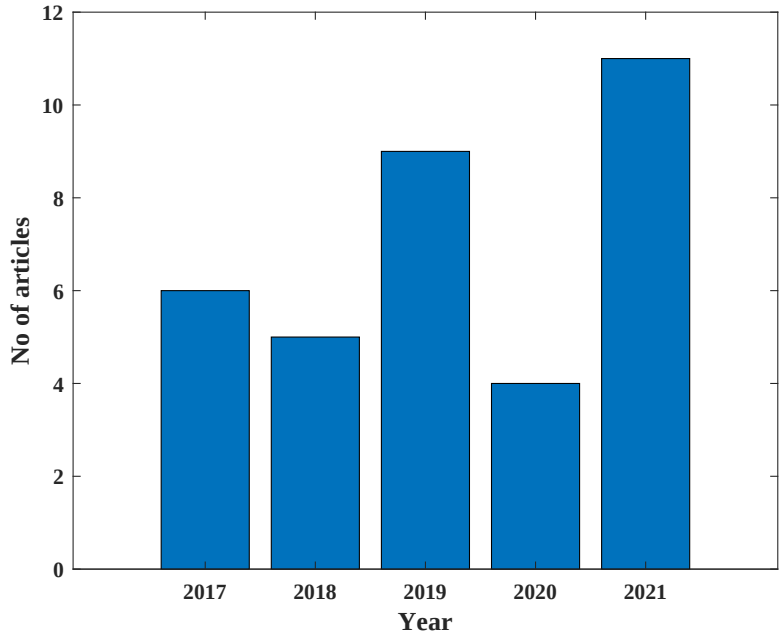


Figure 7.5: No of Articles obtained from Scopus database during year 2017-2021

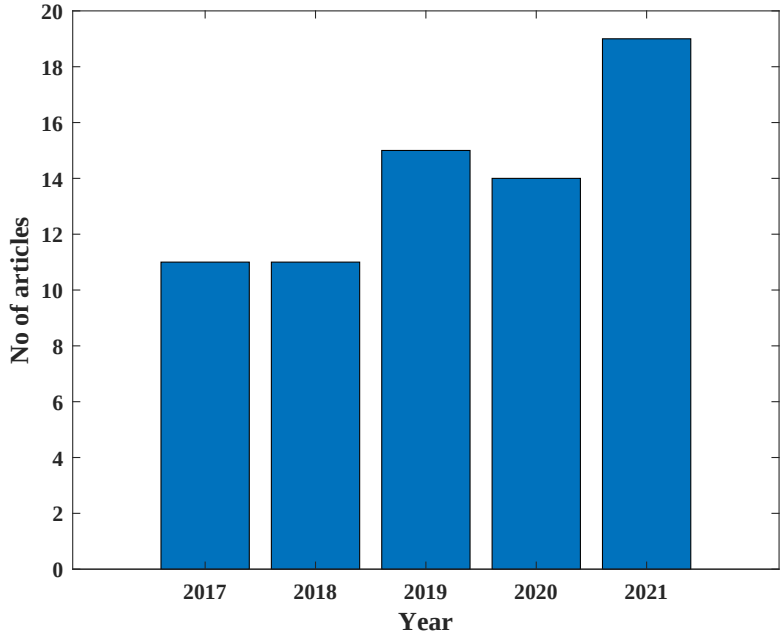


Figure 7.6: No of Articles obtained from Web of Science database during year 2017-2021

7.6.4 Data extraction and analysis

Stage 4 defines the total articles included in the review based on the assessment, which was the same as no additional articles were found during the forward search, a backward search

Table 7.2: Shortlisted Articles Based on Scopus Database Search

Title	Publication Year	Category
Antenna Placement for Distributed MIMO Radar with Different Missions in Different Subareas [305]	2021	Antenna
Weight quantization retraining for sparse and compressed spatial domain correlation filters [306]	2021	Filter
Optimization of the SIW cavity-backed slots antenna for X-band applications using the Particle Swarm Optimization algorithm [307]	2021	Antenna
Emerging evolutionary algorithms for antennas and wireless communications [308]	2021	Antenna
Optimization of LNA Consisting of CCG Stage and Mutually Coupled CS Stage Using PSO Algorithm for UWB Applications [309]	2021	LNA
Antenna Preprocessing and Element-Pattern Shaping for Multi-Band mmWave Arrays: Multi-Port Transmitters and Antennas [310]	2020	Antenna
Wide-Angle Scanning Lens Fed by Small-Scale Antenna Array for 5G in Millimeter-Wave Band [311]	2020	Antenna
Performance analysis of low power LNA using particle swarm optimization for wideband application [302]	2019	LNA
Swarm intelligence optimization techniques for an optimal RFxs integrated spiral inductor design [312]	2018	Filter
Design of Fragment-Type Antenna Structure Using an Improved BPSO [313]	2018	Antenna
The Role of Accurate Dynamic Analysis for Evaluating Time-Modulated Arrays Performance [314]	2017	Antenna

Table 7.3: Shortlisted Articles Based on Association for Computing Machinery Database Search

Title	Publication Year	Category
Complex-Valued Normalized Maximum Versoria Criterion Algorithm for Widely Linear Adaptive Filter [315]	2021	Filter

relevant to our work. Additionally, no further articles were found on the listed databases used for this work during the final stage. Using the above methods, a comprehensive analysis of the literature was conducted, resulting in the identification of gaps and opportunities for future research. Based on the observation, it was found that PSO has not been implemented on mixer circuits, which has been tested and verified in the next section. Likewise, PSO has been applied

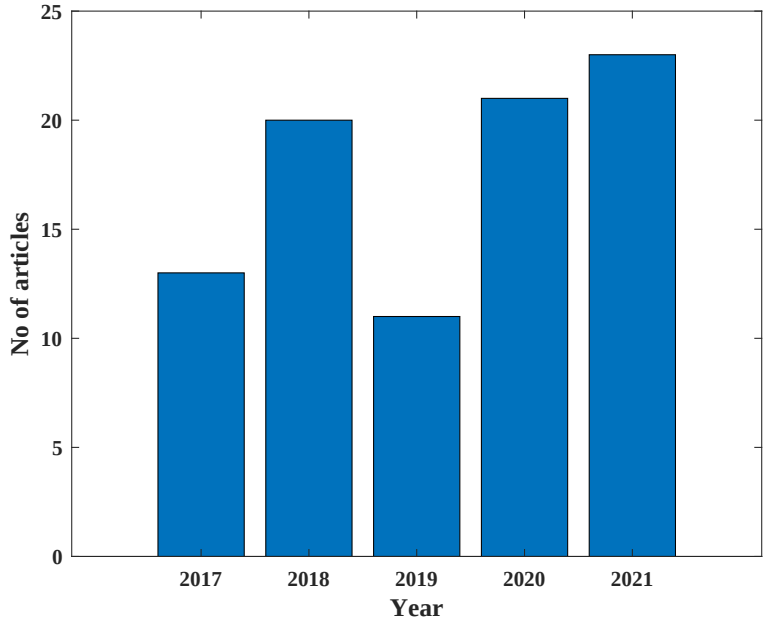


Figure 7.7: No of Articles obtained from ACM database during year 2017-2021

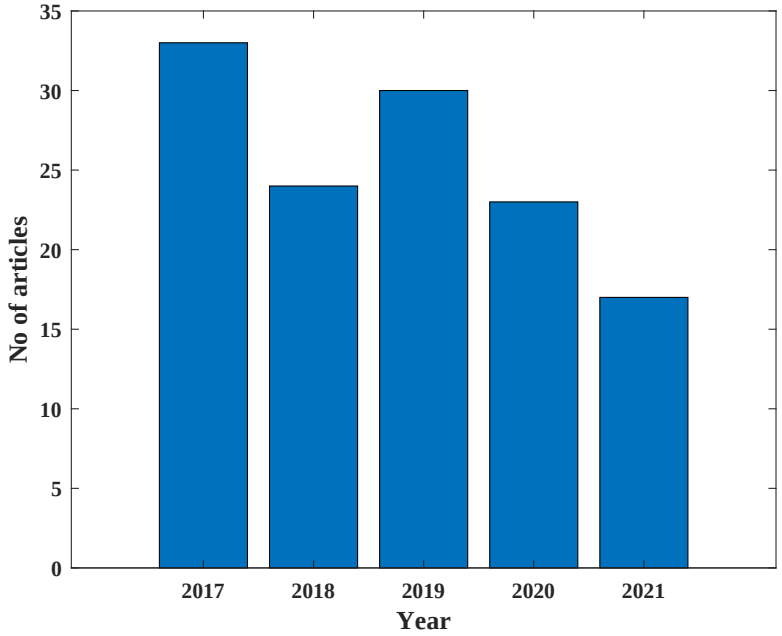


Figure 7.8: No of Articles obtained from Microsoft Academic database during year 2017-2021

to our proposed receiver circuit. Based on the implementation results, this process improved the overall performance of our proposed design.

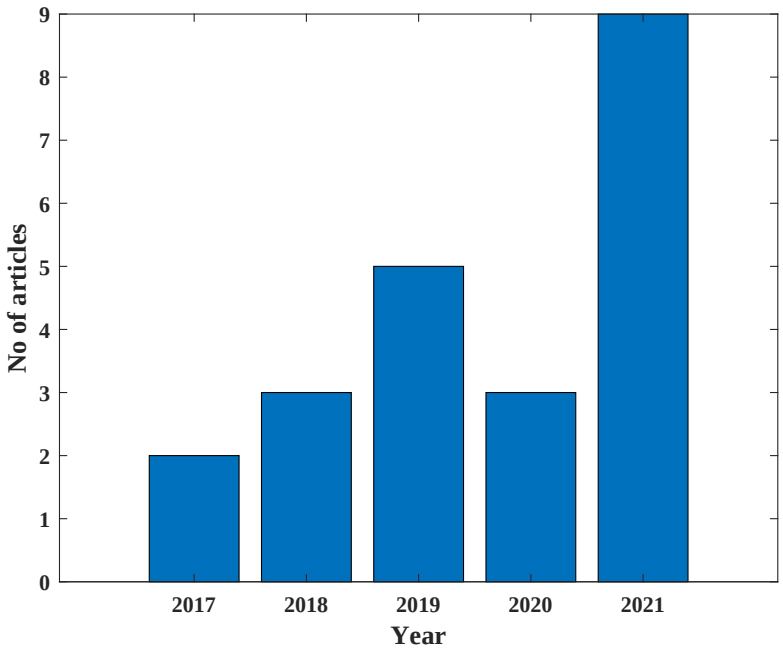


Figure 7.9: No of Articles obtained from Science Direct database during year 2017-2021

Table 7.4: Shortlisted Articles Based on Web of Science Database Search

Title	Publication Year	Category
Multiobjective Particle Swarm Optimization to Design a Time-Delay Equalizer Metasurface for an Electromagnetic Band-Gap Resonator Antenna [316]	2017	Antenna
Scalable Phased Array Architectures With a Reduced Number of Tunable Phase Shifters [317]	2017	Antenna
Nonuniformly Distributed Electronic Impedance Synthesizer [318]	2018	Oscillator
Advanced Pulse Sequence Design in Time-Modulated Arrays for Cognitive Radio [319]	2018	Antenna
The Optimization for Hyperbolic Positioning of UHF Passive RFID Tags [320]	2017	Antenna
Design and Optimization of Sparse Planar Antenna Arrays for Wireless 3-D Local Positioning Systems [321]	2017	Antenna
Mirrored Plasmonic Filter Design via Active Learning of Multi-Fidelity Physical Models [322]	2020	Filter

7.7 Design Optimization

This section provides an overview of the design specifications and variables chosen for the proposed circuits discussed in Chapters 3-6. Additionally, PSO specifications are considered the

Table 7.5: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Optimized Planar Elliptical Dipole Antenna for UWB EMC Applications [323]	2019	Antenna
Automatic EMI Filter Design Through Particle Swarm Optimization [324]	2017	Filter
An Effective Approach for the Synthesis of Unequally Spaced Antenna Array by Estimating Optimum Elements Density on the Aperture [325]	2017	Antenna
Suppressing Sidelobe Level of the Planar Antenna Array in Wireless Power Transmission [326]	2019	Antenna
Beamforming Optimization for Intelligent Reflecting Surfaces without CSI [327]	2020	Antenna
Energy-Efficient Resource Allocation in Cellular Network with Ambient RF Energy Harvesting [328]	2017	Antenna
An Efficient Method for Designing Multiplier-Less Non-uniform Filter Bank Based on Hybrid Method Using CSE Technique [329]	2017	Filter
Particle Swarm Optimization in Multi-Antenna SAR-based Localization for UHF-RFID Tags [330]	2019	Antenna
Design of optimal CMOS ring oscillator using an intelligent optimization tool [331]	2018	Oscillator

Table 7.6: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Performance improvement of high altitude platform using concentric circular antenna array based on particle swarm optimization [332]	2018	Antenna
Antenna Array Failure Correction [Antenna Applications Corner] [333]	2017	Antenna
Synthesis of conformal array antenna for hypersonic platform SAR using modified particle swarm optimisation [334]	2017	Antenna
Optimization of UHF RFID five-slotted patch tag design using PSO algorithm for biomedical sensing systems [335]	2020	Antenna
On the use of external MATLAB-based optimization with full-wave simulation to design resonant cavity antennas (Special session) [336]	2017	Antenna
Performance analysis of particle swarm optimization and genetic algorithm in MIMO systems [337]	2017	Antenna

Table 7.7: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Advanced impedance matching technology to optimize RF circuit design of practical wireless systems [338]	2017	Filter
3D Pattern Optimization Using PSO for an Irregular Dual-Layer Circular Array [339]	2018	Antenna
Antenna Array Output Power Minimization Using Particle Swarm Optimization [340]	2019	Antenna
Rotman lens design and optimization for 5G applications [341]	2018	Antenna
Shaping optimization of double reflector antenna based on manifold mapping [342]	2017	Antenna
An Efficient Hybrid Beamforming Design for Massive MIMO Receive Systems via SINR Maximization Based on an Improved Bat Algorithm [343]	2019	Antenna
Beamsteering and Beamshaping Using a Linear Antenna Array Based on Particle Swarm Optimization [344]	2019	Antenna
Miniaturization of Monopole Patch Antenna with Extended UWB Spectrum via Novel Hybrid Heuristic Approach [345]	2019	Antenna
A New Calibration Method of UWB Antenna Delay Based on the ADS-TWR [346]	2018	Antenna
Design of sixth order butterworth Gm-C filter using Particle Swarm Optimization program for biomedical application [347]	2017	Filter

same for all circuits to maintain uniformity within the process. Upon defining all specifications, the PSO process flow illustrated in the previous section is followed, and the results are obtained based on the defined objective functions, i.e., performance parameters such as CG, NF, IIP3, IRR. The optimized performance results of the designs are obtained and compared with the simulation results, as shown in the following subsections.

7.7.1 Reconfigurable mixer

A reconfigurable mixer is designed and simulated in 8HP CMOS process technology. The proposed mixer operates in a band of 0.9-13.5 GHz and attains low NF, high CG, and reasonable IRR compared to the existing similar works at the expense of IIP3. Thus, to improve the design performance in terms of all performance parameters, PSO has been applied to the mixer by

Table 7.8: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Optimisation of Adaptive Antenna Array Performance Using Particle Swarm Algorithm [348]	2019	Antenna
Non-uniform single-ring antenna array design using wavelet mutation based novel particle swarm optimization technique [349]	2017	Antenna
Optimization of 2.4 GHz CMOS Low Noise Amplifier Using Hybrid Particle Swarm Optimization with Lévy Flight [350]	2017	LNA
Intelligent Tuning of Microwave Cavity Filters Using Granular Multi-Swarm Particle Swarm Optimization [351]	2020	Filter
Polymorphic impedance matching technique for MEMS phase shifter [318]	2018	Filter
Antenna-on-Package Design: Achieving Near-Isotropic Radiation Pattern and Wide CP Coverage Simultaneously [352]	2021	Antenna

Table 7.9: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Optimum design of a new ultra-wideband LNA using heuristic multiobjective optimization [353]	2020	LNA
Antenna Array Optimization for Smart Antenna Technology using Whale Optimization Algorithm [354]	2019	Antenna
Efficient AI-Driven Design of Microwave Antennas Using PSADEA [355]	2019	Antenna
An Improved PSO for Design Optimizations of a Multiband Rectenna for Miniature Energy Harvester [356]	2020	Antenna
3D Beamforming for 5G Millimeter Wave Systems Using Singular Value Decomposition and Particle Swarm Optimization Approaches [357]	2018	Antenna
Exploiting non-radiating currents in reflectarray antenna design [358]	2017	Antenna
Comparison of self-adaptive dynamic differential evolution and particle swarm optimization for smart antennas in wireless communication [359]	2019	Antenna
An improved design method based on polyphase components for digital FIR filters [360]	2017	Filter
Optimal Design of Aperiodic Reconfigurable Antenna Array Suitable for Broadcasting Applications [361]	2020	Antenna

Table 7.10: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Time-domain design of a linear antenna array for wideband shaped beams [362]	2017	Antenna
Concurrent Gain and Bandwidth Improvement of a Patch Antenna with a Hybrid Particle Swarm Optimization Algorithm [363]	2019	Antenna
UAVs-based antenna arrays using time modulation [364]	2020	Antenna
Reflectarray antenna simplification through non-radiating currents synthesis [365]	2017	Antenna
A novel robust design method for a mobile antenna with a metal frame [231]	2017	Antenna
Multi-Beam and Shaped-Beam Reflectarray Antennas [366]	2018	Antenna
Antenna Placement for Distributed MIMO Radar with Different Missions in Different Subareas [305]	2021	Antenna

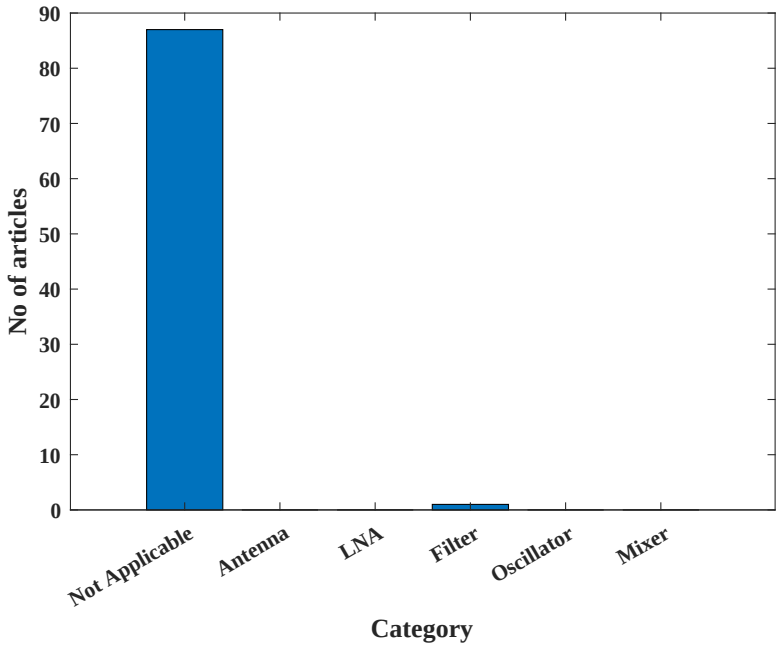


Figure 7.10: Shortlisted articles based on the category-ACM

considering a suitable cost function for improving the CG, NF, IRR, and IIP3, respectively. The design specifications of the mixer are defined below: (a) Supply voltage = 1.2V (b) CG $\geq$ 10 dB (c) NF $\leq$ 6 dB (d) IIP3 >1dBm. Likewise, PSO specifications are expressed as (a) swarm size = 30, (b) iterations = 1000, (c) c_1, c_2 = 1, (d) w = 0.4.

Table 7.11: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Multi-Objective Optimization of an Origami Yagi-Uda Antenna Using an Adaptive Fitness Function [367]	2020	Antenna
PSO AND IFS TECHNIQUES FOR THE DESIGN OF WEARABLE HYBRID FRACTAL ANTENNA [368]	2021	Antenna
Performance Comparison of Evolutionary Algorithms in the Design of a Hand-Pump Shape Microstrip Antenna for 5G Applications [369]	2019	Antenna
Antenna Array Synthesis Through Particle Swarm Optimization for V2V Communications in Urban Intersections [370]	2020	Antenna
Design of the Compact Ultra-Wideband (UWB) Antenna Bandwidth Optimization Using Particle Swarm Optimization Algorithm [371]	2019	Antenna
Dual-band pre-fractal antenna multi-objective optimization design [372]	2017	Antenna
Particle Swarm Optimization for Comprehensive 24 GHz Amplifier Design [373]	2018	Amplifier
5G Wideband Stacked Patch Antennas [374]	2021	Antenna
Optimal design of 5.5 GHz CMOS LNA using hybrid fitness based adaptive De with PSO [375]	2017	LNA
Optimization of Seebeck nanoantenna-based infrared harvesters [376]	2020	Antenna
Multi-objective Optimization of Cross Coupled Resonators Based Microstrip Bandpass Filter using PSO [377]	2020	Filter

The design variables for the mixer are mentioned below. (a) (L_1-L_2)nH = 0.1-5, (b) (R_1-R_3)Ohms = 50-100 (c) (C_1-C_4)pF = 0.1-5, (d) $(\frac{W}{L})_0$-$(\frac{W}{L})_7$ = $\frac{100-250}{0.13}$, (e) $(\frac{W}{L})_{14}$-$(\frac{W}{L})_{15}$ = $\frac{10-50}{0.13}$, (f) $(\frac{W}{L})_8$-$(\frac{W}{L})_{13}$ = $\frac{10-50}{0.13}$

Likewise, the design variables for 9th-order filter circuit are as follows: (a)$(C_1 - C_9)$pF = 0.1-7, (b) (L_1-L_2)nH = 0.1-5.

The PSO is implemented upon defining all the desired parameters, and the optimization results have been obtained. These results have been compared with the previously obtained simulation results. Table 7.20 summarizes the different mixer designs. As per Table 7.20, it has been found that the proposed design attains the best performance while operating in a wideband. The design performance has been further improved by applying PSO as shown in Table 7.20.

Table 7.12: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Realization of adaptive beamforming in smart antennas on a reconfigurable architecture [378]	2018	Antenna
A Wideband Patch Antenna for 5G [379]	2020	Antenna
Performance Analysis of MIMO MC-CDMA System Using Optimization Algorithms [380]	2018	Antenna
An Efficient Hybrid Beamforming Design for Massive MIMO Receive Systems via SINR Maximization Based on an Improved Bat Algorithm [343]	2019	Antenna
Optimization of E-Shaped Microstrip Patch Antenna Using Particle Swarm Optimization (PSO) for Wideband Application [381]	2020	Antenna
Optimization of Low Power LNA Using PSO for UWB Application [382]	2021	LNA
Optimization and parametric analysis of slotted microstrip antenna using particle swarm optimization and curve fitting [383]	2021	Antenna

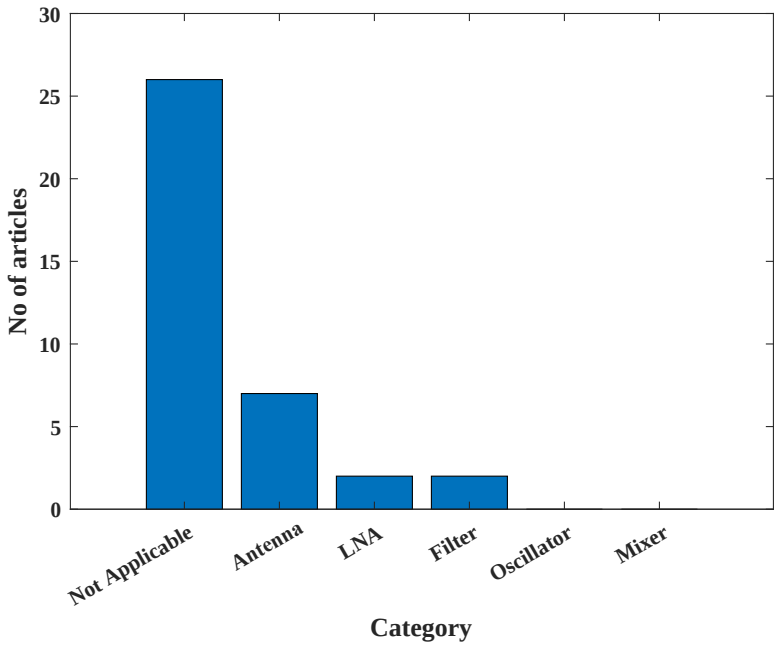


Figure 7.11: Shortlisted articles based on the category-Scopus

Figure 7.15 shows the simulated and optimized results of the proposed mixer. Upon observation, it has been found that the CG performance is slightly improved upon performing optimization.

Table 7.13: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Optimization of an array of smart antennas using PSO for the monitoring of electrical power switches [384]	2021	Antenna
Hybrid Algorithm for Multi-beam Synthesis Based on Time Modulated Antenna Array [385]	2021	Antenna
Optimal Design of 2.4 GHz CMOS LNA Using PSO with Aging Leader and Challenger [386]	2018	LNA
Deep Learning Based Antenna Design and Beam-Steering Capabilities for Millimeter-Wave Applications [387]	2021	Antenna
PSO-based Combined Antenna and Matching Network Optimization for Mobile Terminals [388]	2019	Antenna
Low-Cost Beamforming Concept for the Control of Radiation Patterns of Antenna Arrays Installed onto UAVs [389]	2021	Antenna
Symbol Detection in Multiple Antenna Wireless Systems via Ant Colony Optimization [390]	2017	Antenna
A Microstrip Antenna Design Using an Heuristic Algorithm [391]	2020	Antenna
Objective Resource Beamforming in Broadband SWIPT System by Evolution Algorithms [392]	2020	Antenna
Design of a Phased Array Antenna with Reducing of Both The Number of Phase Shifters and The Maximum Side lobe level [393]	2019	Antenna

A design reconfiguration is made by varying the capacitors. In this way, maximum power is delivered when inductors are used in conjunction with the capacitors. The aspect ratio, (W/L) is obtained when determining the values of V_m, V_{gs}, and V_{ds} using transistor equations. These three factors are based on 8HP CMOS technology's gate-oxide capacitance, threshold voltage and mobility. PSO implements three objective functions, CG, NF, and IIP3, where CG and IIP3 are maximized, and NF is minimized. Additionally, the linearity of the mixer is highly dependent on the condition of the RF stage transistors. The final CG and NF equations are used to obtain optimal CG, NF. NF performance is shown in Figure 7.16. As per Figure 7.16, the optimized NF is less than the simulated NF at the maximum frequency of operation. Likewise, IIP3 and IRR performance results are shown in Figure 7.17 and Figure 7.18, respectively. Upon optimization, it has been found that the mixer's performance has also been improved in terms of

Table 7.14: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Gain characteristics estimation of heteromorphic RFID antennas using neuro-space mapping [394]	2020	Antenna
Performance Analysis of Patch Antenna for Ultra-Wideband using Particle Swarm Optimization [395]	2021	Antenna
A novel pinwheel fractal multiband antenna design using particle swarm optimization for wireless applications [396]	2021	Antenna
Optimization of LNA Consisting of CCG Stage and Mutually Coupled CS Stage Using PSO Algorithm for UWB Applications [397]	2021	LNA
A Novel Graphical User Interface-Based Toolbox for Optimization and Design of Linear Antenna Array [398]	2020	Antenna
A Study on Designing an Aperiodic Antenna Array Using Boolean PSO [399]	2019	Antenna
Design of Thinned Linear Antenna Array using Particle Swarm Optimization (PSO) Algorithm [400]	2019	Antenna

Table 7.15: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
A Compact Ultra-Wide Band E-Shaped Slot Antennas for High Speed Wireless Networks [401]	2021	Antenna
Design of Reconfigurable Microwave Filter [402]	2019	Filter
Optimal Design of Compact Dual-Band Slot Antenna Using Particle Swarm Optimization for WLAN and WiMAX Applications [403]	2019	Antenna
Designing the parameters of an FSS antenna for communication systems using an enhanced UTC-PSO approach [404]	2020	Antenna
An Efficient Design Methodology for Fabry-Perot Cavity Antenna [405]	2020	Antenna
PSO Optimized Nested Slot Structure RFID Tag Antenna at 5.8 GHz for Metallic Applications [406]	2019	Antenna
Design and Optimization of Fractal Antenna for UWB Application [407]	2017	Antenna
RF ANTENNA DESIGN FOR BUTTON-TYPE BEAM POSITION MONITORS USING BIO-INSPIRED OPTIMIZATION METHODS [408]	2020	Antenna

Table 7.16: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Assessment for the Radio Frequency Exposure Worst Case of Multiple Antennas Based on Particle Swarm Optimization [409]	2020	Antenna
Reconfigurable and Conformal Antennas based on the Emerging Liquid Metal and Electro-Textile Materials [410]	2020	Antenna
Antenna Design Optimization With Desired Null Placement Using Particle Swarm Optimization Algorithm [411]	2019	Antenna
Tri-band Impedance Matching Network Design Using Particle Swarm Optimization Algorithm [412]	2019	Antenna
Development Of Narrowband 92 MHz Yagi-Uda Antenna For Use In Passive Radar Applications [413]	2019	Antenna
Global Optimization Techniques for Optimal Placement of HF Antennas on a Shipboard [414]	2019	Antenna
Transmit Beamforming Algorithm of Multi-UAV Based on Particle Swarm optimization [415]	2020	Antenna
Modified Patch Antenna with Matching Network for Energy Harvesting at Multiple Frequencies [416]	2019	Antenna
Parameters of Particle Swarm Optimization for 24 GHz Amplifier Design [417]	2018	LNA
Multi-objective Design Method for Hybrid Active Power Filter [418]	2017	Filter
Economical Approach To Design Of Passive Distributed Antenna System [419]	2017	Antenna
Optimization of Current-Reused LNA with PSO Algorithm [420]	2019	LNA
Improvement and Optimization of Thin Dipole for UWB Applications [421]	2017	Antenna

IIP3 and IRR.

7.7.2 Balanced mixer

A 1.8-5 GHz balanced mixer is proposed, designed, and simulated in 8HP CMOS process technology. The design consumes less power and covers a small chip area. Based on the simulation results before performing the optimization, it has been found that the proposed mixer attains an improved NF, reasonable CG compared to the previous design at the expense of IIP3. However, to further improve the performance of the design, the optimized values of the

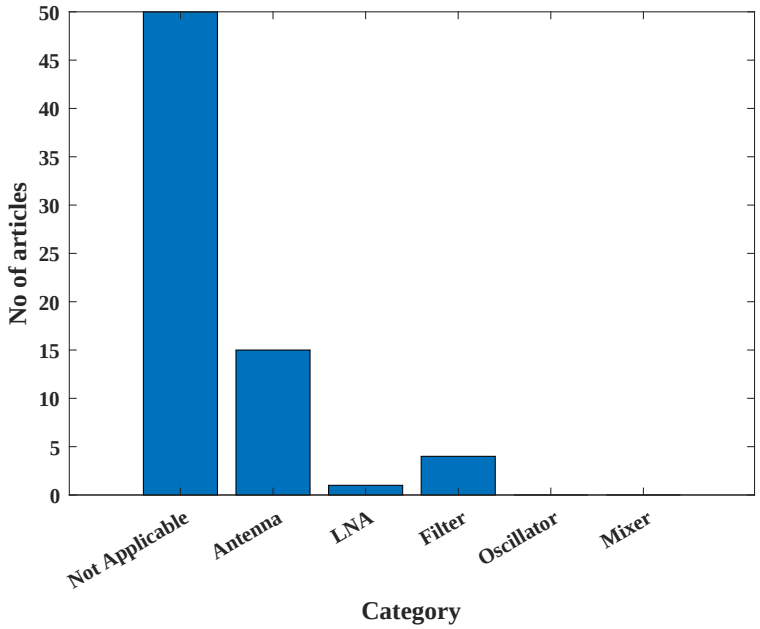


Figure 7.12: Shortlisted articles based on the category-Web of Science

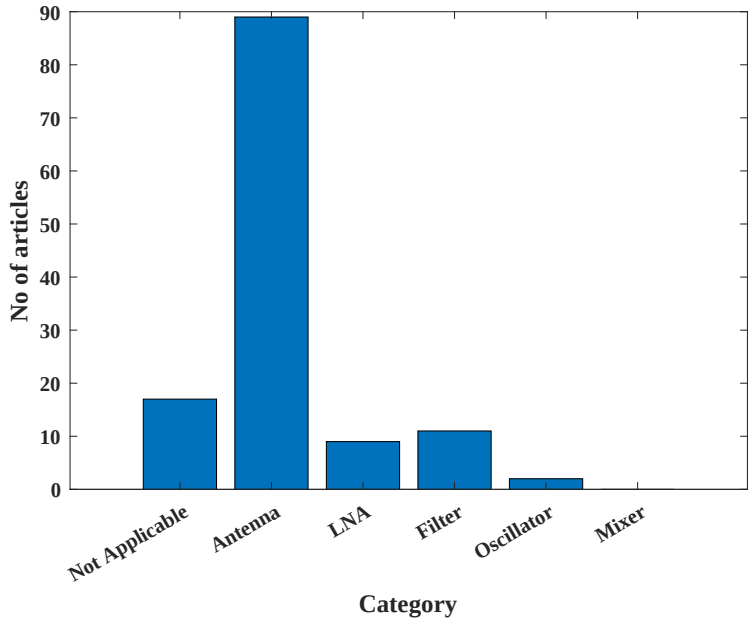


Figure 7.13: Shortlisted articles based on the category-Microsoft Academic

design variables are obtained using PSO by considering a suitable cost function while aiming to improve the CG, NF, and IIP3, respectively. The design specifications for the proposed mixer are defined below: (a) Supply voltage = 1.2V (b) CG $\geq$ 10 dB (c) NF $\leq$ 5 dB (d) IIP3 >1dBm. Likewise, PSO specifications are expressed as (a) swarm size = 30, (b) iterations = 1000, (c) c_1,

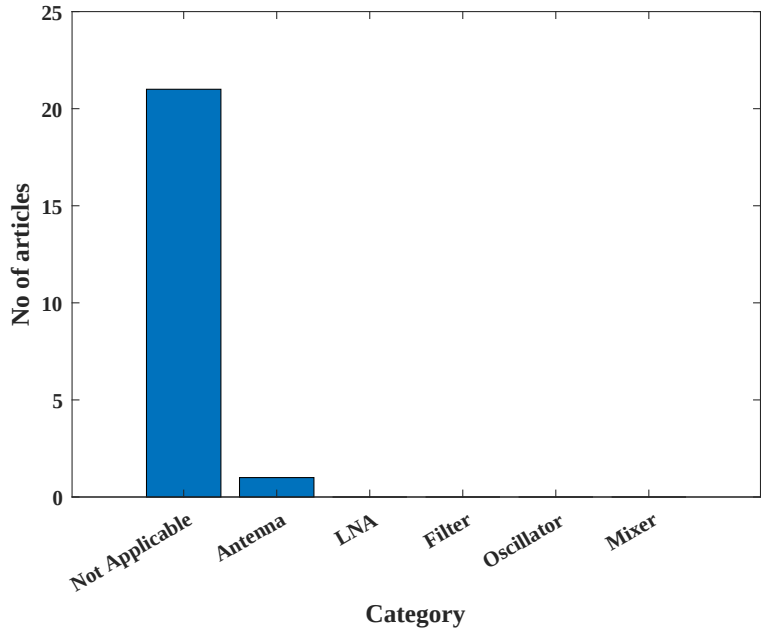


Figure 7.14: Shortlisted articles based on the category-Science Direct

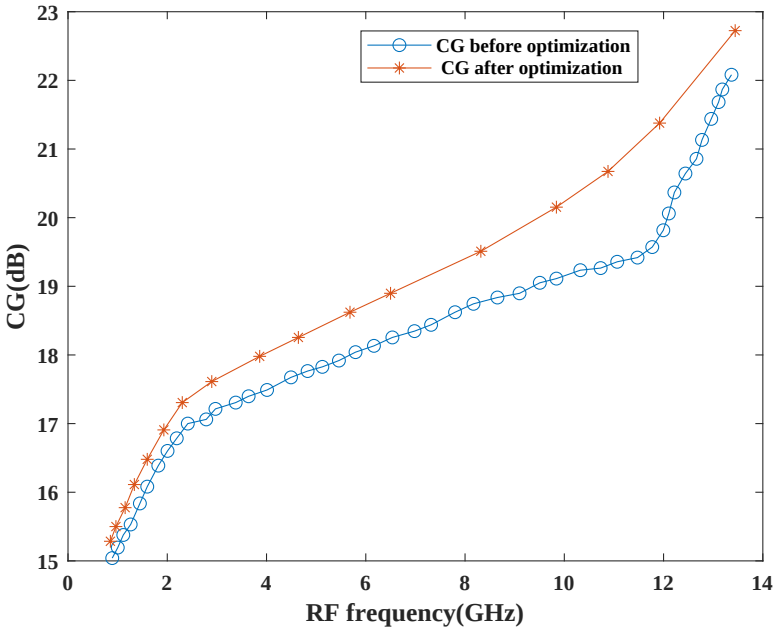


Figure 7.15: Simulated and optimized CG performance

c_2 = 1, (d) w = 0.4.

The design variables for the balanced mixer are defined below: (a) (L_1-L_4)nH = 0.1-5, (b) (C_1-C_4)pF = 0.1-6, (c) (C_5-C_6)pF = 0.1-5, (d) (R_1-R_3)Ohms = 50-250, (e) $(\frac{W}{L})_0$-$(\frac{W}{L})_5$ = $\frac{1-100}{0.13}$.

The optimized design is simulated again in Cadence software. Upon resimulation, it has

Table 7.17: Shortlisted Articles Based on Web of Science Database Search

Title	Publication Year	Category
Experimental Demonstration of a Software-Defined-Radio Adaptive Beamformer [422]	2018	Antenna
Experimental Demonstration of a Software-Defined-Radio Adaptive Beamformer [423]	2018	Antenna
GNSS Receiver Satellite Selection Algorithm Based on Particle Swarm Optimization [424]	2020	Antenna
User Positioning by Exploring MIMO Measurements with Particle Swarm Optimization [425]	2018	Antenna
Quantum Behaved Particle Swarm Optimization Technique Applied to FIR-Based Linear and Nonlinear Channel Equalizer [426]	2018	Filter
Performance analysis of low power LNA using particle swarm optimization for wide band application [427]	2019	LNA
Multipath-Assisted Indoor Localization Using a Single Receiver [428]	2020	Antenna

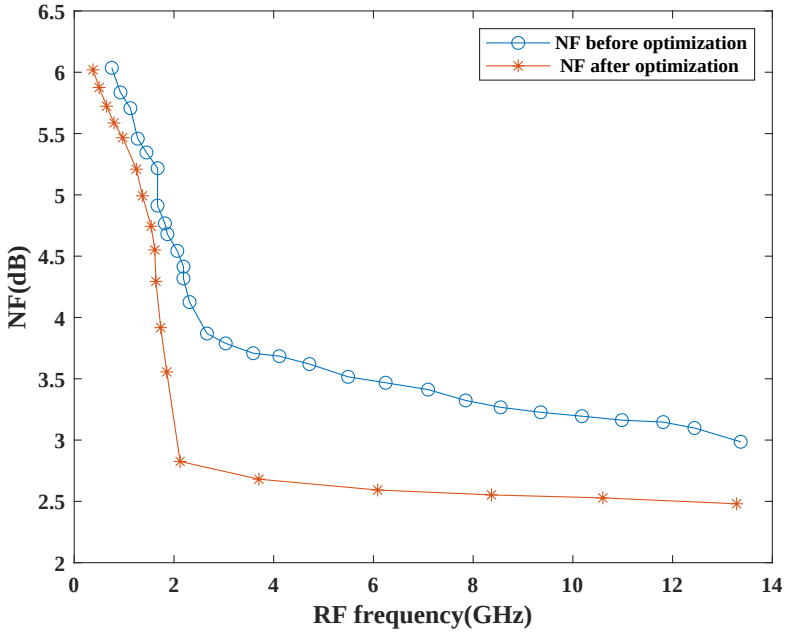


Figure 7.16: Simulated and optimized NF performance

been found that the proposed mixer attains an improved performance in terms of all parameters compared to the previously obtained simulation results. Optimized simulated design is fabricated, and the measurement results have been obtained. For chip evaluation purposes, external baluns

Table 7.18: Shortlisted Articles Based on Web of Science Database Search - Continued

Title	Publication Year	Category
Cooperative beamforming for a double-IRS-assisted wireless communication system [429]	2021	Antenna
A CIPSO-FCM-Based RAIM Algorithm for the GPS/BDS Integrated Navigation System [430]	2021	Antenna
The Design of Two-fold Redundancy Linear Arrays in Aperture Synthesis Radiometers [431]	2017	Antenna
Low-Sidelobe Range-Angle Beamforming With FDA Using Multiple Parameter Optimization [432]	2018	Antenna
Weight Quantization Retraining for Sparse and Compressed Spatial Domain Correlation Filters [433]	2021	Filter
Optimal Multiuser MISO Beamforming for Power-Splitting SWIPT Cognitive Radio Networks [434]	2017	Antenna
An Efficient Hybrid Beamforming Design for Massive MIMO Receive Systems via SINR Maximization Based on an Improved Bat Algorithm [343]	2019	Antenna
Design of Evolutionary Adaptive Notch Filter for GPS Anti-Jamming System [435]	2021	Filter
WDM-VLC Receiver Sensors: Large-Scale Filter-Array Detectors With Optimized Selection Combining Methods [436]	2018	Filter
Programmable Weight Phased-Array Transmission for Secure Millimeter-Wave Wireless Communications [437]	2018	Antenna
Neuroevolution-Based Adaptive Antenna Array Beamforming Scheme to Improve the V2V Communication Performance at Intersections [438]	2021	Antenna
The Method of Maximum Power Transmission Efficiency for the Design of Antenna Arrays [439]	2021	Antenna
Empirical Geometrical Bounds on MIMO Antenna Arrays for Optimum Diversity Gain Performance: An Electromagnetic Design Approach [440]	2018	Antenna

were used with an input matching network that is present at RF and LO ports, respectively. Additionally, an output buffer of 0 dB gain was also used. The measurements were made while fixing the LO frequency to 1GHz. Variations in simulated and measured results can be attributed to the variation in transistors, the parasitic capacitance effect, and the need for external baluns. PSO implements three objective functions, CG, NF, and IIP3, where CG and IIP3 are maximized, and NF is minimized. Additionally, the linearity of the mixer is highly dependent on

Table 7.19: Shortlisted Articles Based on Science Direct Database Search

Title	Publication Year	Category
A near maximum likelihood performance modified firefly algorithm for large MIMO detection [441]	2019	Antenna

Table 7.20: Performance Comparison Summary-Reconfigurable Mixer

Ref.	Tech.	Area (mm^2)	Freq.(GHz)	S_{21}(dB)	NF(dB)	IRR (dB)	IIP_3 (dBm)	S_{11}(dB)
This work(O)	SiGe 8HP	1.8	0.9-13.5	15.2-22.7	2.4-6	24.9-30.2	-1-8.3	-17.14-22.7
This work(S)	SiGe 8HP	1.8	0.9-13.5	15.1-22.1	2.5-5.6	24.9-30	-3.28-9.05	-17.14-22.7
[201]	0.25 um	Nil	0.9	5	8	30	1	-15
[84]	0.065 um	0.19	0.9,1.8-2.5	9.2-13	13.6-18.3	Nil	≥ 10.8	Nil
[207]	0.18 um	Nil	2.42-2.48	10.73	Nil	Nil	-7.31	Nil
[208]	0.18 um	Nil	2.4	9.3	7.4	Nil	8	Nil
[117]	0.18 um	Nil	2.4	17	11	Nil	1	Nil
[192]	0.18 um	Nil	2.44	18.6	7.15	Nil	-8.1	Nil
[209]	0.18 um	<1	3.1-10.6	≥ 10	10	Nil	4	-25
[200]	0.18 um	1.4	5.1	18	13.2	Nil	-5.85	-14.5
[203]	SiGe	0.9	5.1-5.8	14	6.8	36	-5.5	-11
[168]	0.13 um	0.85	7.2-8.4	23.8	4.3	30	-10.5	Nil
[210]	0.18 um	0.11	1.8-2.4	23-26	16-20	Nil	-2	Nil
[211]	0.18 um	0.61	0.5-7.5	5.7	15	Nil	-5.7	Nil
[212]	0.18 um	1.14	3-5	19.8-20.6	7.7-8.7	Nil	>-6	-10.5-15.2
[116]	0.065 um	0.21	1-10.5	10-14.5	6.5-10	Nil	Nil	-20
[213]	0.13 um	0.31	1-5.5	17.5	3.9	Nil	0.84	<-8.8
[89]	0.09 um	0.57	80-110	4.1-11.6	15.8-18.1	Nil	3	-8.7-22
[214]	0.065 um	0.5	17-43	-0.1 ± 1.5	12.4	Nil	3.4	Nil
[170]	0.13 um	0.13	0.87-3.7	13.5-14	2.9-6.5	Nil	-10-13	Nil

* S-Simulation results, O-Optimization results

the condition of the main transistors, T_3 and T_4. The final CG, NF equations are used to obtain optimal CG and NF.

Table 7.21 compares various mixer designs operating at different bands. Upon comparison, it has been found that the proposed design attained the lowest NF and highest CG at the maximum frequency while operating in a wideband.

Figure 7.19-Figure 7.22 shows the optimized simulation and measurement results of the proposed mixer in terms of CG, NF, IIP3, and S_{11}, respectively [185]. From the plots, it has been found that there is a slight degradation in performance was observed while obtaining the measurement results.

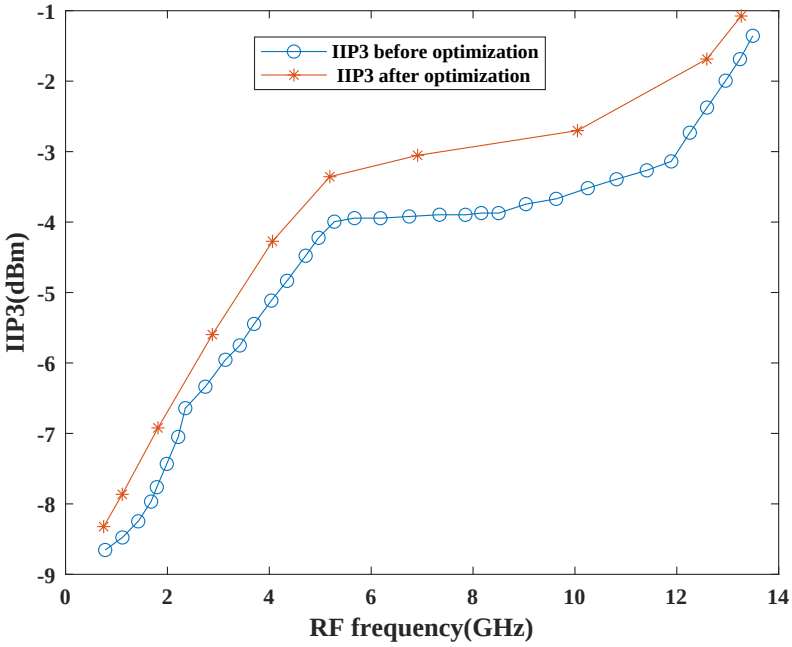


Figure 7.17: Simulated and optimized IIP3 performance

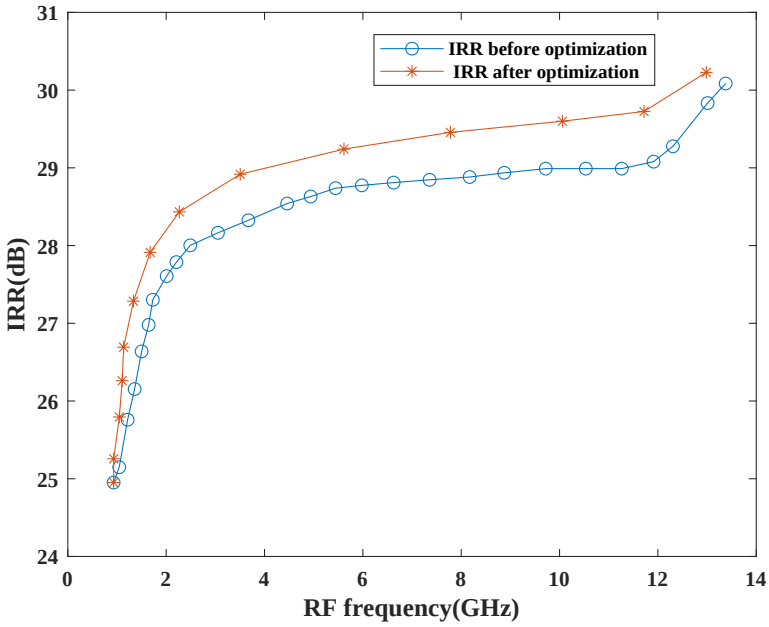


Figure 7.18: Simulated and optimized IRR performance

7.7.3 High Linearity Mixer

A 0.9-7 GHz continuously tunable, high linearity reconfigurable mixer is proposed in this section. The proposed mixer also attains higher CG, reasonable NF than the previously proposed designs.

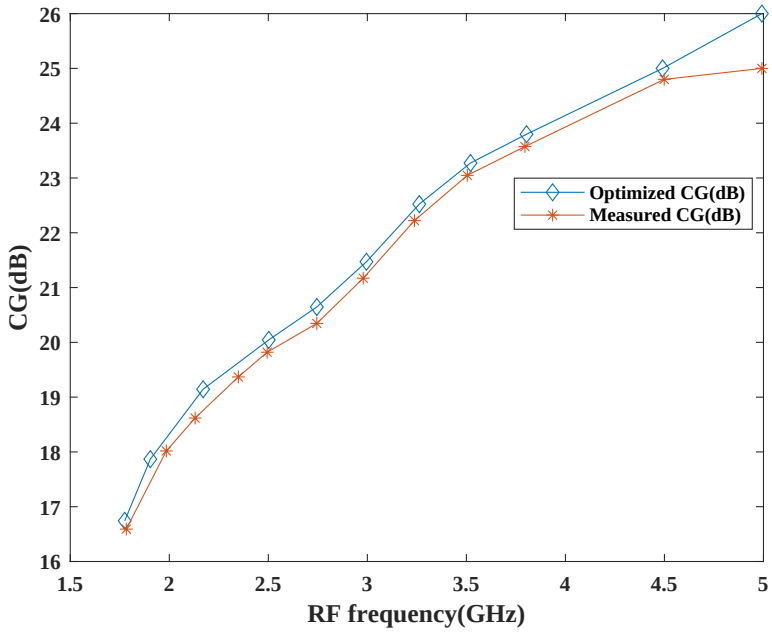


Figure 7.19: Simulated and measured CG after optimization of balanced mixer

Table 7.21: Performance Comparison Summary-Balanced Mixer

Ref	Freq(GHz)	PT(μm)	CG (dB)	NF(dB)	IIP3(dBm)	S_{11}(dB)	P_{diss}(mW)
This work (S2/M2)	1.8-5	8HP	16.7-26/16.5-25	1-1.78/1.01-1.7	-1	>-10	0.28
This work (S1)	1.8-5	8HP	12.9-18.32	1.19-1.89	-5.89	>-10	0.32
[233]	1.8-5	HEMT	5-10	<2	28	Nil	Nil
[167]	5.1	0.09	16	8.39	-1.93	Nil	8.19
[74]	3.43	0.18	8.05	11.3-15	-10.8	-22.9	Nil
[234]	2.4	0.18	15.7	10.7	-9	Nil	18
[51]	3.5	0.15	5.1	11.6	1.5	Nil	39.6
[235]	3.1-4.8	0.35	12-13.5	<8.8	>0	>-4	18
[3]	2.4	0.13	7.5	15	1	Nil	0.572
[186]	2.4/5.2	0.18	16.1/13.07	27.2/30.3	-3.1/-2.8	Nil	0.93
[236]	0.86-0.87	0.13	17	7.5	-4.1	-19.5	6
[85]	2.4	0.11	19	14.2	-7	Nil	3
[116]	1-10.5	0.65	14.5	6.5	15	-30	14.4
[170]	0.8-3.7	0.13	13.5-14	2.7-6.5	-13∼-10	Nil	16.8
[129]	9-50	0.13	≥ 5	16.4	-0.2,1.2,4.5	Nil	97
[85]	2.4	0.40	19	14.2	-7	Nil	3

* S1-Simulation results(before optimization), S2-Simulation results(after optimization), M2-Measurement results(after optimization)

The design consumes high power and covers similar design areas compared to the previous design. To further improve the performance of the proposed design, PSO has been applied by considering a suitable cost function while aiming to improve the CG, NF, and IIP3, respectively. The design specifications for the mixer design are defined below: (a) Supply voltage = 1.2V (b) CG $\geq$ 10 dB (c) NF $\leq$ 5 dB (d) IIP3 >1dBm. Likewise, PSO specifications are expressed as (a) swarm size = 30, (b) iterations = 1000, (c) c_1, c_2 = 1, (d) w = 0.4.

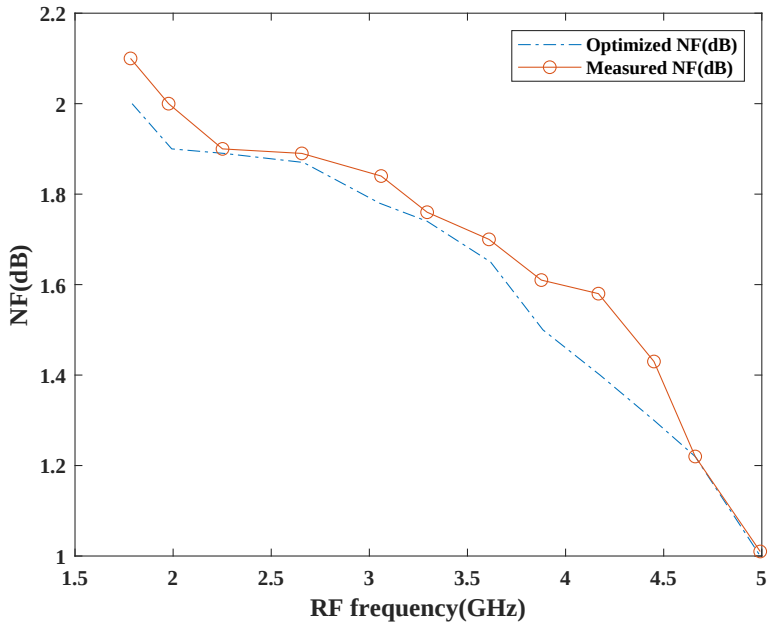


Figure 7.20: Simulated and measured NF after optimization of balanced mixer

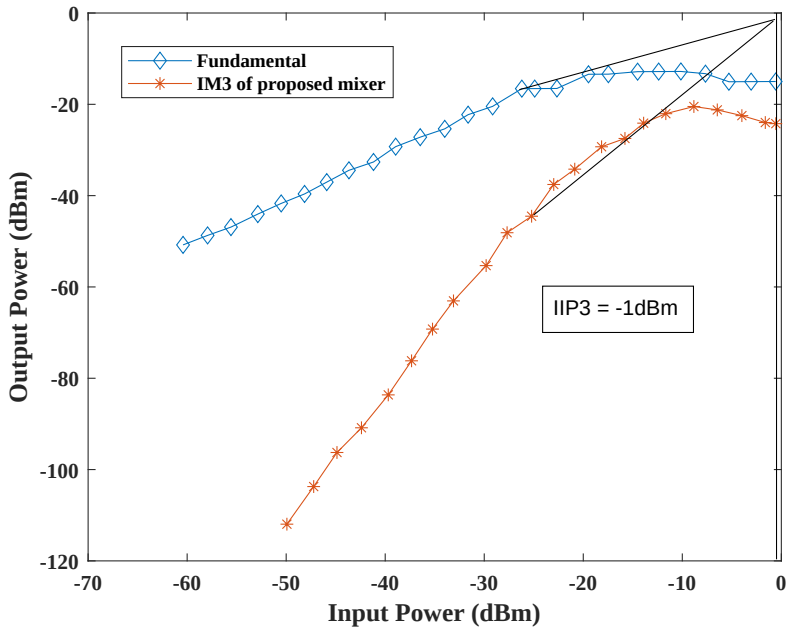


Figure 7.21: Simulated IIP3 after optimization of balanced mixer

The design variables for the linearity mixer are defined below: (a) $(\frac{W}{L})_1$-$(\frac{W}{L})_{16}$ = $\frac{1-200}{0.13}$, (b) (R_0-R_1)Ohms = 50-200, (c) (C_1-C_2)pF = 0.1-5.

PSO is implemented, and the optimization results have been obtained after defining the design variables and PSO parameters. The obtained optimized results have been compared with the

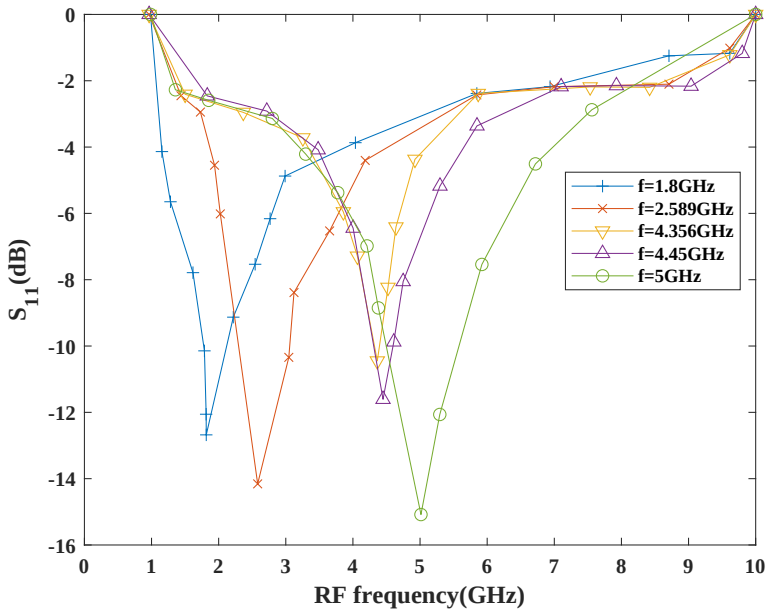


Figure 7.22: Simulated S_{11} after optimization of balanced mixer

previously obtained simulation results. Table 7.22 summarizes various mixer topologies that are simulated in different CMOS technologies. As per Table 7.22, it has been found that the proposed design attains the highest IIP3 in comparison to the other reported mixers while operating in a wideband. Figures 7.23-7.25 show the simulated and optimized results in terms of CG, NF, and IIP3, respectively. Upon performing the optimization, it has been found that the design attained high CG, high IIP3, and reasonable NF compared to the simulation results. The optimisation is performed in the same way as in the previous mixers.

7.7.4 SDR Receiver

This section describes an image-rejection receiver design, operating within a band of 0.9-20 GHz. This receiver is based on the mixer proposed in Chapter 5 that attains an excellent IIP3 and high CG performance while operating within a wideband. The proposed receiver architecture maintains similar IIP3 and CG performance with reasonable NF. PSO has been applied to the receiver for further performance improvement purposes by considering a suitable cost function while aiming to improve the CG, NF, and IIP3, respectively. The design specifications for the receiver design are defined below: (a) Supply voltage = 1.2V (b) CG $\geq$ 10 dB (c) NF $\leq$ 5 dB (d)

Table 7.22: Performance Comparison Summary-Linearity Mixer

References	Technology	Supply	RF(GHz)	NF(dB)	S_{21}(dB)	IIP3(dBm)
This work(O)	0.13um	1.2	0.9-7	3.4-5.78	17-18.9	44.5-48.4
This work(S)	0.13um	1.2	0.9-7	3.5-5.19	16.8-18.8	44.2-47.4
[48]	HEMT	1.2	1.8-5	<2	5-10	28
[123]	0.18um	2.4	2.4	11.2	23.7	-6
[248]	0.18um	1.8	1-10	16.7	6-3	0.15-2
[74]	0.18um	1.8	3.43	11.3-15	8.05	-10.8
[80]	0.09um	1.1	0.5-3.1	6.7	15	9.3
[135]	0.13um	1.2	0.5-6.5	13	10	9.52
[249]	0.18um	1.8	2.4	4.55	14.5	12.5
[238]	0.09um	1.2	2.4	11.4	12	19.6
[240]	0.09um	1	1-5	8.6	11.1	9.9
[250]	0.18um	1.5	2.4	14.87	3.3	5.46
[251]	0.18um	1.8	2.4	15	20.3	20.3
[252]	0.18um	1.8	2.1	14	15	15

* S-Simulation results, O-Optimization results

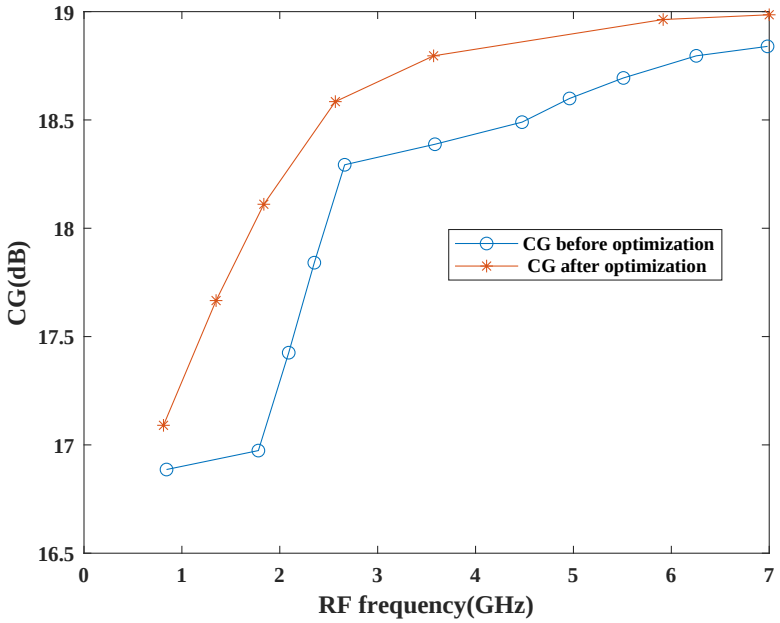


Figure 7.23: Simulated and optimized CG performance

IIP3 >1dBm. Likewise, PSO specifications are expressed as (a) swarm size = 30, (b) iterations = 1000, (c) c_1, c_2 = 1, (d) w = 0.4.

The design variables for the receiver are defined in terms of various blocks used within the circuitry. Starting with the LNA, the design variables for LNA are explained below: (a) $(\frac{W}{L})_1$-$(\frac{W}{L})_4$ = $\frac{10-100}{0.13}$, (b) (L_1-L_4)nH = 0.1-5. Likewise, the design variables for the LNA filter are

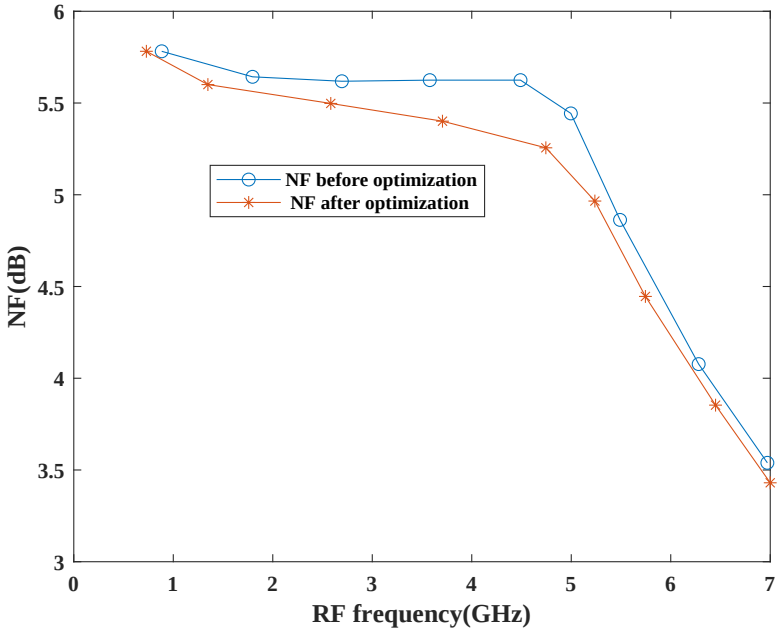


Figure 7.24: Simulated and optimized NF performance

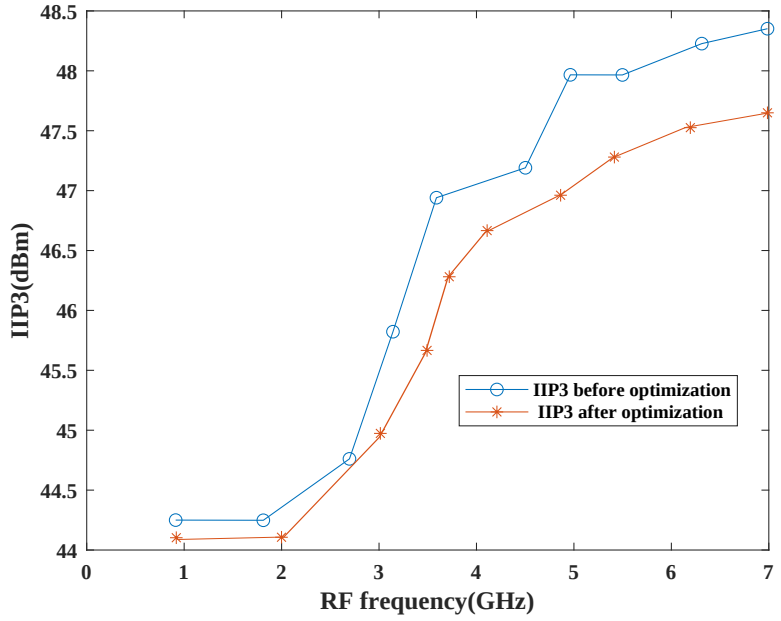


Figure 7.25: Simulated and optimized IIP3 performance

defined below: (a) (L_1-L_8)nH = 0.1-6, (b) (C_1-C_4)pF = 0.1-6. Similarly, the design variables for the mixer are expressed as: (a) $(\frac{W}{L})_1$-$(\frac{W}{L})_{16}$ = $\frac{1-200}{0.13}$, (b) (R_0-R_1)Ohms = 50-200, (c) (C_1-C_2)pF = 0.1-5. Additionally, the design variables for the IF Amplifier1 are expressed as: (a) $(\frac{W}{L})_1$-$(\frac{W}{L})_4$ = $\frac{20-120}{0.13}$, (b) (L_1-L_4)nH = 0.1-7. Furthermore, the design variables for the IF Amplifier2 are

expressed as: (a) $(\frac{W}{L})_1$-$(\frac{W}{L})_8$ = $\frac{10-150}{0.13}$, (b) (L_1-L_4)nH = 0.1-6. Finally, the design variables for the polyphase filter are expressed as: (a) (R_1-R_{18})Ohms = 50-200, (c) (C_1-C_{18})pF = 0.1-7.

Table 7.23: Performance Comparison Summary-Receiver

Ref	Freq(GHz)	Technology(nm)	CG(dB)	NF(dB)	IIP3(dBm)	IRR(dB)	Area(mm^2)	P_{diss}(mW)
This work(O)	0.9-20	130	25	<5	34.4	33	4	320
This work(S)	0.9-20	130	22.9	<5	32	30	4	320
[256]	0.402-0.405	180	40	9.2	Nil	Nil	0.873	0.16
[216]	5	180	28	9.7	-7.8	Nil	2.2	43.9
[143]	2.4	28	60	6	-16	Nil	0.48	0.9
[294]	24.5-43.5	45	35.2	3.2-6.1	Nil	32-56	0.77	60
[261]	3-6	40	>12.8	<5.8	>15.1	Nil	Nil	64.1-69.6
[295]	0.1-0.6	40	26.4-30.1	5.8/6.5	5.8	-20.1/-15.1	>34	41.1
[296]	4	65	25	23	Nil	Nil	1.1	0.267
[297]	0.5-1.2	65	35	6.7	10	>0	0.47	29.4
[253]	0.8-4	130	>25	3.8	-3.5	>38	33	0.25

* S-Simulation results, O-Optimization results

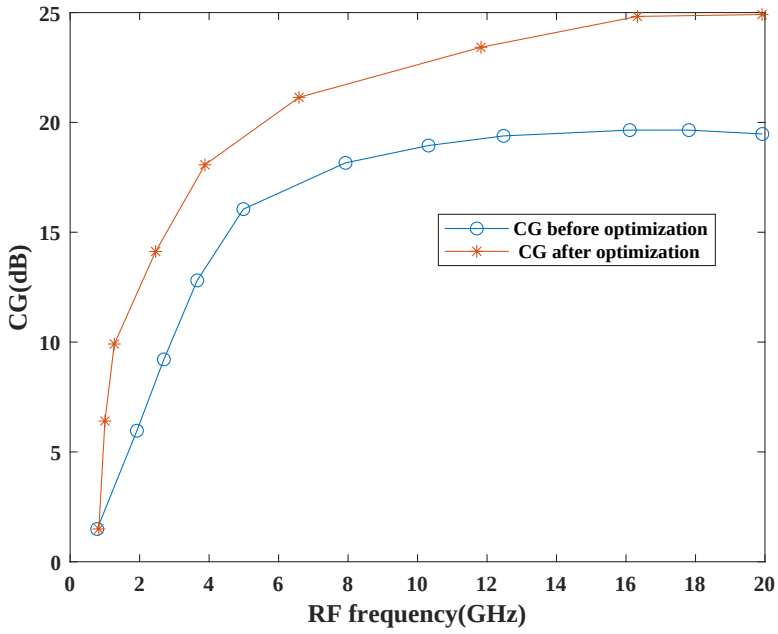


Figure 7.26: Simulated and optimized CG

To check the overall performance of the receiver, PSO is implemented, and optimization results have been obtained. The obtained optimized results have been compared with the previously obtained simulation results. The optimisation of a receiver is performed in the same way as in the previous mixers. Table 7.23 compares different receiver architectures simulated in different CMOS technologies. As per Table 7.23, it has been found that the proposed design attains the highest IIP3 in comparison to the other reported architectures while operating in a wideband.

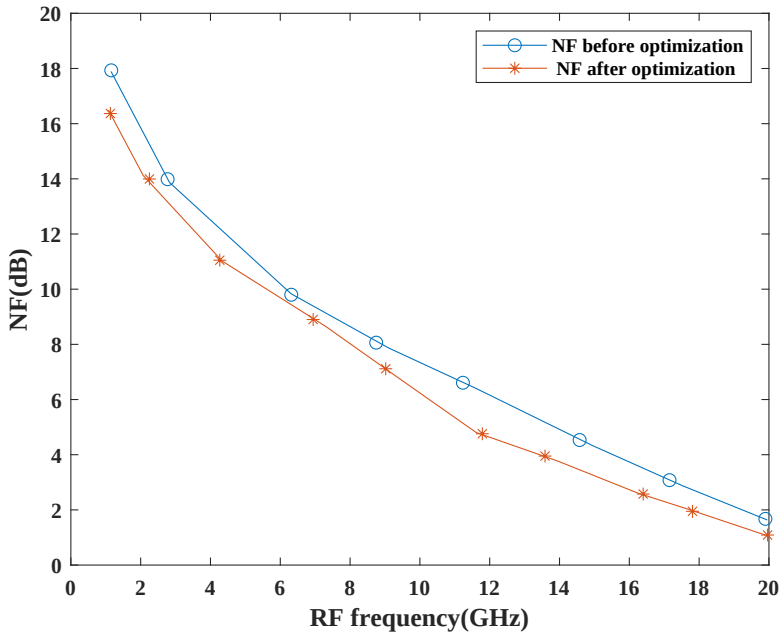


Figure 7.27: Simulated and optimized NF

Figures 7.26-7.29 shows the simulated and optimized results in terms of CG, NF, IIP3, and IRR, respectively. Upon performing the optimization, it has been found that the design attained high CG, high IIP3, and reasonable NF compared to the simulation results.

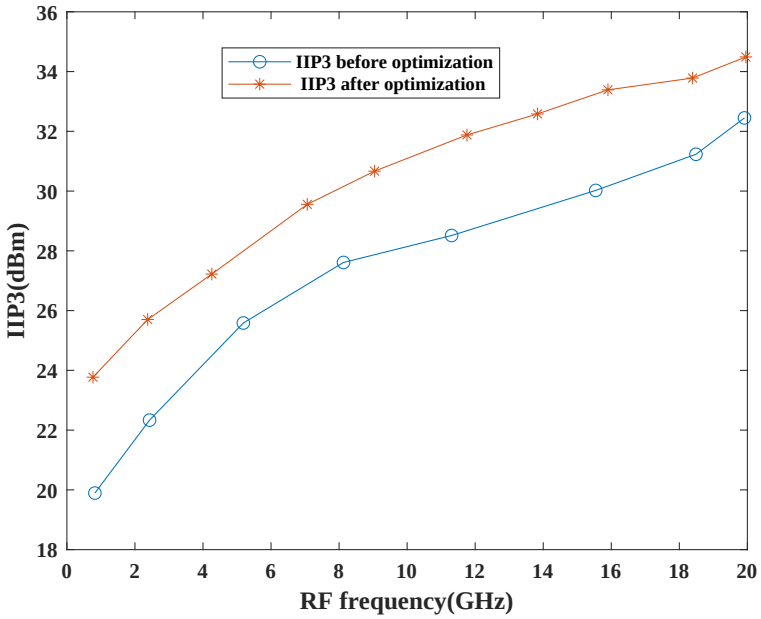


Figure 7.28: Simulated and optimized IIP3

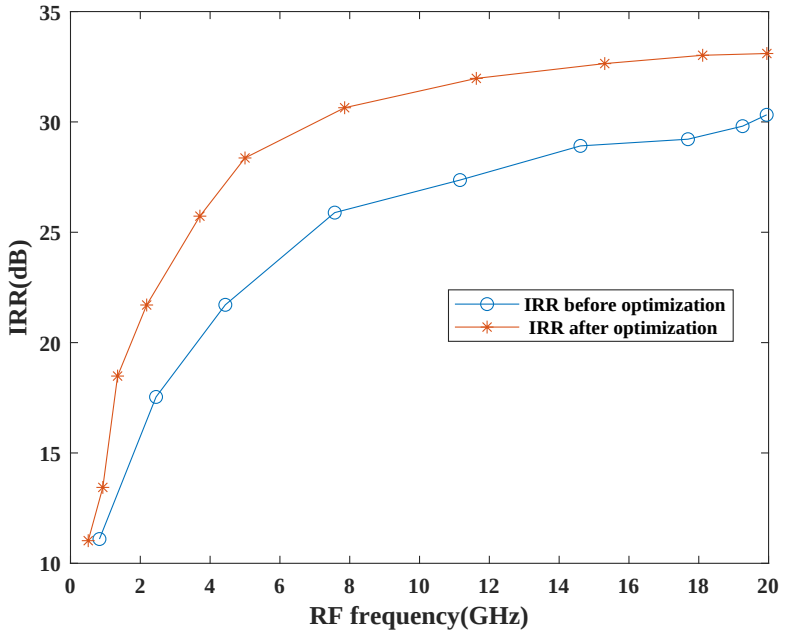


Figure 7.29: Simulated and optimized IRR

7.8 Conclusion

This chapter covers the design and optimization of proposed circuits discussed in previous chapters using the PSO. This, in turn, improves the overall design performance while operating a wideband. Thus, PSO is reliable for reconfigurable circuits with software-defined radio applications.

Chapter 8

Conclusion and Recommendations for Future Work

8.1 Conclusion

Recent advancements in integrated circuits and the almost greedy demand for pervasive wireless connectivity have contributed to the flourishing of wireless communication systems, bringing along an ever-increasing number of communication standards / protocols. Traditional radio systems' hardware is protocol-dependent, making them inadequate to cope with the evolution of wireless standards. As such, software-defined radios (SDRs) were proposed to address the challenge. SDRs are expected to offer reconfigurability, high efficiency, and low cost. Although many components in a traditional radio can be implemented in its software counterpart, a few analogue components, including antennas, low noise amplifiers, and mixers, remain in their analogue form. This thesis focuses on the design of reconfigurable wideband mixers and receivers for SDRs, while considering a good balance among various performance metrics, including frequency range, conversion gain (CG), noise figure (NF), image rejection ratio (IRR), IIP3. Additionally, filtering, signal-to-noise ratio, and spurious-free dynamic range should be considered in the design of SDR mixers. Thus, it is desirable to select the design techniques carefully for the successful implementation of SDR mixers. We have identified the best design

techniques to implement high-performance SDR mixers.

Firstly, we propose the design and analysis of g_m-boosting, image rejection reconfigurable Gilbert mixer. The design has been developed and simulated in Cadence virtuoso software. The proposed mixer operates in 0.9-13.5 GHz band, attains a high CG of 22 dB and an excellent IRR of 30.2 dB. Additionally, the mixer maintains a low NF of 2.5 dB with poor IIP3 of -3.28 dBm. The mathematical analysis provides the detailed mathematical approach for the proposed design. Pre and post-layout results have been obtained and compared to check the feasibility of the design. The simulation results show that the mixer operates in a wide band and attains high CG and IRR. Additionally, the mixer also maintains a low NF at the expense of IIP3. The reliability analysis is done using Relxpert Cadence to check the behaviour proposed after 5 years of aging. Secondly, we propose the design and analysis of a compact, balanced reconfigurable mixer. The proposed design follows a 1.8-5 GHz balanced mixer topology, and the current is controlled using the current mirror technique. Likewise, employment of the current bleeding approach results in low NF and reasonable CG of 18.32 dB and low NF of 1.19 dB. Additionally, it covers a small die area of 0.32 mm^2 and consumes low power of 10 mW with poor IIP3 of -5.89 dBm. Thirdly, we propose the design and analysis of 0.9-7 GHz an active inductor-based reconfigurable mixer. The active inductor circuit is highly tuned with the parasitic capacitance of the proposed mixer. Diode and current mirror loads are employed at the load stages instead of resistors due to the restricted values of the resistors. The current mirror circuit controls the overall current within the mixer. The proposed mixer attains an excellent IIP3 of 47.4 dBm with a NF of 3.5 dB and a CG of 30.35 dB at the highest frequency.

Fourthly, we also propose the design and analysis of 0.9-20 GHz I/Q receiver consisting of front-ends such as LNAs, downconversion I/Q mixers, filters, and IF amplifiers, respectively. The proposed receiver attains high performance while operating in a wideband. The cascode topology has been opted for LNA to maintain high CG. An active inductor-based mixer is proposed for better linearity performance while maintaining a small mixer design area. Furthermore, reconfigurable filter and RC polyphase filters are part of the receiver circuitry for maintaining suitable reconfiguration and rejecting the image obtained from the mixer circuits. IF amplifiers

are responsible for lowering the attenuation from the previous stages and signal amplification for improving the signal strength of the output signal. The proposed receiver shows significant improvement in terms of various performance parameters where IIP3 and CG are 32 dBm and 22.9 dB, respectively. Furthermore, the receiver attains reasonable NF of 5 dB while covering the design area of 4 mm^2.

Optimization is the process of determining the best possible solution for a particular problem under given conditions. PSO is one of the most effective optimization approaches for improving the overall performance of reconfigurable circuits. Thus, it has been adopted in our proposed mixers and receiver designs to strengthen the circuitry's overall performance by using MATLAB. Thereafter, the optimized results are compared with the previously obtained unoptimized simulation results. Based on the observation, it has been found that the optimized results outperform the unoptimized results, making them suitable for SDR applications.

To conclude, the proposed mixer and receiver circuits can operate within a wideband while attaining suitable reconfiguration within the entire band of operation. The proposed mixers and receiver circuits are compared with the recent works. The comparative study shows that the proposed circuits attain high performance in terms of most of the performance metrics.

8.2 Recommendations for Future Work

Although different reconfigurable mixer and I/Q receiver circuits were proposed and presented in this thesis, there is still a possibility to improve these designs. The recommendations for future work are enlisted below:

The current literature study lacks significant research on reconfigurable mixers operating in a wideband and showing high performance while maintaining a small chip area. Inductorless, microstrip line, or transformer-based transformer-based matching techniques are effective solutions to overcome this problem. They cover a small die size and consume low power while maintaining good IIP3.

Cascode techniques are not commonly used in mixer circuits especially cascode current bleeding

or cascode transconductance stage. However, these techniques can be highly beneficial to improve the overall performance of the reconfigurable mixer circuits as the cascode structure maintains good port isolation. This, in turn, will eliminate the Miller effect and hence contributes towards higher bandwidth. Additionally, the design consumes low power and maintains high CG performance.

Switchable reconfigurable mixers can use analog or digital switches for maintaining suitable reconfiguration. Discrete switches are more advantageous than analog switches as they can maintain good return loss while operating within a wideband. However, the literature covers a limited amount of works in this direction. Thus, more research can be done in this direction while keeping in mind the switching speed, efficiency and maintaining a good trade-off among other performance metrics.

Multi-Objective Particle Swarm Optimization (MOPSO) is beneficial for resolving problems with multiple objectives. MOPSO is widely used to resolve various engineering problems. However, this approach is relatively new for the RF domain. Most RF researchers use conventional design approaches or tools for circuit design optimization, which are expensive, time-consuming, and are restricted to narrowband applications. Thus, incorporating the MOPSO approach in reconfigurable circuits will save time and improve the overall performance.

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Appendix A

Derived Formulas

A.1 Derivation of high-frequency noise of mixer

Starting with the noise contribution from the RF stage as per Figure 3.8, the noise signal at the output of the transconductor when multiplied with the switching pair's instantaneous current gain $p_{1(t)}$ results in a current noise , $i_{o14(t)}$ as

$$i_{o14(t)} = n_{o14(t)} p_{1(t)} \tag{A.1}$$

By considering the above process as a time-average wide sense stationary process, the power spectral density of the noise current is expressed as

$$< S^{0}{}_{n014}(\omega t) >= \sum_{n=-\infty}^{\infty} |p_{1,n}|^2 S_{n014}(\omega - n\omega_{LO}) \tag{A.2}$$

For the overall analysis of power spectral density at the RF stage, both correlated and uncorrelated power spectral density factors have to be considered. Thus, the uncorrelated power spectral density is expressed as

$$S^{(u)}{}_{n014}(\omega)|_{\overline{V^2}_{n,rg014}+\overline{V^2}_{n,RG014}} = (\overline{V^2}_{n,rg014} + \overline{V^2}_{n,RG014}) \frac{g^2{}_{m14}}{[\omega(C_{gs14} + C_{gd14})R_{GG014}]^2 + 1} \tag{A.3}$$

where R_{G014}, r_{g014} refer to the external gate resistance (parallel combination of the resistors) and internal gate resistance.

$$S^{(u)}{}_{n014}(\omega)|_{i_{ng014,u}} \approx \overline{I^2{}_{ng014,u}} \frac{g^2{}_{m14}}{[\omega(C_{gs14}+C_{gd14})R_{GG014}]^2+1} \tag{A.4}$$

Likewise, the correlated power spectral density can be expressed as

$$S^{(c)}{}_{n014}(\omega) = [(k_c+1)^2 + k^2{}_c|H_T14(\omega)|^2 - 2k_c(k_c+1)Re[H_{T14}(\omega)]]\overline{I^2{}_{nd014}} \tag{A.5}$$

Thus, the overall power spectral density is expressed as

$$S_{n014}(\omega) = S^{(u)}{}_{n014}(\omega) + S^{(c)}{}_{n014}(\omega) = (k_c+1)^2 A_{s014}\overline{I^2{}_{nd014}}[\frac{1+\frac{1}{A_{s014}}(\frac{\omega}{\omega_{z014}})^2}{1+(\frac{\omega}{\omega p014})^2}] \tag{A.6}$$

Next, the power spectral density due to LO stages is expressed as

$$\begin{aligned} S_{n01}(\omega) + S_{n45}(\omega) = 2[S^{(u)}{}_{n01}(\omega) + S^{(c)}{}_{n01}(\omega) + S^{(u)}{}_{n45}(\omega) + S^{(c)}{}_{n45}(\omega)] = \\ 2[(k_c+1)^2 As_{01}\overline{I^2{}_{nd01}}[\frac{1+\frac{1}{A_{s01}(\frac{\omega}{\omega_{z01}}{}^2)}}{1+(\frac{\omega}{\omega_{p01}}{}^2)}] + (k_c+1)^2 As_{45}\overline{I^2{}_{nd45}}[\frac{1+\frac{1}{A_{s45}(\frac{\omega}{\omega_{z45}}{}^2)}}{1+(\frac{\omega}{\omega_{p45}}{}^2)}]] \end{aligned} \tag{A.7}$$

Considering the noise present at LO ports are stationary. Thus, time- averaged power spectral density of current noise at the output of the proposed mixer due to LO stages is expressed as

$$< S^0{}_{nLO}(\omega t) >= 4kT(R_{LOI}+2r_{G1})\overline{G^2}(t) + 4kT(R_{LOQ}+2r_{G2})\overline{G^2}(t) \tag{A.8}$$

where R_{LOI}, R_{LOQ} refer to equivalent noise resistances and r_{G1}, r_{G2} refer to poly gate resistances. As the image signal does not carry any important information, therefore the single sideband noise figure is considered over the double sideband noise figure as

$$NF_{\text{SSB}} = \frac{\int_0^\infty < S^0{}_{\text{n014}}(\omega,t) > d\omega}{|g_{\text{c}}(\omega)|^2} \frac{1}{4kTR_{\text{G}}}$$
$$= \frac{< S^0{}_{\text{n014}}(\omega,t) > + S^0{}_{\text{n01}}(\omega,t) + S^0{}_{\text{n45}}(\omega,t) + < S^0{}_{\text{nLO}}(\omega,t) > + (4kTR_{10} + 4kTR_{11}||G_{\text{M}})}{|g_{\text{c}}(\omega)|^2} \tag{A.9}$$

The above expression is defined for a single balanced mixer. Similarly, for the double balanced mixer, NF can also be defined which is almost twice the one obtained for a single balanced mixer.