Design of an Efficiency Improved Dual-Output DC-DC Converter Utilizing a Supercapacitor Circulation Technique

ABSTRACT

The Supercapacitor Assisted Low Dropout Regulator (SCALDO) is a novel approach of achieving high end-to-end efficiency (ETEE) in linear, step-down, DC-DC converters. This patented technique is well established and have come up with various proof-of-concept prototypes showing its efficiency advantage in the range of factor of 1.33 to 3 along with the other excellent linear characteristics such as low noise and high slew rate. As a better way of utilizing this approach to multiple voltage rail applications such as mobile battery operated products, processor-based systems, automotive systems, and data centers, a further extension to the technique called Dual-Output Supercapacitor Assisted Low Dropout Regulator (DO-SCALDO) has been suggested. The new approach has dual output levels within the same design which can be the same or different voltage levels. In this paper, the design approach and the practical implementation details of a prototype version of 6V-to-dual 1.8 V DO-SCALDO are discussed.

INTRODUCTION

In battery powered portable devices, multiple output voltage rails are required to power the internal hardware such as memory, USB, Bluetooth, and system core. Because of the low output noise and electromagnetic interference (EMI) requirement of battery powered products, specific low dropout regulators (LDOs) with different voltage levels such as ADP170/171, ADP1706, ADP121 and APD130 from Analog Devices have been introduced into the market [1]. Furthermore, Linear Technology has introduced LT3694 monolithic buck regulator with dual LDO targeting multiple voltage rail requirement in digital loads [2]. Therefore, the necessity of dual output and low noise linear regulators has been risen for wide variety of power electronic applications.

Moreover, the SCALDO technique has been introduced and patented to improve the end-to-end efficiency (ETEE) of linear regulators [3]. In this technique, a single supercapacitor (SC) or arrays of SCs are utilized depending upon the voltage requirements while keeping the switching frequency from few Hz to 100s of Hz [4]-[6]. References [4]-[9] show that the 5-3.3V, 5-1.5V and 12-5V SCALDO topologies can achieve ETEE of 92%, 83% and 83% respectively. Nevertheless, the SCALDO topologies implemented formerly, can only produce single output voltage

level [4]-[12]. This technique can be further extended to generate dual output voltage rails to match the requirements of portable devices with higher efficiency.

SCALDO TECHNIQUE

The Fig.1 shows the basic SCALDO concept where a SC switching arrangement is used to increase the ETEE of a LDO.

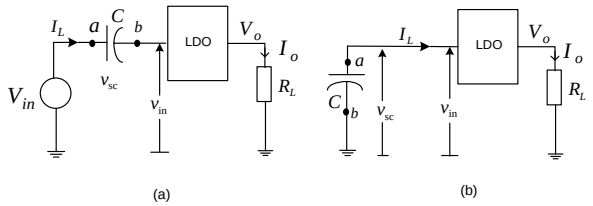


Figure 1. Basic concept of SCALDO: (a) SC charging phase; (b) SC discharging phase

The fundamental concept of choosing a SC as the series loss-less dropper is due to its small voltage difference for a finite amount of time in charging and discharging phases. These characteristics of a SC will reduce the switching frequency and minimize the losses in the overall system [4]-[6]. According to Fig.1(a), the SC charges until the input voltage of LDO drops to its minimum operating voltage of regulation ($V_{\min}$), while the voltage across the SC reaches $V_{in} - V_{\min}$ at the end of the charging cycle; where V_{in} is the unregulated input voltage [5]. The voltage of SC after the charging process should satisfy the criteria; $V_{in} - V_{\min} > V_{\min}$ in order to discharge back to $V_{\min}$ as depicted in Fig.1 (b). Therefore, the topology requirement for this case is $V_{in} > 2V_{\min}$. The circuit draws power from the unregulated input only for the charging phase of the SC. When the control circuit current is neglected, the approximate ETEE efficiency ($\eta_{app(SCALDO)}$) of the $V_{in} > 2V_{\min}$ topology can be found as,

$$\eta_{app(SCALDO)} = \frac{P_{out}}{P_{in}} = \frac{I_L V_{out}}{V_{in}(I_{in}/2)} = 2\frac{V_{out}}{V_{in}} \quad (1)$$

Where; P_{in}, P_{out}, I_{in}, I_L and V_{out} are the input power, output power, unregulated input current, load current and regulated output voltage respectively. If the LDO is operated from the same unregulated supply without use of the SCALDO technique, the approximate ETEE efficiency is V_{out}/V_{in}. Therefore it can be seen that the SCALDO technique applied for the topology of $V_{in} > 2V_{\min}$, the approximate ETEE is enhanced by the factor of 2.

When designing dual output DC-DC converters with the existing SCALDO technique, separate SCALDO units should be added to each regulation stage which will ultimately increase the number of switches and SCs in the

circuit [4]-[12]. As a better way of utilizing the SCALDO concept into application specific designs, DO-SCALDO method is introduced as a compact single converter having reduced switches and SCs.

THEORETICAL BACKGROUND OF DO-SCALDO TECHNIQUE

The main objective of the DO-SCALDO technique is to make two output voltage levels available in a single design while maintaining the useful hallmarks of the original SCALDO approach. In order to achieve the dual outputs, two LDOs with different output voltage levels can be cascaded as shown in Fig.2 (a).

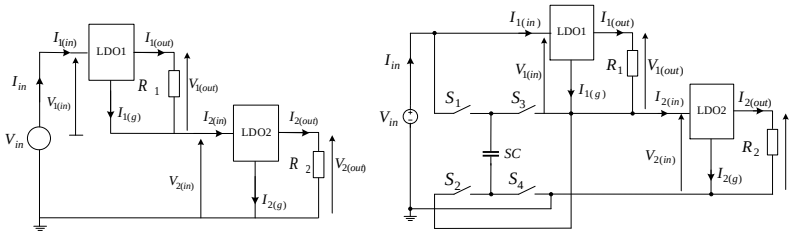


Figure 2: (a): Cascaded two LDOs; (b): Cascaded two LDOs with SC switching arrangement

The cascaded LODs in Fig.2 (a) can be operated if and only if their ground pin currents and output currents are equal (These derivations will be provided in the final paper) [13]-[14]. However, in practical circumstances, DC-DC converters with dual outputs, are not always required to handle the equal loads currents. Therefore, when the two loads currents are different, a SC can be introduced as a bypass element to pass the excess current of two LDOs with a switch arrangement as shown in Fig.2 (b). When the regulated output of two LDOs are equal, only single SC is required as the bypass element. This is known as the identical-DO-SCALDO technique. Conversely, two or more SCs are required if the regulated output voltages are different which is known as the different-DO-SCALDO technique. In this digest, the discussion is limited only for the identical-DO-SCALDO.

IDENTICAL-DO-SCALDO TECHNIQUE

In this approach, two LDOs are cascaded to deliver two different load currents with the same regulated output voltage. This topology needs satisfy the condition $V_{in} > 2V_{\min}$ for the implementation to be achievable. The SC is switched between the inputs of two LDOs depending on the output current difference.

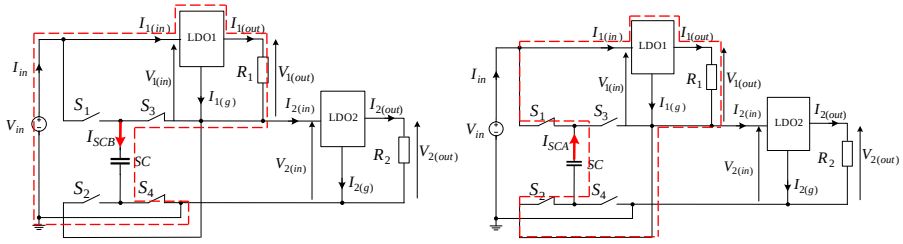


Figure 3: SC witching arrangement for steady state current $I_{1(out)} > I_{2(out)}$: (a) SC charging phase (b); SC discharging phase

When the load currents of two LDOs are equal in the steady state, the SC will neither charges nor discharges and remains in the last switched position. If the steady state output current of LDO1 is greater than output current of LDO2 ($I_{1(out)} > I_{2(out)}$), the switches S_3 and S_4 are kept close and S_1 and S_2 are kept open to place the SC across the input of LDO2 to pass the difference of the load currents ($I_{1(out)} - I_{2(out)}$) as shown in Fig.3 (a). At this stage the SC charges and the input voltage of LDO1 decreases. The SC is kept in this position until the input voltage of LDO1 reaches the minimum working voltage of the LDO ($V_{\min}$). When the LDO1 input voltage drops to $V_{\min}$ at the end of the charging cycle, the SC is placed across the LDO1 for discharging as depicted in Fig.3 (b). Since the voltage of SC falls at this stage, the input voltage of LDO1 also decreases back to $V_{\min}$. This process continuous until the condition $I_{1(out)} > I_{2(out)}$ is valid. The SC charging time ($t_{cB(app)}$) and discharging time ($t_{dA(app)}$) can be found as,

$$t_{cB} = t_{dA} = C\left[V_{in} - 2V_{\min} - 2(2r_s + r_c)(I_{1(out)} - I_{2(out)})\right] / I_{1(out)} - I_{2(out)} \quad (2)$$

Where; C is the capacitance of the SC, r_s is the resistance of a single switch, r_c is the ESR of SC

In the case where, steady state currents $I_{2(out)} > I_{1(out)}$, the SC is placed across the input of LDO1 to pass the surplus current $I_{2(out)} - I_{1(out)}$. The SC releases its stored energy when it is placed back to input of LDO2. The charge balance of the SC is controlled throughout the whole process. The charging and discharging times of the SC in this scenario follow the same format defined in (2). It can be shown that the theoretical maximum ETEE improvement factor ($\alpha_{th(\max)}$) of identical -DO-SCALDO is 2 (The derivations will be shown in the final paper).

DESIGN OF 6V-TO-DUAL-1.8 V DO-SCALDO REGULATOR

Applying above design concepts, a proof-of-concept prototype of 6V-to-dual-1.8 V was developed using two LT3086 adjustable LDOs and 5F supercapacitor. Four photovoltaic switches were used as S_1 to S_4 and were controlled by a ATTiny861A microcontroller. (The schematics and a detailed implementation will be provided in final paper).

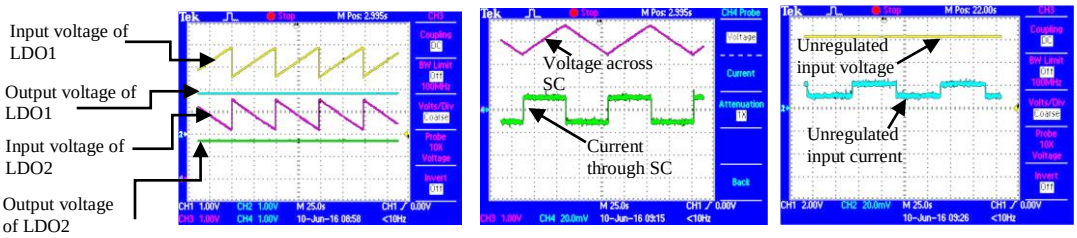
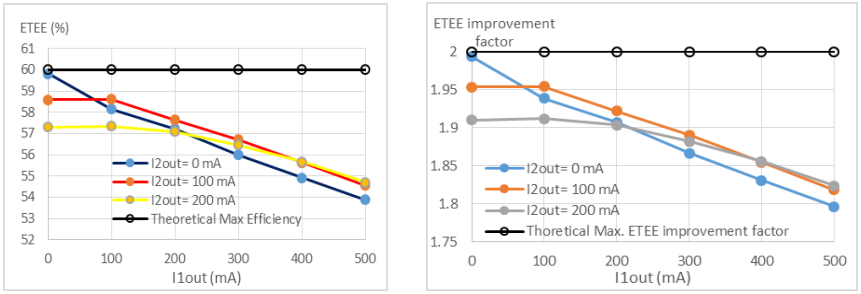


Figure 4: (a) LDO1 and LDO2 input and output voltage waveforms; (b) Voltage and current waveforms of supercapacitor; (c) Voltage and current waveforms of unregulated input

Fig.4 (a), (b) and (c) show the oscilloscope waveforms when the load currents of LDO1 and LDO2 were set to 100 mA and 200 mA respectively. The input supply current and the current through the SC were measured using a hall-effect current sensor of 100mV/A gain. According to Fig.4 (a), both LDOs achieved a fixed output voltage of 1.8V. The charging and discharging current of the SC is 100mA and the voltage difference of each phase was around 1.4 V as depicted in Fig. 4 (b). The unregulated input current is 200mA in the SC charging phase and 100mA in the SC discharging phase as displayed in Fig.4 (c). The prototype was tested for different output currents. Fig.5 (a) and Fig.5 (b) summarize the ETEEs and the ETEE improvement factors obtained for the 6V-to-dual-1.8 V DO-SCALDO prototype for different steady state currents.



(a) (b)

Figure 5: (a) End-to-end efficiencies; (b) End-to-end efficiency improvement factors

The theoretical maximum ETEE achievable from a single stage independent 6V to 1.8V dual LDOs (without cascading) is 30%. With the introduction of DO-SCALDO technique, the ETEE of two LDOs can be increased up to a maximum of 60%. Fig.5 (a) shows that the ETEE of the prototype is in the range of 54% to 60% for the tested current levels. Due to resistance of the switches, ESR of the SC and the wire resistances, the ETEE of the initial prototype is less than 60% and drops with the difference of the two load currents. Similarly, from Fig. 5 (b), it can be seen that the ETEE improvement factor also declines with the load current difference.

CONCLUSIONS AND FUTURE WORK

In this paper, the design concepts and the implementation details of the DO-SCALDO technique is discussed. This technique can be applied to increase the end-to-end efficiency of linear regulators by a factor of 2. A 6V-to-dual-1.8V DO-SCALDO prototype was successfully implemented to show that the identical-DO-SCALDO can reach the theoretical maximum end-to-end efficiency improvement factor of 2 compared to independent operation of two LDOs. Further design and research work to utilize this concept to implement a Positive and Negative DC-DC converter are currently under way.

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