Advanced Analysis of Supercapacitor-Assisted Low-Dropout (SCALDO) Regulator

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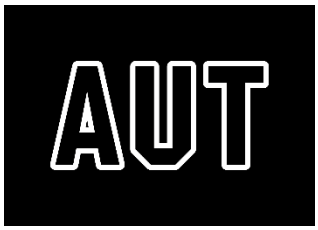

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Abstract

DC-DC converters can be found in three basic forms which are the linear regulators, the switch-mode power supplies (SMPSs) and the charge pumps. The combinations of these topologies are prevalent in power management circuits where the designers try to achieve cost-effectiveness, low output noise, high end-to-end efficiency and predictable transient response in these converters to make them suitable for a steady and constant power supply with regulation and multiple outputs.

Combining an array of low equivalent series resistance (ESR) supercapacitors (SCs) and a linear low-dropout (LDO) regulator, a unique DC-DC converter topology has been developed over the past nine years; this technique is called the supercapacitor-assisted low-dropout (SCALDO) regulator. In the SCALDO approach, one or more supercapacitors are used in the series path of a LDO regulator as a lossless dropper and the excess energy accumulated in the SCs is re-circulated at a very low frequency to increase the end-to-end efficiency by a multiplication factor in the range of 1.33 to 3. During the past several years, the SCALDO technique was further developed into many applications by introducing the reduced-switch topology and DC-UPS capability. Also, this technique has been identified as a potential area where further research can be carried out to match various power management requirements.

After a comprehensive investigation of feasible SCALDO implementation scenarios for multiple outputs, it was found possible to narrow them down to a detailed analysis of two output stages in a single converter which is substantial research for a PhD thesis. This dual-output converter is called the dual-output SCALDO (DO-SCALDO) regulator. In this method, dual-polarity voltage levels are generated from a single input voltage source whilst maintaining the useful characteristics of the original SCALDO approach such as high efficiency, low noise, fast dynamic response and low EMI/RFI issues. This thesis describes the conceptual background of the DO-SCALDO technique together with the working principles related to the different modes of operation. The theoretical concept is validated by the experimental results of a prototype version of a 12 V to ±5 V DO-SCALDO regulator. The steady-state and transient responses are investigated. The end-to-end efficiencies and the losses are

also determined, and the unique characteristics and potential advantages are compared with the commercial dual-output DC-DC converters.

In addition to the DO-SCALDO concept, the stability analysis of the single-stage SCALDO regulator is also considered as another potential area for further research. Since the SCALDO approach works based on a low-frequency SC circulation technique at the front end of a LDO regulator, the stability of the LDO regulator might be affected due to this external SC circulation network. Therefore, the overall circuit should be analysed for stability. The outcomes of this study can be used to stabilise the discrete SCALDO regulators or SoC (System on a Chip) designs. This thesis explores the design parameters and constraints regarding the stability of the fundamental SCALDO topology with the aid of the small-signal model. The open-loop transfer function is derived, and the possible frequency compensation techniques are identified. The theoretical small-signal model is validated from the simulated and experimental results of a 12 V to 5 V discrete SCALDO regulator, and the conclusions are made accordingly.

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Attestation of Authorship

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person (except where explicitly defined in the acknowledgements), nor materials which to a substantial extent has been submitted for the award of any other institution of higher learning.

Kasun Subasinghage: ……..

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Nomenclature

Abbreviations

Abbreviation	Description
AC	Alternative current
ADC	Analog-to-digital converter
BJT	Bipolar-junction transistor
DAC	Digital-to-analog converter
DC	Direct current
DO-SCALDO	Dual-output supercapacitor-assisted low-dropout regulator
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESR	Equivalent series resistance
ETEE	End-to-end efficiency
GND	Ground
IC	Integrated circuit
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCD	Liquid crystal display
LDO	Low-dropout regulator
MCU	Microcontroller unit
PCB	Printed circuit board
PM	Phase margin
PMOS	P-channel MOSFET
PSRR	Power supply rejection ratio
RFI	Radio frequency interference
SC	Supercapacitor
SCC	Switched-capacitor converter
SCALDO	Supercapacitor-assisted low-dropout regulator
SMD	Surface mount device
SMPS	Switch-mode power supply

SoC	System-on-Chip
VRM	Voltage regulator module
t	Time
T	Periodic time
TF	Transformer
UGF	Unity gain frequency
UPS	Uninterrupted power supply

List of Symbols and Definitions

Symbol	Definition
C_b	Bypass capacitor
C_{DS}	Drain-source parasitic capacitances of the PMOS
C_F	Feedforward capacitor
C_{FL}	Flying capacitor
C_{GD}	Gate-drain parasitic capacitances of the PMOS
C_{GS}	Gate-source parasitic capacitances of the PMOS
C_o	Output capacitor
C_{sc}	Capacitance of the Supercapacitor
G_{ea}	Gain of the error amplifier
G_{fb}	Feedback gain
g_m	Transconductance of the PMOS
GND_{in}	Common ground of the circuit
GND_V	Virtual ground terminal
$G(s)$	Plant transfer function of the SCALDO regulator
$H(s)$	Transfer function of the feedback network
I_{diff}	Differential load current
$I_{g(LDO)}$	Ground pin current of the LDO regulator
I_{in}	Current of the input power source
$I_{in(LDO)}$	Input current of the LDO regulator
I_L	Load current
I_{MCU}	Input current of the microcontroller unit

$I_{o(LDO)}$	Output current of the LDO regulator
I_{SC}	Current through the SC
$I_{SC(c)}$	Charging current of the SC
$I_{SC(d)}$	Discharging current of the SC
LDO_N	Negative-rail LDO regulator
LDO_P	Positive-rail LDO regulator
R_C	*Series resistor used to charge the SC
r_D	Resistance of the drain terminal of the PMOS
r_{ds}	Output resistance of the PMOS for small-signals
R_{ESR}	Equivalent series resistance (ESR) of the output capacitor
r_G	Resistance of the gate terminal of the PMOS
R_{in}	Equivalent resistance of the switching network
R_L	Output load resistance
R_o	Series output resistance of the error amplifier
R_{pa}	The sum of the output resistance of the error amplifier and the gate terminal of the series-pass device
r_S	Resistance of the source terminal of the PMOS
R_{SC}	Equivalent series resistance of the supercapacitor
R_{SW}	Equivalent resistance of a switch
S_1, S_2, S_3, S_4, S_5	Switches
t_c , t_d	Duration of the charging phase and the discharging phase of the SCALDO regulator, respectively
$T(s)$	Open-loop gain of the SCALDO regulator
V_{fb}	Voltage of the feedback network
v_{fb}	Small signal of the feedback voltage
v_{gs}	Gate-source small-signal voltage
V_{in}	Voltage of the input power source
$V_{in(LDO)}$	Input voltage of the LDO regulator
V_{min}	The minimum input voltage required for the regulation of the LDO
V_{oe}	Amplified error signal
v_{oe}	Small signal of the amplified error
$V_{o(LDO)}$	Output voltage of the LDO regulator
v_{out}	Small-signal output voltage of the SCALDO regulator

v_{ref}	Small-signal of the reference voltage
V_{ref}	Reference voltage
V_{SC}	Voltage across the supercapacitor
ω	Angular frequency
ω_{p1}, ω_{p2}, ω_{p3}, ω_{p4}	First pole, second pole, third pole, and fourth pole of the SCALDO open-loop transfer function, respectively
$\omega_{p1(ea)}$	Low-frequency pole of the error amplifier
ω_{z1}, ω_{z2}, ω_{z3}	First zero, second zero and third zero of the SCALDO open-loop transfer function, respectively
z_o	Output impedance of the LDO regulator
λ	Channel length modulation

* A different definition is used for R_C in appendix A.

Chapter 1 Introduction

This chapter introduces the scope of the thesis along with the conceptual background, and the evolution of the supercapacitor-assisted low-dropout (SCALDO) regulator. Further development pathways of the SCALDO technique are considered, the motivation of the research work is expressed, and the potential research contribution is identified. In addition, this chapter provides an overview of the structure of the thesis and a list of international publications related to the research.

1.1 Background

Power management with higher energy efficiency is a key challenge in modern DC electronic systems, such as portable devices, medical instruments, and data centres. Energy efficiency, in fact, is essential for battery longevity in battery-powered products, whereas the optimised power management leads to durability, usability, and functionality in all the devices. Therefore, product manufacturers always strive to look for DC-DC converters that can offer not only high end-to-end efficiency (ETEE) but also other essential requirements including low noise, fast transient response, simplicity, and reduced EMI/RFI [1-3].

Linear regulators, switch-mode power supplies (SMPSs) and switched-capacitor converters (SCCs) also known as charge pumps are the common design approaches for DC-DC converters [4]. These three techniques have merits and drawbacks [5]. For example, SMPSs can perform both step-up and step-down DC-DC conversion while operating at high efficiencies [6]. Nevertheless, they bring a major design issue of EMI/RFI [6]. On the other hand, SCCs are limited to low current applications, for example, memory circuits where step-up or inversion of voltage is required [7-9]. Linear regulators offer simplicity, compact design and several performance advantages including low output noise, fast dynamic response, and no-minimum load restriction [10]. Nonetheless, they can only provide step-down voltage conversion. In addition, the efficiency of a linear regulator drops dramatically when the voltage headroom increases. Since the quiescent current of a commercial off-the-shelf linear regulator is very low compared to its full load current, this efficiency issue is mainly due to the excessive power dissipation of the series-pass transistor

[5]. These three techniques are combined in some designs to provide an overall solution addressing efficiency, noise, dynamic response and size [4].

Low-dropout regulators (LDOs) are a special type of linear regulator, which are designed to operate under very low input to output voltage difference to achieve high ETEE. LDOs, with their low headroom voltage, provide very low noise and high current slew rate capable linear DC power rails [11]. Commercial off-the-shelf LDOs can be found in the form of silicon ICs which occupy a very small PCB area. In addition, LDOs are used as post regulators with SMPSs in wider DC power management solutions, because in switching regulators, although the efficiency is enhanced, several other issues, for instance, the switching noise, the poor dynamic response could arise. LDOs are the ideal candidate to power up processors, microcontroller units (MCUs) and mixed-signal circuits which require a fast dynamic response and low noise. Typical applications of the LDOs include cell phones, cameras, PDAs, and notebooks. They are also used in automotive, industrial and wireless applications.

The supercapacitor-assisted low-dropout (SCALDO) regulator was discovered and developed by the power electronics research team in the School of Engineering at the University of Waikato, New Zealand [12-18] to overcome the low-efficiency of a linear regulator circuit when the input-output voltage difference is high. This technique was granted a US patent in 2011[19]. Also, it has been identified as a unique new approach to design DC-DC converters applicable to processor power supplies with very high ETEE. An in-depth theoretical analysis was carried out, and the additional improvements were conducted as the first PhD study to evaluate the applicability of the SCALDO technique in modern power supply requirements [14]. Another PhD was completed to investigate its potential applications in voltage regulator modules (VRM) used for high power processor power supplies [20]. The SCALDO research team in the University of Waikato collaborated with the University of Southampton to develop an integrated circuit (IC) version of a 12-5 V SCALDO circuit. This IC has been fabricated by AMS Fab in Austria and delivered to the University of Waikato for further testing. Subsequently, due to the many IEEE and IET publications [12, 15, 16, 21, 22] related to the SCALDO, this technique is now being researched in other countries, such as South Korea [23, 24].

The milestones of this SC-assisted technique are displayed in Figure 1-1.

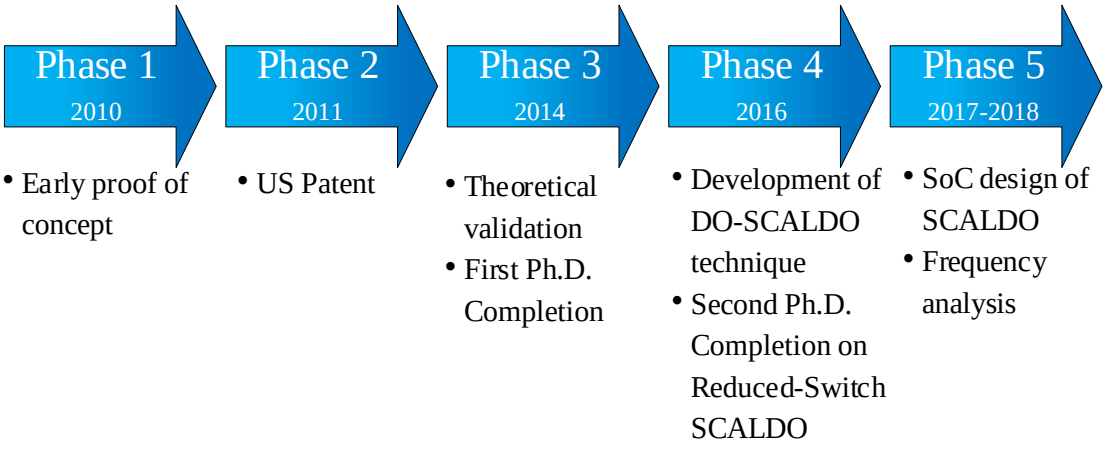
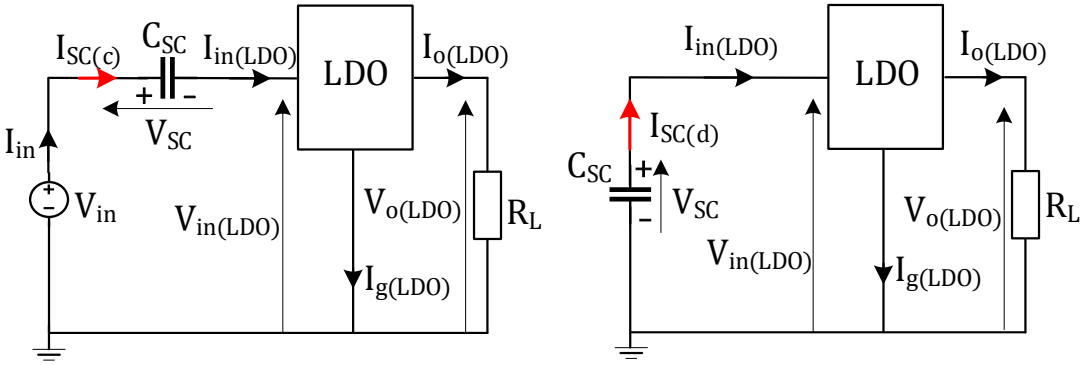


Figure 1-1: Development stages of the SCALDO technique.

The operating principle of this method is based on a supercapacitor (SC) or an array of SCs that acts as a lossless voltage dropper in the series path of a LDO regulator [14]. The simplest SCALDO configuration, based on a single supercapacitor is displayed in Figure 1-2 (a) and (b). This circuit has two operating modes: charging and discharging. Four low-speed switches are used to operate between these two modes (more details are provided in Chapter 2).



(a) (b)

Figure 1-2: The fundamental circuit configuration of the SCALDO technique: (a) SC charging phase (b) SC discharging phase.

The voltage difference (Δv) across the SC is very small due to its large capacitance (C_{sc}) when a finite current (i(t)) flows for a limited time (t) as shown in (1-1). Therefore, the DC current of the circuit is not blocked, and the regulation of the LDO regulator is maintained for a finite time. The switching of the SC between the charging and the discharging phases are done at a very low frequency while maintaining the charge balance.

$$\Delta v = \frac{1}{C_{sc}} \int_0^t i(t)dt \tag{1-1}$$

This approach can push the operating voltage of the LDO regulator close to its minimum input voltage (V_{min}) when the input-output voltage difference is high. Thus, the SCALDO technique enhances the overall ETEE of the circuit while keeping the superior specifications of a linear solution. For example, the ETEE can be increased from 41.7 % to 83.3 % in a 12 V-to- 5 V SCALDO regulator. Other topologies of this technique aim at improving the ETEE by a factor in the range of 1.33 to 3 [14]. It is important to emphasise that this method is not a variation of traditional SCCs and it does not produce RFI/EMI emissions due to its ultra-low operating frequency and inductor-less architecture [17]. This SC-assisted technique has been successfully matched for the requirements of different power supplies as well [12]. In addition, this technique has been modified to enable DC-UPS capability [25]. Some of the potential applications of the SCALDO approach are noise-sensitive circuits, RF circuits, portable devices, and medical instruments.

1.2 Research objectives

Starting from the topology establishment of the SCALDO regulator [19], there have been several studies carried out to further the development of this technique [12]. The theoretical background and the experimental validation of the generalised SCALDO concept are descriptively presented in [14], and it aims at exploring the requirement of number of SCs and switching matrices for a given input-output step-down voltage combination. Some of the major performance parameters, for example, line/load regulation, efficiency, and transient response are also experimentally validated with several prototypes and presented in the literature [13-15]. In addition, waveform analysis of different operating phases, design limitations, and power losses are discussed in [16, 26].

Even though the experimental measurements on several dynamic responses of the SCALDO regulators have been obtained under different conditions [14], a detailed analysis regarding the stability of this approach has not been conducted. This kind of analysis is essential to identify the design parameters and constraints regarding the stability of the overall circuit for reliable operation, especially when designing discrete SCALDO regulators or SoC designs. Consequently, this thesis provides an

important opportunity to advance the understanding of the small-signal model and the frequency compensation of this technique.

Moreover, the SCALDO regulators implemented formerly can produce only a single output voltage level [14]. The literature review related to this study has identified that the further development of this technique into a dual-output version can bring some competitive advantages over conventional inductor-less dual-output converters. These advantages are low output noise, fast dynamic response, voltage regulation and high output power. Therefore, this study aims at the design and implementation of a dual-polarity SCALDO regulator targeting noise sensitive applications where the conventional inductor-less topologies have limited usage.

1.3 Thesis outline

This thesis is organised as follows:

- Chapter 1 presents the general background of the SCALDO regulator and its evolution over the past years. The motivation factors behind the further development of this technique are also highlighted.
- Chapter 2 presents the literature review of this study. It gives a brief overview of the SCALDO concept and identifies the gaps in the implementations related to this technique. It explores the applicability of a dual-output version of this technique in inductor-less split-rail utilisations. In addition, the research scope and methodology are established.
- Chapter 3 discusses the stability analysis of the SCALDO technique. The small-signal model, the voltage control loop and the frequency compensation of this method are also presented with step-by-step derivations.
- Chapter 4 is constructed based on the experimental validation of the stability of the basic SCALDO configuration. A simulated framework is also developed and compared with experimental results.
- Chapter 5 establishes the DO-SCALDO concept. It describes the theoretical aspects of a dual-output and split-rail version of the SCALDO technique.
- Chapter 6 validates the dual-output SCALDO model with the experimental results of a 12 V to ±5V prototype design. The steady-state and transient responses of this DO-SCALDO prototype are analysed, and some of the major

design features are compared with commercial split-rail and dual-output converters.

- Chapter 7 provides the conclusions, the contributions of this study to the scientific knowledge, and the recommendations for further work.

1.4 Publications

1. **Kasun Subasinghage**, Kosala Gunawardane, Nihal Kularatna, and Tek Lie "Selection of the Stable Range of the Equivalent Series Resistance (ESR) of the Output Capacitor for a SCALDO Regulator," 2018 27th International Symposium on Industrial Electronics (ISIE).
2. **Kasun Subasinghage**, Kosala Gunawardane, and Nihal Kularatna, "DO-SCALDO Design Approach versus Other Split-Rail, Inductor-less DC-DC Converter Techniques," 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES).
3. **Kasun Subasinghage**, Kosala Gunawardane, and Nihal Kularatna, "Pole-Zero Analysis of Supercapacitor-Assisted Low-Dropout (SCALDO) Regulator," 2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES).
4. **Kasun Subasinghage**, Kosala Gunawardane, T. T. Lie, and Nihal Kularatna, "Single-input, dual polarity, dual output DC-DC converter implementation based on the SCALDO technique," 2017 IEEE International Conference on Industrial Technology (ICIT).
5. **Kasun Subasinghage,** Kosala Gunawardane**,** Tek Lie**,** and Nihal Kularatna**, "**Design of an efficiency improved dual-output DC-DC converter utilizing a supercapacitor circulation technique**,"** 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)**.**
6. **Kasun Subasinghage**, Kosala Gunawardane, Tek Lie, and Nihal Kularatna, "Design concepts and preliminary implementations of dual output supercapacitor-assisted low-dropout regulators (DO-SCALDO)," 2016 Australasian Universities Power Engineering Conference (AUPEC).
7. Kosala Gunawardane, **Kasun Subasinghage**, and Nihal Kularatna, "Efficiency Enhanced Linear DC-DC converter topology with integrated DC-UPS capability," 2018 IEEE International Conference on Industrial Technology (ICIT).

Chapter 2 Literature Review and Research Design

In reviewing the literature related to the proposed project, the conceptual framework, the theoretical foundation and the experimental work of the SCALDO technique are thoroughly studied to check the possible direction of further research. In addition, the literature is explored in the direction of dual-output DC-DC converters to identify the advantages of developing a dual-output version of the SCALDO regulator for inductor-less split-rail applications. Based on the gaps found in the literature review, two research questions are identified. These questions are addressed by establishing the quantitative research methodology.

2.1 Introduction

The literature review of the SCALDO concept has been done based on the previously published work (2011-to-2018) including the journal articles, conference papers, and PhD theses. This preliminary work aims to identify gaps in the SCALDO research field and add the further development of this technique. Although the details are readily available in the publications [12-19, 21, 22, 26, 27], the basics of this method are covered in this chapter to help the reader to understand the content of this thesis.

Furthermore, this literature review primarily brings the attention of the reader to two key advancement areas of the SCALDO method. First, the frequency domain analysis of the SCALDO approach is considered regarding the previous work and gaps are identified. Next, the possibility of the development of this technique into a dual-output version is investigated. Since the SCALDO technique is based on an inductor-less architecture, the literature is reviewed in the direction of conventional inductor-less and dual-output topologies. The limitations of these conventional architectures are highlighted, and the advantage of the design of a dual-output SCALDO regulator are also discussed.

2.2 Operating principle of the basic SCALDO regulator

The SCALDO regulator is a technique that is designed to achieve high ETEE for DC-DC converters based on linear regulators. In this approach, a low-frequency SC

circulation stage is combined with a LDO regulator. The concept and the experimental validation of this method are presented in [13-16]. This section discusses the fundamental operating principle of this SC-assisted technique.

The basic SCALDO regulator is composed of a single SC, a LDO regulator and four switches (S_1-to-S_4) as shown in Figure 2-1.

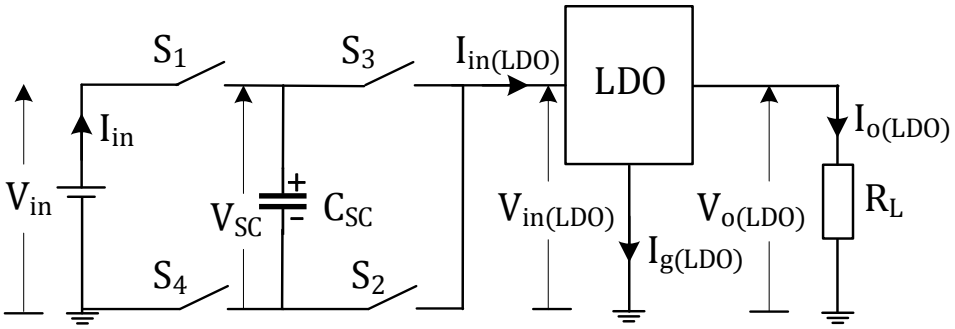


Figure 2-1: The configuration of the fundamental SCALDO regulator.

The input source voltage, the voltage across the SC, the input and output voltages of the LDO regulator, respectively, are V_{in}, V_{SC}, $V_{in(LDO)}$ and $V_{o(LDO)}$. Similarly, the current of the power source, the SC current, the input current, the ground pin current and the output current of the LDO regulator are represented as I_{in}, I_{SC}, $I_{in(LDO)}$, $I_{g(LDO)}$, $I_{o(LDO)}$, respectively. In addition, the capacitance of the SC is given by C_{sc}. The resistance of the output load (R_L) is considered as a constant load for simplicity of analysis.

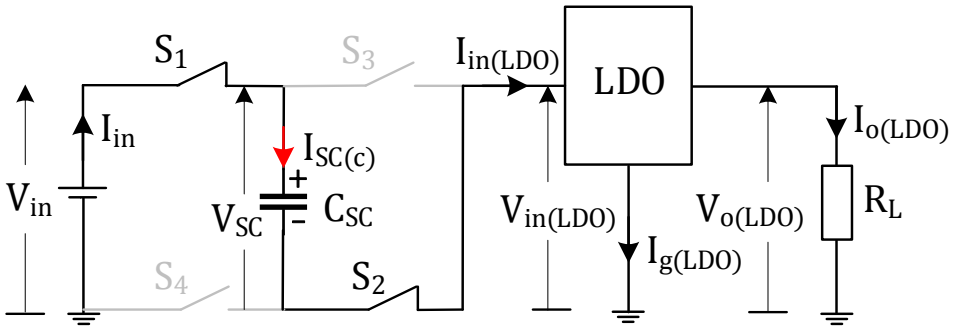


Figure 2-2: The charging phase of the fundamental SCALDO regulator.

The operating phases of this method depend on the state of the SC in the circuit, and they are defined as the charging mode and the discharging mode. The charging phase is initiated when S_1 and S_2 are closed, and S_3 and S_4 are opened. During this stage, the input voltage source, the SC, and the LDO regulator are connected in series as displayed in Figure 2-2.

Because of the large capacitance and small ESR of the SC, the DC current of the circuit can be passed through the SC for a finite time without terminating the regulation of the LDO regulator. Hence, the SC acts as a lossless voltage dropper in the series path of the LDO regulator. If the ground pin current of the LDO regulator is neglected, the source current, the charging current of the SC ($I_{SC(c)}$) and the output current of the LDO regulator are approximately the same during this period. As the SC charges, $V_{in(LDO)}$ tends to fall. The SC is kept in this position until $V_{in(LDO)}$ falls to its minimum working voltage (V_{min}). If the resistance of the switches and the ESR of the SC are negligible, the voltage across the SC at the end of the charging cycle is approximately V_{in} - V_{min}.

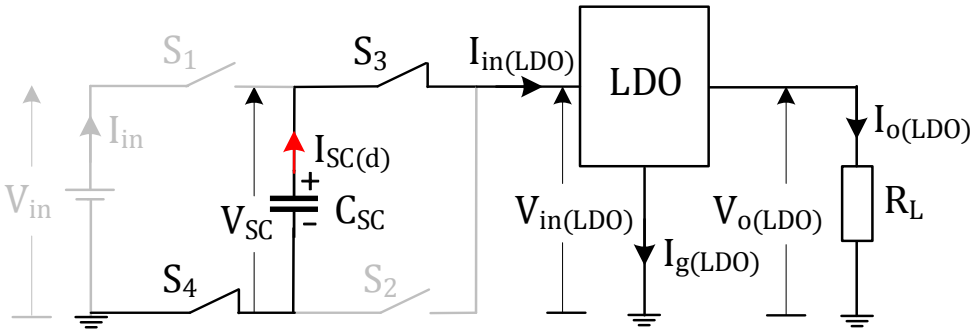


Figure 2-3: The discharging phase of the fundamental SCALDO regulator.

After the charging process is terminated, S_1 and S_2 are turned off, and S_3 and S_4 are turned on to initiate the discharging phase as depicted in Figure 2-3. The discharging current of the SC is denoted as $I_{SC(d)}$ in this diagram. The power source is completely disconnected in this mode. Also, the LDO regulator and the SC are connected in parallel. The initial voltage of the SC at the beginning of the discharging cycle is approximately V_{in} - V_{min}. This voltage should be greater than V_{min} to maintain the continuous operation of the LDO regulator. This criterion is identified as the $V_{in} > 2V_{min}$ requirement in the basic SCALDO regulator. If this condition is met, the regulation of the LDO regulator can be kept for a finite time until $V_{in(LDO)}$ falls back to V_{min}. These charging and discharging steps are conducted in a periodic manner while maintaining the charge balance of the SC. Interestingly, the operating frequency of a typical SCALDO circuit is about several hundred millihertz.

Moreover, in practical SCALDO circuit implementations, a capacitor is connected at the input of the LDO regulator (which is not shown in the basic circuit design) as an energy buffer. This buffer capacitor ensures the continuous operation of the regulator during the switching transients. It is sized based on the maximum value of

the load current and the turn-on and turn-off delays of the switches. In addition, its value is kept very small compared to the capacitance of the SC to minimise the losses due to the voltage mismatches at the beginning of every switching cycle. More details about this buffer capacitor are discussed in [14].

Furthermore, the LDO regulator is driven from the input power source only during the charging mode of the SC. If the sum of the ground pin current of the LDO regulator and the control circuit current of the SCALDO regulator is small, the input source current and the load current become equal. Therefore, the average input source current ($I_{in(avg)}$) for a complete switching period becomes half the load current ($I_{o(LDO)}/2$) at steady state. When these factors are considered, the approximate ETEE (η_{SCALDO}) of the basic SCALDO topology can be defined as (2-1).

$$\eta_{SCALDO} = \frac{V_{o(LDO)} I_{o(LDO)}}{V_{in} I_{in(avg)}} = \frac{V_{o(LDO)} I_{o(LDO)}}{V_{in} (I_{o(LDO)} / 2)} = 2 \frac{V_{o(LDO)}}{V_{in}} \qquad (2\text{-}1)$$

Conversely, when the LDO regulator is operated directly from the input voltage source for the same input-output voltage combination, the ETEE turns to $V_{o(LDO)}/V_{in}$. Hence, it is evident that the application of the SCALDO technique has improved the ETEE of this linear regulator circuit by a factor of two.

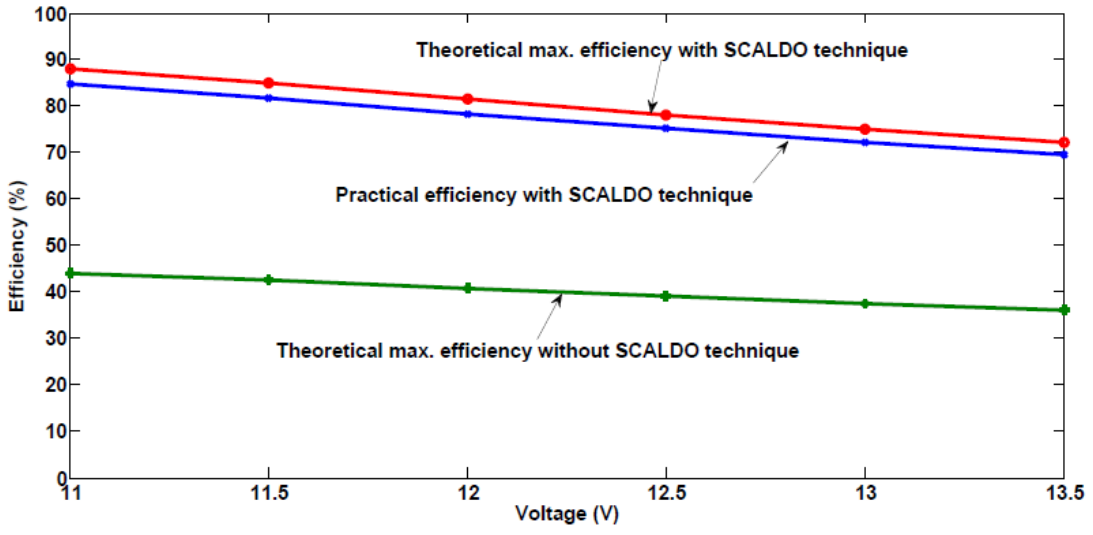


Figure 2-4: The end-to-end efficiency advantage of a 12 V to 5 V SCALDO regulator [14].

The experimental results related to the SCALDO concept are presented in [13-16]. For example, the ETEE advantage achieved from a 12 V to 5 V SCALDO regulator has a pattern as shown in Figure 2-4 [14]. The upper trace depicts the theoretical

efficiency of the SCALDO regulator against the input voltage while the middle trace shows the practical performance of this implementation. According to Figure 2-4, the SCALDO regulator can achieve a theoretical maximum ETEE around 83.3 % at the rated input voltage. The measured ETEE is approximately about 80 % at the same input voltage. On the other hand, if the 5 V linear regulator is run without using the SCALDO method, the theoretical maximum efficiency drops to 41.7 % at 12 V as shown in the bottom trace of this diagram.

2.3 Generalised SCALDO topology establishment and further advancement

The SCALDO concept has been further developed to match various power supply requirements [14-16] based on the source voltage and the minimum input voltage of the applied LDO regulator. The previous research has established two generalised SCALDO topologies: the Series to Parallel SC Array configuration and the Parallel to Series SC Array configuration [14, 15].

The Series to Parallel SC Array topology is applied when the $V_{in} > 2V_{min}$ criterion is satisfied. It should be noted here that the basic SCALDO topology discussed in Section 2.2 is a variation of the Series to Parallel SC Array method where a single SC is utilised. Nevertheless, the generalised concept has been developed to apply an array of identical SCs. The maximum number of SCs (n_{max}) used in the converter is determined based on the requirement defined in (2-2).

$$n_{\max} \leq \frac{V_{in} - V_{\min}}{V_{\min}} \tag{2-2}$$

The two operating modes of this configuration are displayed in Figure 2-5. The charging current, the discharging current and the voltage across the SC array are denoted as $I_{SCA(c)}$, $I_{SCA(d)}$, and V_{SCA}, respectively. The SCs are connected in series in the charging cycle (as shown in Figure 2-5 (a)) and kept in the same position until the input voltage of the LDO regulator reaches to V_{min}. These charged SCs are then connected in parallel in the discharging phase to release their stored energy back to the LDO regulator as illustrated in Figure 2-5 (b). This discharging cycle is terminated when $V_{in(LDO)}$ drops back to V_{min}.

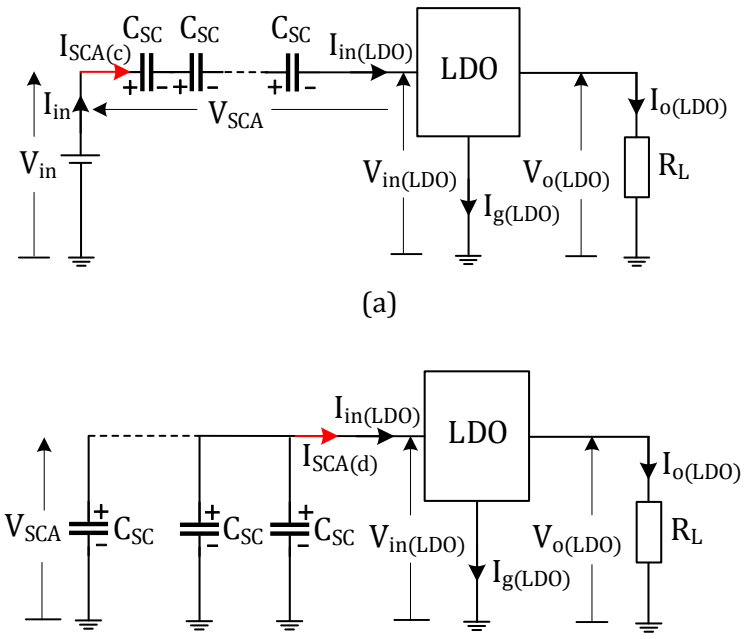


Figure 2-5: Series to Parallel SC Array SCALDO configuration: (a) SC charging phase, (b) SC discharging phase.

The theoretical maximum ETEE efficiency of the Series to Parallel Array configuration (η_{SPA}) is defined in (2-3).

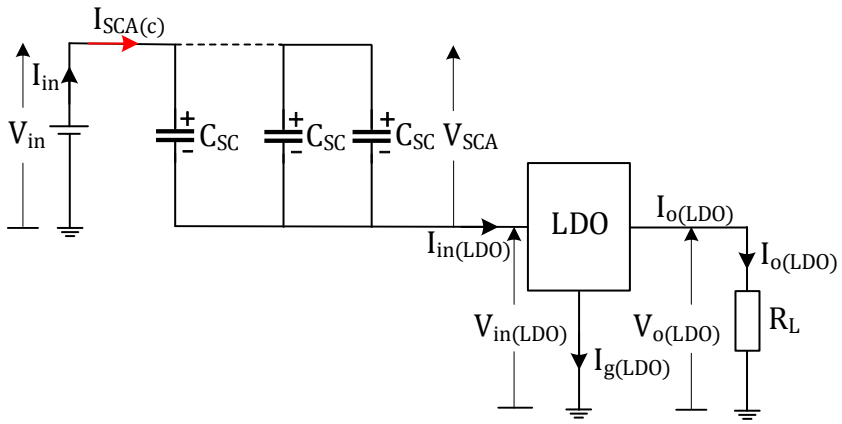
$$\eta_{SPA} = (n_{\max} + 1)\frac{V_{o(LDO)}}{V_{in}} \tag{2-3}$$

On the other hand, the Parallel to Series SC Array configuration is used when the $V_{in} < 2V_{min}$ condition is met. The circuit arrangements of the charging and discharging modes of this topology are displayed in Figure 2-6. This configuration needs a minimum number of SCs (n_{min}) as defined in (2-4) for its operation.

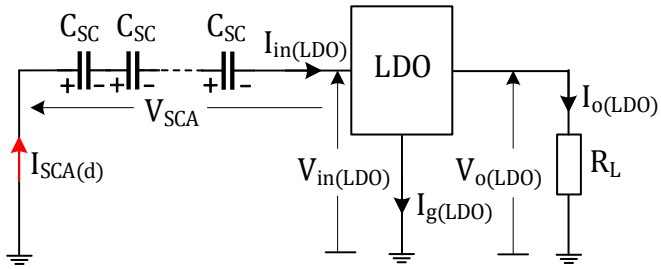
$$n_{\min} \geq \frac{V_{\min}}{V_{in} - V_{\min}} \tag{2-4}$$

At the beginning of the operation, the SCs are connected in parallel and placed in series with the LDO regulator as displayed in Figure 2-6 (a). This charging process is terminated when $V_{in(LDO)}$ falls to V_{min}. Conversely, all the SCs are connected in series in the discharging mode as depicted in Figure 2-6 (b). The power supply is completely disconnected in this cycle, and the LDO regulator is run by the stored energy of the series SC array. These SCs can deliver their energy until $V_{in(LDO)}$ reduces to V_{min}. The approximated ETEE of this configuration (η_{PSA}) is given in (2-5).

$$\eta_{PSA} = \left(1 + \frac{1}{n_{\min}}\right)\frac{V_{o(LDO)}}{V_{in}} \tag{2-5}$$



(a)



(b)

Figure 2-6: Parallel to Series SC Array SCALDO configuration: (a) SC charging phase, (b) SC discharging phase.

Table 2-1: End-to-end efficiency improvement factors of three different SCALDO topologies.

End-to-end regulation requirement	LDO minimum input voltage (V)	Capacitor Requirements				Approximate efficiency at different operating stages (%)		
		Number of Supercapacitors	*Voltage (V)*					
			Maximum	*Medium*	*Minimum (discharge)*	*Maximum Voltage*	*Medium Voltage*	*Minimum voltage (discharge)*
5 V - 3.3 V	3.5	3	1.5	1.4	1.2	73	92	92
5 V - 1.5 V	1.6	2	1.7	3.2	1.6	88	83	93
12 V – 5 V	5.3	1	6.5	6.0	5.3	77	83	93

Experimental results of three different SCALDO topologies are summarised in Table 2-1 [14]. These results include the input-output voltage combination of the particular topology, the number of SCs utilised, the minimum voltage requirement and the ETEE.

After successful implementation of various prototypes, the reduced-switch SCALDO (RS-SCALDO) regulator has been introduced [20, 22]. The topological advantage of this method is the reduction in the switch count which allows the SCALDO regulator to handle high output current. Thus, this reduced-switch method targets high-current applications such as VRMs.

The DC-UPS feature has been integrated into the SCALDO regulator by selecting an oversized SC and without using any additional hardware. Because of the extra-large capacitance offered by this SC, it can be used as an energy buffer to safeguard against short-term line interruptions in a DC power supply. This novel feature expands the SCALDO technique into versatile applications. The preliminary work related to this DC-UPS SCALDO project is published in [25].

2.4 Topological differences of the SCALDO technique and switched-capacitor converters

Switched-capacitor converters have a limited output current capability, and they are mostly applied in inverting or boost applications such as memory circuits, continuous time filters, and RS-232 transceivers [28, 29]. The basic operation of these converters is based on the charge share between a flying capacitor and a reservoir capacitor [7, 30]. In one part of the operating phase, the flying capacitor is charged in parallel with the input source [28]. In the next step, the accumulated energy of the flying capacitor is delivered back to the reservoir capacitor.

Compared to the charge pump converters, the SCALDO regulator has entirely different characteristics as summarised in Table 2-2[17].

Table 2-2: Topological differences of the charge pump converters and the SCALDO regulator

Switched-capacitor converter	SCALDO regulator
A flying capacitor and a reservoir capacitor are used for the voltage conversion.	Enormously large capacitance (e.g., a SC) is used, and this capacitor acts as a lossless voltage dropper in the series path of a LDO regulator.
Switching frequency is fixed and determined by the internal oscillator frequency (typically in the kilohertz range).	Variable frequency which depends on the load current (typically in the millihertz range).
Load regulation and line regulation are not precise, and additional regulators such as linear type may be required for more precision output voltage.	Precise load/line regulation since the load experiences a high-quality output of a linear regulator.
The maximum output current is typically a few hundreds of milliamperes.	Technique can be applied to design regulators with high output current based on the requirement.
Dynamic losses in the switches are significantly large.	Dynamic losses are negligible due to the very low operating frequency.

2.5 Losses in a SCALDO regulator

The implementation losses of a SCALDO regulator are listed below [15, 26].

1. Losses in the Supercapacitors

   The main loss contributor is the DC ESR of a SC applied in a SCALDO regulator. When the charging or the discharging current passes through a SC, heat is dissipated due to the voltage drop across the ESR. Similarly, the leakage current of a SC can also be treated as a loss. Since this leakage current is typically within the range of 5 μA to about 50 μA, its loss contribution is very small compared to the loss due to the ESR.
2. Losses due to the switches

The switches cause static and dynamic losses. The static losses are mainly due to the ohmic resistance and can be reduced by selecting switches with minimum resistance. On the other hand, the dynamic losses are minimal in a SCALDO regulator due to its low-frequency operation compared to switch-mode power supply techniques and charge pump converters [14, 15].

3. Losses due to the paralleling of capacitors with different voltages
   The buffer capacitor used as an energy buffer (as discussed in Section 2.2) is in parallel with the SC in the discharging phase of the SCALDO operation. These two capacitors have different voltages when they are connected. This voltage mismatch causes an inrush current to flow through these capacitors, and the energy is dissipated within the ESR components. This loss can be minimised by selecting the lowest possible capacitance for the buffer capacitor considering the maximum output current rating of the LDO regulator and the transition delays of the switches. Interestingly, this buffer capacitor is very small compared to the SC in practical implementations, and the losses associated with the voltage mismatch are minimal. Also, the control circuit algorithm can be changed to minimise the voltage difference between the capacitors when switching.

2.6 Research Gaps

P-channel MOSFET (PMOS) based commercial LDO regulators are mostly utilised in SCALDO designs [14] due to the advantages, such as compactness, low quiescent current, and very low dropout voltage compared to other types of linear regulators [31]. These PMOS LDO regulators are typically frequency compensated using the ESR of the output capacitor. When the SC circulation network is connected in front of this LDO regulator, the stability of the overall design might be affected. Research to date has not yet determined the effect of this switching network on the stability of the overall SCALDO circuit. Therefore, one part of this study aims at stability analysis of the SCALDO regulator.

Up to now, scant attention has been paid to the further development of the SCALDO technique for the requirements of dual-output and split-rail DC-DC converters. Because of the inductor-less architecture of this technique, a dual-output version would be useful for low noise and low EMI/RFI applications, for example, portable devices, medical instruments, and industrial equipment. Similarly, a dual-output

SCALDO regulator can provide other useful features of a linear solution such as fast dynamic response and high ripple rejection. Therefore, the advantages of the development of a dual-output and split-rail DC-DC converter of the SCALDO regulator are identified. The following section is constructed based on two conventional inductor-less split-rail design approaches. Finally, it establishes the limitations of these conventional split-rail approaches and explains how a dual-output SCALDO version might eliminate these issues.

2.7 Prior art of conventional inductor-less split-rail topologies

Modern electronic systems such as portable devices, wireless applications, industrial equipment, and auto accessories often use multiple voltage rails to power their internal circuits [32]. The use of dual power supplies is one solution for some applications, such as LCDs (Liquid Crystal Displays), ADCs (Analog-to-Digital Converters), DACs (Digital-to-Analog Converters), localised microprocessors, and operational amplifiers. These dual outputs are generated using a single voltage source in most cases. Up to now, there have been many methods that can produce dual outputs, including the switching converters [33-39]. Nonetheless, the switch-mode topologies produce considerable EMI/RFI due to their bulky inductors and the high-frequency operation. Therefore, they have limited usage in applications where the EMC is a major concern.

Alternatively, inductor-less split-rail power supplies are preferred over switch-mode dual DC-DC converters for noise sensitive and low EMI/RFI applications. A split-rail DC-DC converter divides the input voltage into equal halves with reference to a new zero-volt reference point. This reference is known as the virtual ground (GND_V), and it is different from the common ground of the circuit. The output voltages can be treated as positive and negative with respect to this GND_V [40].

Split-rail power supplies are widely used in applications where symmetrical outputs are required for downstream components such as op-amps, active filters and other components without a need for common mode range ground. Some application notes and data sheets of the commercial virtual ground IC suppliers highlight the above applications in their reference designs [41, 42].

Moreover, split-rail DC-DC converters can vary from straightforward designs to complex methods. The buffer circuits and the charge pump converters are the two

conventional approaches, which are widely used in modern power electronic systems with low power output [30, 33, 43, 44]. These two methods have merits and demerits based on their design architecture. Since the SCALDO concept is also based on an inductor-less architecture, a dual-output version of the SCALDO might be a better solution compared to the conventional split-rail approaches.

2.7.1 Buffer circuits

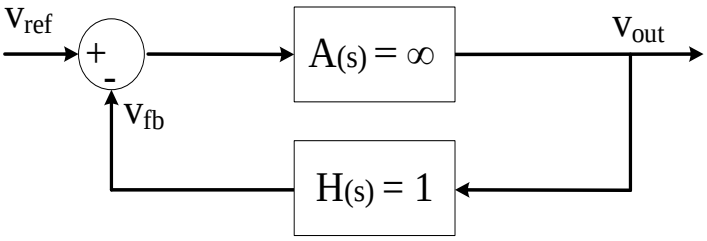


Figure 2-7: The voltage control loop of a buffer circuit.

Buffer circuits are designed based on the feedback control displayed in Figure 2-7. The terms v_{ref}, v_{fb}, and v_{out} stand for the small-signal quantities of the reference voltage, the feedback voltage, and the output voltage, respectively. The negative feedback gain (H(s)) is adjusted to unity in this control loop. Since the open-loop gain (A(s)) of this error amplifier is very high (ideally infinity), the output voltage is equal to the reference voltage. An example circuit of a unity-gain buffer is shown in Figure 2-8.

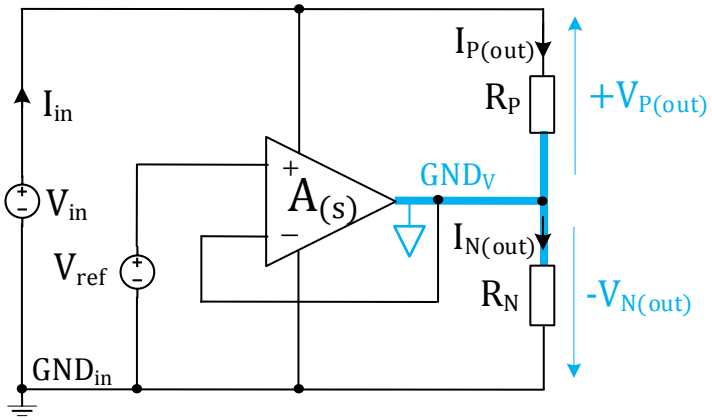


Figure 2-8: A basic schematic of a unity-gain buffer circuit.

The error amplifier of this circuit is typically an op-amp (operational amplifier). The reference voltage source can be simply a resistor divider or a bandgap voltage reference. The inverting input of the op-amp is directly connected to the output for unity gain feedback. This configuration makes the error amplifier to adjust the output voltage always to the reference voltage. When the reference voltage is set to

half of the input voltage, the outputs become bipolar voltages with respect to the GND_V. The positive rail has a potential of $+V_{P(out)}$; the negative rail is at a potential of $-V_{N(out)}$. If the power consumption of the op-amp is ignored, the input source current directly passes through the outputs when the loads are equal ($R_P = R_N$). Conversely, if the loads are unbalanced, excess current is created, and this current is controlled by the op-amp to maintain the output voltage at the desired level. As an example, if $R_P > R_N$, the differential current ($I_{N(out)} - I_{P(out)}$) is sourced from the op-amp into the GND_V.

A similar approach is used in commercial off-the-shelf virtual ground ICs, such as TLE2425 and TLE2426. They are commonly applied in low-noise applications. The output currents of these ICs are typically about a few tens of milliamperes. On the other hand, the BUF 634 IC can handle relatively a high output current compared to TLE2425 and TLE2426. An example of a ±12 V split-rail converter designed with BUF 634 IC is displayed in Figure 2-9 [42]. The reference voltage (12 V) of this converter is generated using a resistor divider at the input side. The two output capacitors (C_1 and C_2) are sized based on the manufacturer's specifications [42]. The maximum differential output current and the output power of this circuit are 250 mA and 3 W, respectively.

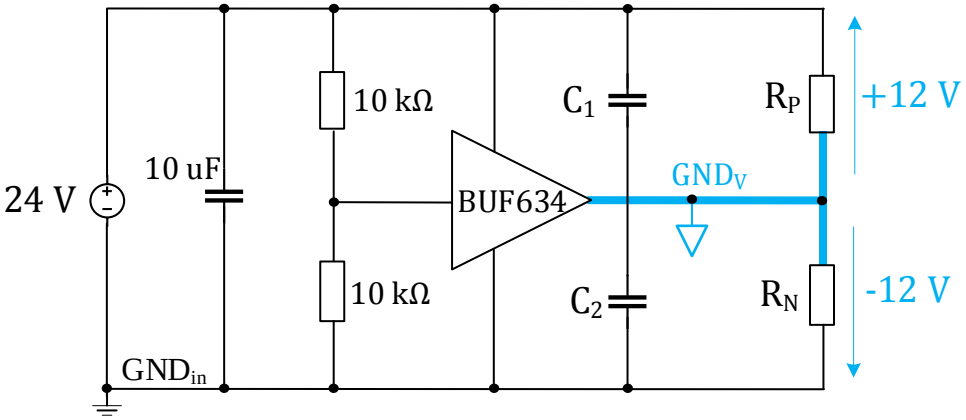


Figure 2-9: A ±12 V split-rail converter with BUF 634 IC.

One drawback of the op-amp based split-rail converter is the power consumption during standby mode as highlighted in [33]. For example, the maximum quiescent current of BUF 634 is 20 mA at no load and wide bandwidth mode. In addition, the output impedance of the op-amp limits the maximum differential current. Consequently, the maximum differential output power is mainly determined by the

output current capability of the op-amp. Besides, these split-rail converters bring stability issues when the output loads are heavily capacitive [45].

2.7.2 Switched-capacitor split-rail circuit

The basic circuit diagram of a switched-capacitor split-rail converter is illustrated in Figure 2-10. The operating principle of this circuit is based on the charge sharing between the flying capacitor (C_{FL}) and the output capacitors (C_1 and C_2).

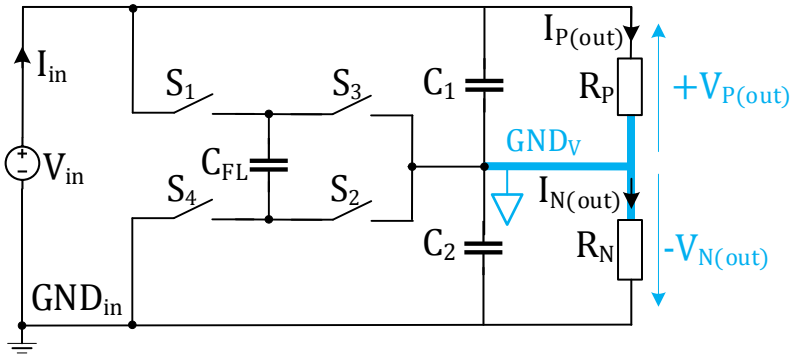


Figure 2-10: The basic configuration of a switched-capacitor split-rail circuit.

In one part of the operating phase, C_{FL} and C_1 are connected in parallel by closing the switches S_1 and S_2, and opening S_3 and S_4. In the next phase, S_3 and S_4 are closed, and S_1 and S_2 are opened to allow C_{FL} and C_2 to connect in parallel.

The switching frequency of the flying capacitor of a commercial split-rail charge pump converter typically falls in the kilohertz range. This switching ripple is directly passed to the output side of the converter. A low-pass filter may be required to filter out this noise. Even though the generated outputs are positive/negative with respect to the GND_V, they drift dramatically during an unbalanced loading situation. Also, the outputs can be affected by the tolerances of the capacitors.

Interestingly, the output impedance of a switched-capacitor split-rail converter is usually low, and it is mainly governed by the resistance of the switches, the ESR of the capacitors and the switching frequency. Therefore, these converters can drive output currents up to several hundreds of milliamperes. For instance, MAX1681 commercial charge pump IC can deliver an output current of 250 mA [46]. Similarly, MAX829 and MAX1681 are two other examples that are used in split-rail applications such as LCD panels and portable devices.

The circuit in Figure 2-11 shows a generic application of MAX829 IC that splits the input source voltage into equal halves. The flying capacitor is C_{FL}, and the output capacitors are C_1-to-C_4. The value of the input capacitor (C_{in}) is normally specified in the datasheet of the IC. This converter uses a switching frequency of 35 kHz. The output current of this circuit is limited up to 25 mA.

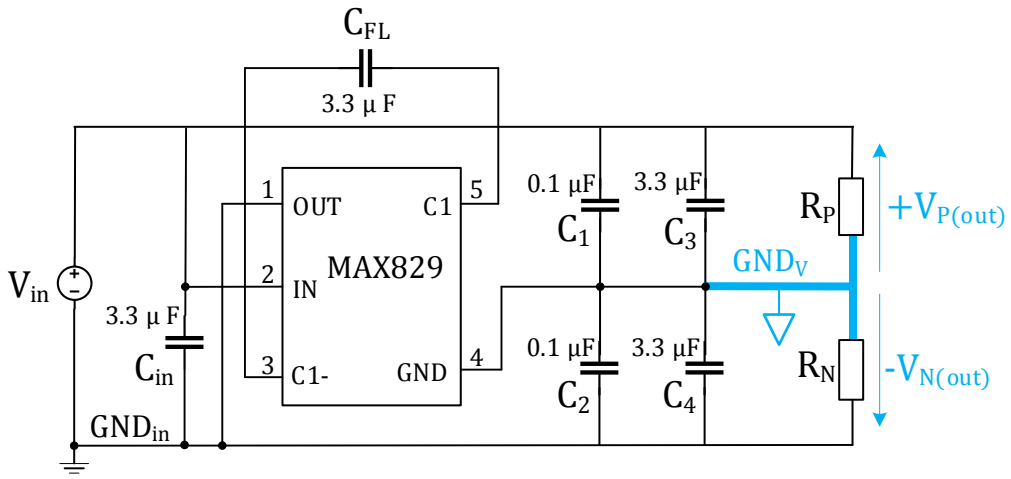


Figure 2-11: Use of MAX829 as a charge pump split-rail converter.

2.7.3 Limitations of conventional split-rail design topologies

The basic features of these two techniques are summarised in Table 2-3. According to Table 2-3, buffer circuits offer compactness and simplicity. Nevertheless, the output voltages are unregulated, and the output current level is low due to the significant output impedance of the error amplifier. On the other hand, SCCs require more components to split the input voltage. In addition, they do not provide voltage regulation and produce considerable noise in the output voltages. The output power levels of both techniques are low.

Table 2-3: Comparison of two inductor-less split-rail techniques

Feature	Switched-capacitor converters	Buffer circuits
Voltage regulation	Unregulated	Unregulated
Output current	Low	Lowest
Differential output power	Low	Low
Complexity	High	Low
Components	Moderate	Fewest
Output noise	High	Low

Due to the low differential output current levels of these two conventional approaches, they are limited to low output power (<2 W) utilisation. Similarly, some applications require other important features such as voltage regulation, low noise and fast dynamic response which cannot be provided by the conventional split-rail approaches. Thus, there is a potential advantage of designing an inductor-less split-rail converter with increased output power, low output noise, and fast dynamic response compared to the conventional topologies. These factors are the motivations behind this study to develop a split-rail SCALDO regulator for virtual ground circuits.

2.8 Research design

2.8.1 Research questions

Based on the literature review, two research questions have been identified, and there are as follows:

1. Is the overall SCALDO design stable when the SC circulation network is applied in front of the LDO regulator?
2. How can the SCALDO method be modified to generate dual outputs for split-rail applications to overcome the limitations of existing topologies?

2.8.2 Research scope

1. This study is based on the fundamental SCALDO configuration that is composed of a single SC and four switches.
2. The supercapacitor is modelled using the first-order (RC) model
3. The P-channel MOSFET of the LDO regulator is modelled using the Shichman and Hodges equations, and the fixed junction capacitances.

2.8.3 Research methodology

The research methodology of this study is quantitative, and it is built on theory, experimentation, and observation.

The first research question falls into the frequency domain analysis. This frequency analysis is performed utilising a discrete 12 V to 5 V SCALDO regulator that consists of a discrete LDO regulator and a SC switching circuitry. First, the SCALDO regulator is designed using essential elements. Secondly, it is modelled applying the circuit theory. Next, the model is simulated in the MATLAB Simulink environment using the

Linear Analysis Toolbox. The experimental results related to the loop gain measurement are obtained with the aid of the signal injection method. The dynamic behaviour of the SCALDO regulator is tested utilising a DC electronic load. Afterwards, these experimental results are used to validate the proposed theoretical model.

The second research question is related to the further development of the SCALDO technique for the requirement of inductor-less split-rail applications. This question is addressed by developing an analytical model that can produce dual outputs using the SCALDO technique. A 12 V to ±5 V proof of concept split-rail converter is designed and tested to validate the theoretical model. The steady-state and transient responses are obtained using an isolated channel oscilloscope and a DC electronic load. Finally, the experimental results of this prototype are compared with the features of conventional dual-output DC-DC converters.

All the PCBs of the prototypes are designed using the Altium Designer software. Atmel microcontrollers are utilised in the control circuits of these prototypes. The microcontroller firmware is developed in the Atmel Studio software. An ISP programmer is used for programming and debugging purposes.

Chapter 3 Stability Analysis of the SCALDO Regulator

Abstract- This chapter discusses the theoretical background of the stability criterion of the SCALDO topology. The small-signal model of a discrete SCALDO regulator is developed based on a PMOS LDO regulator. The open-loop transfer function is derived, and the poles and zeros are extracted. The possible frequency compensation methods have been identified to stabilise the voltage control loop of the SCALDO design.

3.1 Introduction

The SCALDO technique is designed based on a low-frequency SC circulation network and a LDO regulator as discussed in Chapter 2. Despite the fact that a frequency compensated LDO regulator is used, the SC circulation network may affect the overall stability. The locations of the poles and zeros of the open-loop transfer function may be changed due to the external parameters introduced by this switching network. Therefore, the overall circuit is analysed for stability, and appropriate frequency compensation techniques are investigated in this study.

The stability analysis of the basic SCALDO topology is developed based on a discrete PMOS LDO regulator. The use of a discrete design is helpful when determining the frequencies of poles and zeros using the known circuit parameters. Also, the outcome of this stability analysis can be used for SoC design of the SCALDO regulator as the next stage of the SCALDO research. The preliminary work related to this stability analysis has been presented in [47, 48]. Compared to these two publications, an in-depth analysis is conducted in this chapter in the following areas.

- Modelling of the pass device including the dominant parasitic capacitances
- Modelling of the error amplifier
- Derivation of the open-loop transfer function and its poles and zeros
- Identification of the appropriate frequency compensation techniques

3.2 The basic circuit diagram of the discrete SCALDO regulator

The circuit diagram of the discrete SCALDO regulator is shown in Figure 3-1. This discrete SCALDO is composed of two main sections: the low-frequency SC switching circuit and the discrete LDO regulator. The major components of the LDO regulator

are the series-pass device, the error amplifier, the voltage reference (V_{ref}), the feedback network (R_1 and R_2), the output capacitor (C_o), the bypass capacitor (C_b), and the load. This output load is modelled as a constant current load (I_L) for the simplicity of analysis. The ESR of the output capacitor is denoted as R_{ESR}. The ESR of the bypass capacitor is typically kept small for decoupling purposes and can be neglected in this design.

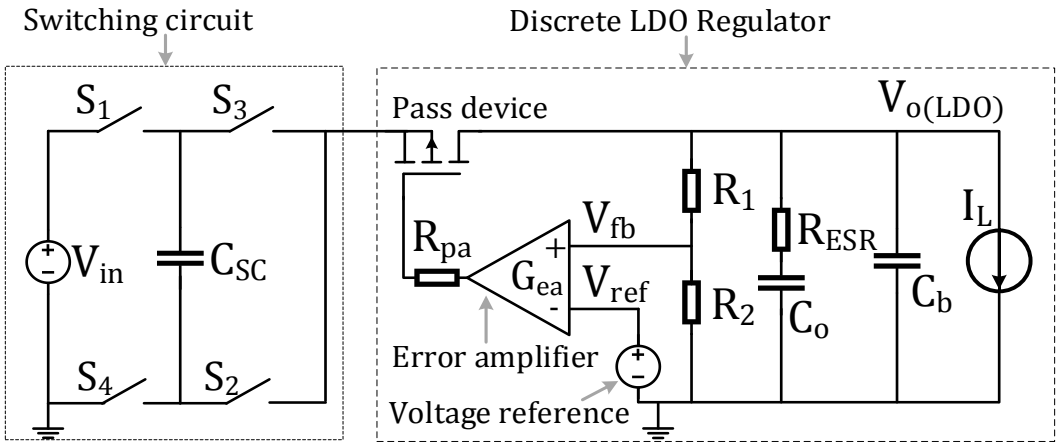


Figure 3-1: The basic circuit diagram of the discrete SCALDO regulator.

The non-inverting input of the error amplifier is connected to the feedback network. The voltage and the gain of the feedback network are denoted as V_{fb} and G_{fb}, respectively. This feedback gain is defined in (3-1).

$$G_{fb} = R_2/(R_1 + R_2) \tag{3-1}$$

The reference voltage source is connected to the inverting input of the error amplifier. The gain of the error amplifier is defined as G_{ea}. This amplifier compares V_{ref} and V_{fb} and controls the gate voltage of the pass device to maintain a fixed output voltage ($V_{o(LDO)}$) at the load. The sum of the output resistance of the error amplifier and the gate terminal of the series-pass device is represented as R_{pa}.

3.3 Small-signal analysis of the basic SCALDO regulator

3.3.1 Modelling of the pass device

Among the possible pass device configurations, the PMOS transistor is used as the series-pass element of the LDO regulator in most of the SCALDO designs due to some advantages such as very low dropout voltage, low quiescent current, and high-speed operation. Therefore, PMOS LDO regulator based SCALDO circuit is chosen for this study.

The typical small-signal model of a PMOS transistor is displayed in Figure 3-2 [49]. The symbols, D, G, and S in this diagram represent the drain, the gate and the source of the pass device, respectively. The parasitic capacitances of the PMOS are the gate-source (C_{GS}) capacitance, the gate-drain (C_{GD}) capacitance, and the drain-source capacitance (C_{DS}). In addition, the gate resistance, the source resistance, and the drain resistance are, respectively, denoted as r_G, r_S, and r_D. The output resistance of this pass device for small signals is shown as r_{ds}. Similarly, the voltage-dependent current source of the PMOS is the product of the transconductance (g_m) and the gate-source small-signal voltage (v_{gs}).

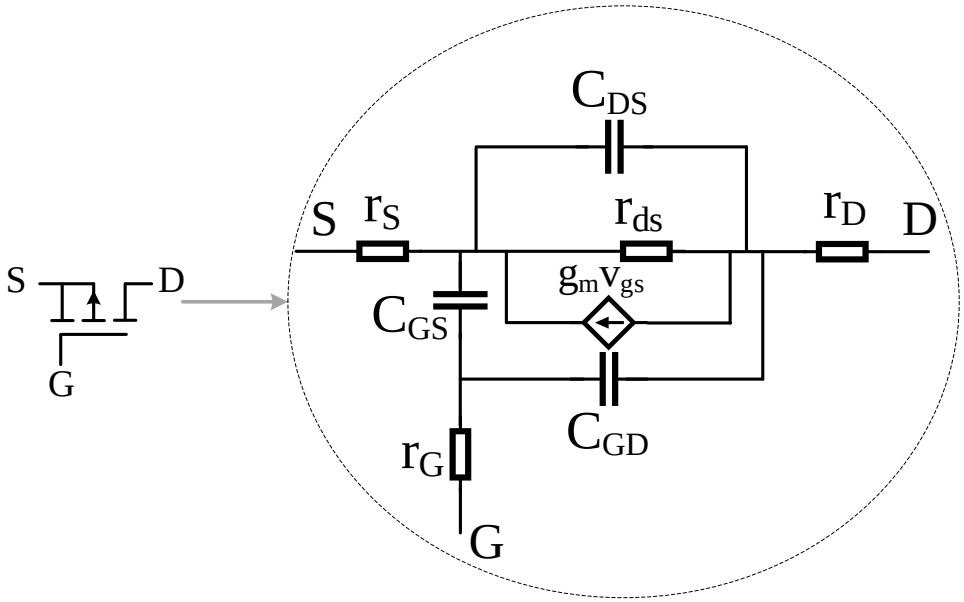


Figure 3-2: The small-signal model of the PMOS transistor.

3.3.2 Modelling of the error amplifier

Architecture

In this discrete SCALDO design, the error amplifier topology is developed using a resistively loaded BJT differential pair (two matched NPN transistors: Q_1 and Q_2) as shown in Figure 3-3. This method is one of the conventional error amplifier topologies applied in LDO regulators [50]. The following points describe the reasons for selecting this method in the stability analysis.

- Low-cost and simple architecture.
- Improves the DC PSR of the LDO regulator.
- Ideal for worst-case stability analysis of the SCALDO regulator due to the high output impedance. This effect is explained as follows:

The high output current LDO regulator in a discrete SCALDO design requires a larger output capacitance to improve the load-transient response. This large output capacitor creates a dominant low-frequency pole in the LDO open-loop transfer function [51]. On the other hand, the high output impedance of this error amplifier together with the gate-source parasitic capacitance of the PMOS pass device make another low-frequency pole in the open-loop transfer function of a LDO regulator [51]. Therefore, the use of conventional error amplifier topology will lead to the lowest phase margin for a given SCALDO design.

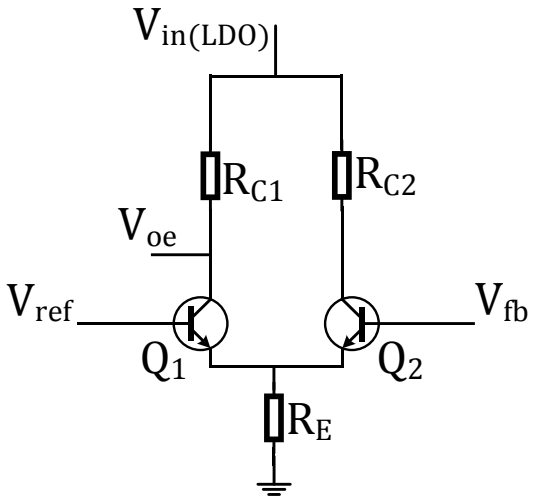


Figure 3-3: The NPN BJT differential pair.

The reference voltage is fed to the base terminal of Q_1, and the feedback voltage is fed to the base of Q_2. The amplified error signal (V_{oe}) is taken from the collector of Q_1. The emitter follower is shown as R_E while R_{C1} and R_{C2} represent the collector resistors of Q_1 and Q_2, respectively. The values of R_{C1} and R_{C2} resistors are kept equal.

Small-signal model

The ratio of the output voltage to the differential input signal for small signals of this error amplifier topology is defined in (3-2). The derivation of the first-order model of this error amplifier topology is provided in Appendix A.

$$\frac{v_{oe}}{(v_{fb}-v_{ref})}=\frac{G_{ea}}{(1+s/\omega_{p1(ea)})} \tag{3-2}$$

Where; G_{ea} and $\omega_{p1(ea)}$ are the gain and the low-frequency pole of the error amplifier, respectively. Also, v_{fb}, v_{ref}, v_{oe} are the small-signal quantities of feedback voltage, reference voltage, and the error amplifier output voltage, respectively.

The output of the error amplifier is converted to a voltage-controlled voltage source and a series output resistance (R_o) by using the circuit theory. This simplified block diagram of the error amplifier is shown in Figure 3-4.

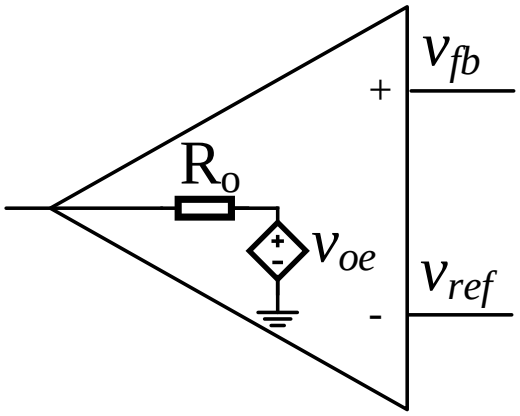


Figure 3-4: The simplified error amplifier model.

3.3.3 Modelling of the SCALDO converter

The small-signal modelling of SMPS topologies is conventionally done with the aid of the state-space averaging technique [52, 53]. In this approach, the switching ripple is averaged out, and the low-frequency components of the reference voltage perturbation are extracted. In other words, this method low-pass filters the signal with a corner frequency of the switching frequency [52]. Consequently, the state-space averaging method is accurate for modelling the systems only for frequencies less than the switching frequency.

The SCALDO regulator is also a periodic and time-varying system as discussed in section 2.2. Nonetheless, the operating frequency of this regulator is typically in the millihertz (mHz) range. Hence, the state-space averaging technique is not applicable to investigate the system behaviour for control signals which have frequencies higher than the switching frequency. In that case, this study uses the circuit averaging method and classical control due to the uniqueness and the low-frequency nature of the SCALDO regulator compared to SMPS topologies.

Moreover, the stability analysis of the LDO regulators is done based on the reference voltage perturbations assuming that the voltage of the input power source is fixed [54, 55]. On the other hand, the theory of super-positioning is used to model the DC-DC converter circuits with disturbances due to both reference and power source voltages [56]. In this method, the transfer impedance $V_{o(LDO)}/V_{in}$ is derived for a fixed

reference voltage. Similarly, the transfer function of $V_{o(LDO)}/V_{ref}$ is obtained for a constant power supply voltage. Since the transfer function of $V_{o(LDO)}/V_{in}$ is subjected to PSRR analysis [50, 57, 58], it is left out of the scope of this analysis. Therefore, the control system of the SCALDO regulator is modelled for a constant input source voltage as with the conventional stability analysis of the LDO regulators.

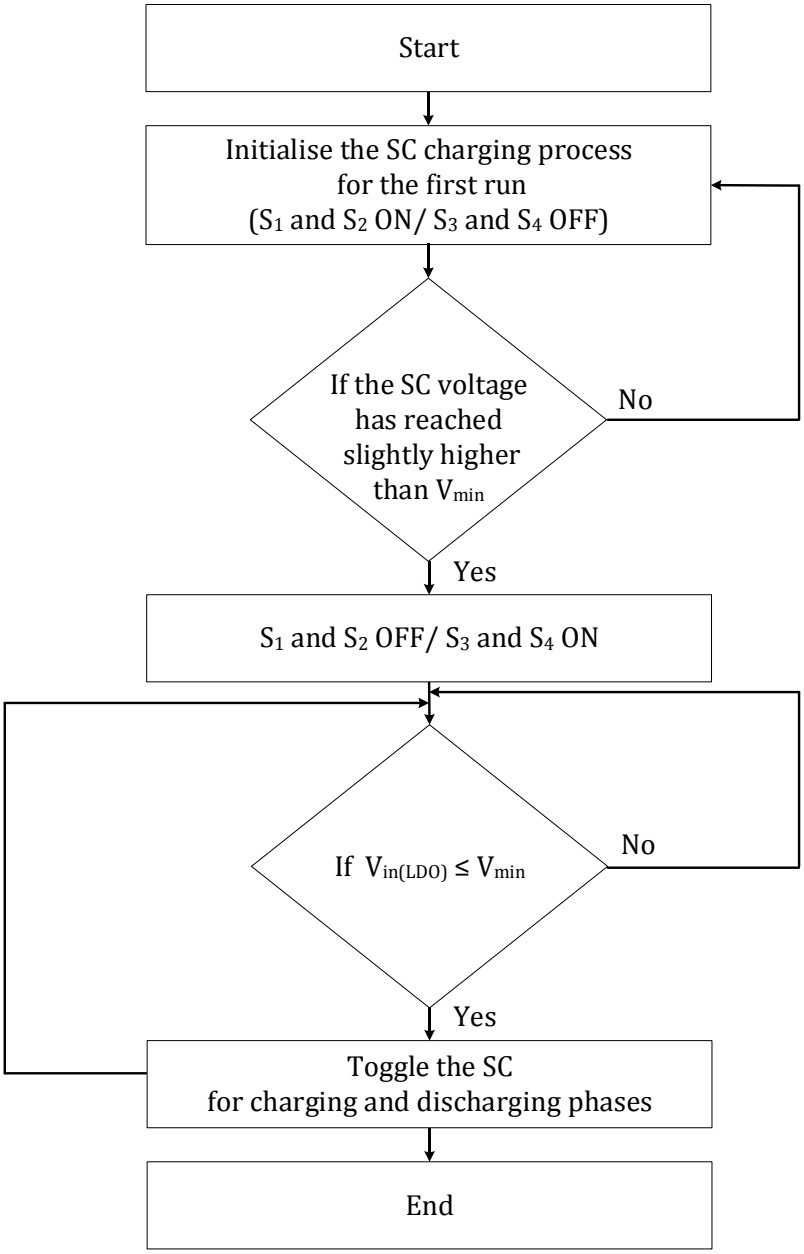


Figure 3-5: The switching algorithm of the basic SCALDO topology.

The switching controller

The switching method of the SCALDO regulator is based on the comparison of the input DC voltage of the LDO regulator with V_{min}. The algorithm of the switching controller is displayed in Figure 3-5 (Refer Figure 2-1 for switching arrangement). The key parameters, which govern the switching frequency of the SCALDO

regulator, are the load current, the capacitance of the SC, the ESR of the SC, the resistance of the switches, and the voltage of the power source. Because the capacitance of the SC, the ESR of the SC, and the resistance of the switches are fixed values in a particular design, the switching frequency is a constant for a given input voltage and a load current. In addition, this logic control circuit has minimum influence due to the reference voltage perturbations because of the extra low impedance of the SC and the switches. Therefore, this switching mechanism can be considered as a frequency independent system for control loop analysis of the SCALDO regulator.

Linearisation of the switching network

The simplified first-order model of the SC [59, 60] with the ideal capacitance (C_{SC}) and the ESR (R_{SC}) is used to reduce the mathematical complexity of this analysis. Also, a basic assumption is made that the four switches are identical and have the same resistance ($R_{S1}=R_{S2}=R_{S3}=R_{S4}=R_{SW}$). The sum of the ESR of the SC and the resistance of two switches (which always come in series with the SC in each phase) is defined as R_{in} (equivalent resistance of the switching network) according to (3-3).

$$R_{in} = 2R_{sw} + R_{sc} \tag{3-3}$$

The switching transient events of the single-stage SCALDO regulator are illustrated in Figure 3-6. The voltage across the SC and the input voltage of the LDO regulator in each transient event can be derived considering a constant input current ($I_{in(LDO)}$ is a constant).

The equivalent circuit model of the switching network can be derived by using the charge balance of the SC as follows:

According to Figure 3-6 (a), the voltage across the SC at the end of the charging phase ($V_{SC(a)}$) can be written as (3-4).

$$V_{SC(a)} = V_{in} - V_{\min} - I_{in(LDO)}R_{in} \tag{3-4}$$

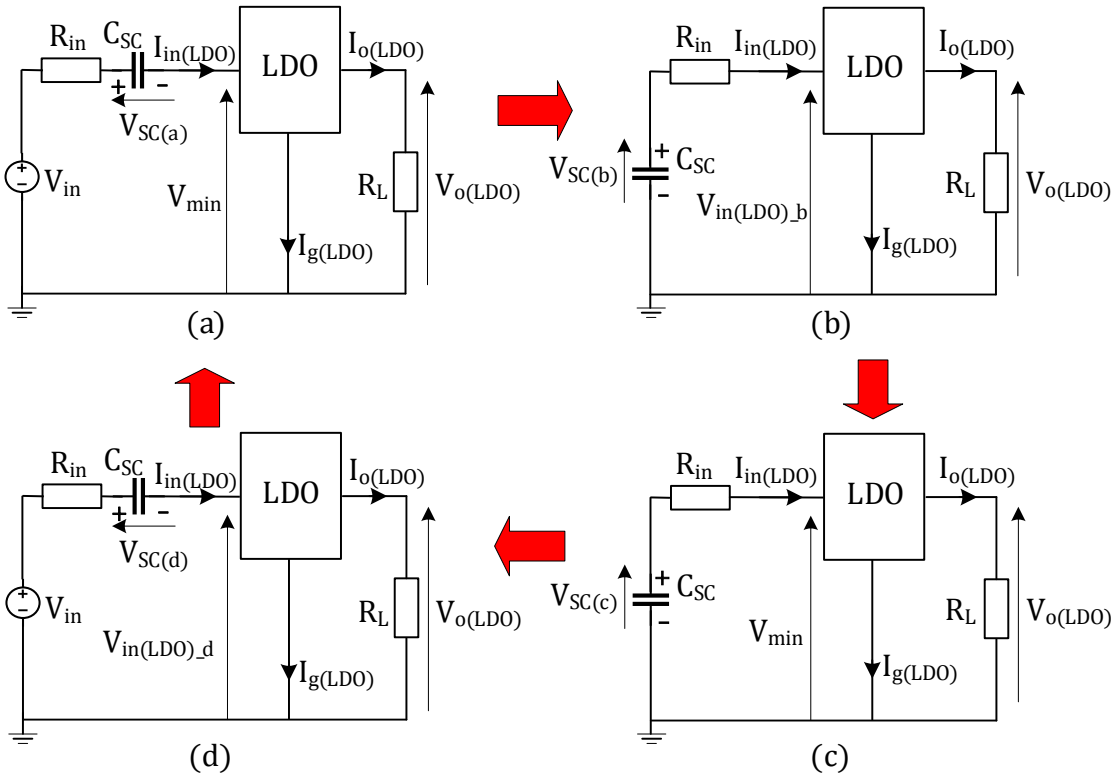


Figure 3-6: SCALDO operation cycle: (a) End of the charging phase, (b) Start of the discharging phase, (c) End of the discharging phase, (d) Start of the charging phase.

Since the voltage of a capacitor does not change instantaneously, the initial voltage of the SC at the beginning of the discharging phase ($V_{SC(b)}$) is the same as $V_{SC(a)}$. Therefore, the initial input voltage of the LDO regulator at this point ($V_{in(LDO)\_b}$) can be obtained as per (3-5) with reference to Figure 3-6 (b).

$$V_{in(LDO)\_b} = V_{SC(b)} - I_{in(LDO)} R_{in} = V_{in} - V_{\min} - 2I_{in(LDO)} R_{in} \tag{3-5}$$

The following two relationships can be derived related to Figure 3-6 (c) and (d) using the same method.

$$V_{SC(c)} = V_{\min} + I_{in(LDO)} R_{in} \tag{3-6}$$

$$V_{in(LDO)\_d} = V_{in} - V_{SC(d)} - I_{in(LDO)} R_{in} = V_{in} - V_{\min} - 2I_{in(LDO)} R_{in} \tag{3-7}$$

The input and output voltage waveforms of the LDO regulator and the variation of the SC voltage are displayed in Figure 3-7. The periodic time of one complete cycle is denoted as T. Similarly, the duration of the charging phase and the duration of the discharging phase are, respectively, t_c and t_d. According to this diagram, $V_{in(LDO)}$ is a sawtooth waveform that has a ripple amplitude of $V_{in(LDO)\_amp}$ as defined in (3-8).

$$V_{in(LDO)\_amp} = V_{in} - 2V_{\min} - 2R_{in}I_{in(LDO)} \quad (3\text{-}8)$$

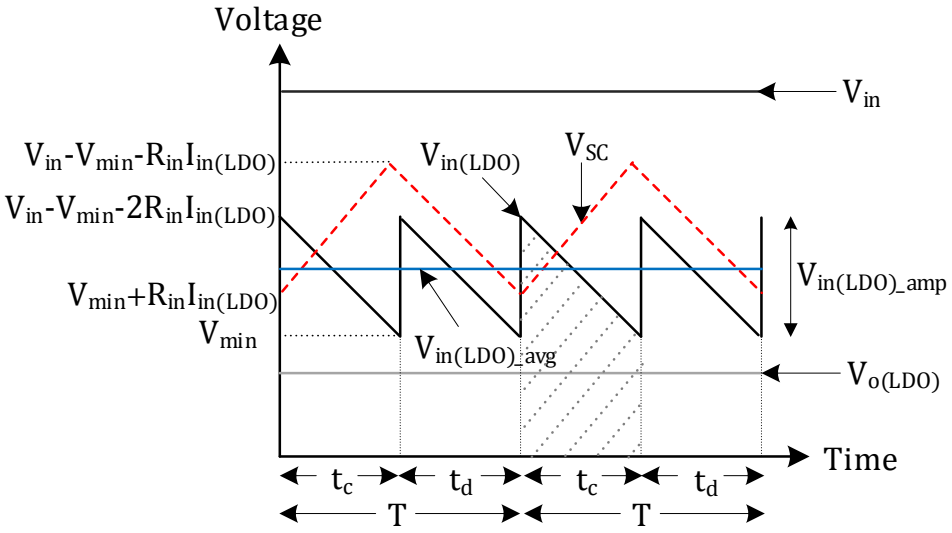


Figure 3-7: The variation of voltages of the single-stage SCALDO regulator.

For a given switching frequency (Where; f = 1/(T/2)), $V_{in(LDO)}$ can be written using the Fourier series as;

$$V_{in(LDO)} = \frac{V_{in}}{2} + \frac{V_{in(LDO)\_amp}}{\pi}\sin(2\pi ft) + \frac{V_{in(LDO)\_amp}}{2\pi}\sin(4\pi ft) + \frac{V_{in(LDO)\_amp}}{3\pi}\sin(6\pi ft)\ldots \quad (3\text{-}9)$$

Since $t_c = t_d = T/2$ at steady state, the average input voltage of the LDO regulator $V_{in(LDO)\_avg}$ can be obtained considering the shaded area in Figure 3-7 as per (3-10).

$$V_{in(LDO)\_avg} = \frac{(V_{in} - V_{\min} - 2I_{in(LDO)}R_{in} + V_{\min})(T/2)}{2(T/2)} = \frac{V_{in}}{2} - R_{in}I_{in(LDO)} \quad (3\text{-}10)$$

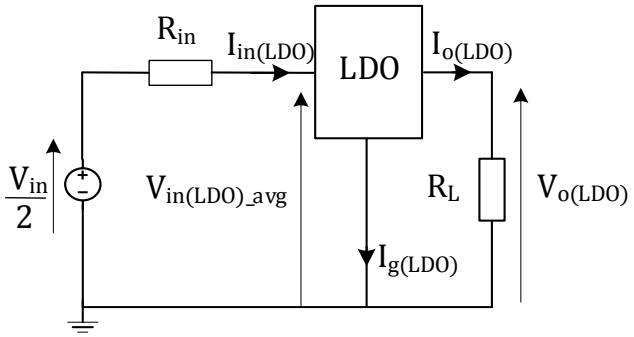


Figure 3-8: The equivalent circuit model of the SCALDO regulator.

According to (3-10), the equivalent circuit model of the SCALDO regulator at steady state can be constructed as Figure 3-8. For the linearity of this model, $V_{in(LDO)\_amp}$ should be kept as low as possible. When this ripple is kept small, the DC bias point

of the series-pass device remains unchanged, and the device is not pushed into the large-signal variation throughout the switching cycles. $V_{in(LDO)\_amp}$ can be minimised by using an effective value for V_{min} in the SCALDO switching controller. In the 12 V to 5 V SCALDO case, for example, if R_{in}= 0.19, $I_{in(LDO)}$ = 0.1 A and V_{min} = 5.95 V, the amplitudes of the fundamental and the second harmonic of $V_{in(LDO)}$ become 20 mV and 10 mV, respectively according to (3-9). Due to the high PSRR of the LDO regulator at low frequencies [50, 57, 58, 61], the switching frequency and its harmonics are attenuated, and their effect on the output voltage is negligible.

According to (3-10), the DC current and the DC input voltage of the LDO regulator are $I_{in(LDO)}$ and $V_{in(LDO)\_avg}$, respectively. Consider that the perturbation (v_{ref}) is applied at the reference voltage source. The changes in the input voltage and current of the LDO regulator due to the reference perturbation are defined in (3-11).

$$V_{in(LDO)\_avg} + v_{in(LDO)} = \frac{V_{in}}{2} - R_{in}(I_{in(LDO)} + i_{in(LDO)}) \tag{3-11}$$

Where: $i_{in(LDO)}$ and $v_{in(LDO)}$ are the small-signal quantities of the input current and the input voltage of the LDO regulator due to the reference voltage perturbation.

Subtracting (3-10) from (3-11), the AC components can be extracted as per (3-12).

$$v_{in(LDO)} = -R_{in} i_{in(LDO)} \tag{3-12}$$

According to (3-12), the linear circuit model of the SCALDO regulator for small-signal analysis is shown in Figure 3-9.

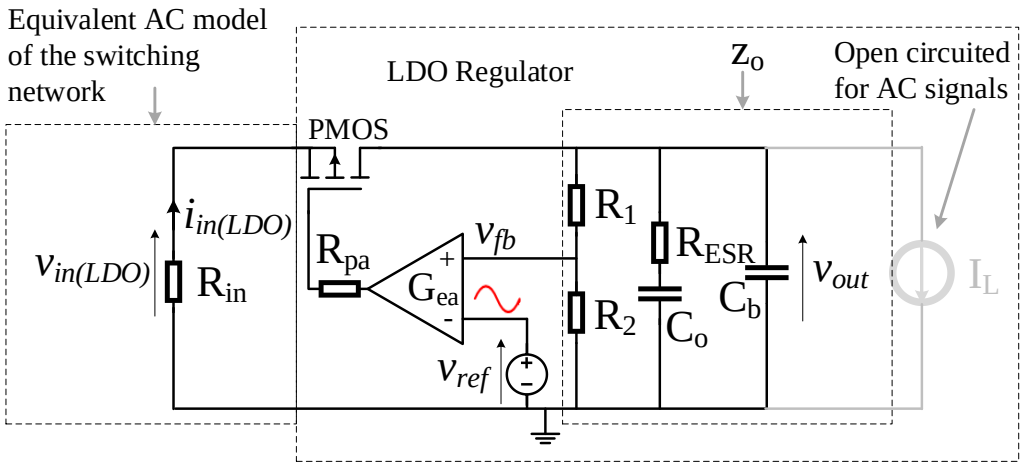


Figure 3-9: The linear circuit model of the SCALDO regulator.

3.4 The open-loop gain transfer function

The open-loop analysis is conventionally used to determine the stability of a LDO regulator [54, 55, 62]. Therefore, the same approach is considered for the stability of the SCALDO regulator in this study.

The linear small-signal model of the SCALDO regulator is displayed in Figure 3-10. This diagram is constructed with the aid of the linear circuit model in Figure 3-9, the MOSFET model in Figure 3-2, and the error amplifier model in Figure 3-4.

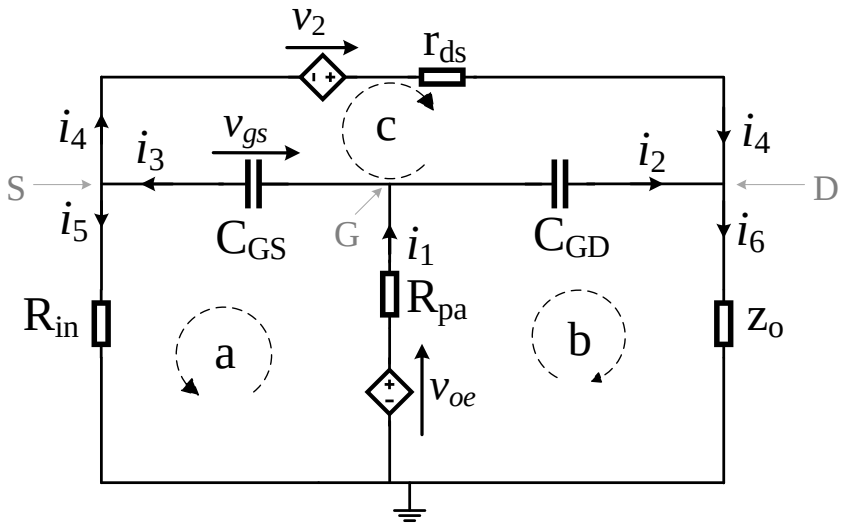


Figure 3-10: The small-signal model of the SCALDO regulator.

The following assumptions are made to reduce the complexity of the analysis in this circuit model. Nevertheless, all these parameters are included in the simulations.

- The source terminal resistance, the drain terminal resistance, and the source-drain parasitic capacitance are neglected ($r_D \approx 0$, $r_S \approx 0$, $C_{DS} \approx 0$).
- Only the low-frequency pole ($\omega_{p1(ea)}$) of the error amplifier is considered.
- The feedback resistor network is not considered for output impedance (z_o).

The parameters used in Figure 3-10 are defined as follows;

$$v_{oe} = \frac{G_{ea}}{(1 + s/\omega_{p1(ea)})}(v_{fb} - v_{ref}) \tag{3-13}$$

$$v_2 = -g_m v_{gs} r_{ds} \tag{3-14}$$

$$z_o \approx \left(R_{ESR} + 1/sC_o\right)//(1/sC_b) \tag{3-15}$$

$$R_{pa} = r_G + R_o \tag{3-16}$$

The following equations are derived by applying the KCL (Kirchhoff's Current Law) to nodes G, S, D, and the KVL (Kirchhoff's Voltage Law) to loops a, b, and c in Figure 3-10.

$$i_1 - i_2 - i_3 = 0 \tag{3-17}$$

$$i_3 - i_4 - i_5 = 0 \tag{3-18}$$

$$i_2 + i_4 - i_6 = 0 \tag{3-19}$$

$$v_{oe} - i_1 R_{pa} - i_3 sC_{GS} - i_5 R_{in} = 0 \tag{3-20}$$

$$v_{oe} - i_1 R_{pa} - i_2 sC_{GD} - i_6 z_o = 0 \tag{3-21}$$

$$v_2 - i_4 r_{ds} + i_2 sC_{GD} - i_3 sC_{GS} = 0 \tag{3-22}$$

The equations (3-13)-to-(3-22) can be solved to obtain the v_{out} to v_{oe} relationship (plant transfer function of the SCALDO regulator) by using the MATLAB Symbolic Math Toolbox. The SCALDO plant transfer function (G(s)) is defined in (3-23).

$$G(s) = \frac{v_{out}}{v_{oe}} = \frac{n(s)}{d(s)} \tag{3-23}$$

Where;

$$n(s) = z_o[r_{ds}(z_{GS}(g_m(z_{GD} - R_{in}) - 1)) - R_{in}(z_{GS} + z_{GD})] \tag{3-24}$$

$$\begin{aligned} d(s) = {} & r_{ds}(R_{pa}(z_o + z_{GD}) + (z_{GS} + R_{in})(R_{pa} + z_o + z_{GD})) \\ & + r_{ds} g_m z_{GS}(R_{pa}(z_o + R_{in}) + R_{in}(z_o + z_{GD})) \\ & + R_{pa}(z_{GS} + z_{GD})(z_o + R_{in}) \\ & + z_{GS} z_o(z_{GD} + R_{in}) + z_{GD} R_{in}(z_o + z_{GS}) \end{aligned} \tag{3-25}$$

For the convenience of the reader, the s-domain impedance of C_{GS} and C_{GD} are denoted as z_{GS} and z_{GD}, respectively in two equations above.

The numerator (n(s)) and the denominator (d(s)) of G(s) can be further simplified as (3-26) and (3-27), respectively, assuming that r_{ds} is much greater than R_{in}, and R_{ESR}.

$$n(s) \approx -r_{ds} g_m (1 + sR_c C_o)\left(a_z s^2 + b_z s + 1\right) \tag{3-26}$$

Where; $a_z = -(C_{GS} G_{GD} R_{in} / g_m)$, $b_z = (C_{GD} r_{ds}(1 + g_m R_{in}) + R_{in}(C_{GS} + C_{GD}))/(g_m r_{ds})$

$$d(s) \approx \left(a_p s^4 + b_p s^3 + c_p s^2 + d_p s + 1\right) \tag{3-27}$$

Where; $a_p = C_o C_b C_{GS} C_{GD} R_{pa} R_{ESR} R_{in} r_{ds}$,

$b_p = C_o C_b R_{pa} R_{ESR} r_{ds}((C_{GS} + C_{GD}) + C_{GD} g_m R_{in})$,

$c_p = R_{pa}(C_{GS} + C_{GD})(C_o(R_{ESR} + r_{ds}) + C_b r_{ds}) + C_o C_{GD} R_{pa} g_m r_{ds}(R_{ESR} + R_{in}) + C_o C_b R_{ESR} r_{ds}$,

$d_p = r_{ds}(C_o + C_b)(1 + g_m R_{in}) + C_{GD} R_{pa}(1 + g_m r_{ds}) + C_{GS} R_{pa} + C_o R_{ESR}$

The equations (3-26) and (3-27) can be factorised assuming the zeros and poles are real numbers, and they are widely separated. Therefore, the SCALDO plant transfer function can be approximated as (3-28).

$$G(s) \approx \frac{-g_m r_{ds}(1 + s/\omega_{z1})(1 + s/\omega_{z2})(1 + s/\omega_{z3})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})(1 + s/\omega_{p4})} \tag{3-28}$$

The angular frequencies of the zeros of G(s) can be approximated as:

$$\omega_{z1} = -\frac{1}{C_o R_{ESR}} \tag{3-29}$$

$$\omega_{z2} \approx \frac{g_m r_{ds}}{C_{GS} R_{in} + C_{GD}(r_{ds}(1 + g_m R_{in}) + R_{in})} \tag{3-30}$$

$$\omega_{z3} \approx -\frac{1}{C_{GS}}\left(\frac{1}{R_{in}}+\frac{1}{r_{ds}}+g_m\right)-\frac{1}{C_{GD}r_{ds}} \tag{3-31}$$

Similarly, the angular frequencies of the poles of G(s) can be approximated as:

$$\omega_{p1} \approx -\frac{1}{C_o(R_{ESR}+r_{ds})(1+g_m R_{in})} \tag{3-32}$$

$$\omega_{p2} \approx -\frac{1+g_m R_{in}}{C_{GS}R_{pa}+C_{GD}R_{pa}(1+g_m R_{in}+R_{ESR}g_m)} \tag{3-33}$$

$$\omega_{p3} \approx -\frac{1}{(R_{ESR}\,//\,r_{ds})C_b} \tag{3-34}$$

$$\omega_{p4} \approx -\frac{1+g_m R_{in}}{C_{GS}R_{in}}-\frac{1}{C_{GD}R_{in}} \tag{3-35}$$

3.5 Voltage control loop

The voltage control loop of the basic SCALDO regulator is constructed in Figure 3-11 using the plant transfer function in (3-28) and the output voltage of the error amplifier in (3-13). Since v_{ref} is considered as a positive term in this control loop, the differential input voltage of the error amplifier becomes $v_{ref} - v_{fb}$ that is the negative value of (3-13). Therefore, the output voltage of the error amplifier is multiplied by (-1) and shown as $-v_{oe}$. The SCALDO plant transfer function (G(s)) should also be multiplied by (-1) to remove this effect.

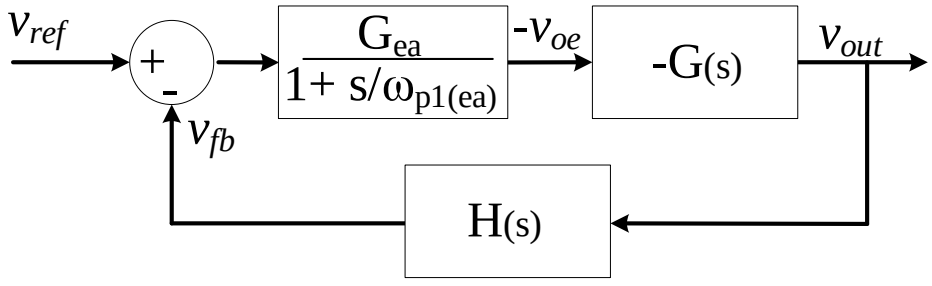


Figure 3-11: The voltage control loop of the basic SCALDO topology.

The term H(s) in this diagram is the transfer function of the feedback network, which is defined in (3-36).

$$H(s) = \frac{R_2}{R_1 + R_2} = G_{fb} \tag{3-36}$$

The open-loop gain transfer function of the SCALDO regulator (T(s)) is defined in (3-37).

$$\begin{aligned} T(s) &= \frac{G_{ea}}{(1 + s/\omega_{p1(ea)})}(-G(s))H(s) \\ &= \frac{G_{ea}G_{fb}g_m r_{ds}(1 + s/\omega_{z1})(1 + s/\omega_{z2})(1 + s/\omega_{z3})}{(1 + s/\omega_{p1(ea)})(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})(1 + s/\omega_{p4})} \end{aligned} \tag{3-37}$$

The DC gain of T(s) is given in (3-38).

$$A_{DC} = G_{ea}G_{fb}g_m r_{ds} \tag{3-38}$$

3.6 Relative locations of the poles and zeros of the SCALDO regulator

The loop gain information of voltage regulators is most often provided in the form of a Bode plot [63] which plots the gain (dB) and phase versus frequency. The Bode plot of a typical discrete SCALDO regulator is illustrated in Figure 3-12. The phase margin and the unity gain frequency are denoted as PM and UGF, respectively in this diagram.

The open-loop transfer function of the SCALDO regulator has three zeros and five poles as can be seen from (3-37). The first zero (ω_{z1}) is due to the capacitance of the output capacitor (C_o) and its ESR (R_{ESR}). This zero falls at low frequencies compared to the other two zeros of T(s) as shown in Figure 3-12. The second zero (ω_{z2}) is due to the parasitic capacitances, the transconductance, and the output resistance of the MOSFET, and the ESR of the input switching network (R_{in}). Interestingly, this zero is a right-hand-plane zero, which gives non-minimum phase behaviour. The frequency of this zero reduces when C_{GS}, C_{GD} and R_{in} increase. The third zero (ω_{z3}) is also composed of the same parameters of ω_{z2}. The frequency of ω_{z3} occurs at relatively high frequencies for typical circuit component parameters of a discrete SCALDO regulator. The frequency of this zero is also inversely proportional to R_{in}.

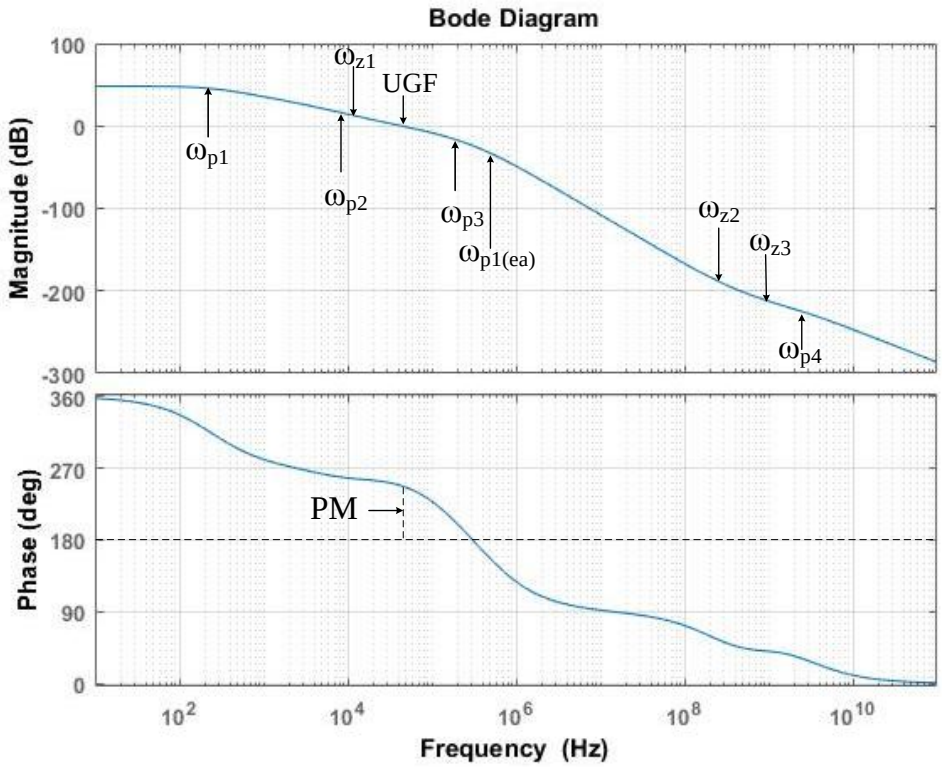


Figure 3-12: Bode plot of the SCALDO regulator.

When the first pole (ω_{p1}) of T(s) is considered, it can be observed that this pole is mainly governed by C_o, R_{ESR}, r_{ds}, g_m, and R_{in}. Since r_{ds} depends on the load current, the frequency of this pole changes accordingly. Also, it is a low-frequency pole which typically occurs before the unity gain frequency of a SCALDO regulator. When R_{in} increases, the frequency of this pole drops slightly.

The second pole (ω_{p2}) is primarily due to the C_{GS} and C_{GD} parasitic capacitances, R_{pa}, g_m, R_{ESR}, and R_{in}. Based on the parasitic capacitances and R_{pa}, this pole may fall before or after the UGF. Nevertheless, it is also a low-frequency pole of the SCALDO regulator. Interestingly, the frequency of this pole increases with R_{in} when C_{GD} is much smaller than C_{GS}.

The other two poles (ω_{p3} and ω_{p4}) occur at relatively high frequencies compared to the first two poles of the SCALDO regulator. The frequency of ω_{p3} depends on the load current of the SCALDO regulator. The error amplifier dominant pole also contributes to phase lag in T(s).

It is important to note here that the frequencies of the fourth pole and the third zero of T(s) are approximately the same ($\omega_{p4} \approx \omega_{z3}$) and their effect is cancelled out.

3.7 Comparison of pole-zero frequencies of the LDO and the SCALDO regulators

The frequencies of the poles and zeros of the SCALDO regulator are compared with the pole-zero frequencies of the generic PMOS LDO regulator in Table 3-1. This table is constructed using the prior art of the frequency analysis of the PMOS based LDO regulators [31, 54, 55, 64].

Table 3-1: DC gain and pole-zero frequencies of LDO and SCALDO regulators

		LDO Regulator	**SCALDO Regulator**
DC gain		$G_{ea}G_{fb}g_m r_{ds}$	$G_{ea}G_{fb}g_m r_{ds}$
Zeros	1	$-\frac{1}{C_o R_{ESR}}$	$-\frac{1}{C_o R_{ESR}}$
	2	Not applicable	$\frac{g_m r_{ds}}{(C_{GS}R_{in} + C_{GD}(r_{ds}(1+g_m R_{in}) + R_{in}))}$
	3	Not applicable	$-\frac{1}{C_{GS}}\left(\frac{1}{R_{in}} + \frac{1}{r_{ds}} + g_m\right) - \frac{1}{C_{GD} r_{ds}}$
Poles	1	$-\frac{1}{C_o(R_{ESR} + r_{ds})}$	$-\frac{1}{C_o(R_{ESR} + r_{ds})(1+g_m R_{in})}$
	2	$-\frac{1}{C_{GS}R_{pa} + C_{GD}R_{pa}(1+R_{ESR}g_m)}$	$-\frac{1+g_m R_{in}}{C_{GS}R_{pa} + C_{GD}R_{pa}(1+g_m R_{in} + R_{ESR}g_m)}$
	3	$-\frac{1}{(R_{ESR} // r_{ds})C_b}$	$-\frac{1}{(R_{ESR} // r_{ds})C_b}$
	4	$-\omega_{p1(ea)}$	$-\omega_{p1(ea)}$
	5	Not applicable	$-\frac{1+g_m R_{in}}{C_{GS}R_{in}} - \frac{1}{C_{GD}R_{in}}$

Table 3-1 reveals that both regulators have the same parameters for their DC gains, the first zero, and the third pole. Similarly, the error amplifier low-frequency pole is

also identical for both regulators. Nevertheless, the frequency of this pole depends on the particular error amplifier topology applied in the LDO regulator. In addition, a single-stage SCALDO regulator has two high-frequency zeros and a high-frequency pole due to the low-frequency SC circulation network.

Closer inspection of the frequency of the first pole of these two regulators shows that the SCALDO regulator consists of an extra term: $1/(1+ g_m R_{in})$ which has a value less than 1. Therefore, the frequency of the first pole of the LDO regulator is slightly higher than the frequency of the first pole of the SCALDO regulator. On the other hand, if the value of $C_{GD} << C_{GS}$, the frequency of the second pole of the LDO regulator becomes slightly lower than the frequency of the same pole of SCALDO regulator.

3.8 Frequency compensation of the SCALDO regulator

The phase margin (PM) of a control system is the algebraic sum of the phase shifts of the individual poles and zeros [10]. Since the effect of ω_{z3} and ω_{p4} is cancelled out in the basic SCALDO topology, the PM of this regulator is approximated in (3-39).

$$PM \approx 180 + \tan^{-1}\left(\frac{UGF}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{UGF}{\omega_{z2}}\right) - \tan^{-1}\left(\frac{UGF}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{UGF}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{UGF}{\omega_{p3}}\right) - \tan^{-1}\left(\frac{UGF}{\omega_{p1(ea)}}\right) \quad (3\text{-}39)$$

According to (3-39) it can be seen that four poles (ω_{p1}, ω_{p2}, ω_{p3}, and $\omega_{p1(ea)}$) together with the right-half-plane zero (ω_{z2}) cause a phase lag. Closer inspection of the locations of ω_{p1} and ω_{p2} in Figure 3-12 shows that they occur at relatively low frequencies and might cause a maximum of -180° phase shift at UGF. The other two poles (ω_{p3}, and $\omega_{p1(ea)}$) and the high-frequency zero ω_{z2} might also contribute to a considerable phase lag at UGF.

Pushing the dominant pole of the error amplifier to high frequencies and selection of the optimal value for the decoupling capacitor (C_b) might reduce the phase lag due to $\omega_{p1(ea)}$, and ω_{p3}, respectively. Also, using multi-stage amplifiers instead the conventional differential pair can reduce the output impedance of the error amplifier and set the frequency of ω_{p2} to occur at high frequencies accordingly. Even though the parasitic capacitance of a high-current MOSFET is a significant factor, the phase lag due to ω_{z2} can be reduced by selecting the switches with lowest possible

resistance and the SC with a small ESR in a SCALDO design. Similarly, if the ESR of the input switching network is reduced, the phase lag due to ω_{p1} can also be reduced.

3.8.1 Compensation using the output capacitor ESR

Only the zero due to the output capacitor (ω_{z1}) contributes a phase lead. Therefore, this SCALDO circuit design should be carefully designed to stabilise the control loop. The location of ω_{z1} should be determined from no-load to a full load output current to provide a sufficient phase margin. Therefore, the selection of the stable range of the output capacitor ESR is crucial in this scenario to make the discrete SCALDO regulator stable. Typically, the output capacitor ESR should provide a phase margin of no less than 30° for the full range of output load current [10, 62, 63]. If the ESR itself not sufficient to provide the required phase margin, the other phase margin improvement techniques (e.g., feedforward compensation) should be applied to stabilise the SCALDO design.

3.8.2 Feedforward compensation

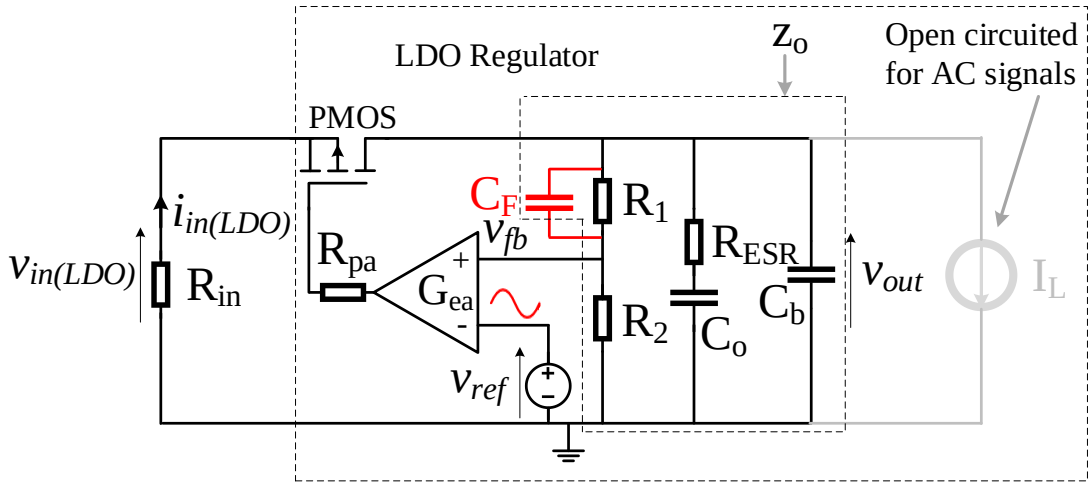


Figure 3-13: Feedforward compensation of the SCALDO regulator.

In practical circumstances, the output capacitor ESR might be able to provide a sufficient phase margin in the SCALDO regulator. Nevertheless, the temperature dependence of the ESR of the output capacitor might cause stability issues even in a properly compensated regulator [63, 65]. One solution to improve the phase margin is the use of feedforward compensation; this is also applied in LDO regulator designs [51]. This compensation is done by connecting a feedforward capacitor (C_F) in parallel with the upper resistor (R_1) of the feedback network as shown in Figure 3-13.

After C_F is connected, the feedback network is changed to a new transfer function $H_F(s)$ as defined in (3-40).

$$H_F(s) = G_{fb}\frac{1+sC_F R_1}{1+sC_F(R_1 // R_2)} \tag{3-40}$$

Equation (3-40) shows that the feedforward compensation adds a pole-zero pair to the open-loop transfer function. The frequencies of the feedforward zero (ω_{zF}) and the pole (ω_{pF}) are defined in (3-41) and (3-42), respectively.

$$\omega_{zF} = -\frac{1}{C_F R_1} \tag{3-41}$$

$$\omega_{pF} = -\frac{1}{C_F(R_1 // R_2)} \tag{3-42}$$

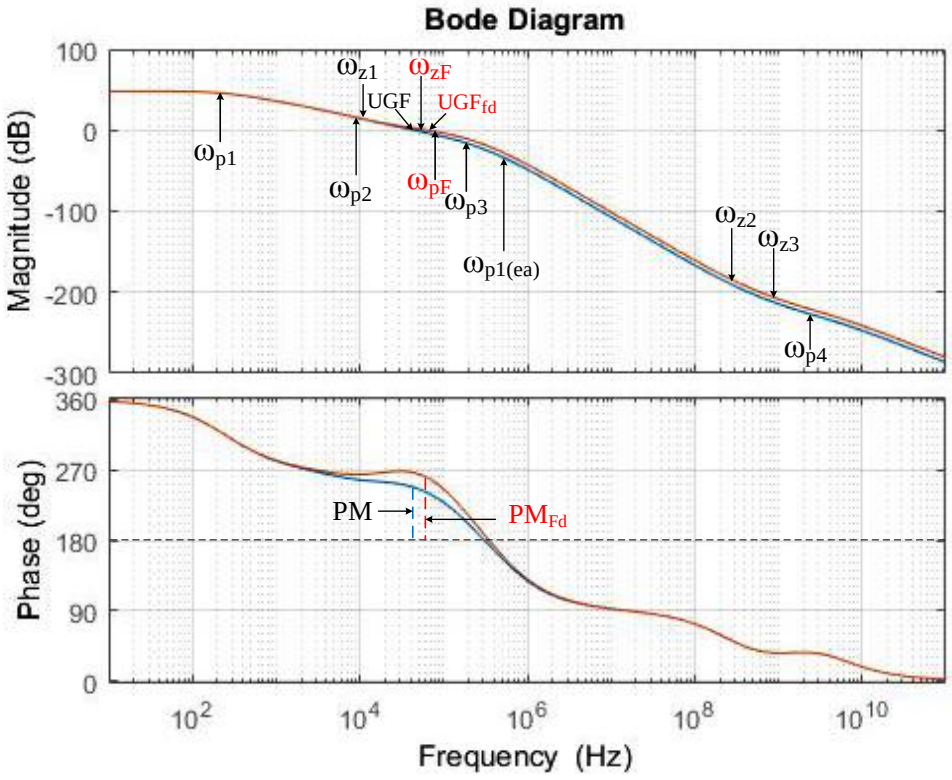


Figure 3-14: Bode plot of the SCALDO regulator when the feedforward compensation is used along with the output capacitor ESR compensation.

If the output voltage to the reference voltage ratio ($V_{o(LDO)}/V_{ref}$) is increased, the R_1/R_2 ratio also increases. Therefore, this method can make a much larger improvement in the phase margin when the $V_{o(LDO)}/V_{ref}$ ratio is high. If this condition

is satisfied, ω_{zF} and ω_{pF} can be designed to occur far apart in the frequency axis [51]. The location of ω_{zF} is typically set about 1/3 of the UGF for optimum phase margin achievement in some LDO regulators when other compensation techniques are not used [51].

The red trace in Figure 3-14 shows the Bode plot when the feedforward compensation is applied. The ESR of the output capacitor is not changed in this case to make the comparison clear. The blue trace represents the same Bode plot of Figure 3-12. The new unity gain frequency and the phase margin are denoted as UGF_{Fd} and PM_{Fd}, respectively. The feedforward capacitor is selected in a way that ω_{zF} falls slightly before UGF_{Fd}. Also, it is assumed that the feedback resistors are equal in value. Therefore, $V_{o(LDO)}/V_{ref} = 2$ and the frequency of ω_{pF} becomes twice the frequency of ω_{zF}. The phase margin has increased from PM to PM_{Fd}.

3.9 Discussion

The stability of the basic SCALDO regulator is investigated using a discrete design. This circuit is composed of a LDO regulator built with a p-channel MOSFET and a supercapacitor circulation network. The small-signal model of the overall circuit is constructed by using the circuit averaging method and classical control. The open-loop gain transfer function is obtained from this small-signal model. It has been found that this transfer function has three zeros and five poles, including the error amplifier dominant pole of its first-order model, whereas all of them are independent of the capacitance of the supercapacitor. The relative locations of the poles and zeros are investigated. The ESR of the input switching network affects the frequencies of some of the low-frequency poles. It also creates two high-frequency zeros and one pole. One of the high-frequency zeros is a right-hand-plane zero.

Two techniques have been identified for the frequency compensation of the SCALDO regulator. The first method is the use of the output capacitor ESR as with the conventional PMOS based LDO regulators. The second method is the application of the feedforward compensation by adding a feedforward capacitor to the feedback resistor network. The validation of the stability of the basic SCALDO regulator is discussed in the next chapter with experimental and simulation results.

Chapter 4 Experimental Validation of the Stability of the SCALDO Regulator

Abstract- A 12 V to 5 V discrete SCALDO regulator is designed to validate the small-signal model. The worst-case analysis is performed to ensure the regulator is stable for the corner values of the circuit parameters. The frequencies of the open-loop poles and zeros are determined by changing the resistive parameter of the switching network. A simulation framework is also developed in the MATLAB Simulink environment to observe the open-loop response and the load-transient response. The system response is observed experimentally for different values of the output capacitor ESR and the resistance of the switching network. The conclusions are made by comparing the findings of the simulations and experiments.

4.1 Introduction

A 12 V to 5 V SCALDO regulator is designed by using a discrete LDO regulator based on the fundamental SCALDO configuration where the ETEE of the linear regulator is enhanced from 41.7 % to 83.3 % theoretically. The maximum output current level of this discrete SCALDO prototype is limited to 200 mA, and the other design parameters are defined in Section 4.2. It should be noted here that this experiment does not target any optimisation of process parameters of SoC design of LDO regulators. It covers only the validation of the small-signal model of a discrete SCALDO regulator.

4.2 Discrete SCALDO design parameters

4.2.1 LDO regulator

The specifications of the LDO regulator used in a SCALDO regulator depend on the particular application [14]. Since this study focuses only on the stability criteria and does not target a specific application, a typical low power 5 V LDO regulator is considered for the ease of implementation. The design parameters of this LDO regulator are defined as follows:

- Output voltage: 5 V
- Input voltage range: 5.4 V to 8 V

- Input reference voltage: 2.5 V
- Maximum output current: 200 mA
- Quiescent current: < 5 mA
- Output capacitor: 10 μF (multilayer ceramic) with 10% tolerance
- Decoupling capacitor: 1 μF (multilayer ceramic) with 10% tolerance
- Operating temperature: 25°C

Series-pass element

Si2343 CDS P-channel MOSFET is chosen for this application based on the following factors:

- ✓ Drain-to-Source breakdown voltage: 30 V (higher than the maximum operating voltage of the LDO regulator)
- ✓ Pulsed maximum Drain current: 25 A (assume that the SCALDO short circuit current level is less than 25 A)
- ✓ Gate-Source Threshold voltage: 1.2 V to 2.5 V (less than the nominal LDO regulator input voltage range)
- ✓ On-Resistance: 0.075 mΩ at V_{GS} = 4.5 V when driving a Darin current of 4.6 A in magnitude
- ✓ Gate capacitances: Typically fall in the pF range. Hence they give improved LDO performance by shifting parasitic poles well beyond the UGF
- ✓ Power dissipation: 2.5 W at 25°C ambient temperature. If the V_{min} of the SCALDO is set to 6 V (in the worst-case scenario), the calculated maximum power is 0.2 W which is less than the manufacturer's specified maximum power.

The reference voltage and the feedback network

The reference voltage (2.5 V) is fed from the AD 780 IC from Analog Devices. This IC is an ultrahigh precision bandgap reference voltage source. The minimum and maximum input voltages of this device are 4 V and 36 V, respectively, and they are within the operating voltage specification of the LDO regulator. The maximum output voltage drift is 1 mV, and the quiescent current is less than 1 mA. Besides, the output noise level is specified as $100\text{nV}/\sqrt{\text{Hz}}$. Interestingly, the AD 780 is designed to drive any output capacitance which makes it ideal for MOSFET based LDO design applications.

Based on the output voltage ($V_{o(LDO)}$) and the reference voltage (V_{ref}), the feedback factor (G_{fb}) of this LDO regulator becomes 2 according to the relationship defined in (3-1). This feedback gain can be provided by using two equal resistors connected in series. Since the feedback resistors also contribute to quiescent current consumption, the values of the resistors should be large. Conversely, an enormous resistance might add noise. Therefore, a compromise should be made when selecting the appropriate values for the feedback resistors. Two 2.2 kΩ metal film SMD (surface mount device) resistors are used in the feedback network considering the above factors. These resistors limit the shunt current of the feedback network to 1 mA which is well below the required quiescent current specification defined for this LDO regulator.

4.2.2 Supercapacitor switching controller

The basic SCALDO topology requires four switches to control the supercapacitor operation as highlighted in Section 2.2. Since the SCALDO switching network typically uses back-to-back connected MOSFETs to avoid any short-circuit paths when switching [21], four photovoltaic relays are used in this design to provide the same requirement. They are controlled by the digital output pins of a microcontroller (ATtiny261). Two analog input channels are also used to monitor the input voltage of the power source and the input voltage of the LDO regulator. The firmware of the microcontroller is developed according to the algorithm shown in Figure 3-5.

4.2.3 Circuit design

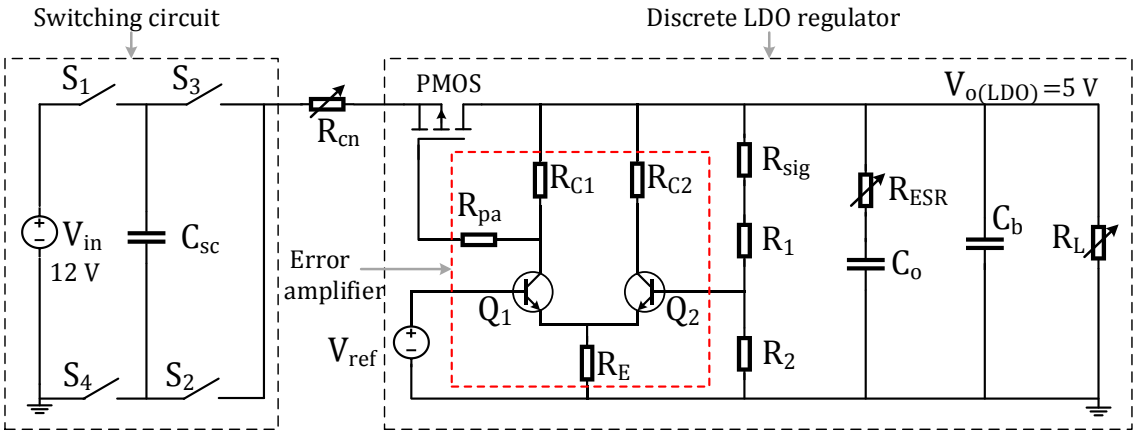


Figure 4-1: The experimental design of the discrete SCALDO regulator.

The basic arrangement of the experimental design of the discrete SCALDO regulator is shown in Figure 4-1. The schematic and the PCB of the complete design are given in Appendix B. The parameters of the essential circuit components of this SCALDO design are summarised in Table 4-1.

Table 4-1: Parameters of the circuit components

Device	Type	Circuit Notation	Design Properties
Series-pass device	P-channel MOSFET: Si2343CDS	PMOS	Threshold voltage (V_{th})= -2.38 V Channel length modulation (λ) = 0.34 V^{-1} Gain = 3.15 AV^{-2} r_S: 0.02 Ω r_D: 0.013 Ω r_G= 5 Ω C_{GS}= 1100 pF C_{GD}= 500 pF C_{DS}= 50 pF
Error amplifier	NPN BJT Differential pair	Q_1, Q_2= BC546B R_{C1}= 3.3 kΩ (1 %) R_{C2}= 3.3 kΩ (1 %) R_E = 1.5kΩ (1 %)	G_{ea}= 25.1 dB $\omega_{p1(ea)}$= 536 kHz
MOSFET gate and error amplifier coupling resistor	SMD Metal film chip resistor	R_{pa}	18 kΩ (1 %)
Supercapacitor	Nesscap	C_{SC}	C_{SC} = 3.3 F (±5 %) Maximum DC voltage= 8.1 V ESR (R_{SC})= 90 mΩ
Switches	photovoltaic relays: TLP3543	S_1, S_2, S_3, S_4	On-Resistance (R_{SW}) = 50 mΩ (each)
Feedback Resistors	SMD Metal film chip resistor	R_1 and R_2	2.2 kΩ (±0.1 %)
Small-signal injection resistor	SMD Metal film chip resistor	R_{sig}	50 Ω (±0.1 %)
Output capacitor	SMD Multilayer Ceramic Capacitor	C_o	10 µF (±10 %) R_{ESR}=400 mΩ at 1 kHz
External ESR resistor	SMD Metal film chip resistor	R_{ESR}	1 Ω (±0.1 %)
Decoupling capacitor	SMD Multilayer Ceramic Capacitor	C_b	1 µF (±10 %) ESR is negligible from 10 Hz to 1 MHz
Switching network variable resistor	SMD Metal film chip resistor	R_{cn}	Discrete: 100 mΩ, 200 mΩ, 300 mΩ

As the first step, the LDO regulator is developed considering a typical 5 V discrete design. Next, the SC switching network is designed. Since the resistance offered by the ESR of the SC and the switches is fixed, a control resistor (R_{cn}) is placed between the switching network and the input of the LDO regulator to adjust the resistive parameter. After the values of the circuit components are defined, a PCB is developed. The SCALDO prototype is tested in the laboratory to obtain frequency behaviour and dynamic response.

4.3 Theoretical calculations

This 12V to 5V experimental SCALDO design is developed based on the stability analysis of the SCALDO regulator with PMOS pass device as described in Chapter 3. Therefore, the ESR of the output capacitor is used as the frequency compensation technique for this SCALDO regulator. After selecting a stable value for the output capacitor ESR, the stability is determined for the extreme values of the critical circuit parameters.

4.3.1 Determination of the stable range of the output capacitor ESR

The ESR of the output capacitor is one of the major design considerations for a PMOS LDO regulator [31, 64]. Similarly, it is also an essential requirement for the stability of a SCALDO regulator built with a PMOS LDO regulator as discussed in Section 3.8. The stable range of the output capacitor ESR against the load current of this SCALDO design is shown in Figure 4-2. At least 45° of phase margin is considered to maintain the stability of the SCALDO regulator for this calculation.

Figure 4-2 suggests that the stable range of the output capacitor ESR varies approximately from 0.6 Ω to 5 Ω for the desired output current levels. Since the ceramic output capacitor has a very low ESR as shown in Table 4-1, an external 1 Ω resistor is added in series with this capacitor to stabilise the voltage control loop. Therefore, the equivalent stable ESR (R_{ESR}) of this SCALDO prototype is considered as 1.4 Ω. Since this value is able to provide a phase margin higher than 45°, other frequency compensation techniques such as feedforward compensation is not used in this experiment for the simplicity of analysis.

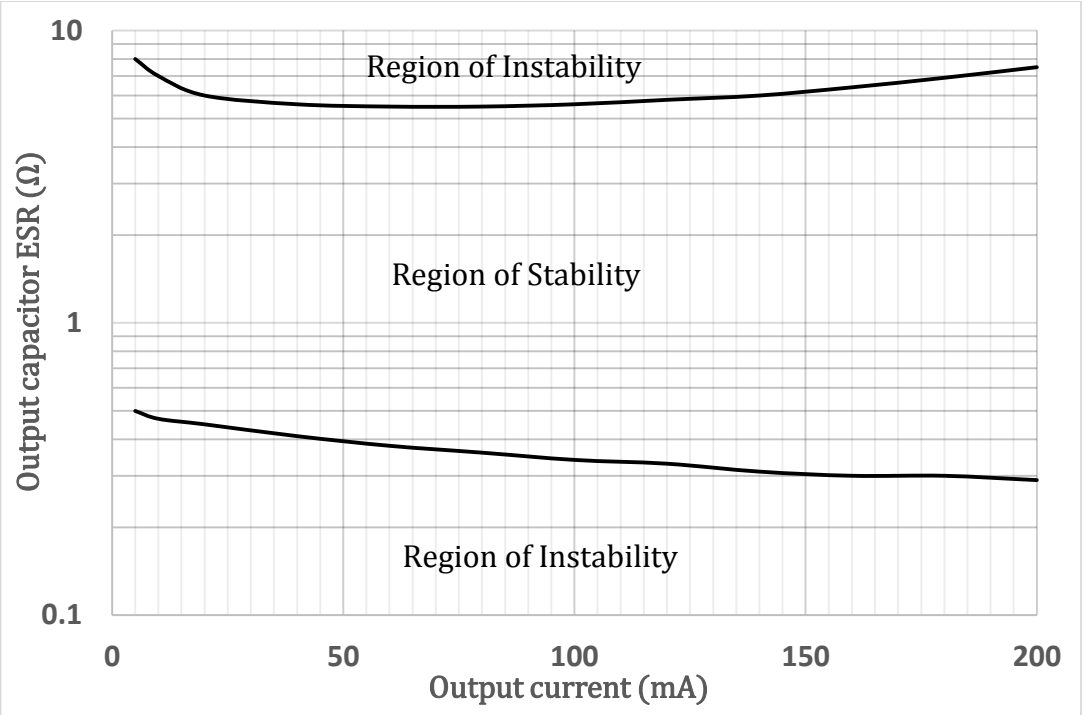


Figure 4-2: The stable range of the output capacitor ESR of the SCALDO regulator.

4.3.2 Gain and phase calculation

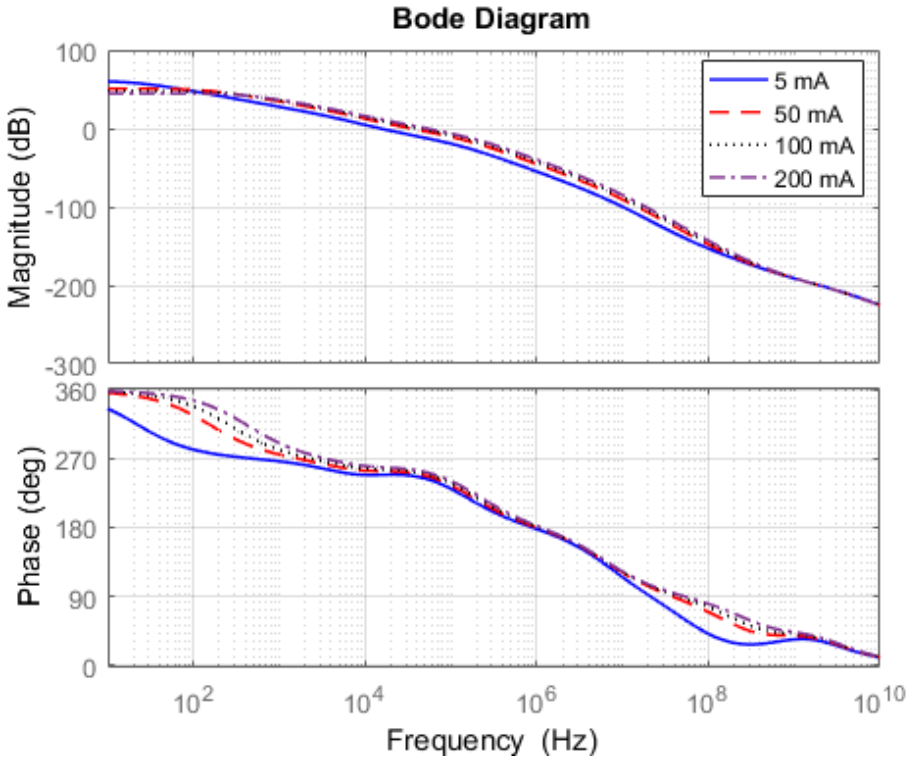


Figure 4-3: Calculated phase and gain behaviour of the SCALDO regulator for different levels of load current.

Using the selected stable ESR value of the output capacitor, the phase and gain plots of the SCALDO regulator are obtained for different levels of load currents and

displayed in Figure 4-3. As this diagram shows, the phase margins for 5 mA, 50 mA, 100 mA, and 200 mA are 68.9°, 71.7°, 71.9° and 72.3°, respectively. Besides, the UGFs for the same currents, respectively, are 14kHz, 35kHz, 42kHz, and 51kHz. These calculated results show that the phase margin is well beyond the 45° minimum phase margin requirement.

4.3.3 Calculation of pole-zero frequencies against the equivalent resistance of the switching network

Table 4-2: Calculated pole-zero frequencies against the equivalent resistance of the switching network

Pole/zero	**Load current = 5 mA**				**Load current = 100 mA**				**Load current = 200 mA**			
	Equivalent resistance of the switching network (Ω)				**Equivalent resistance of the switching network (Ω)**				**Equivalent resistance of the switching network (Ω)**			
	0.19	**0.29**	**0.39**	**0.49**	**0.19**	**0.29**	**0.39**	**0.49**	**0.19**	**0.29**	**0.39**	**0.49**
A_{DC} (dB)	58.8	58.8	58.8	58.8	45.8	45.8	45.8	45.8	42.8	42.8	42.8	42.8
ω_{z1} (kHz)	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4
ω_{z2} (MHz)	63	62	61	60	245	225	209	194	321	287	260	237
ω_{z3} (MHz)	792	529	402	326	910	648	520	444	981	718	590	515
ω_{p1} (Hz)	22.0	21.7	21.3	21.0	259	248	237	228	417	395	376	358
ω_{p2} (kHz)	6.14	6.21	6.28	6.34	7.71	7.90	8.08	8.27	8.32	8.55	8.76	8.96
ω_{p3} (kHz)	177	177	177	177	211	211	211	211	230	230	230	230
ω_{p4} (GHz)	2.47	1.63	1.22	0.97	2.57	1.73	1.32	1.08	2.62	1.78	1.37	1.13
$\omega_{p1(ea)}$ (kHz)	536	536	536	536	536	536	536	536	536	536	536	536
PM (deg)	68.9	69.2	69.4	69.6	71.9	72.2	72.5	72.8	72.3	72.6	72.9	73.2

The frequencies of the open-loop poles and zeros are calculated for different levels of the load current by varying the equivalent resistance of the switching network

(R_{in}) and listed in Table 4-2. This input resistance is controlled by adjusting the value of the external R_{cn} resistor. The values of R_{in} are selected in a way that they fall within the boundaries of the minimum and maximum input resistance which could occur in a typical SCALDO regulator. In other words, this resistor represents the sum of the switch resistance and the ESR of the SC. The nominal value of R_{in} is 190 mΩ when the resistance of the switches and the ESR of the SC are added together, and the maximum value could be 490 mΩ for the worst-case scenario.

Only the frequencies of ω_{z2}, ω_{z3}, ω_{p1}, ω_{p2}, and ω_{p4} depend on the equivalent resistance of the switching network as derived in (3-30), (3-31), (3-32), (3-33), and (3-35), respectively. The frequency of the ESR zero (ω_{z1}) is independent of the load current and R_{in}. The calculated results further show that ω_{z2}, ω_{z3}, and ω_{p4} fall at relatively high frequencies. Besides, for a given load current, the frequencies of these high-frequency poles and zeros decrease when R_{in} is increased. Nevertheless, these frequencies occur well beyond the UGF of the SCALDO regulator even for the maximum value of R_{in}.

When the two low-frequency poles are considered, the frequency of ω_{p1} reduces with the increase of R_{in} and the frequency of ω_{p2} rises when R_{in} is increased.

Interestingly, the variations of the phase margins are minimal (maximum of around 2% deviation) when the R_{in} is changed from its nominal value to the maximum level. This low variation in the phase margin is because of the occurrence of ω_{z2}, ω_{z3}, ω_{p4} at high frequencies compared to the UGF and the net zero impact caused by ω_{p1} and ω_{p2} due to the change of R_{in}.

4.3.4 Worst-case analysis to determine the circuit behaviour against the variation of design parameters

The most widely used method to determine the circuit behaviour against the variation of design parameters are the worst-case and Monte-Carlo analyses. The worst-case analysis is a method of finding the worst possible variation expected in some parameters while the Monte-Carlo analysis is a process of determining the variations with the aid of probability distributions.

In this study, a discrete SCALDO regulator is implemented by using the circuit components of different manufacturers. Since the manufacturers do not always provide the probability distribution of parameters of individual circuit components,

it is a difficult task to apply the Monte-Carlo analysis to this stability analysis. Nevertheless, the extreme values of the circuit components are readily available in the datasheets. Therefore, the worst-case analysis is applied to determine the worst possible variations regarding the stability of this SCALDO regulator.

Six critical circuit parameters are identified based on the open-loop transfer function defined in (3-37), and their extreme values are provided in Table 4-3. These corner values are set out according to the datasheet specifications. It should be noted here that the SCALDO prototype is designed to work at 25°C and the worst-case analysis is done based on this temperature.

Table 4-3: Critical circuit parameters and their ranges

Critical circuit parameter	**Extreme corners**
Output capacitance (C_o) (± 10% deviation from the nominal value)	9 µF to 11 µF
Equivalent output capacitor ESR (R_{ESR}) (based on the ESR of C_o and the external ESR resistor)	1 Ω to 2 Ω
Error amplifier gain (G_{ea}) (± 20% deviation from the nominal value)	14.4 to 21.6
Threshold voltage of the MOSFET (V_{th}) (Min/max values)	-1.2 V to -2.5 V
Channel length modulation of the MOSFET (λ) (± 20% deviation from the nominal value)	0.272 V^{-1} to 0.408 V^{-1}
Gate-Source capacitance (C_{GS}) (± 20% deviation from the nominal value)	880 pF to 1320 pF

Phase margin variation for extreme circuit values

Sixty-four different combinations are developed using the extreme corners of the critical circuit parameters, and the phase margins are determined accordingly. Based on the results obtained from this evaluation, it is found that the minimum phase margin occurs when C_o = 9 µF, R_{ESR} = 1 Ω, G_{ea} = 14.4, V_{th} = 2.5 V, λ = 0.408 V^{-1} and C_{gs} = 1320 pF. Similarly, the maximum phase margin occurs when C_o = 11 µF, R_{ESR} = 2 Ω, G_{ea} = 14.4, V_{th} = 1.2 V, λ = 0.207 V^{-1} and C_{gs} = 880 pF. These phase margins are plotted against the load current in a resolution of 1 mA and illustrated in Figure 4-4.

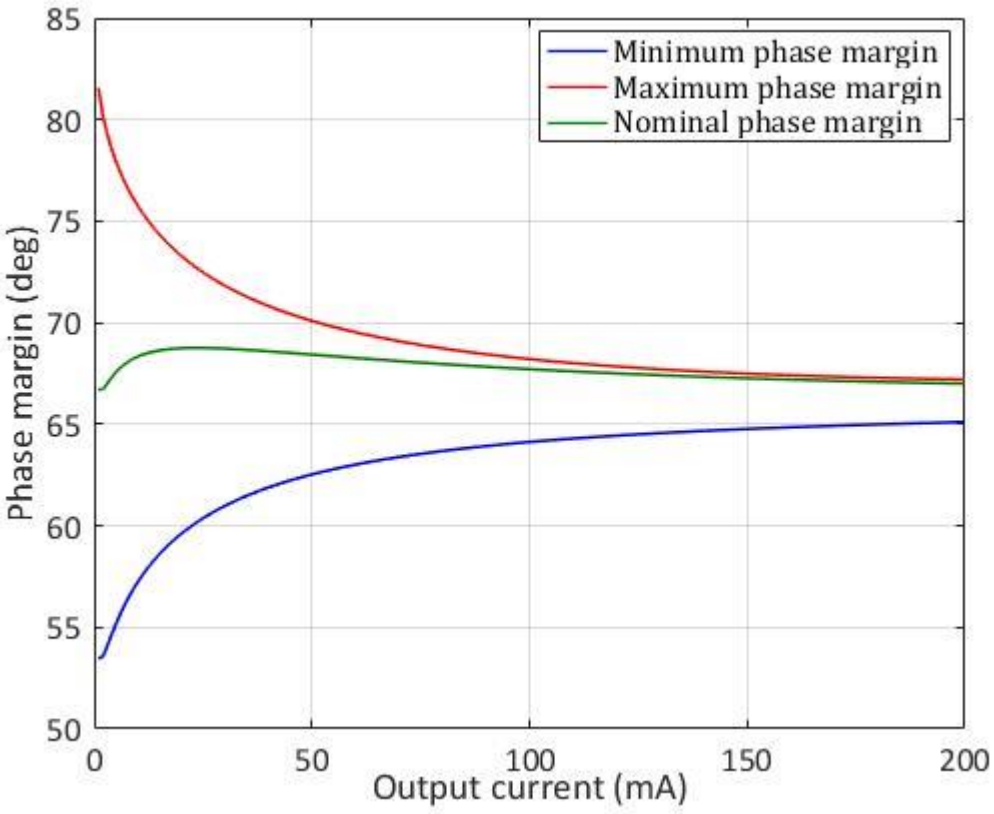


Figure 4-4: Extreme variation of the phase margin against the load current.

As can be seen from Figure 4-4, the nominal phase margin varies between 66° and 68° from no-load to the maximum load current. The maximum phase margin is around 82°at 1 mA of load current as shown in the upper trace of Figure 4-4.

What is striking about lower trace in Figure 4-4 is that the phase margin doesn't fall below 53° when the parameters are set to extreme edges. Therefore, the worst-case analysis confirms that this SCALDO design has satisfied the minimum phase margin specification (45°) for the corner values of the critical circuit parameters.

Variation of the poles and zeros

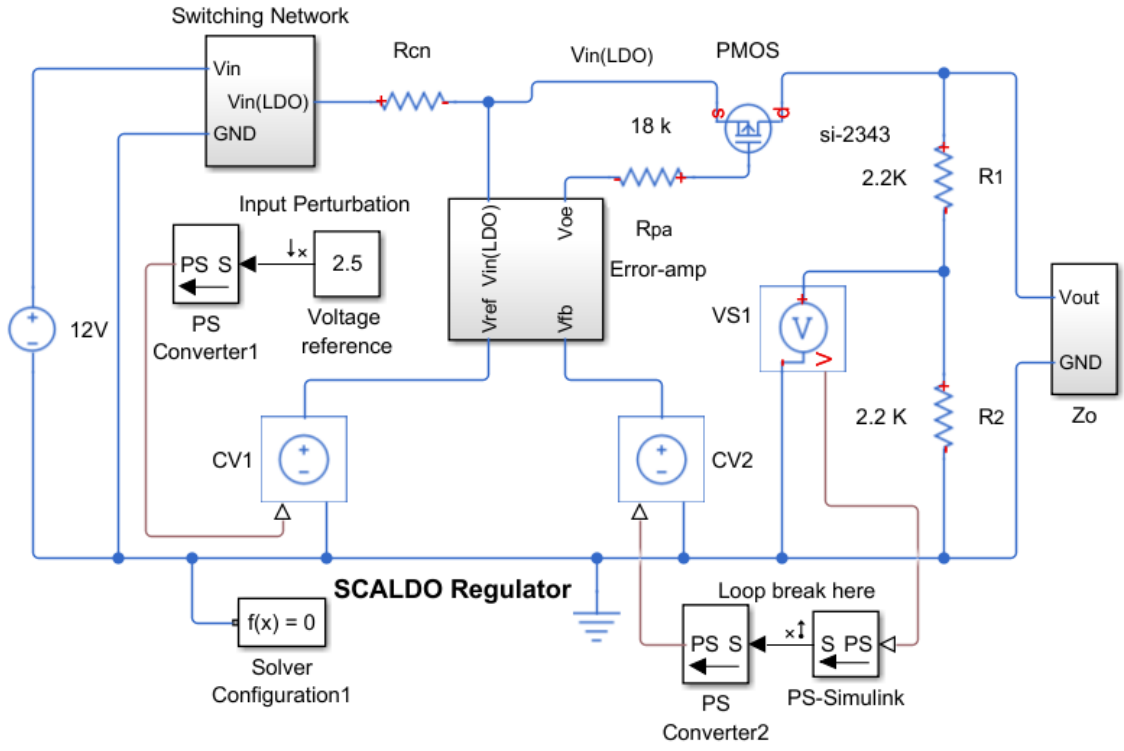
The minimum and maximum values of the frequencies of the poles and zeros along with the DC gain are listed in Table 4-4. According to Table 4-4, the maximum possible value of the DC gain is 64.9 dB, which occurs when the load current is 5mA. Similarly, the lowest DC gain (40.35 dB) occurs at full load. The frequency of the zero due to the output capacitor ESR (ω_{z1}) can vary from 7.23 kHz to 17.68 kHz independent of load current. The lowest possible frequency of the error amplifier dominant pole is 384.5 kHz.

Table 4-4: Extreme values of the pole-zero frequencies

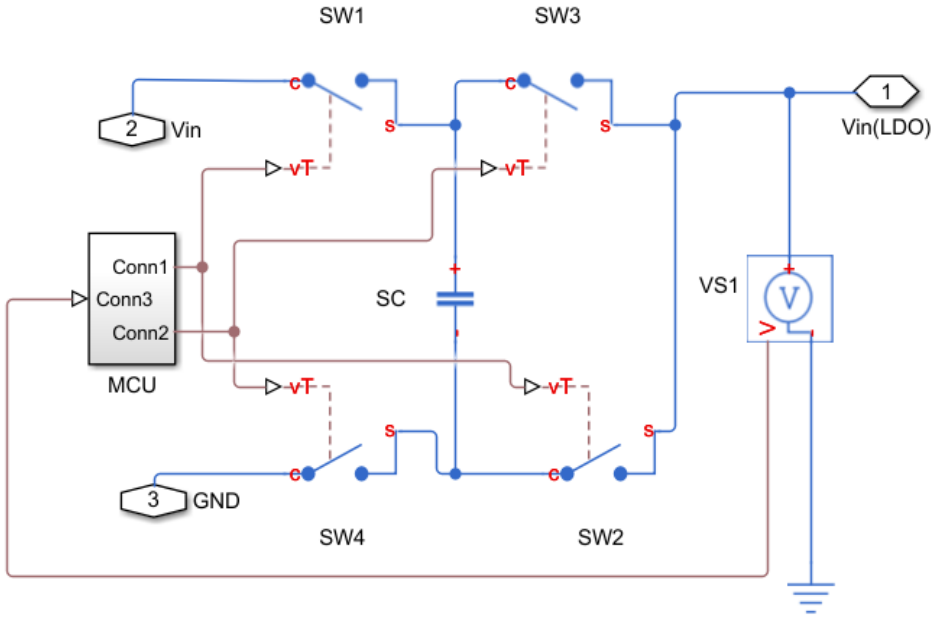
Pole/zero	**Load current**							
	5 mA		**50 mA**		**100 mA**		**200 mA**	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
A_{DC} (dB)	56.37	64.90	46.37	54.90	43.39	51.89	40.35	48.88
ω_{z1} (kHz)	7.23	17.68	7.23	17.68	7.23	17.68	7.23	17.68
ω_{z2} (MHz)	47.53	78.08	126.0	224.4	135.6	299.4	156.2	390.0
ω_{z3} (MHz)	268.2	994.7	319.9	1094.7	353.8	1160.3	404.9	1259.4
ω_{p1} (Hz)	15.03	29.83	97.77	213.42	159.45	360.34	249.13	583.73
ω_{p2} (kHz)	5.041	7.965	5.709	10.12	6.066	11.186	6.531	12.497
ω_{p3} (kHz)	91.57	214.84	107.45	245.29	117.10	264.38	130.78	292.15
ω_{p4} (GHz)	0.8582	2.8551	0.9049	2.9453	0.9331	2.999	0.9732	3.0772
$\omega_{p1(ea)}$ (kHz)	384.5	792.3	384.5	792.3	384.5	792.3	384.5	792.3

The second zero (ω_{z2}) which depends on the SC switching network parameters does not fall less than 47.53 MHz even when the circuit parameters are changed to their extreme values. Similarly, the minimum value that ω_{z3} can have is 268.2 MHz. On the other hand, the high-frequency pole (ω_{p4}) due to the SC switching network can fall to 858.2 MHz. Therefore, this worst-case estimation reveals that the values of the high-frequency zeros and the pole of the SCALDO regulator occur at relatively high frequencies even for the extreme values of circuit parameters.

4.4 Simulation framework



(a)



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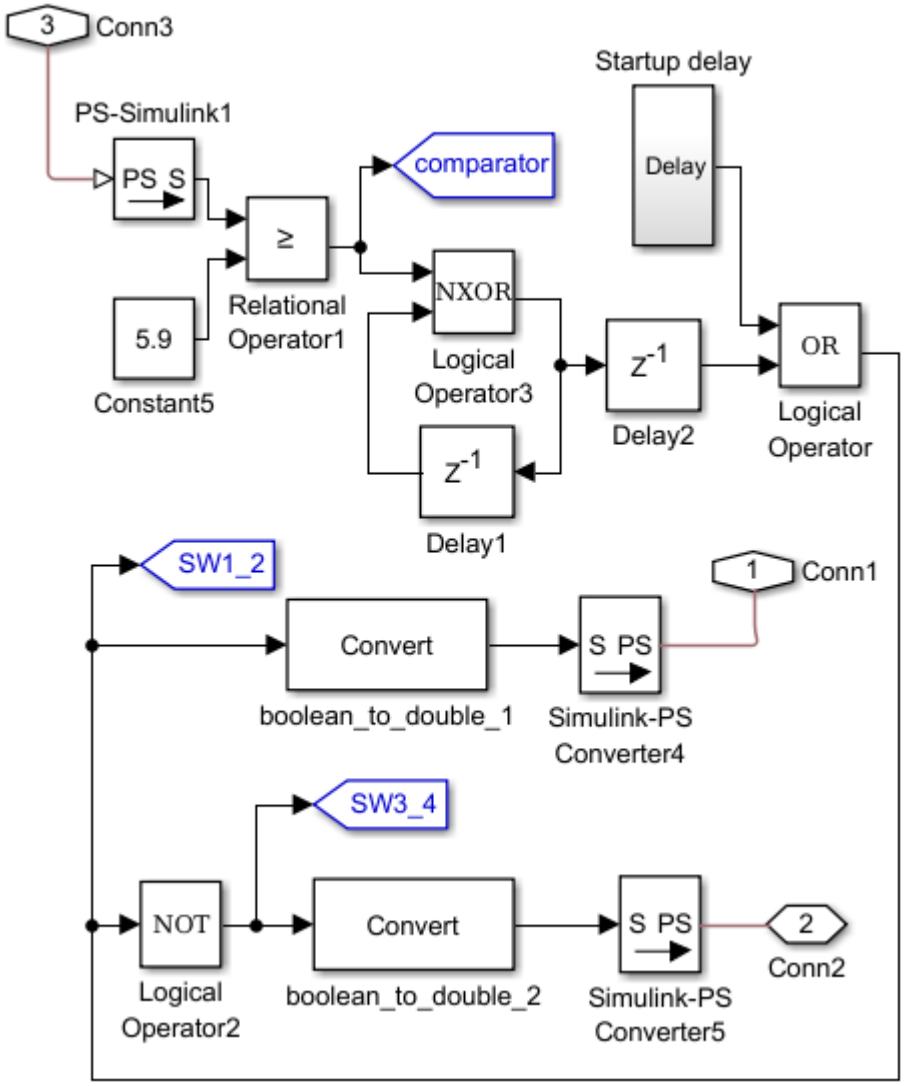
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Logical
Operator3
Startup delay
Delay
OR
Logical
Operator
z^{-1}
Delay2
z^{-1}
Delay1
SW1_2
Convert
boolean_to_double_1
S PS
Simulink-PS
Converter4
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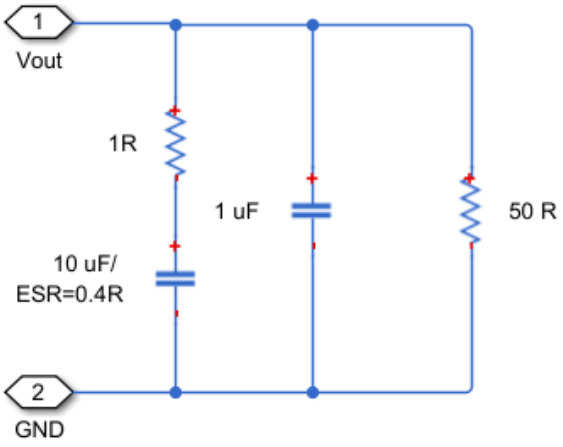
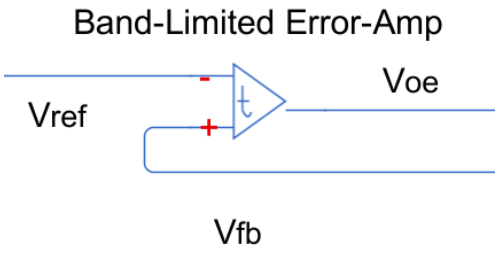
Conn1
SW3_4
NOT
Logical
Operator2
Convert
boolean_to_double_2
S PS
Simulink-PS
Converter5
2
Conn2

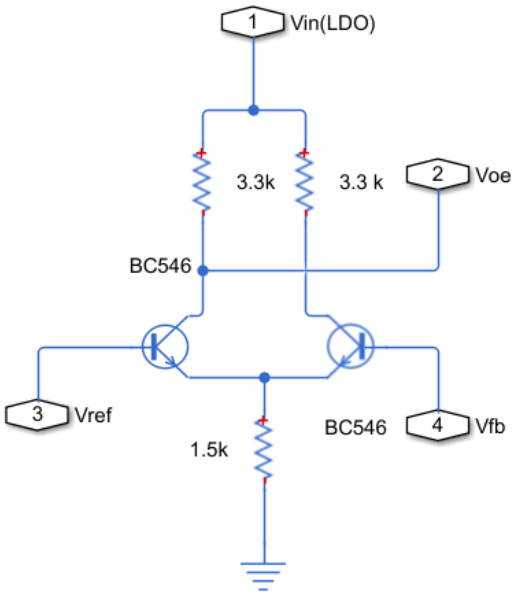
(c)


1
Vout
1R
1 uF
50 R
10 uF/
ESR=0.4R
2
GND

(d)



(e)



(f)

Figure 4-5: The simulation model of the SCALDO Regulator: (a) Compacted model, (b) Switching Network, (c) Logic circuit (MCU) (d) Output impedance (z_o), (e) first-order model of the error amplifier, (f) high-frequency model of the error amplifier.

The simulation framework of the SCALDO regulator is developed in the MATLAB Simulink environment. The block diagram of the Simulink model is displayed in Figure 4-5. The parameters of the Simulink blocks of the discrete SCALDO prototype are defined by using the datasheet specifications of the circuit components.

The control unit displayed by the MCU subsystem in Figure 4-5 (b) controls the four switches based on the SCALDO algorithm. The logic circuit of this controller is displayed in Figure 4-5 (c). Two delay blocks (Delay1 and Delay2) are introduced to avoid the algebraic loops when doing the simulation.

The output impedance of the SCALDO regulator is composed of the output capacitor (10 μF), the external ESR resistor (1 Ω), the 1μF bypass capacitor, and the load

resistor. The resistance of the load is changed to adjust the output current of the SCALDO regulator for simulations. Two blocks are developed for the error amplifier: first-order model and high-frequency model. These two blocks are used separately for the simulations, and further details are given in the next section.

4.4.1 Simulated open-loop response

The open-loop frequency response of the SCALDO regulator is obtained by using the linear analysis of the Control System Toolbox in MATLAB Simulink. The input perturbations are fed at the reference voltage source (2.5 V), and the loop is broken at the output of the feedback network as shown in Figure 4-5 (a).

The open-loop response is found for two different cases. First, the observations are taken by using the first-order model of the error amplifier as shown in Figure 4-5 (e). This process is done by replacing the BJT differential pair with a band-limited error amplifier block. The gain and the pole of this simplified first-order model are defined as 25.1 dB and 536 kHz, respectively. The main reason for the use of this first-order model is to avoid complexity. It also helps to visualise the high-frequency poles and zeros of the SCALDO regulator without interference with the high-frequency poles and zeros of the error amplifier. Second, the complete circuit model of the error amplifier (See Figure 4-5 (f)) is used to obtain the open-loop response which includes the high-frequency poles and zeros of the error amplifier.

The simulated open-loop response of the SCALDO regulator for the first-order model of the error amplifier is depicted in Figure 4-6. This simulation is done by setting the equivalent resistance of the switching network to its nominal value (R_{in} = 190 mΩ).

As shown in this diagram, the UGFs for 5 mA, 50 mA, 100 mA and 200 mA occur at about 13 kHz, 27 kHz, 33 kHz, and 41 kHz, respectively. The corresponding phase margins for these load currents are 64.5°, 67.9°, 68.4°, and 68.6°, respectively. Since the phase margins are greater than 45°, the simulated results verify the selection of the stable ESR (1.4 Ω) of the output capacitor. Interestingly, the UGFs and the phase margins are close to the calculated results in Figure 4-3.

Moreover, Figure 4-6 shows the presence of two low-frequency poles and one low-frequency zero in the Bode diagram (see Table 4-5 for the exact values of the

frequencies). The pole due to the decoupling capacitor falls between 135 kHz and 180 kHz. The error amplifier pole occurs at about 538 kHz. Two high-frequency zeros are also visible, and one is a right-hand-plane zero. Besides, one high-frequency pole can be seen in this frequency response graph. Therefore, this simulation matches with the poles and zeros defined in (3-37).

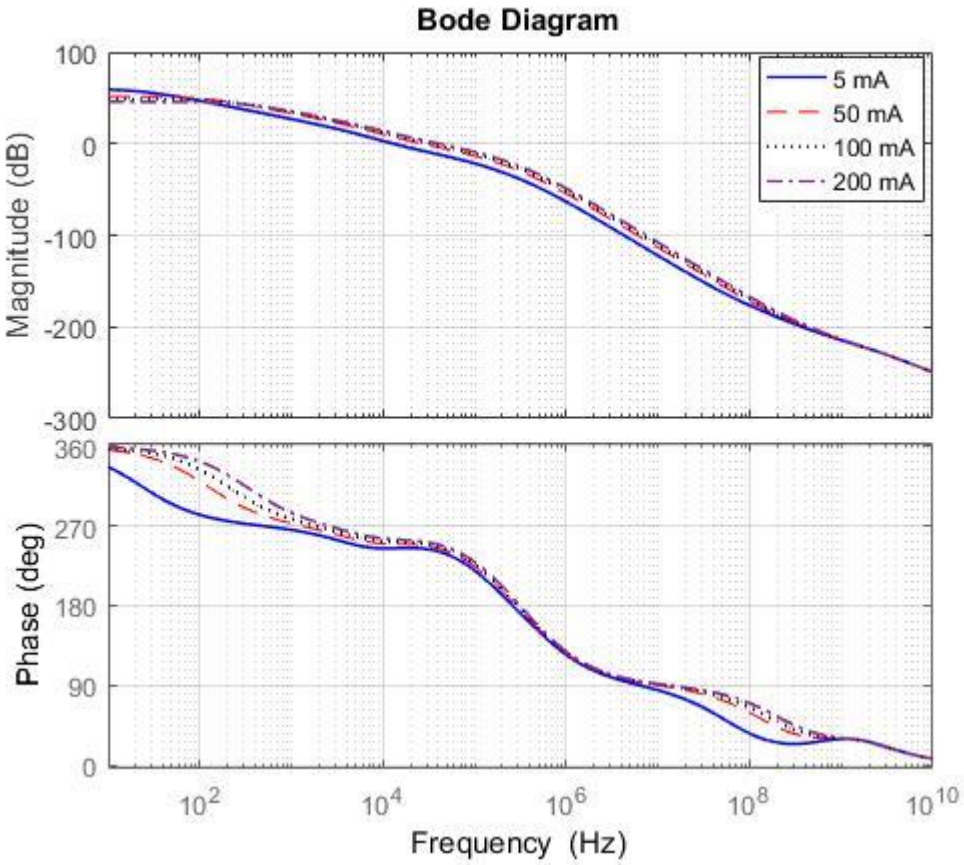


Figure 4-6: Simulated phase and gain behaviour of the SCALDO regulator for the first-order model of the error amplifier.

Secondly, the open-loop response of the SCALDO regulator is simulated by using the high-frequency model of the error amplifier (BJT differential pair). The simulated results of this case are provided in Figure 4-7. In this simulation, the high-frequency poles and zeros of the error amplifier also fall with the poles and zeros of the SCALDO regulator.

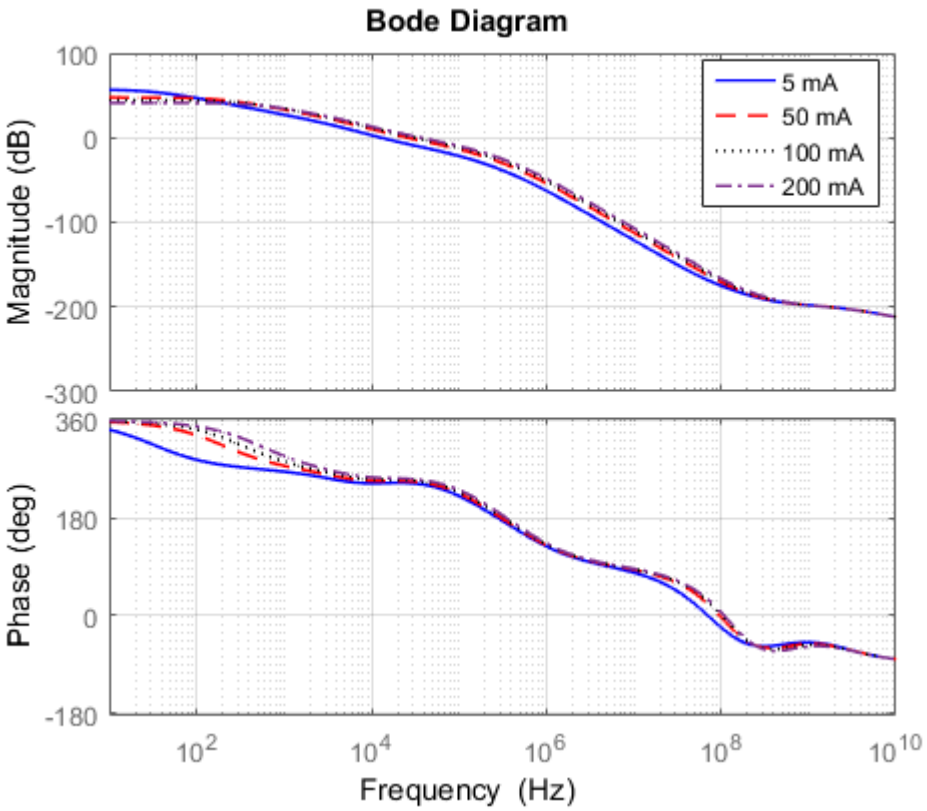


Figure 4-7: Simulated phase and gain behaviour of the SCALDO regulator for the high-frequency model of the error amplifier.

4.4.2 Simulated pole-zero frequencies

The SCALDO regulator is further simulated with the high-frequency model of the error amplifier for different values of the ESR by varying the value of R_{cn} resistor. The frequencies of the poles and zeros, the DC gain, and the phase margins are shown in Table 4-5.

The simulated results, as shown in Table 4-5, indicate that the DC gain, poles, and zeros fall within the calculated boundary values. These simulated results further reveal that the frequencies of ω_{z2}, $\omega_{z3,}$ and ω_{p4} decrease when the equivalent resistance of the switching network is increased for a given load current. This pattern agrees with the theoretical derivations. Besides, ω_{z2}, $\omega_{z3,}$ and ω_{p4} occur at relatively high frequencies compared to the other poles and zeros.

When the low-frequency poles are considered it can be seen that ω_{p1} decreases with the value of R_{in}. On the other hand, ω_{p2} increases when R_{in} rises. The frequency of the first zero (ω_{z1}) and the error amplifier low-frequency pole are independent of R_{in}.

Table 4-5: Simulated pole-zero frequencies against the equivalent resistance of the switching network

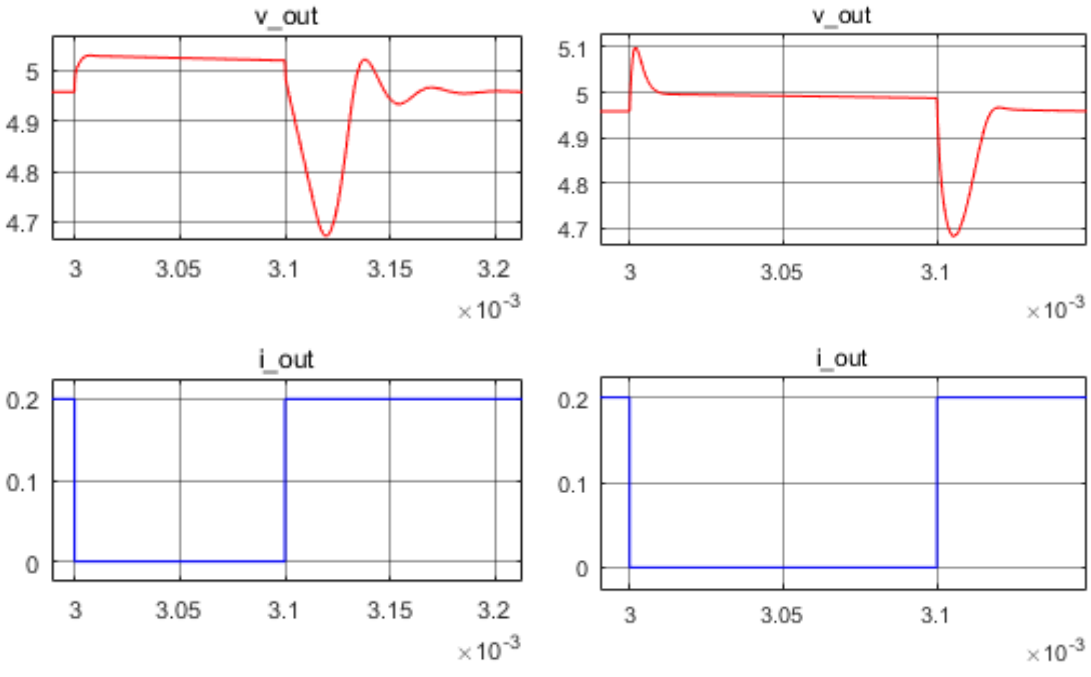
Pole/ zero	**Load current = 5 mA**				**Load current = 100 mA**				**Load current = 200 mA**			
	equivalent resistance of the switching network (Ω)				**equivalent resistance of the switching network (Ω)**				**equivalent resistance of the switching network (Ω)**			
	0.19	**0.29**	**0.39**	**0.49**	**0.19**	**0.29**	**0.39**	**0.49**	**0.19**	**0.29**	**0.39**	**0.49**
A_{DC} (dB)	57	57	57	57	44.4	44.4	44.4	44.4	41.2	41.2	41.2	41.2
ω_{z1} (kHz)	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4
ω_{z2} (MHz)	61.2	58.2	55.6	51.37	189.6	168.59	152.8	140.5	239.1	208.25	185.88	168.75
ω_{z3} (MHz)	781.5	556.99	440.56	320.74	1018	775.43	645.77	564.3	1132	879.6	743.0	656.57
ω_{p1} (Hz)	22.34	22.01	21.69	21.10	196.0	188.45	181.46	175.25	317.22	304.0	292.0	280.99
ω_{p2} (kHz)	5.38	5.44	5.49	5.61	6.86	7.00	7.15	7.29	7.42	7.58	7.74	7.89
ω_{p3} (kHz)	135.5	135.3	135.3	135.18	168.5	167.33	166.19	165.18	186.98	184.56	182.27	180.25
ω_{p4} (GHz)	2.1081	1.4656	1.1269	0.77568	2.216	1.573	1.235	1.025	2.281	1.638	1.299	1.089
$\omega_{p1(ea)}$ (kHz)	536	536	536	536	536	536	536	536	535	536	536	536
PM (deg)	64.5	64.7	64.9	65.4	68.36	68.69	69.03	69.36	68.64	69.02	69.4	69.77

Although the theoretical frequency of ω_{p3} is independent of R_{in}, the simulations show some small discrepancies. These discrepancies are possible in the simulations since the R_{in} parameter is neglected in the simplification process of (3-34). Therefore, these results match the theoretical analysis and the calculated values.

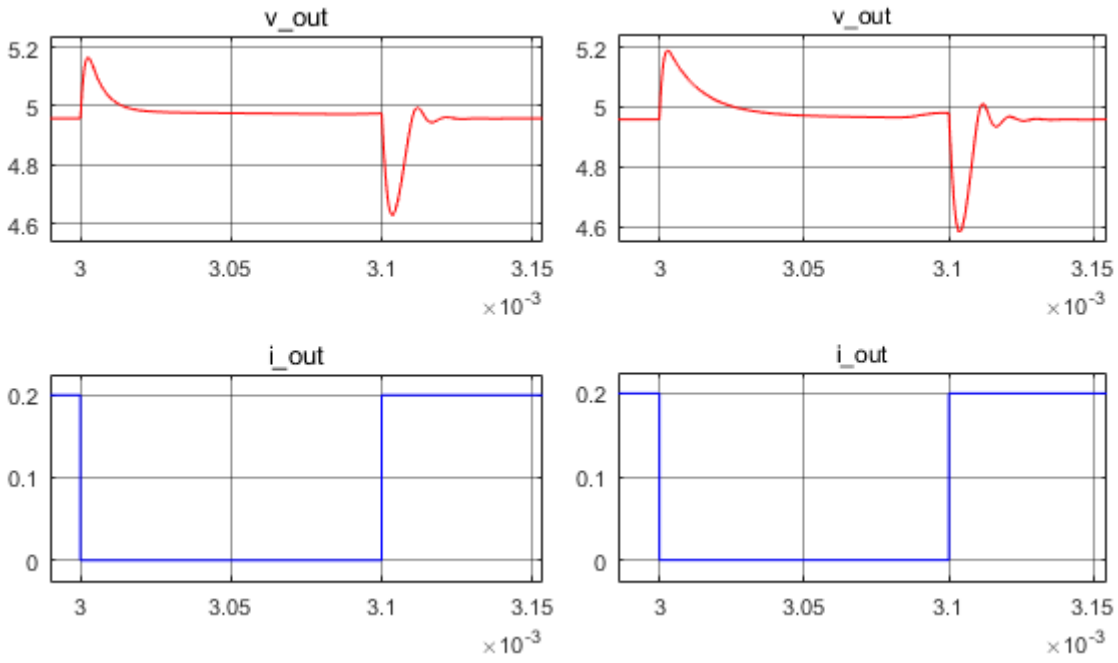
The variation of the phase margin over R_{in} is also minimal. This effect is due to the presence of the switching network dependent high-frequency pole and zeros well beyond the UGF and the cancellation of the effects of ω_{p1} and ω_{p2}.

4.4.3 Simulated load-transient response

The UGF and the phase margin affect the overall transient response of a voltage regulator [66]. Drastic load variations generate a significant change in the output current dependent poles and zeros of a regulator. If the regulator is stable, it will respond to the transient in a smooth and controlled manner. On the other hand, when the regulator is unstable or quasi-stable, the more oscillatory response is produced [66]. Since the frequency compensation method used in this SCALDO prototype design is the output capacitor ESR, the transient load responses are obtained for different values of this ESR, and the results are shown in Figure 4-8. The step load current is changed from 0.005 A to 0.2 A and vice versa. The time axis is shown in seconds (S), and one segment is 50 µS.



(a) (b)



(c) (d)

Figure 4-8: Simulated load-transient response for different ESR values of the output capacitor: (a) R_{ESR} = 0.4 Ω, (b) R_{ESR} = 1.4 Ω, (c) R_{ESR}= 5.4 Ω, (d) R_{ESR}= 10.4 Ω.

Figure 4-8 (a) depicts the regulator response when R_{ESR} is set to 0.4 Ω. This ESR value is less than the lower margin of the calculated stable range. Similarly, subplots (c) and (d) of Figure 4-8 show the transient responses when the ESR is out of the stable upper margin. On the other hand, Figure 4-8 (b) presents the dynamic response when the ESR is set to a stable value (R_{ESR} = 1.4 Ω in this design). The time domain performance characteristics of these simulations are summarised in Table 4-6.

These time domain characteristics show how the output capacitor ESR affects the dynamic behaviour of the SCALDO regulator. The regulator suffers from ringing in the output voltage when the output capacitor ESR is out of the stable region as shown in Figure 4-8 (a), (c), and (d). This effect is mainly due to the low phase margins of the regulator when the ESR of the output capacitor is out of the stable region.

Moreover, the fastest settling time of the output voltage for the rising edge of the load current occurs when the ESR is set a stable value as shown in Table 4-6. The overshoot for the rising edge of the load current is the lowest when the ESR is 1.4 Ω

compared to the other three cases. Therefore, it is apparent from these simulations that a stable value of the output capacitor ESR produces a better transient response.

Table 4-6: Characteristics of the simulated load-transient response

Characteristic	**Equivalent output capacitor ESR (Ω)**			
	0.4	**1.4**	**5.4**	**10.4**
Overshoot (falling edge of the current)	10 mV	100 mV	200 mV	220 mV
Overshoot (rising edge of the current)	-290 mV	-270 mV	-310 mV	-350 mV
Settling time (falling edge of the current)	20 µS	20 µS	30 µS	70 µS
Settling time (rising edge of the current)	110 µS	25 µS	30 µS	35 µS

4.5 Experimental results

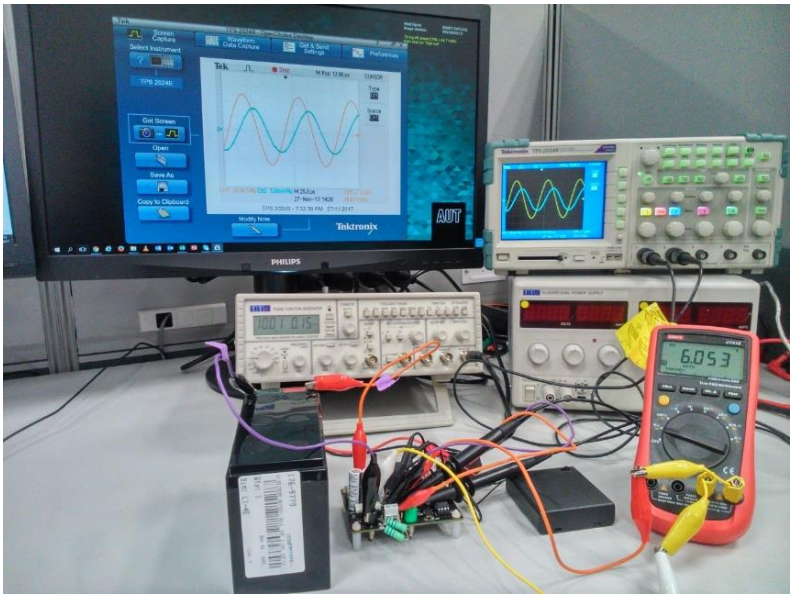


Figure 4-9: The experimental setup of the stability analysis.

The theoretical and simulated results are validated experimentally by using the 12 V to 5 V SCALDO prototype. The experimental setup is displayed in Figure 4-9.

4.5.1 Open-loop measurement

The open-loop gain and phase are observed by injecting a small sinusoidal voltage signal into the feedback network as illustrated in Figure 4-10.

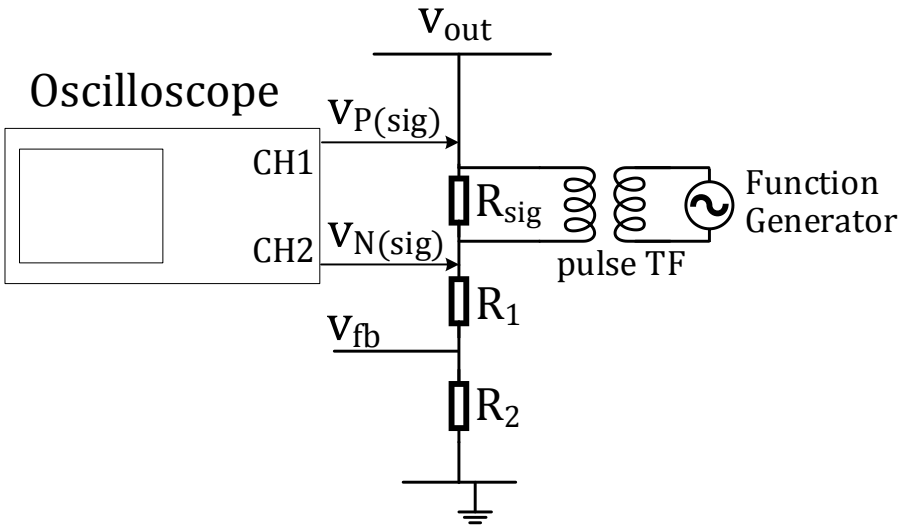


Figure 4-10: The signal injecting method.

This open-loop measurement method is applied to both switch-mode and linear topologies. There are more details available about this approach in [67, 68]. The feedback network is broken at the low impedance output node (v_{out}), and a small resistance (R_{sig}) is added in series with the feedback resistors (R_1 and R_2). In this prototype, the value of R_{sig} is selected as 50 Ω. Since the value of R_{sig} is very small compared to the values of R_1 and R_2, the influence on the output voltage drift is negligible.

The small-signal sinusoidal signals are injected into the R_{sig} resistor by using a function generator. The pulse transformer (pulse TF) provides electrical isolation between the function generator and the SCALDO regulator for DC voltages. The alternating voltage across the R_{sig} resistor is measured with the aid of two channels (CH1: $v_{P(sig)}$ and CH2: $v_{N(sig)}$) of an oscilloscope. The amplitude of the sinusoidal signals is always kept below 50 mV to avoid large-signal behaviour of the regulator. Also, the measured frequencies are narrowed down to a 100 Hz -1 MHz range due to some limitations such as the bandwidth of the pulse transformer and the resolution of the oscilloscope. Even so, the dominant poles and the zero of the

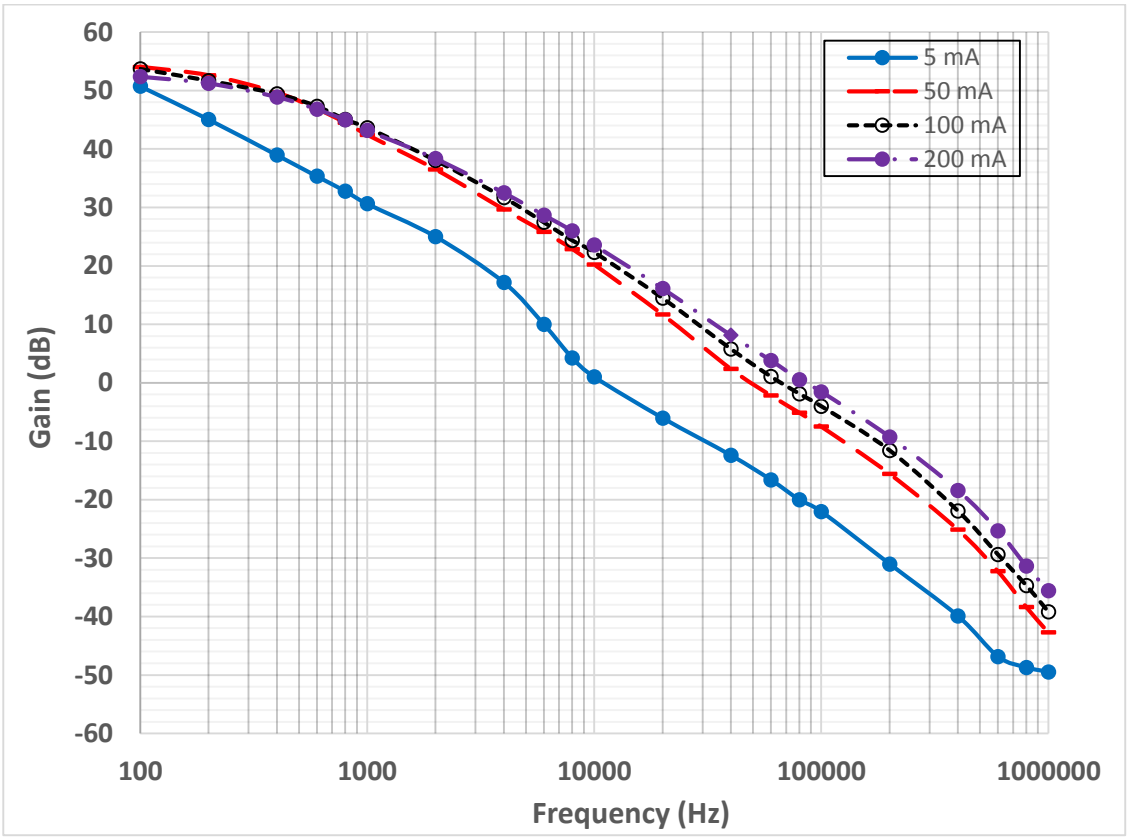
SCALDO regulator fall within this frequency range of interest. The samples of open-loop measurements are given in Appendix C. The open-loop gain and the open-loop phase are calculated according to (4-1) and (4-2), respectively.

$$Gain(dB) = 20\log_{10}\left(v_{P(sig)} - v_{N(sig)}\right) \tag{4-1}$$

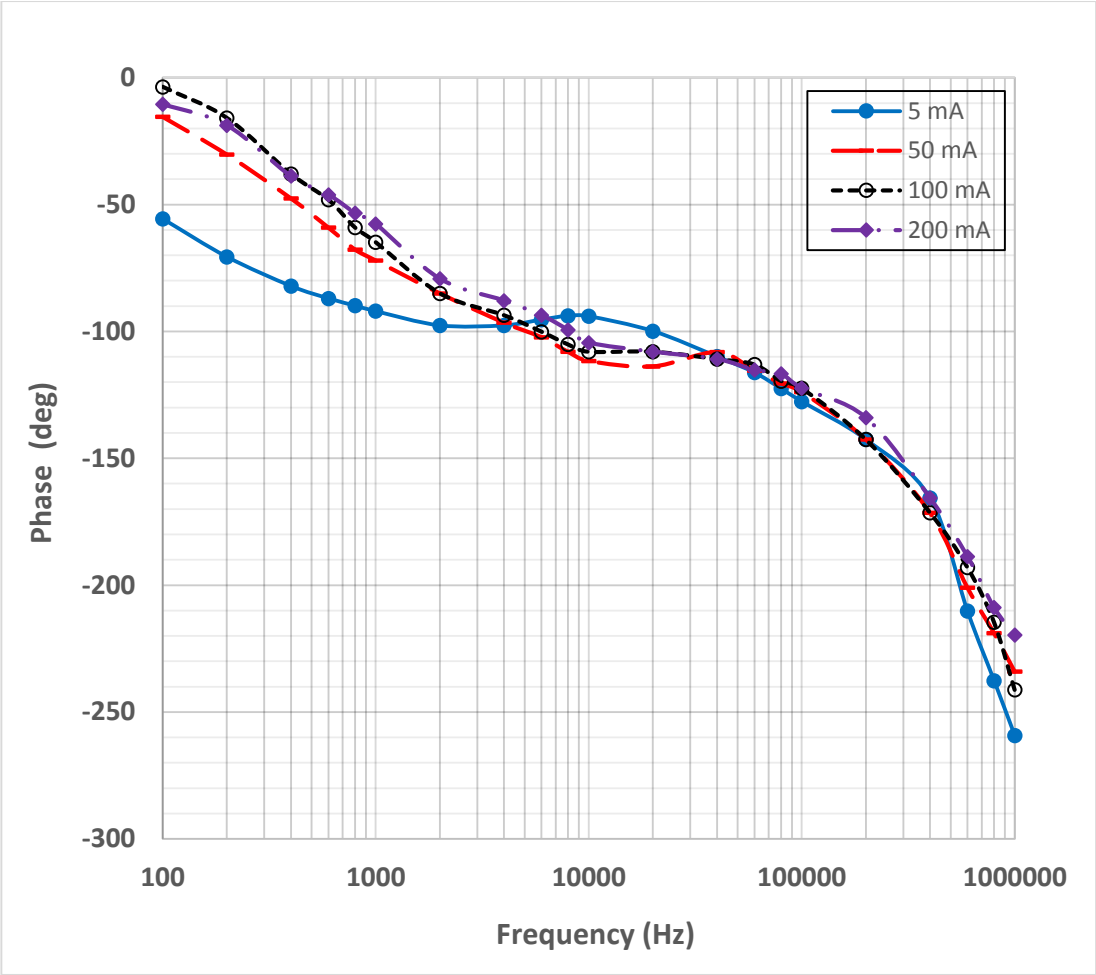
$$Phase(deg) = [(\Delta t)f/360^{\circ}] - 180^{\circ} \tag{4-2}$$

Where; f is the frequency, Δt is the time lag of the two small signals ($v_{P(sig)}$ with respect to $v_{N(sig)}$).

The open-loop response of the SCALDO regulator is displayed in Figure 4-11. According to Figure 4-11, the measured UGFs for 5 mA, 50 mA, 100 mA, and 200 mA, respectively, are around 10 kHz, 50 kHz, 70 kHz and 90 kHz. The corresponding phase margins for these load currents are 86°, 68°, 65° and 62°, respectively. These experimental results show that the SCALDO regulator is highly stable, having a phase margin of over 45°. The frequencies of the open-loop poles and zeros of the SCALDO regulator are extracted from the frequency response curves and listed in Table 4-7.



(a)



(b)

Figure 4-11: Experimental frequency response of the SCALDO regulator: (a) Open-loop gain, (b) Open-loop phase.

Table 4-7: Measured frequencies of open-loop poles and zeros of the SCALDO regulator

Pole/zero	**Frequency**			
	I_{out} = 5 mA	**I_{out} = 50 mA**	**I_{out} = 100 mA**	**I_{out} = 200 mA**
ADC (dB)	> 50.75	54.05	53.70	52.39
ω_{z1} (kHz)	10	20	20	20
ω_{p1} (Hz)	<100	200	250	300
ω_{p2} (kHz)	5	8	9	10
ω_{p3} (kHz)	100	200	200	200
$\omega_{p1(ea)}$ (kHz)	400	400	400	400

It can be seen from this table that the DC gain decreases when the load current is increased. This pattern can be explained with reference to the DC gain defined in (3-38), and it is caused due to the fact that the decrease in the small-signal output resistance (r_{ds}) of the pass device with the rise of the load current [64]. Even though the simulated and calculated frequencies of ω_{z1} are around 11 kHz, the measured values slightly deviate from this value. One factor for these discrepancies may be due to the frequency dependence of the capacitance and the ESR of the multilayer ceramic capacitor [69] used in this prototype.

When the open-loop poles are compared, it can be observed that the frequencies of the low-frequency poles (ω_{p1} and ω_{p2}) increase with the load current and they fall within the calculated margins.

In addition, the third pole (ω_{p3}) and the error amplifier pole ($\omega_{p1(ea)}$) occur at 200 kHz and 400 kHz, respectively. The measured results suggest that ω_{p3} and $\omega_{p1(ea)}$ are independent of the load current as discussed in the theoretical analysis. The frequencies of these two poles are close to the simulated results, and they fall within the calculated margins. The two high-frequency zeros (ω_{z2} and ω_{z3}) and the high-frequency pole (ω_{p4}) are not visible within the measured frequency range.

4.5.2 SCALDO regulator behaviour against the output capacitor ESR

Phase margin variation

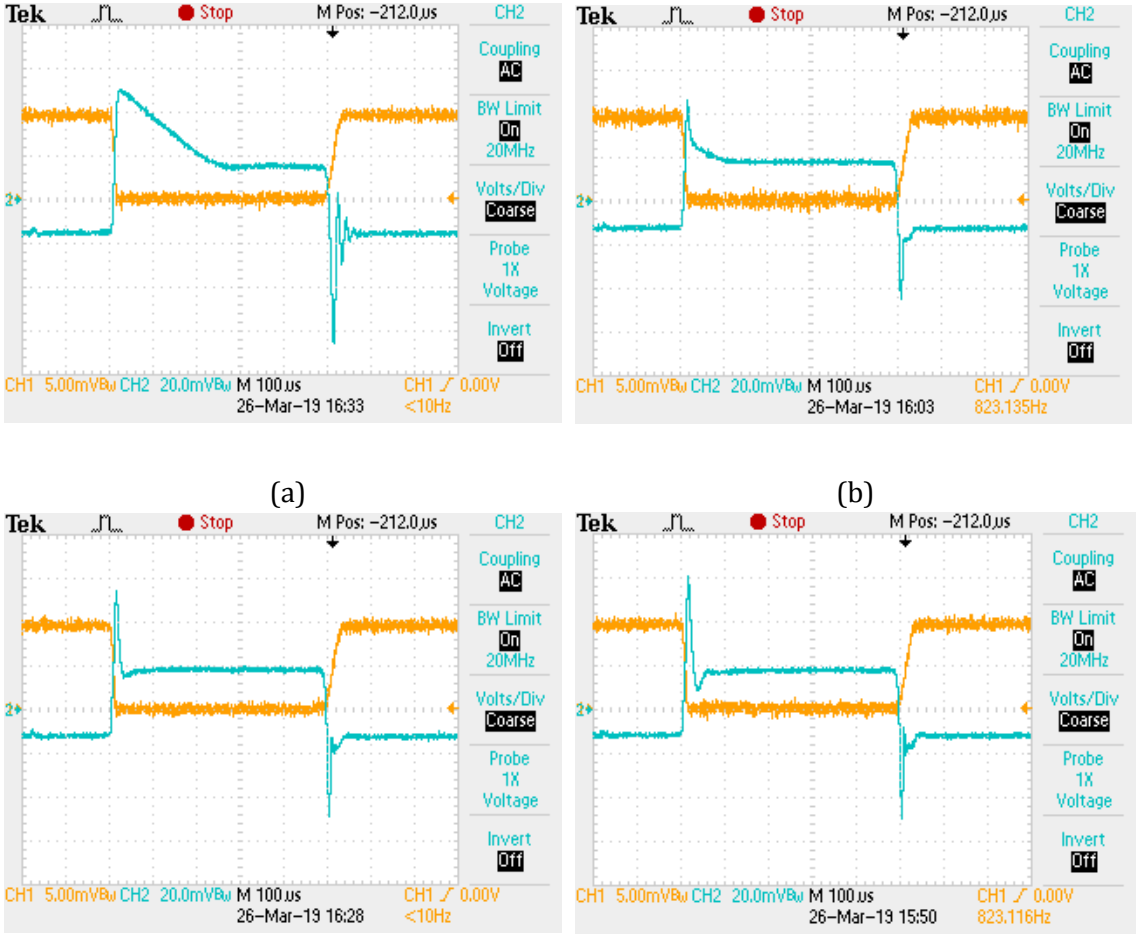
It is apparent from Figure 4-11 that the measured phase margins are well beyond the 45° threshold margin for the selected R_{ESR} value (1.4 Ω). Besides, the phase margins of the prototype are measured against the load current for different values of R_{ESR}. This process is done by replacing the external ESR resistor with different values. The phase margins for several values of the R_{ESR} are provided in Table 4-8.

What is interesting about the data in Table 4-8 is that the higher phase margins are produced when the output capacitor ESR is 1.4 Ω. The phase margins become less than the 45° threshold level when R_{ESR} is out of the stable range (0.4 Ω or 10.4 Ω). Interestingly, 5.4 Ω of ESR can keep the phase margin close to its minimum requirement. Therefore, these practical results match the theoretical derivation of the stable range of the output capacitor ESR shown in Figure 4-2.

Table 4-8: Measured phase margins for different values of the output capacitor ESR.

output capacitor ESR	Phase margin (degrees)			
	I_{out} = 50 mA	I_{out} = 100 mA	I_{out} = 150 mA	I_{out} = 200 mA
0.4	33	25	23	24
1.4	68	65	64	62
5.4	48	48	50	50
10.4	24	28	31	30

Load-transient response



(a) (b)

(c) (d)

CH1 (DC coupling): Load current waveform (ratio: 1mV→20 mA),

CH2 (AC coupling): Output voltage waveform

Figure 4-12: Experimental load-transient response for different ESR values of the output capacitor: (a) R_{ESR} = 0.4 Ω, (b) R_{ESR} = 1.4 Ω, (c) R_{ESR} = 5.4 Ω, (d) R_{ESR} = 10.4 Ω.

The experimental results related to the load-transient response of the SCALDO regulator are obtained by following the methods described in [40, 41]. A small shunt resistance of 50 mΩ is added between the load and the ground return path of the regulator to observe the transient load current. Figure 4-12 shows the variation of the output voltage of the SCALDO regulator for different values of R_{ESR} when the load is changed from 0.005 A to 0.2 A at a slew rate of 10 mA/μs.

According to Figure 4-12 (b), the ripple amplitude of the output voltage is about 32 mV and 28 mV for the rising edge and the falling edge, respectively when the ESR is 1.4 Ω. Since the measured phase margin is higher than 45° for this stable ESR value, there are almost no oscillations in the output voltages.

Although the fastest settling time for the falling edge of the load current occurs when the ESR = 5.4 Ω, there is some ringing in the output voltage for the rising edge as shown in Figure 4-12 (c). Also, the output voltage ripple is higher compared to Figure 4-12 (b).

Conversely, when the ESR is dropped to 0.4 Ω, the phase margin becomes lower than the 45° threshold level, and the ripple amplitude becomes 52 mV in the rising edge of the step current as shown in Figure 4-12 (a). There are severe oscillations in the output voltage before it settles down to the new value since this ESR is out of the stable range. Also, the slowest settling time is observed in this case compared to the other three graphs.

Similarly, when the ESR is changed to 10.4 Ω which is also a value out of the stable ESR range, the ripple amplitude becomes 44 mV for the falling edge of the step load current. Also, the settling of the loop shows more pronounced ringing in the output voltage in the rising edge of load current.

When the four cases are compared, it is clear that the best performance can be achieved when R_{ESR} is within the stable region. These responses show a good agreement with the calculated results in Figure 4-2 and the simulation results in Figure 4-8.

4.5.3 Regulator behaviour against the equivalent resistance of the switching network

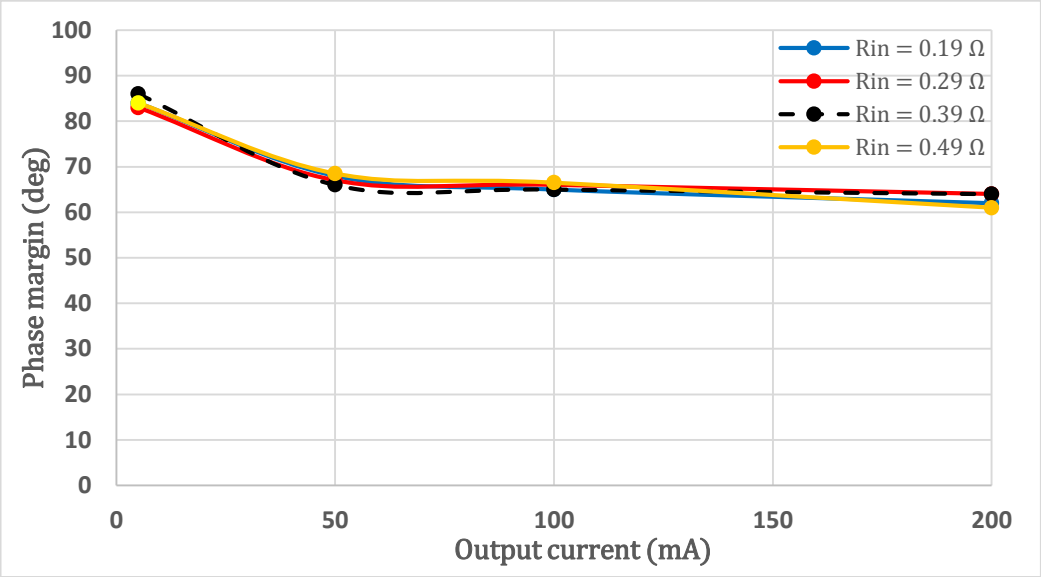
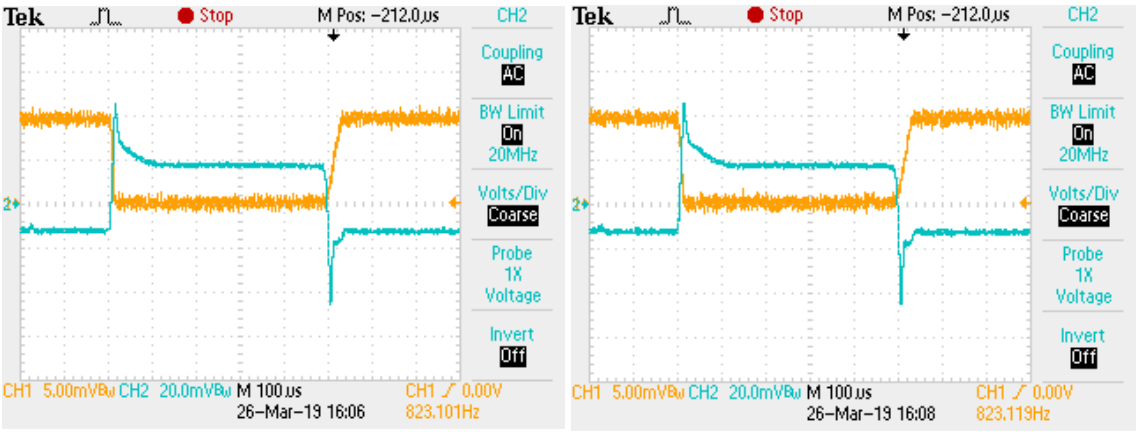


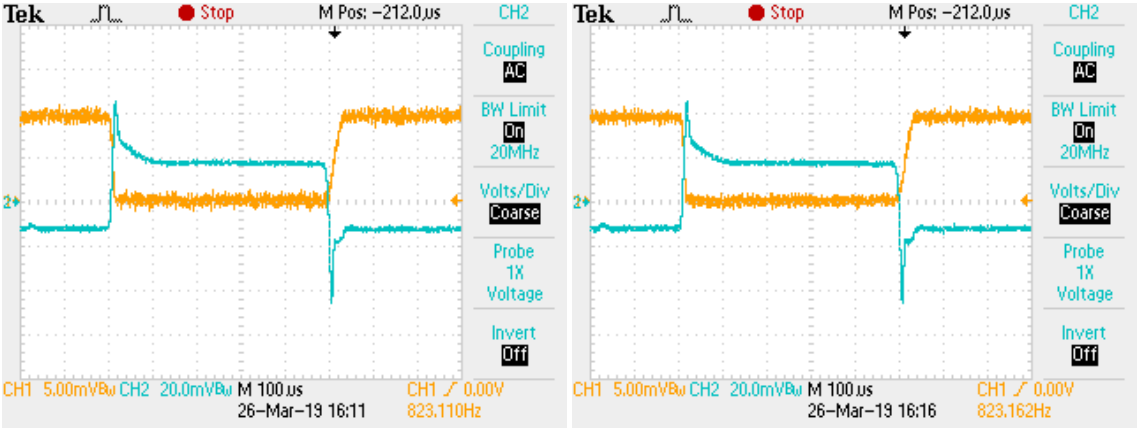
Figure 4-13: The experimental phase margin variation against the equivalent resistance of the switching network.

Figure 4-13 displays the phase margin variation of the SCALDO regulator against the load current for different values of R_{in}. These observations are done by adjusting the value of R_{cn} resistor as discussed in Section 4.3.3.

Figure 4-13 suggests that there is a minimal influence on the phase margin when the equivalent resistance of the switching network is changed between the typical values. These open-loop measurements are further verified by the load-transient results displayed in Figure 4-14.



(a) (b)



(c) (d)

CH1 (DC coupling): Load current waveform (ratio: 1mV→20 mA),

CH2 (AC coupling): Output voltage waveform

Figure 4-14: Load-transient response over equivalent resistance of the switching network: (a) R_{in} = 0.19 Ω, (b) R_{in} = 0.29 Ω, (c) R_{in} = 0.39 Ω, (d) R_{in} = 0.49 Ω.

According to Figure 4-14, there are hardly any changes in the output voltage due to the equivalent resistance of the switching network. Therefore, these results reveal that there is almost no effect on the stability of the SCALDO regulator due to the typical values of the equivalent resistance of the switching network.

4.6 Comparison of the results

4.6.1 Frequencies of the open-loop poles and zeros

The theoretical small-signal model of the SCALDO regulator consists of three zeros and five poles including the error amplifier dominant pole of its first-order model as discussed in Section 3.5. The frequencies of these open-loop poles and zeros are calculated for corner values of the critical circuit parameters and listed in Table 4-4. Similarly, the open-loop poles and zeros extracted from the simulations are displayed in Table 4-5. The simulated results indicate that the number of open-loop poles and zeros matches the theoretical derivations for the first-order model of the error amplifier. Due to practical limitations of the experimental setup, only the low-frequency open-loop poles and zeros could be extracted as shown in Table 4-7. When these three tables are compared, it can be seen that the simulated and experimental poles and zeros fall within the boundaries of the calculated frequency margins.

4.6.2 Effect of the output capacitor ESR on stability

It is shown in Section 3.8 that the selection of the stable range of the output capacitor ESR is crucial to make the SCALDO regulator stable. The calculated values of output capacitor ESR for the stability of this SCALDO prototype are displayed in Figure 4-2. The simulated frequency response in Figure 4-7 suggests that the 12 V to 5 V SCALDO regulator model is stable for the selected ESR value (1.4 Ω) in this design. Also, the experimental results of the open-loop response of the prototype in Figure 4-11 indicate that the regulator is stable having a phase margin over 45° for this ESR value.

Moreover, the simulated load-transient results in Figure 4-8 and the outcomes of the experiment in Figure 4-12 demonstrate the effect of the output capacitor ESR on stability. Also, these results verify the selection of the stable value of the output capacitor ESR for the stability of the SCALDO regulator.

4.6.3 Effect of the resistive parameter of the switching network on stability

The sum of the resistance of the switches and the ESR of the supercapacitor is considered as the equivalent resistance of the switching network (R_{in}) in the SCALDO regulator. This equivalent resistance generates two high-frequency zeros (ω_{z2}, ω_{z3}) and one high-frequency pole (ω_{p4}) in the open-loop transfer function as discussed in Section 3.7. In addition, R_{in} causes discrepancies in the frequencies of the two low-frequency poles (ω_{p1}, ω_{p2}).

Calculated values in Table 4-2 show that ω_{z2}, $\omega_{z3,}$ and ω_{p4} fall at relatively high frequencies for typical values of R_{in} in a SCALDO regulator. These results are further confirmed by the simulated values given in Table 4-5. Besides, both theoretical and simulated values in these two tables show that the frequencies of these high-frequency pole/zeros decrease with the increase of R_{in}. Interestingly, these results further demonstrate that the frequency of one low-frequency pole (ω_{p1}) decreases with the increase of R_{in} while the frequency of the other low-frequency pole (ω_{p2}) increases when R_{in} is raised.

Furthermore, the phase margins are calculated against R_{in} and listed in Table 4-2. These values are compared in Section 4.4.2 with the outcomes from the simulations. This comparison also suggests that there is a minimal influence on the phase margin

due to R_{in}. Also, the experimental values displayed in Figure 4-13 and the load-transient results in Figure 4-14 further support this fact. This small variation in the phase margin is because of the occurrence of ω_{z2}, ω_{z3}, ω_{p4} at high frequencies compared to the UGF and the net zero impact caused by ω_{p1} and ω_{p2} due to the change of R_{in}.

4.7 Discussion

The stability of the SCALDO technique is investigated by developing a 12 V to 5 V discrete regulator. This circuit is composed of a discrete LDO regulator and a supercapacitor circulation network. The frequency compensation of this SCALDO regulator is done by using the ESR of the output capacitor. The range of stable values of the output capacitor ESR is determined to provide at least 45° of phase margin. The open-loop frequency response is obtained theoretically for the selected output capacitor ESR. The worst-case analysis is also performed to ensure that the SCALDO regulator is stable even at the corners of the critical circuit parameters. The calculated results show that the frequencies of poles and zeros due to the SC circulation network occur at relatively high frequencies. Also, it is found that there are some discrepancies in low-frequency poles due to the resistive parameter of the switching network. Interestingly, calculated results suggest that the net effect on the phase margin of the SCALDO regulator is minimal due to the equivalent resistance of the switching network.

The discrete SCALDO regulator is simulated in the MATLAB Simulink environment to observe its frequency and load-transient responses for different values of the output capacitor ESR and the switching network parameters. The simulated frequencies of the open-loop poles and zeros are close to the calculated values. Also, these simulations show that the high-frequency pole and zeros due to the SC circulation network fall well beyond the UGF of the SCALDO regulator and their effect on the phase margin is minimal. The changes in the low-frequency poles against the switching network parameters match with the theoretical derivations. Besides, the simulated results related to the load-transient response demonstrate the influence of the output capacitor ESR on the stability of the SCALDO regulator.

The SCALDO regulator is tested experimentally to obtain the open-loop frequency response. The measured values of the low-frequency poles and zeros are within the

calculated margins. The experimental phase margins and the load-transient responses show how the output capacitor ESR affects the stability of the SCALDO regulator.

In addition, the open-loop and dynamic responses are obtained by changing the equivalent resistance of the switching network of the switching network. These outcomes confirm that there is a less influence on the stability of the SCALDO regulator due to the resistive parameter of the switching network.

Chapter 5 Theoretical Background of the Dual-Output SCALDO Technique

Abstract- This chapter discusses the development of a split-rail DC-DC converter using the fundamental concepts of the SCALDO technique. The potential advantages of this dual-output version are discussed and the conceptual background is described. The circuit topology is explained related to modes of operation and parameters are defined. The major losses are identified and the end-to-end efficiencies at different operating phases are derived.

5.1 Introduction

After the establishment of the SCALDO theory and implementation of various prototypes, further improvements have been considered. This study demonstrates the design of a dual-output DC-DC converter as an extension of the SCALDO research. This concept is also named as the dual-output SCALDO (DO-SCALDO) regulator, and it can be designed to generate dual outputs with the same polarity or with dual-polarity. The preliminary work related to the DO-SCALDO concept is published in [70-73]. Therefore, this chapter and the next chapter exclusively explore the dynamic behaviour, loss estimation, and efficiency advantage along with a quantitative comparison with other well-known split-rail topologies.

Since this research is based on the dual-polarity version, it can fill some gaps related to the limitations of the state-of-the-art split-rail techniques as highlighted in Section 2.7.3. The connected downstream loads can enjoy the low-noise and high slew rate capable output of a LDO regulator. Also, the low-frequency SC circulation approach can reduce the burden of EMI/RFI issues. The same ETEE of a single-stage SCALDO topology is obtained in this DC-DC converter. The potential applications of this dual-output regulator are noise sensitive applications, portable devices, and industrial equipment.

5.2 Dual-polarity SCALDO concept

A negative-rail regulation type LDO regulator (LDO_N) and a positive-rail regulation type LDO regulator (LDO_P) are cascaded to produce dual outputs as shown in Figure 5-1. The output loads and the ground pins of the two LDO regulators create a

virtual ground (GND_V), and it is at a floating voltage with reference to the common ground (GND_{in}) of the circuit. The terminals of the circuit which are connected to GND_V are highlighted in light blue traces. Even though the GND_V varies with time, the generated outputs are regulated and dual-polarity.

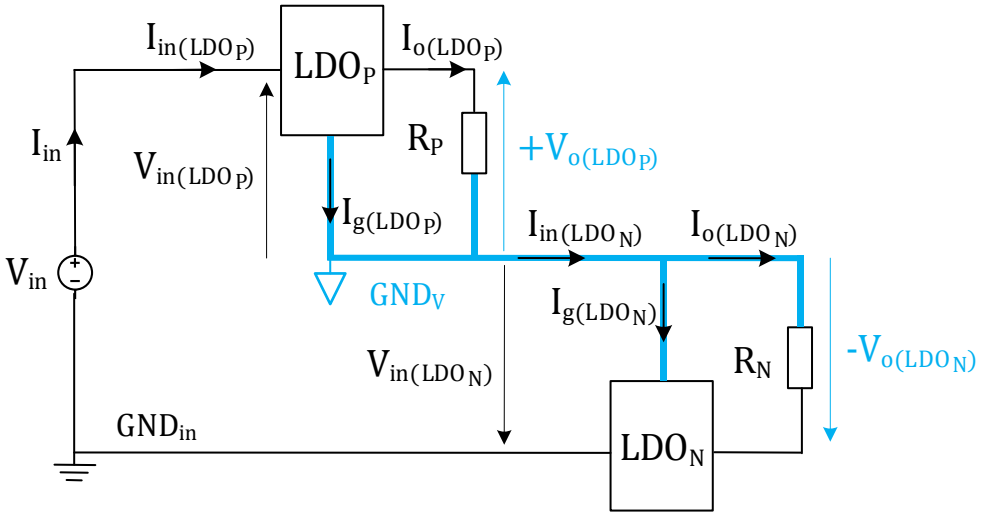


Figure 5-1: Cascaded positive and negative LDO regulators with dual-polarity outputs.

The relationship between the voltage source and the input voltages of the LDO regulators of this circuit is defined in (5-1). Similarly, the current in each node is given in (5-2). The input current of a single LDO regulator is the sum the output current and the ground pin current according to the operation principles [10].

$$V_{in} = V_{in(LDO_P)} + \left|V_{in(LDO_N)}\right| \tag{5-1}$$

$$I_{in} = I_{in(LDO_P)} = I_{o(LDO_P)} + I_{g(LDO_P)} = I_{in(LDO_N)} = I_{o(LDO_N)} + I_{g(LDO_N)} \tag{5-2}$$

Where V_{in}, $V_{in(LDOP)}$, $V_{in(LDON)}$ are the source voltage, the input voltage of the positive LDO regulator and the input voltage of the negative LDO regulator, respectively. Similarly, I_{in} is the source current, and $I_{in(LDOP)}$, $I_{o(LDOP)}$, $I_{g(LDOP)}$ are the input current, the output current, and the ground pin current of the positive LDO regulator, respectively. The currents of the negative LDO regulator are marked by using the same notation and with the N subscript.

The source voltage should be greater than the summation of the minimum input voltages of the two LDO regulators to maintain the regulation of the circuit as defined in (5-3).

$$V_{in} > V_{\min(LDO_p)} + \left|V_{\min(LDO_N)}\right| \quad (5\text{-}3)$$

Where; $V_{min(LDO_P)}$ is the minimum working voltage of the positive LDO regulator, and $V_{min(LDO_N)}$ is the minimum input voltage of the negative LDO regulator.

Equation (5-2) shows that the sum of the ground pin current and the load current of LDO_P should be equal to the sum of the ground pin current and the load current and of LDO_N. Since the ground pin currents of well-designed LDO regulators are very small [31, 32], the regulation is continued if and only if their output currents are equal. Due to this reason, the regulation is not possible when the loads are unbalanced. A voltage-balancing circuit can simply solve this issue [18, 21, 27]. These circuits typically change the effective resistance of each output rail and create a path to pass the excess current due to the unbalanced loads. Thus, it will reduce the overall efficiency due to the energy loss in the path where the excess current flows. As a better approach, the SCALDO technique can be used to solve this issue without degrading the efficiency of the circuit. The cascaded LDO regulators with the SCALDO method are illustrated in Figure 5-2.

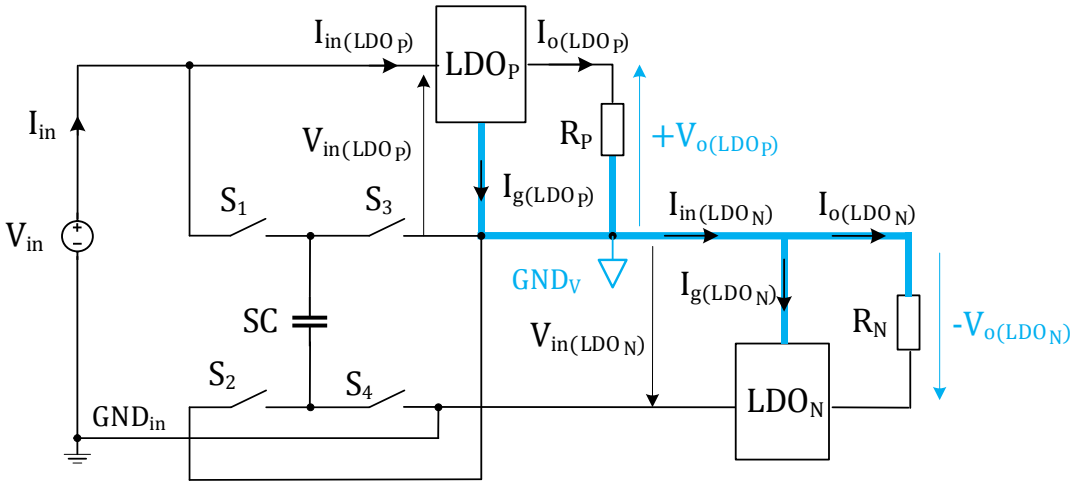


Figure 5-2: The cascaded dual LDO regulators with the SCALDO approach.

Once the SCALDO technique is integrated into the cascaded dual LDO regulators, the SC can be used as a lossless element to control the differential load current. In one phase of the circuit operation, the SC charges, allowing the differential current to pass through it. In the next cycle, the stored energy of the SC is delivered back to the circuit.

The following design constraints are chosen in the proposed dual-output DC-DC converter.

- The output voltages of the positive and negative LDO regulators should have equal magnitudes.

$$V_{o(LDO_P)} = \left|V_{o(LDO_N)}\right| \tag{5-4}$$

- The minimum working voltages of the two LDO regulators should be equal in magnitude as per (5-5).

$$V_{\min(LDO_p)} = \left|V_{\min(LDO_N)}\right| = V_{\min} \tag{5-5}$$

- The source voltage should be higher than twice the minimum operating voltage of the LDO regulators as defined in (5-6). This condition is derived from (5-3) and (5-5).

$$V_{in} > 2V_{\min} \tag{5-6}$$

- The SC should be rated to work under the maximum operating voltage as shown in (5-7).

$$V_{SC(\max)} \geq V_{in} - V_{\min} \tag{5-7}$$

Where; $V_{SC(max)}$ is the maximum voltage that the SC can withstand in the proposed DC-DC converter.

5.3 Operational modes of the DO-SCALDO technique

The DO-SCALDO method works based on four operating modes.

- Phase 1: Initial charging process.
- Phase 2: Output current of LDO_P is greater than the output current of LDO_N ($I_{o(LDO_P)} > I_{o(LDO_N)}$).
- Phase 3: Output current of LDO_P is lower than the output current of LDO_N ($I_{o(LDO_P)} < I_{o(LDO_N)}$).
- Phase 4: Two LDO regulators have equal output currents ($I_{o(LDO_P)} = I_{o(LDO_N)}$).

5.3.1 Phase 1: Initial charging process

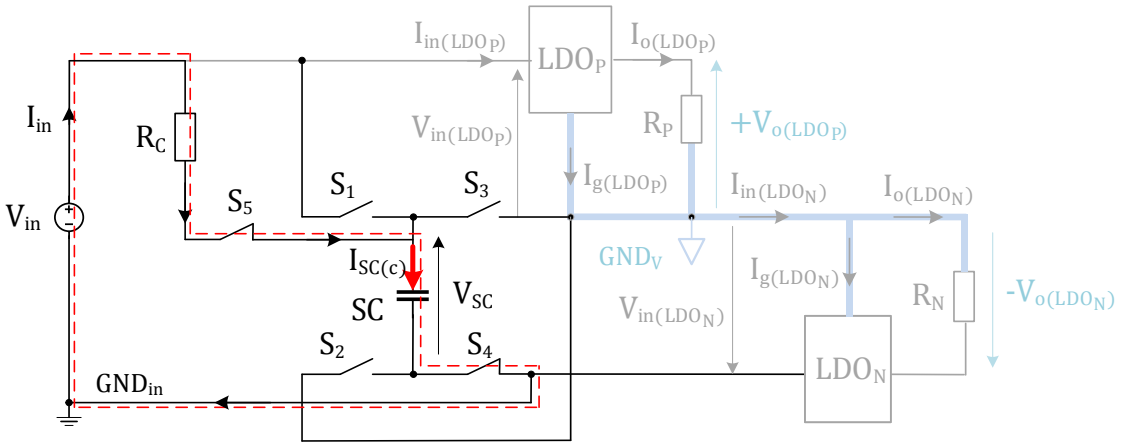
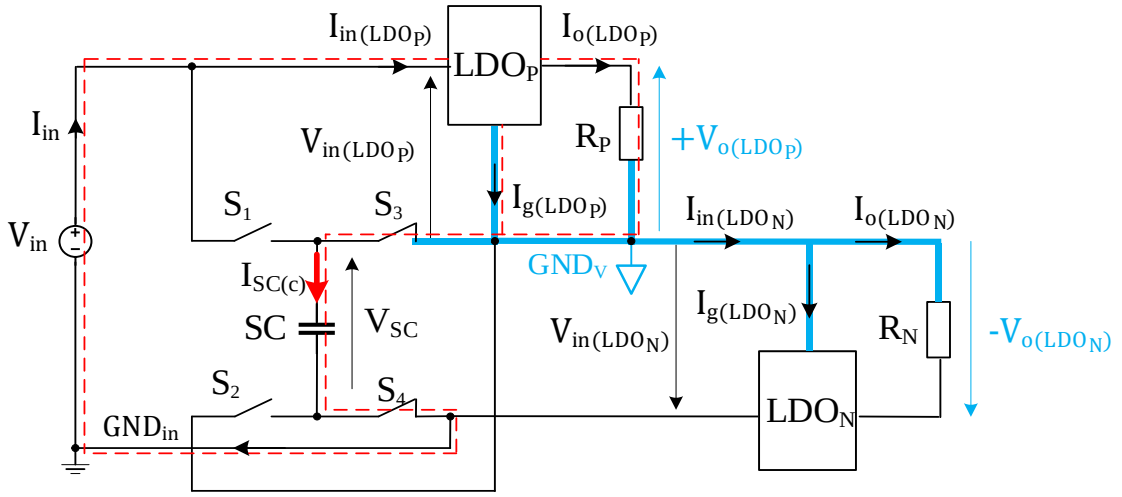


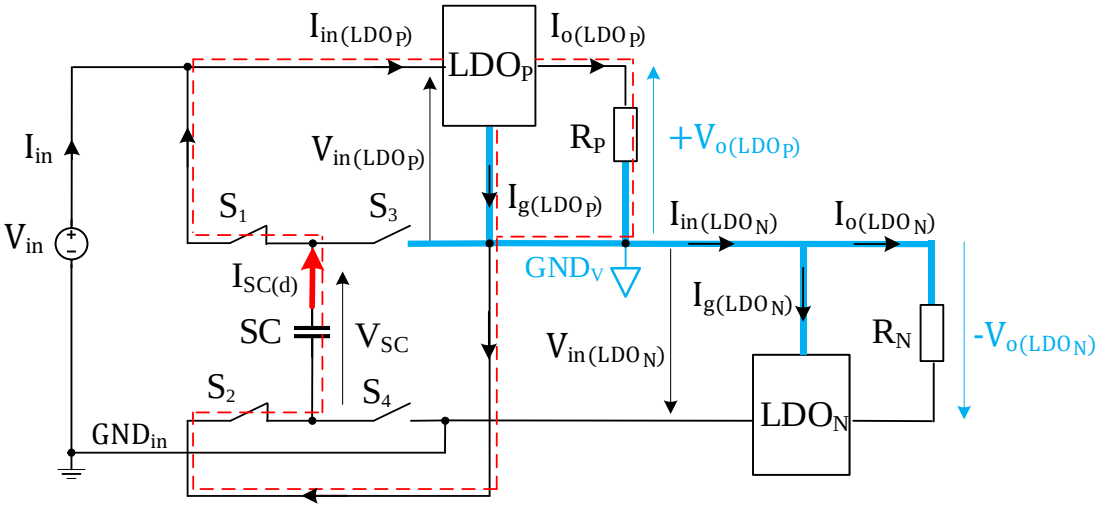
Figure 5-3: Initial charging process.

At the very beginning of the power-up of the circuit, the SC is charged to bring its voltage slightly higher than V_{min}. This initial charging process is done by using the charge-control resistor (R_C) as depicted in Figure 5-3. The switches S_4 and S_5 are closed, and all the other switches are opened to pass the charging current ($I_{SC(c)}$) through the SC. Besides, the two LDO regulators are turned off and the loads are isolated from the source to avoid oscillations in the supply voltage. The initial charging time of the SC is mainly determined by the source voltage, the R_C resistor, and the capacitance of the SC. Once the charging process is completed, the SC can be switched to one of the inputs of the two LDO regulators. Then the other circuit modes are activated by turning on the LDO regulators.

5.3.2 Phase 2: ($I_{o(LDO_P)} > I_{o(LDO_N)}$)



(a)



(b)

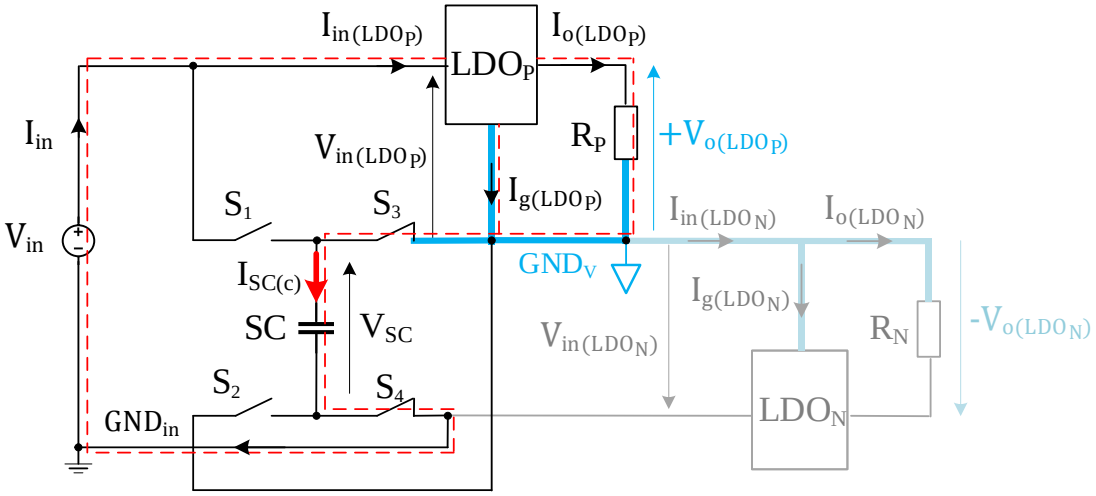
Figure 5-4: DO-SCALDO circuit operation in phase 2: (a) charging cycle (b) discharging cycle.

A differential current of $I_{o(LDO_P)}$ - $I_{o(LDO_N)}$ is created due to the effect of the unbalanced loads in phase 2, and it is handled by the charge balance method of the SC. The switches S_3 and S_4 are closed, and S_1 and S_2 are opened to connect the SC and LDO_N in parallel in the charging phase as shown in Figure 5-4 (a). The path of the differential current (which is the same as the charging current of the SC) is illustrated by the segmented lines. The source current turns to $I_{o(LDO_P)}$ during this period. If the approximate initial voltage of the SC is V_{min}, the input voltage of LDO_N ($V_{in(LDO_N)}$) rises from V_{min}. At the same time, the input voltage of LDO_P ($V_{in(LDO_P)}$) descends from V_{in}-V_{min}. The SC is kept in parallel to LDO_N until $V_{in(LDO_P)}$ drops to V_{min}. The SC voltage (V_{SC}) at the end of the charging phase is approximately V_{in}-V_{min}.

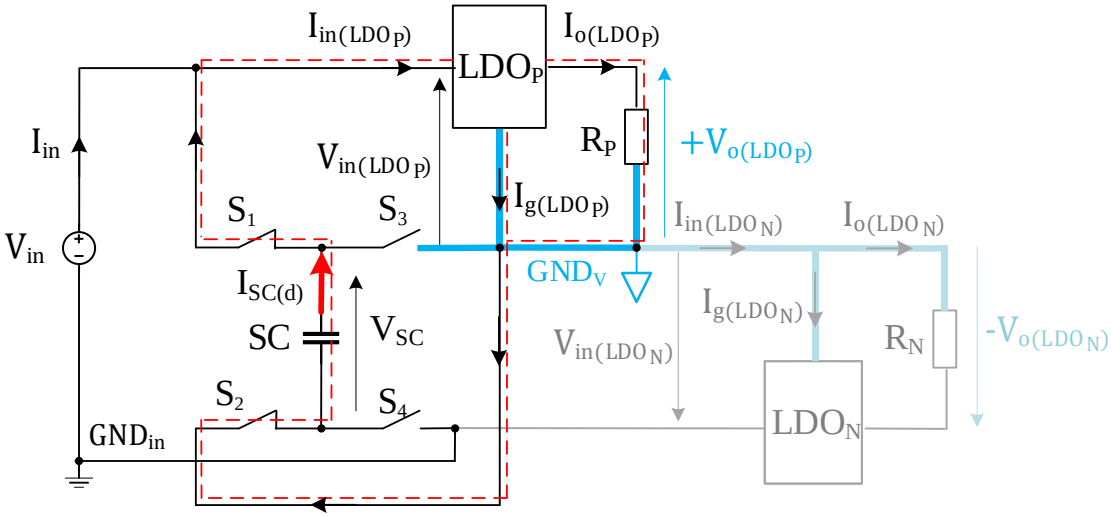
When the charging cycle is completed, the SC is disconnected from the input of LDO_N, and connected in parallel with LDO_P. Since the differential load current is supplied by the discharging process of the SC (as shown in Figure 5-4 (b)), the source current falls to $I_{o(LDO_N)}$ during this period. This process is stopped when $V_{in(LDO_P)}$ reaches V_{min}. These charging and discharging processes are continued until the $I_{o(LDO_P)} > I_{o(LDO_N)}$ condition is satisfied.

The circuit operation of phase 2 falls into a special scenario if $I_{o(LDO_N)}$ becomes zero. Theoretically, LDO_N can be considered as OFF. The circuit operation in this situation is displayed in Figure 5-5 (a) and (b). The SC, LDO_P, and the power source are connected in series in the charging phase as shown in Figure 5-5 (a). The differential

load current approximately becomes $I_{o(LDO_P)}$. Even though the input source is connected to the circuit in the discharging phase (shown in Figure 5-5 (b)), its current drops to zero as the SC delivers the required current to LDO_P. Therefore, this situation is similar to the operation of the basic SCALDO regulator.



(a)



(b)

Figure 5-5: Basic SCALDO operation when the LDO_N is OFF: (a) charging cycle (b) discharging cycle.

5.3.3 Phase 3: ($I_{o(LDO_P)} < I_{o(LDO_N)}$)

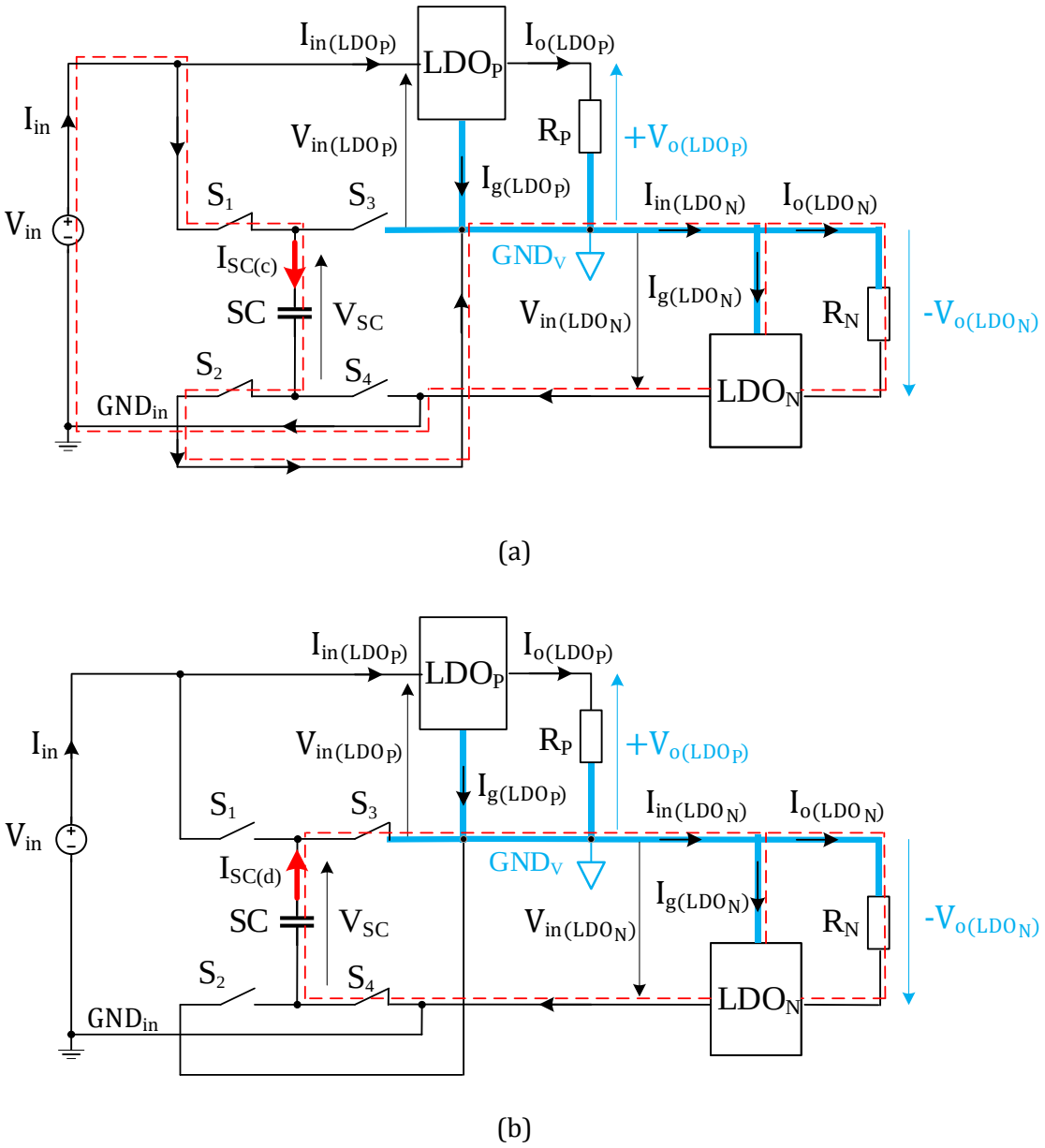
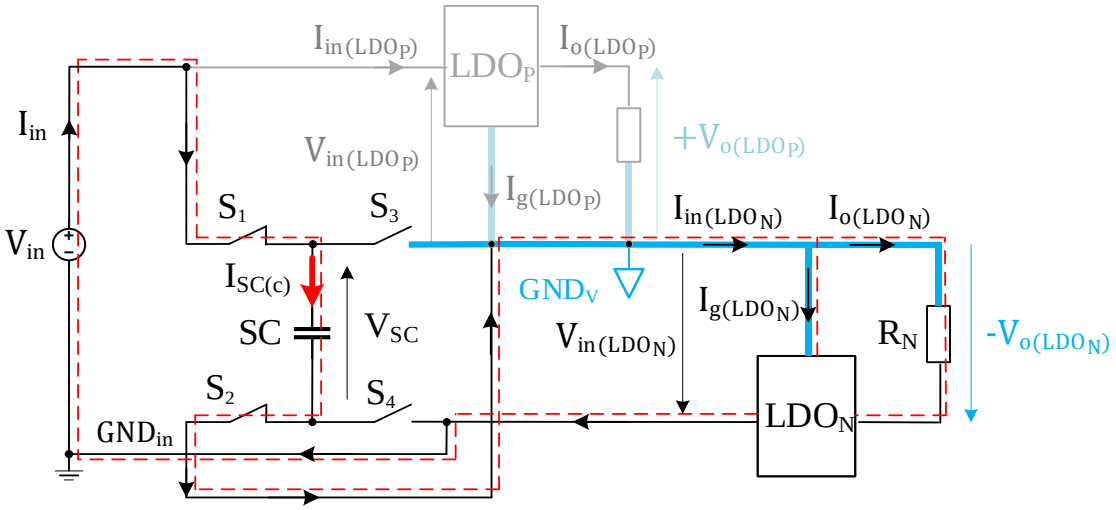


Figure 5-6: DO-SCALDO circuit operation in phase 3: (a) charging cycle (b) discharging cycle.

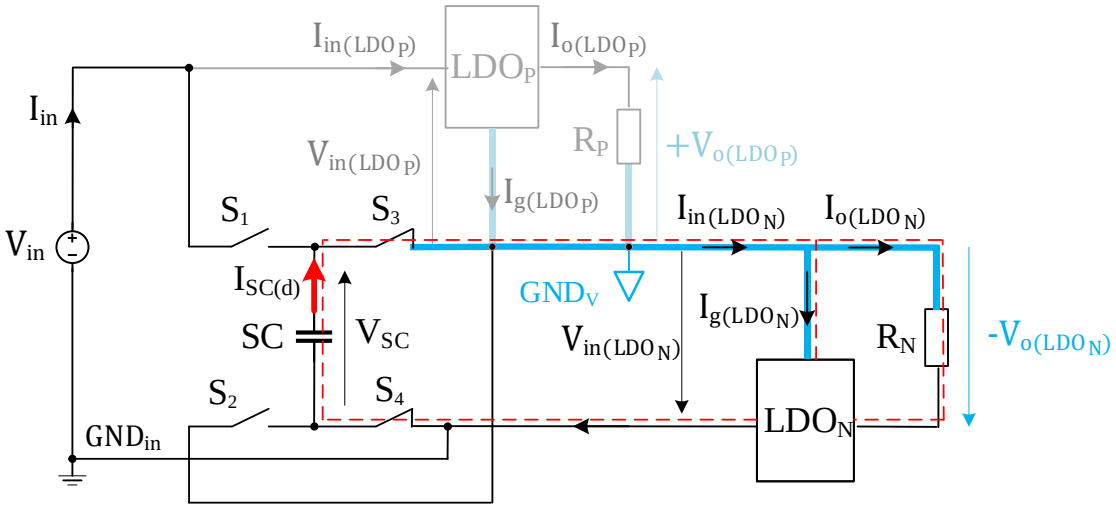
When $I_{o(LDO_P)} < I_{o(LDO_N)}$, the differential load current becomes $I_{o(LDO_N)} - I_{o(LDO_P)}$. In the charging phase, the SC and the LDO_P are in parallel, and the excess current is passed through the SC as depicted by the dashed lines in Figure 5-6 (a). Only the switches S_1 and S_2 are closed during this period. $V_{in(LDO_P)}$ ascends from the V_{min} value, $V_{in(LDO_N)}$ descends from V_{in}-V_{min}, and the source current turns to $I_{o(LDO_N)}$. The charging cycle is terminated when $V_{in(LDO_N)}$ drops to V_{min}. After that, the SC is disconnected from the current position and connected in parallel to LDO_N by closing the switches S_3 and S_4 as shown in Figure 5-6 (b). The source current falls to $I_{o(LDO_P)}$,

and the differential current is provided by the stored energy of the SC during this period. This processed is finished when $V_{in(LDO_N)}$ falls back to V_{min}.

LDO_P falls to the OFF state when its load current drops to zero while keeping the $I_{o(LDO_P)} < I_{o(LDO_N)}$ condition true. This situation is identical to the basic SCALDO approach where a negative-rail regulator is now in operation as illustrated in Figure 5-7 (a) and (b).



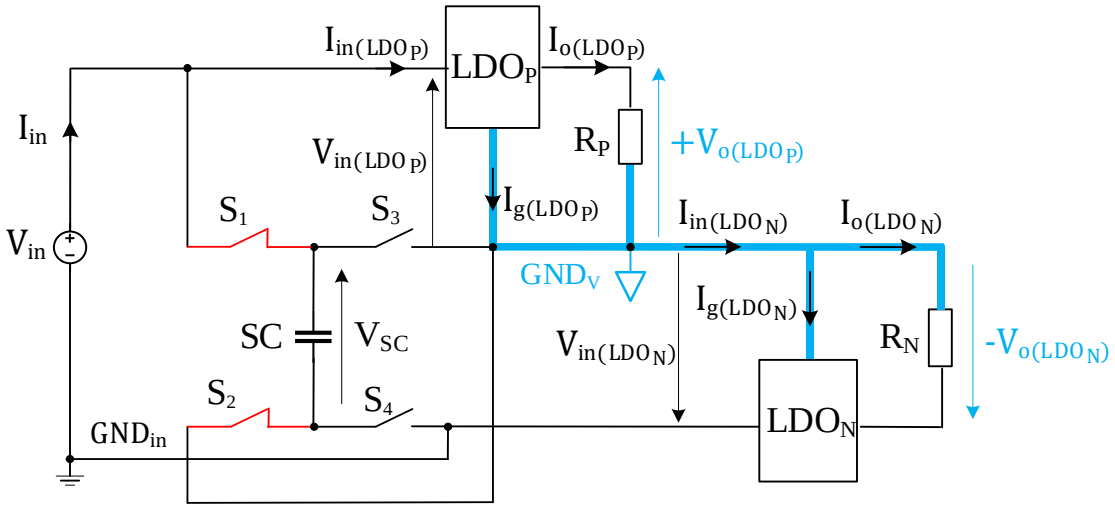
(a)



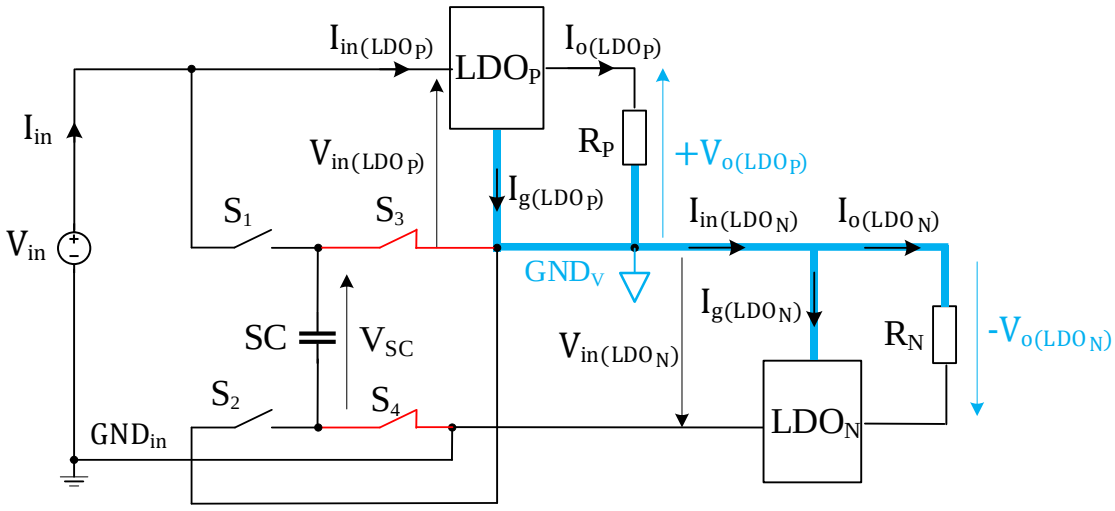
(b)

Figure 5-7: Basic SCALDO operation when the LDO_P is inactive; (a): SC charging phase (b): SC discharging phase.

5.3.4 Phase 4: ($I_{o(LDO_P)} = I_{o(LDO_N)}$)



(a)



(b)

Figure 5-8: DO-SCALDO circuit operation in phase 4 (a) SC is in parallel to the LDO_P (b) SC is in parallel to the LDO_N.

When the load currents become equal, the SC current falls to zero, and the source current is directly passed through the LDO regulators ($I_{in} \approx I_{o(LDO_P)} \approx I_{o(LDO_N)}$). The SC can be placed in parallel to either LDO_N or LDO_P as shown in Figure 5-8. When LDO_P and the SC are in parallel as depicted in Figure 5-8 (a), $V_{in(LDO_P)}$ equals V_{SC}. Similarly, $V_{in(LDO_N)} = V_{SC}$ when LDO_N and the SC are in parallel as illustrated in Figure 5-8 (b).

Moreover, the circuit operation is governed by the difference of the ground pin currents if the two load currents reduce to zero. Since the ground pin currents of the commercial LDO regulators are very small, the transient time between the charging and discharging cycles is significantly high compared to the time duration of the other phases of the DO-SCALDO operation.

5.4 Parameters of the circuit modes of the DO-SCALDO regulator

The key parameters of the four operational phases of the DO-SCALDO regulator are listed in Table 5-1. The constant current loading is considered for the simplicity of analysis for phase 2, 3 and 4. In phase 1, where the initial charging of the SC is performed, the ESR of the SC and the resistance of the switches are not used in parameter calculations since R_C is typically higher than these values.

Table 5-1: Parameters of different operating phases

Phase		Input source current	SC current	SC voltage at the end of the phase	The time duration of the phase
1: Initial charging process		$\approx \frac{V_{in}}{R_C} e^{-\left(t/R_C C_{SC}\right)}$	$\approx \frac{V_{in}}{R_C} e^{-\left(t/R_C C_{SC}\right)}$	$\approx V_{\min}$	$\approx R_C C_{sc} \ln(\frac{V_{in}}{V_{in} - V_{\min}})$
2: $I_{o(LDO_P)} > I_{o(LDO_N)}$	Charging	$I_{o(LDO_P)} + I_{MCU} + I_g$	$I_{o(LDO_P)} - I_{o(LDO_N)}$	$V_{in} - V_{\min} - (2R_{sw} + R_{sc})(I_{o(LDO_P)} - I_{o(LDO_N)})$	$\frac{C_{SC}[V_{in} - 2V_{\min} - 2(2R_{sw} + R_{sc})(I_{o(LDO_P)} - I_{o(LDO_N)})]}{I_{o(LDO_P)} - I_{o(LDO_N)}}$
	Discharging	$I_{o(LDO_N)} + I_{MCU} + I_g$	$I_{o(LDO_P)} - I_{o(LDO_N)}$	$V_{\min} + (2R_{sw} + R_{sc})(I_{o(LDO_P)} - I_{o(LDO_N)})$	$\frac{C_{SC}[V_{in} - 2V_{\min} - 2(2R_{sw} + R_{sc})(I_{o(LDO_P)} - I_{o(LDO_N)})]}{I_{o(LDO_P)} - I_{o(LDO_N)}}$
3: $I_{o(LDO_P)} < I_{o(LDO_N)}$	Charging	$I_{o(LDO_N)} + I_{MCU} + I_g$	$I_{o(LDO_N)} - I_{o(LDO_P)}$	$V_{in} - V_{\min} - (2R_{sw} + R_{sc})(I_{o(LDO_N)} - I_{o(LDO_P)})$	$\frac{C_{SC}[V_{in} - 2V_{\min} - 2(2R_{sw} + R_{sc})(I_{o(LDO_N)} - I_{o(LDO_P)})]}{I_{o(LDO_N)} - I_{o(LDO_P)}}$
	Discharging	$I_{o(LDO_P)} + I_{MCU} + I_g$	$I_{o(LDO_N)} - I_{o(LDO_P)}$	$V_{\min} + (2R_{sw} + R_{sc})(I_{o(LDO_N)} - I_{o(LDO_P)})$	$\frac{C_{SC}[V_{in} - 2V_{\min} - 2(2R_{sw} + R_{sc})(I_{o(LDO_N)} - I_{o(LDO_P)})]}{I_{o(LDO_N)} - I_{o(LDO_P)}}$
4: $I_{o(LDO_P)} = I_{o(LDO_N)}$		$I_{o(LDO_P)} + I_{MCU} + I_g = I_{o(LDO_N)} + I_{MCU} + I_g$	0	Does not change	Infinite

Where; R_{SW} is the equivalent resistance of a switch, R_{SC} is the DC-resistance (ESR) of the supercapacitor, I_g is the common ground pin current of the two LDO regulator, I_{MCU} is the current of the control circuit, and t is the time.

5.5 Power losses

Since the DO-SCALDO regulator is based on the basic SCALDO technique, the main power losses are similar to those for SCALDO regulators [15, 26]. In addition, the initial charging process of the SC can also be taken as another loss. These key power losses can be listed as follows.

1. The ohmic losses due to the switches and the ESR of the SC.
2. The dynamic losses due to the switching transient events.
3. The power usage of the control circuit.
4. The energy loss when the capacitors with different voltages are connected in parallel.
5. The power losses in the LDO regulators.
6. The power dissipation of the current limit resistor (R_C) during the initial charging process of the SC.

If the maximum differential output current of the DO-SCALDO regulator is $I_{max(diff)}$, the ohmic losses (P_{ohmic}) can be calculated as per (5-8).

$$P_{ohmic} = I^2_{\max(diff)}\left[2R_{sw} + R_{sc}\right] \tag{5-8}$$

Item (2) depends on the operating frequency of the converter [74, 75], and it is very small in the DO-SCALDO regulator due to the very low switching frequency. According to item (3), the power consumption of the control circuit (MCU in this case) accounts for another loss.

The LDO regulators applied in the proposed DC-DC converter typically require input capacitors for stability. At the beginning of the charging or discharging steps, there is always a voltage difference between these input capacitors and the SC. Because of this voltage difference, energy is wasted across the ESR of the SC and the ESR of the input capacitors. Some portion of the charge is delivered to the LDO regulators at the same time. The calculation of the exact amount of the energy loss due to this effect is out of the scope of this analysis and more research is needed. Nevertheless, the worst-case energy loss can be estimated considering that the loss factor is entirely due to the ESR of the capacitors [15]. This worst-case power loss of a single input capacitor (P_{cap}) at steady state is defined in (5-9) considering a complete switching cycle with a period of T. This equation is derived assuming that the

capacitance of the SC is much larger than the capacitance of the input capacitor. Also, it is assumed that the input capacitors in both rails have the same capacitance (C_{in}).

$$P_{cap} = \frac{C_{in}(V_{SC} - V_{in(cap)})^2}{T} \tag{5-9}$$

Where; $V_{in(cap)}$ is the voltage of the input capacitor which comes in parallel with the SC at the start of a single switching cycle.

The power losses in the LDO regulators are similar to the typical losses inherited in a linear regulator. These losses mainly depend on the input-output voltage difference, the output current and the power consumption of the control unit [76]. The power loss in the controller is very small due to the use of the low quiescent current LDO regulators whereas the energy loss across the series-pass device (typically the pass transistor/MOSFET) can be obtained by taking the integral of the product of the instantaneous output current and voltage across the LDO regulator over the time.

The voltage of the SC is brought to a value close to V_{min} at the start as highlighted in Section 5.3.1. Therefore, the energy stored in the SC can be approximated as $0.5C_{SC}(V_{min})^2$ at the end of the initial charging process. Also, the same amount of energy is wasted due to the current limit resistor R_C, ESR of the SC and the resistance of the switches. Since this process is done only for one time (at the very beginning of the power-up of the circuit), its effect on efficiency can be neglected if the regulator is operated significantly large time duration compared to the initial charging time of the SC.

5.6 End-to-end efficiency

After the initial charge up of the SC, the circuit is operated in either phase 2, 3 or 4, as highlighted in section 5.3. The ETEE of the DO-SCALDO regulator can be calculated considering the zero net-charge accumulation in the SC and constant load currents at the outputs. The ETEE for phase 2 or 3 ($\eta_{2,3}$) is given in (5-10). The numerator of this equation represents the energy delivered by the two LDO regulators in a complete cycle, and the denominator shows the energy consumed by the converter during the same period.

$$\eta_{(2,3)} = \frac{(V_{o(LDO_P)} I_{o(LDO_P)} + \left|V_{o(LDO_N)} I_{o(LDO_N)}\right|)(t_c + t_d)}{V_{in}[I_{in(c)} t_c + I_{in(d)} t_d]} \quad (5\text{-}10)$$

Where; $I_{in(c)}$, $I_{in(d)}$, t_c, and t_d, are the source current of the charging cycle, the source current in the discharging cycle, the charging time, and the discharging time, respectively.

The charging or discharging periods are theoretically infinite in phase 4. Therefore, the ETEE of this phase can be calculated by taking the limit of (5-10) when the charging and discharging times go to infinity.

If the losses due to the control circuit and the ground pin currents of the LDO regulators are neglected, the theoretical maximum ETEE (η_{max}) can be obtained as:

$$\eta_{\max} = \frac{V_{o(LDO_P)} + \left|V_{o(LDO_N)}\right|}{V_{in}} \quad (5\text{-}11)$$

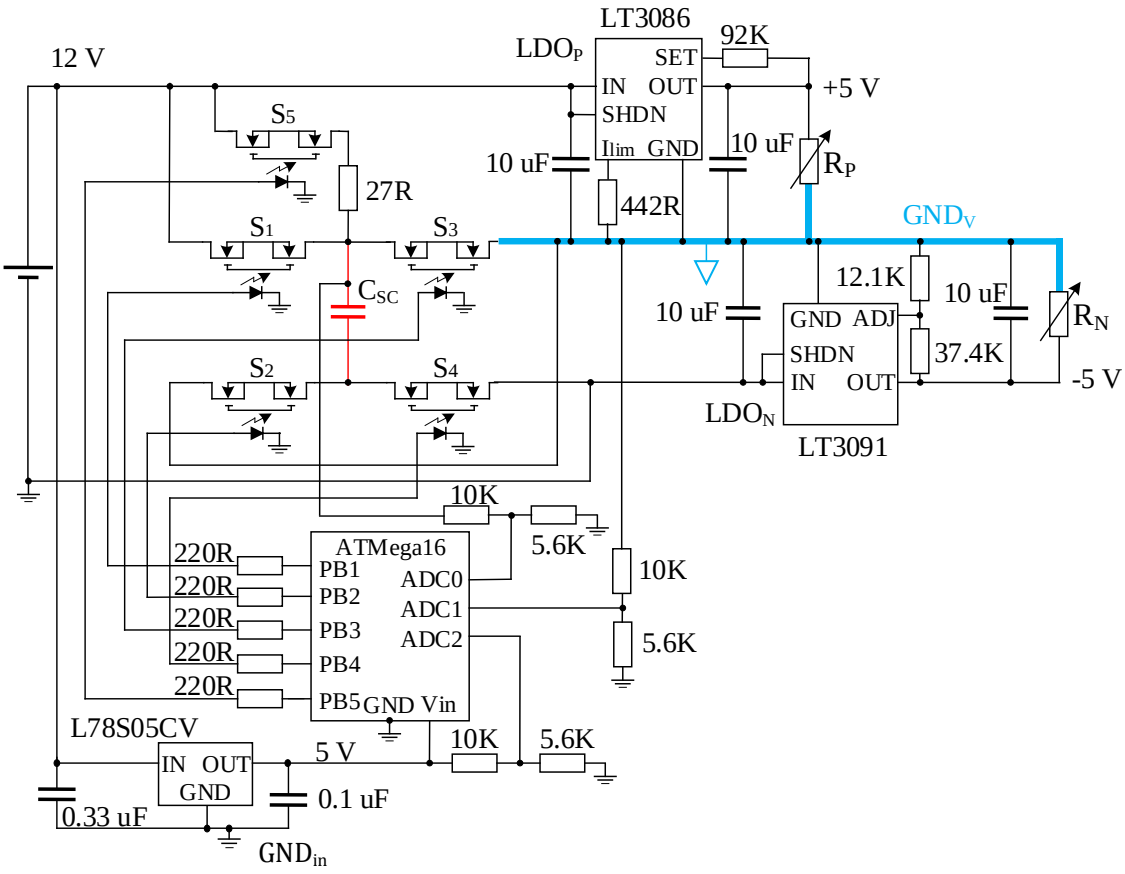
5.7 Discussion

A split-rail DC-DC converter was developed by extending the concept of the SCALDO regulator, and it is named the DO-SCALDO regulator. The dual-polarity voltages are generated by cascading a positive-rail type LDO regulator and a negative-rail type LDO regulator with a virtual ground at the output. A low-frequency supercapacitor circulation technique is used to control the differential load current, and the circuit operation can be derived from the basic SCALDO method. The voltage of the SC used in the circuit is raised to the minimum working voltage of the LDO regulators in the initial stage, and the charge balance of this SC is maintained throughout the switching cycles thereafter. It was identified that the switching frequency depends on the capacitance and the ESR of the SC, the supply voltage, the minimum voltage of the LDO regulators, the differential load current and the resistance of the switches. It was also found that the power losses in this dual-output SCALDO regulator are similar to the losses inherited in a basic SCALDO design. The maximum achievable ETEE of the proposed design at steady state is the ratio of the sum of the absolute values of output voltages of the LDO regulators to the supply voltage. The next chapter focuses on the validation of the DO-SCALDO model with experimental results.

Chapter 6 Experimental Validation of the DO-SCALDO Concept

Abstract- The theoretical concept of the dual-output SCALDO regulator is validated with experimental results in this chapter. A 12 V to ±5 V DO-SCALDO regulator prototype is implemented, and the steady-state characteristics and transient responses are experimentally investigated. The end-to-end efficiencies and the losses are also experimentally observed and analysed. The unique characteristics of the DO-SCALDO regulator are highlighted and compared to commercial split-rail and dual-output converters.

6.1 Implementation aspects of the 12 V to ±5 V DO-SCALDO prototype



(a)

(b)

Figure 6-1: The 12 V to ±5 V DO-SCALDO proof of concept prototype: (a) schematic (b) PCB design.

The 12 V to ± 5 V DO-SCALDO proof-of-concept prototype is constructed with a positive-rail LDO regulator of the type LT3086, and a negative-rail regulator (LT3091) from Linear Technology. This prototype is shown in Figure 6-1 along with the simplified circuit diagram. The complete schematic and the PCB design are available in Appendix D. The nominal ground pin current of the two LDO regulators chosen is about 5 mA. The maximum output current of these two LDO regulators is adjusted to 1.5 A. The capacitance, and the DC ESR of the SC are 3.3 F and 90 mΩ, respectively. The switches (S_1 to S_5) are the photovoltaic relays of the type TLP3543, and they are selected based on the maximum output current of the LDO regulators. Since these photovoltaic relays are made with back-to-back connected MOSFETs, they do not create any short circuit paths due to the body diodes. The typical value of the DC resistance of a single switch is around 50 mΩ. These relays are controlled using five digital output channels of the ATMega16 microcontroller unit (MCU). This microcontroller consumes about 25 mA of continuous current at 5 V, and it is driven by a 5 V linear regulator (L78S05).

The source voltage, the virtual ground potential and the SC voltage are monitored with the aid of the analog-to-digital (ADC) channels of the MCU as shown in Figure 6-1 (a). The minimum input voltage of the LDO regulators (V_{min}) is defined as 5.4 V in the MCU program to satisfy the criterion defined in (5-6). This value is 150

mV higher than what is specified in the data sheets of the LDO regulators. The input and output capacitors are used to ensure the stability of the LDO regulators according to the datasheet specifications. Initially, the SC is charged up to 5.4 V using the 27 Ω resistor, and the switches S_4 and S_5. All the other switches are turned off during this period. Then the pre-charged SC is placed in parallel to LDO_N, and the switching scheme is started based on the differential load current. The MCU algorithm of the prototype is given in Figure 6-2.

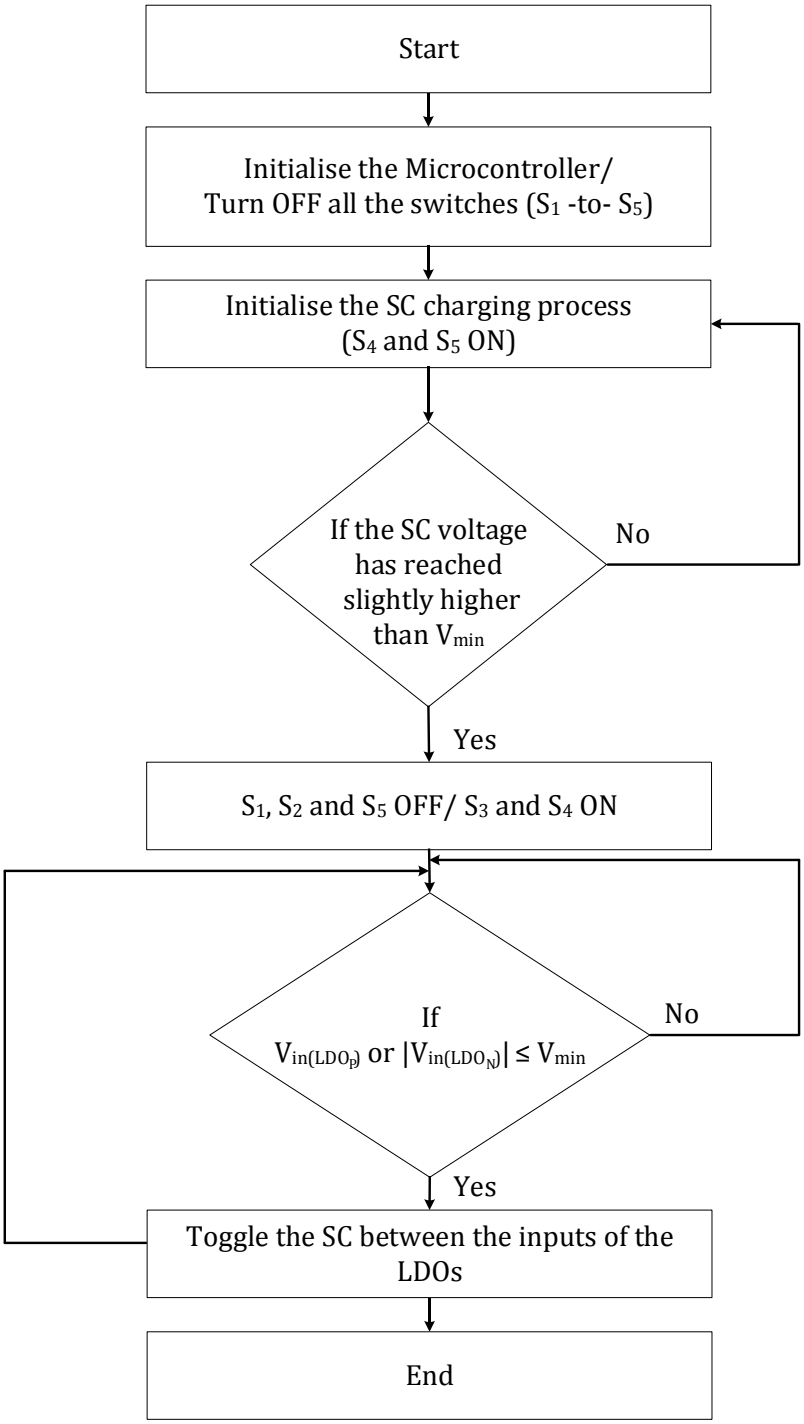
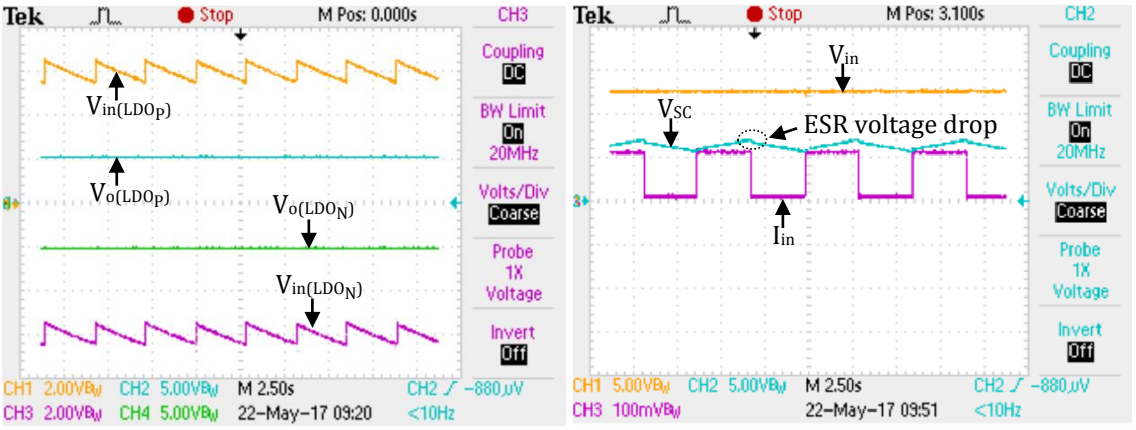


Figure 6-2: The MCU algorithm of the prototype.

6.2 Steady-state performance

The steady-state performance of the DO-SCALDO prototype is observed for different levels of the load currents ranging from zero mA to 1.5 A. The source voltage is adjusted to its rated value (12 V) during the testing. The source current is measured by using a hall-effect current sensor with a scale of 100 mV/A. The input and output voltages of the positive and negative LDO regulators are measured with respect to the virtual ground (GND_V). Even though GND_V varies over time relative to the common ground (GND_{in}), the output voltages of the LDO regulators are regulated all the time with respect to GND_V. It is important to note here that GND_V is not measured and shown separately. Even so, the input voltage of the negative-rail LDO regulator ($V_{in(LDO_N)}$) represents the inverted GND_V with respect to GND_{in}.

6.2.1 Phase 2 ($I_{o(LDO_P)} > I_{o(LDO_N)}$) observations



(a) (b)

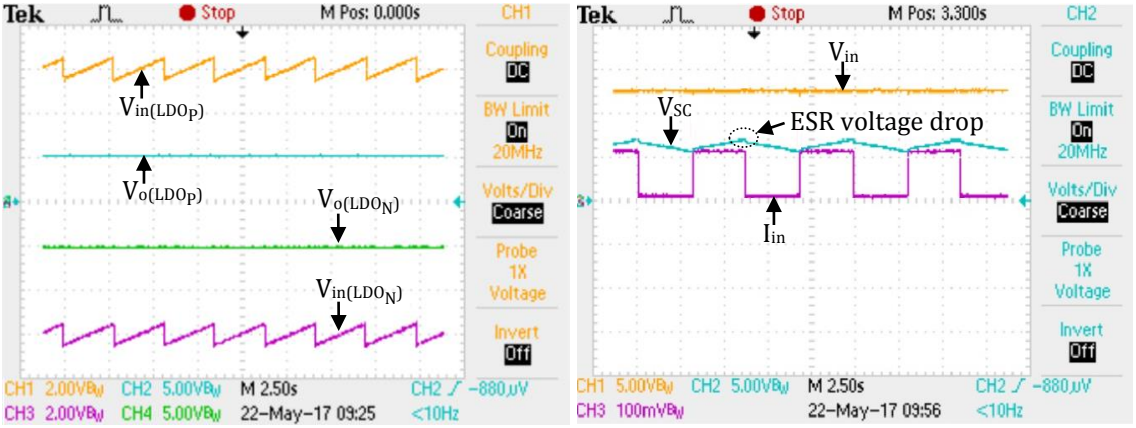
Figure 6-3: Steady-state results of phase 2 when $I_{o(LDO_P)}$ = 1100 mA and $I_{o(LDO_N)}$ = 100 mA; (a): Input and output voltages of the LDOs (b): Voltage and current of the power source, voltage across the supercapacitor.

In Figure 6-3 where the test results of $I_{o(LDO_P)} > I_{o(LDO_N)}$ criteria is displayed, the load current of LDO_P and LDO_N are 1100 mA and 100 mA, respectively. $V_{in(LDO_P)}$ reduces from 6.6 V to 5.4 V (V_{min}) whereas $V_{in(LDO_N)}$ varies from -5.4 V to -6.6 V relative to GND_V. These triangular voltage waveforms are generated by the charging and discharging steps of the SC. In the first phase, the SC charges in parallel to the input of LDO_N allowing the differential load current (1 A) to pass through it, and in the next phase, it discharges in parallel to LDO_P releasing the same amount of current. The duration of the charging and discharging steps is approximately 2.8 s while the

calculated period is around 2.7 s. The measured output voltages of LDO_P and LDO_N are + 5 V and – 5 V, respectively.

Similarly, the source voltage, the source current and the voltage across the SC are depicted in Figure 6-3 (b). The control circuit current and the ground pin current of two LDO regulators are around 30 mA. According to this oscilloscope trace, the source current increases to 1130 mA in the charging phase and reduces to 130 mA in the discharging phase. The ESR of the SC creates a small voltage drop in every cycle.

6.2.2 Phase 3 ($I_{o(LDOP)} < I_{o(LDON)}$) observations



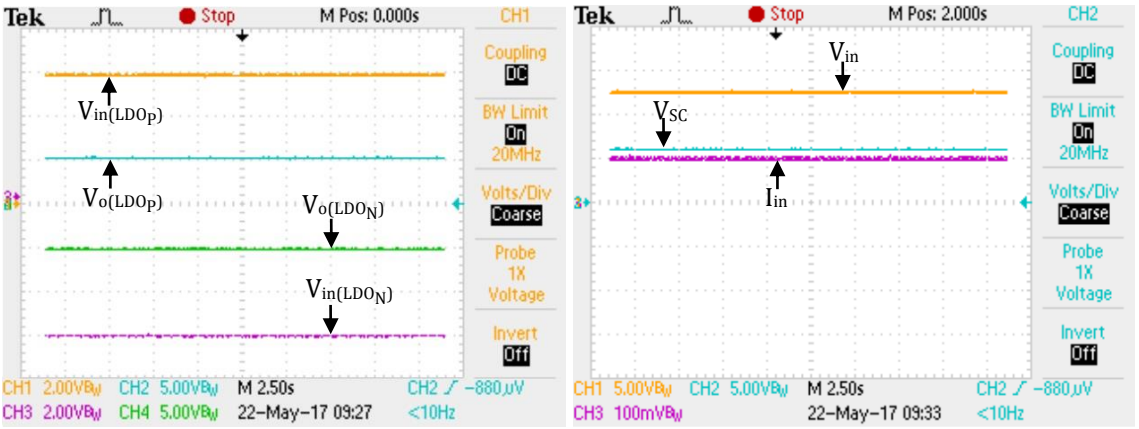
(a) (b)

Figure 6-4: Steady-state results of phase 3 when $I_{o(LDOP)}$ = 100 mA and $I_{o(LDON)}$= 1100 mA; (a): Input and output voltages of the LDOs (b): Voltage and current of the power source, voltage across the supercapacitor.

The prototype is further tested by setting the output current of LDO_P to 100 mA and LDO_N to 1100 mA. The input source voltage is kept around 12 V. In this phase, the input voltage of LDO_P tends to increase from 5.4 V to 6.6 V in each cycle as displayed in Figure 6-4 (a). The measured period of one charging/discharging cycle is around 2.8 s and the corresponding calculated duration of a single step is about 2.7 s. Furthermore, the input voltage of LDO_N varies from -5.4 V to -6.6 V and the regulated output voltages of LDO_P and LDO_N, are respectively 5 V and – 5 V. The variation of the source voltage, SC voltage, and the source current of this phase are depicted in Figure 6-4 (b).

6.2.3 Phase 4 ($I_{o(LDO_P)} = I_{o(LDO_N)}$) observations

The output currents of LDO_P and LDO_N are set to 1 A to investigate the behaviour of the proposed DC-DC converter at equal load currents. From Figure 6-5 (a), it can be seen that the input voltages of LDO_P and LDO_N are fixed at 6 V and -6 V, respectively. Besides, their regulated output voltages are 5 V and -5 V for LDO_P and LDO_N, respectively. Figure 6-5 (b) shows that the SC voltage is constant and has a value of around 6 V. The observed input source current is about 1030 mA, and it passes through both LDO regulators. Interestingly, the SC current falls to zero in this phase.



(a) (b)

Figure 6-5: Steady-state results of phase 4 when $I_{o(LDO_P)}$ = 1000 mA and $I_{o(LDO_N)}$= 1000 mA; (a): Input and output voltages of the LDOs (b): Voltage and current of the power source, voltage across the supercapacitor.

6.2.4 Operating frequencies

The SC switching frequency of the DO-SCALDO regulator depends on the differential load current, the supply voltage, the capacitance of the SC, the resistance of the switches, and the DC ESR of the SC. The operating frequencies are observed for different load currents, and the results are listed along with the calculated values in Table 6-1. These calculations are done based on the equations defined in Table 5-1 and the circuit component values in Figure 6-1.

Table 6-1 implies that the switching frequency increases with the differential load current. Besides, when the load currents are equal, the differential current falls to zero and the energy circulation process of the SC stops. For the given capacitance of the SC and the resistance of the switches, the operating frequency varies between zero Hz and 350 mHz for different levels of the load current.

Table 6-1: The steady-state operating frequencies of the DO-SCALDO prototype

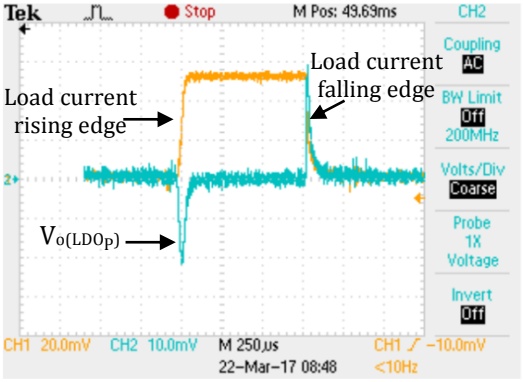
Load current of the positive LDO regulator (A)	**Load current of the negative LDO regulator (A)**	**Differential load current (A)**	**Calculated switching frequency (Hz)**	**Experimental switching frequency (Hz)**
0	1.5 A	1. 5 A	0.361	0.353
0.1 A	1.5 A	1.4 A	0.318	0.307
0.1 A	1.1 A	1 A	0.185	0.179
1 A	1 A	0	0	0
1.1 A	0.1 A	1 A	0.185	0.179
1.5 A	0.1 A	1.4 A	0.318	0.307
0 A	1.5 A	1.5 A	0.361	0.353

6.3 Load-transient response

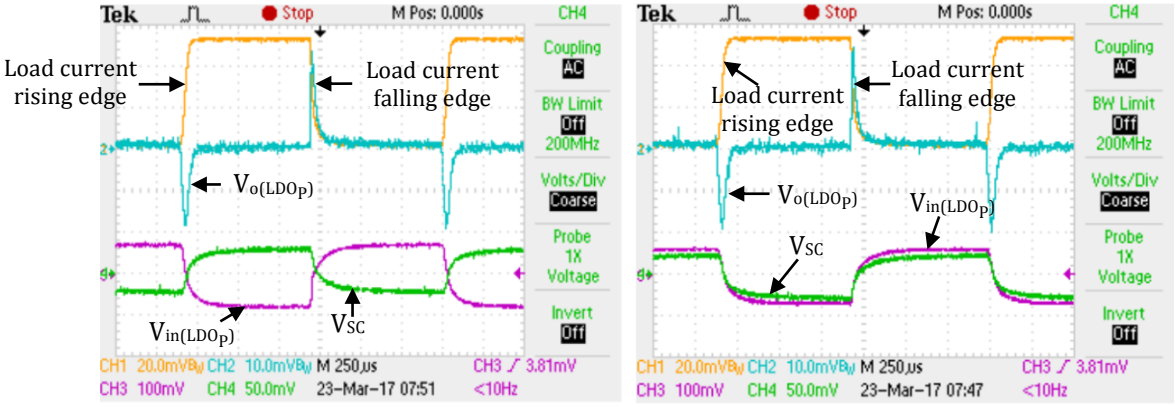
6.3.1 Positive-rail LDO regulator response

In the beginning, the step load test is done to each LDO regulator without applying the SCALDO switching sequence. In this case, LDO_N is disabled, and 6 V is applied to the input of LDO_P. This method keeps LDO_P active while all the other parts of the circuit are isolated. Then the load current is changed from 0 mA to 500 mA at a slew rate around 10 mA/µs. The variation of the output voltage and current of LDO_P is displayed in Figure 6-6 (a). According to Figure 6-6(a), the output ripple voltage of the rising edge and the falling edge load currents are about 22 mV and 29 mV, respectively.

In the next stage, the switching sequence is initiated, and the two LDO regulators are tested for the step load change using the same output current levels. Figure 6-6 (b) depicts the input and output voltages of LDO_P and the voltage across the SC in the charging phase. Similarly, Figure 6-6 (c) shows the variations in the discharging phase.



(a)



(b) (c)

Figure 6-6: Load-transient measurement of LDO_P; (a): Before applying the SCALDO method (b): After applying the SCALDO method - SC charging phase (c) SC discharging phase.

Figure 6-6 (b) shows that the output ripple voltages of the rising and falling edges are about 18 mV and 24 mV, respectively. The excess current of the rising edge passes through the SC and generates a voltage of about 45 mV. Similarly, the SC voltage falls about 45 mV in the falling edge of the transient load current. Also, the input voltage of LDO_P trends to drop at about 140 mV during the rising edge and it ascends by the same amount in the falling edge. The 100 mV difference between the change of voltages of the SC and the input voltage of LDO_P is due to the resistance of the switches in the charging and discharging paths.

Furthermore, Figure 6-6 (c) depicts the load-transient response of the discharging phase. The output voltage of LDO_P is about 19 mV in the rising edge, and it is about 26 mV in the falling edge. Both the SC voltage and the input voltage of LDO_P fall during the rising edge due to the fact that SC and LDO_P are in parallel. The drop in the SC voltage is 40 mV whereas the reduction in the input voltage of LDO_P is 130

mV. Similarly, in the falling edge of the transient load current, the input voltage of LDO_P rises about 130 mV and the SC voltage increases about 40 mV. There is almost 90 mV voltage difference across the switches during this period.

According to Figure 6-6 (b) and (c), there is about a 140 mV voltage drop at the input of LDO_P during the transient event. Nevertheless, the continuous voltage regulation is maintained by setting the V_{min} value 150 mV higher than the manufacturer-specified minimum input voltage of a LDO regulator for a maximum step load change.

The output voltage regulation of LDO_N is unaffected when the LDO_P is tested for load transient response. Since the SC and LDO_N are in parallel during the charging phase of LDO_P, the ripple at the input of LDO_N is same as the fluctuation of the SC voltage. This low-frequency ripple of $V_{in(LDO_N)}$ is attenuated due to the high power supply rejection ratio (PSRR) of the LDO regulator and its effect on the output voltage is minimal.

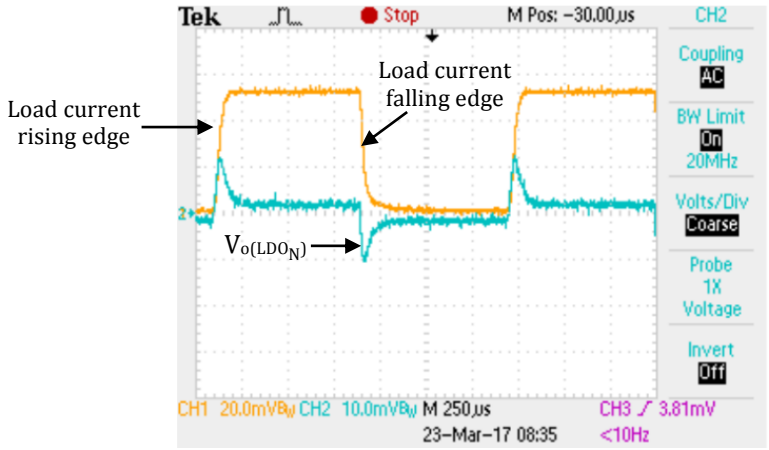
Furthermore, it can be observed from Figure 6-6 that the output voltage variation of the LDO_P regulator is the same in all three cases. Therefore, these step load results imply that the DO-SCALDO regulator produces the same quality voltage regulation as a LDO regulator for transient loads.

6.3.2 Negative-rail LDO regulator response

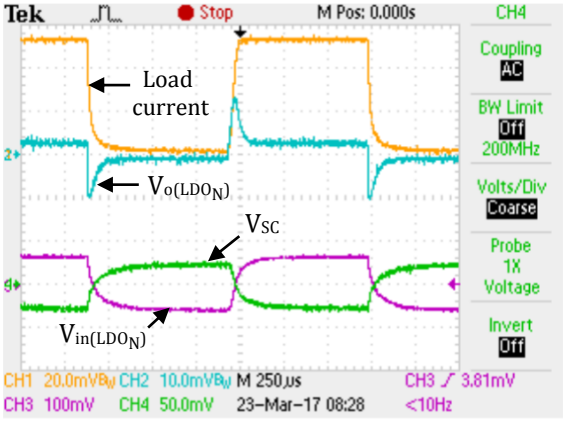
The results obtained from the load-transient test of the negative-rail LDO regulator are displayed in Figure 6-7. First, LDO_N is tested before applying the SCALDO technique by setting the input voltage to -6 V. Figure 6-7 (a) illustrates the transient response of LDO_N when the output load is changed from 0 mA to 500 mA at a slew rate of 10 mA/µs. The output ripple voltage is about 14 mV for both rising and falling edges of the load current.

Figure 6-7 (b) depicts the load-transient response of LDO_N in the charging phase of the SC when the SCALDO method is used. Similarly, the load- transient response of the discharging period is displayed in Figure 6-7 (c). According to Figure 6-7 (b) and (c), the ripple voltage is about 14 mV for both rising and falling edges of the transient current. This ripple voltage is the same as the value shown in Figure 6-7 (a) when LDO_N is tested without applying the SCALDO approach. Therefore, the results in

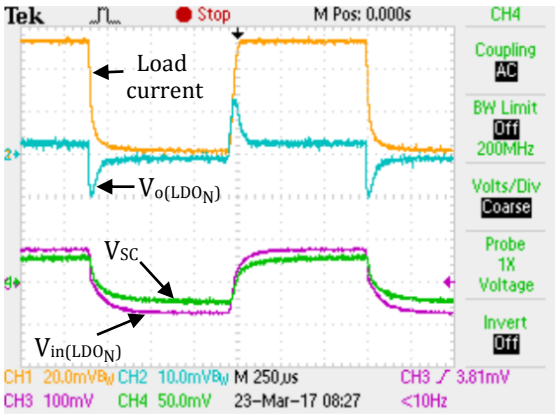
Figure 6-7 further indicate that the DO-SCALDO regulator has similar behaviour as compared to a LDO regulator for the load-transient test.



(a)



(b)



(c)

Figure 6-7: Load-transient measurement of LDO_N; (a): Before applying the SCALDO technique (b): After applying the SCALDO technique - SC charging phase (c) SC discharging phase.

6.4 Loss estimation

The main losses of the DO-SCALDO DC-DC converter are similar to the losses associated with a basic SCALDO regulator as highlighted in Section 5.5. These key implementation losses are estimated based on the maximum differential load current (1.5 A) and the rated voltage (12 V) and listed in Table 6-2. The estimated total power loss is about 1.89 W when the above factors are concerned. The DO-SCALDO prototype has approximately 20 % losses at 12 V and 1.5 A of differential load current for the worst-case scenario.

Table 6-2: Power losses in the 12 V to ± 5 V DO-SCALDO regulator

Loss factor	Description	Estimated value
1	Ohmic losses due to the ESR of the SC and the switches	428 mW
2	Dynamic losses during switching	≈ 0 W
3	The power consumption of the control unit	300 mW
4	Energy loss due to the paralleling of capacitors with different voltages	2.57 µW
5	Power losses in a single LDO regulators	
	1) Due to the series-pass device	1.101 W
	2) Due to the ground pin current	60 mW

6.5 Efficiency estimation

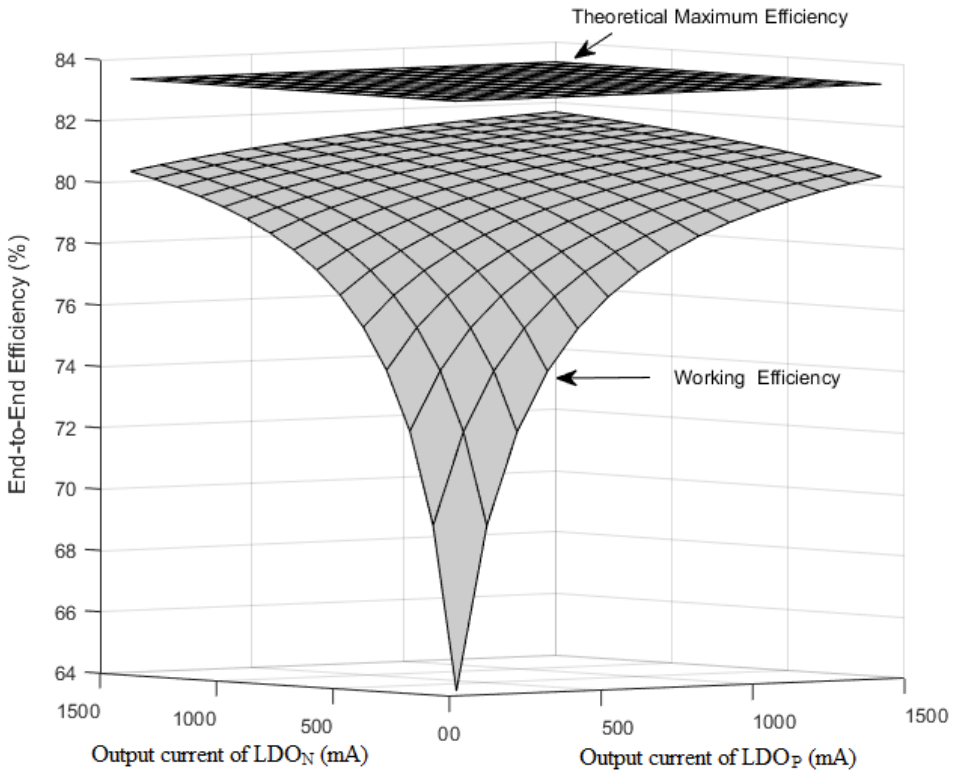


Figure 6-8: End-to-end efficiency of the 12 V to ± 5 V split-rail regulator at the rated input voltage.

The maximum theoretical ETEE of the prototype is 83.3 %, according to (5-11). Nevertheless, the measured efficiency of the DO-SCALDO regulators is around 81 % for 15 W output power (1.5 A load in each LDO regulator). Figure 6-8 depicts the ETEE of the proposed regulator plotted against the load current in each rail. According to this diagram, the efficiency drops at light loads due to the sum of the control circuit and ground pin currents. This issue can be minimised by using low quiescent current LDO regulators and replacing the MCU with low power analog comparators and logic circuits.

The ETEE of the prototype is observed by varying the source voltage ± 5 % from its rated value while keeping the load current to its maximum. The calculated and experimental efficiencies are plotted in Figure 6-9. This diagram implies that the DO-SCALDO prototype can reach up to 86.2 % of the ETEE if the source voltage is reduced by 5 % from the rated value. Similarly, the ETEE does not fall below 78 % when the supply voltage is raised by 5 %. The corresponding estimated ETEE efficiencies for these two cases are 87.8 % and 79.5 %, respectively.

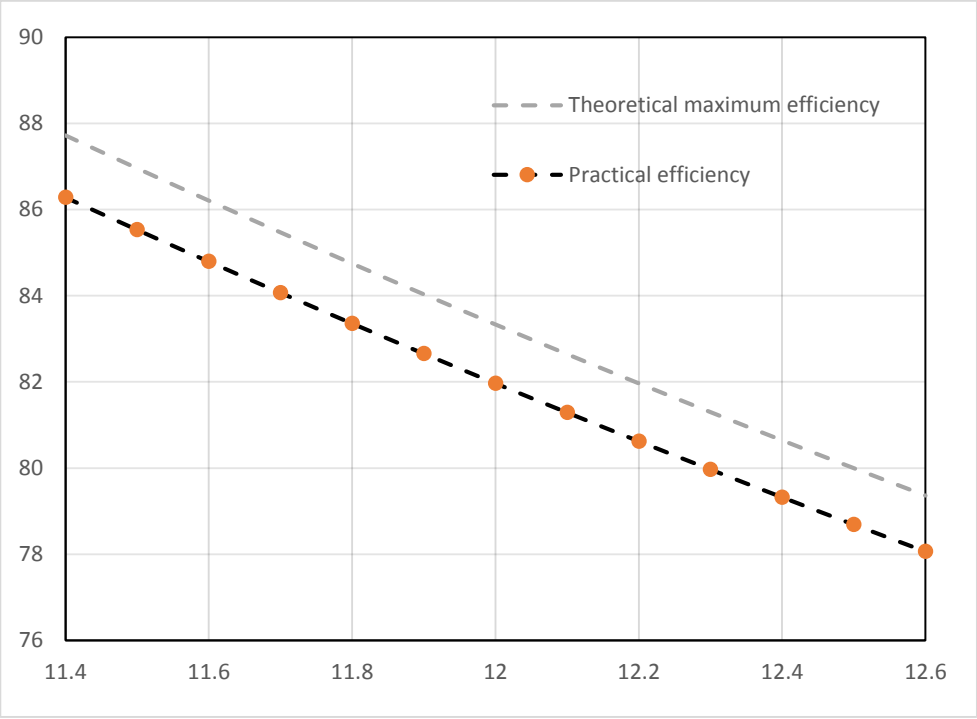


Figure 6-9: End-to-end efficiency for ± 5% difference of the rated input voltage at maximum load current.

6.6 Comparison of the basic features of the DO-SCALDO concept with other split-rail DC-DC converters

Table 6-3 summarises the key features of the DO-SCALDO concept compared to conventional split-rail techniques. This table is constructed extracting the datasheet specifications of commercial dual-output DC-DC converters typically used in low voltage applications.

Table 6-3: Comparison of the DO-SCALDO regulator with other split-rail topologies

Feature	**12 V to ±5 V DO-SCALDO regulator**	**Buffer circuits**	**Charge pumps**	**Switch-mode converters**
Voltage regulation	Regulated	Unregulated	Unregulated*(1)	Regulated
Typical switching frequency	Less than 1 Hz (C_{SC}= 3.3 F, R_{SC} = 0.09 Ω, R_{SW} = 0.1 Ω, V_{in} = 12 V)	No switching	10 kHz -to- 100 kHz	100 kHz –to- 2 MHz
Maximum differential output current	1.5 A (using 1.5 A LDO regulators)	TLE2425: 20 mA BUF 634: 250 mA	LM27762: 250 mA MAX 865: 20 mA	LT1956: Positive rail = 700 mA, Negative rail = 550 mA*(2) [77] ADP1613: 50 mA *(3) [78] TPS54160: 500 mA (output1), 200 mA (output2)*(4) [79]
Efficiency	81 % (at 1.5 A differential output current)	BUF 634 ≈ 90 %	LM27762: 85% at 250 mA MAX 865: 62 % (negative rail), 77 % (positive rail)	When the differential output current ≥ 100 mA TPS54160: 85-91 % LT1956: 78-82 %, ADP1613: 70-84 %

Feature	12 V to ±5 V DO-SCALDO regulator	Buffer circuits	Charge pumps	Switch-mode converters
Output noise	LDO_P noise = 40 μV_{RMS} with 300 µV of SCALDO ripple*(5) LDO_N noise = 18 μV_{RMS} with 100 µV ripple*(5)	BUF 634: 4 nV/√Hz	MAX 865: Positive rail: 10 mV, Negative rail: 20 mV (for 3.3µF capacitors and 1 mA load)	ADP1613 ≈ 20 mV (for 10 uF output capacitance, 1.3 MHz, 5 V and 50 mA output settings)
Essential components	2 LDO regulators, 5 switches, 1 Supercapacitor, a switch controller, 2 input capacitors, 2 output capacitors (typically small ceramic capacitors 1 µF- 10 µF)	Error amplifier, a voltage reference	MAX 865: 8 switches, 2 flying capacitors, 2 reservoir caps (typically 1 µF- 10 µF), a switch controller	SEPIC-Ćuk (ADP1613): 2 coupled inductor, 2 diodes, 8 capacitors, single switch Buck (LT1956): single switch, 3 diodes, 2 inductors, 5 capacitors, Buck (TPS54160): single switch, 2 diodes, 1 coupled inductor, 4 capacitors

*(1) some charge pump converters such as LM27762 use LDO regulators for voltage regulation.

*(2) based on the typical application shown in Fig.14 of the datasheet.

*(3) based on the ±5 V test circuit.

*(4) based on the dual-output regulator reference design.

*(5) The SC switching ripple at the input of the LDO regulators is attenuated based on PSRR.

The DO-SCALDO regulator offers regulated output voltages compared to the buffer circuits and the switched-capacitor converters. The essential component count of the DO-SCALDO regulator is in the range of what is required for the high-frequency switching converters. Also, the load current and the efficiency of the proposed split-rail circuit are comparable with the switching converters.

The switching frequency of the DO-SCALDO regulator depends on the differential load current, and it is less than 1 Hz in the 12 V to ±5 V prototype. Nonetheless, this operating frequency is very low compared with SCCs or the switch-mode dual-output converters. The output noise of the proposed design is mainly due to the internal noise of the LDO regulators and the low-frequency switching of the SC.

Interestingly, the low-frequency voltage ripple is attenuated because of the high PSRR of the two LDO regulators.

In addition, the inductor-less architecture and the low-frequency operation of this method might reduce the EMI/RFI issues, and further research is required to design a DO-SCALDO regulator for a specific EMI/RFI requirement.

The power density of the DO-SCALDO regulator is not compared in this stage since the prototype is a discrete version and the other commercialised dual-output converters are ICs. As the next stage of DO-SCALDO research, an integrated chip version developed with dual LDOs and five switches would reduce the PCB area and increase the power density.

6.7 Discussion

A 12 V to ± 5 V proof-of-concept prototype is designed to validate the DO-SCALDO theoretical model. The steady-state results show that the voltage regulation of the output rails is maintained with respect to the virtual ground throughout the switching cycles. The switching frequency varies with the differential load current, and the maximum frequency of this prototype is less than 400 mHz. The dynamic losses and the losses due to the voltage mismatch of the capacitors are minimal in the DO-SCALDO design. The ohmic losses due to the resistance of the switches and the ESR of the SC add a significant contribution to the loss factor along with the power consumption of the control circuit. The theoretical achievable ETEE is 83.3 %, while the maximum working efficiency is about 81 % for the rated input voltage and 15 W of output load. The ETEE can be increased up to 86 % if the supply voltage is reduced by 5 % from its rated value. The transient results indicate that the output loads experience the same quality voltage regulation as a linear solution. The comparison of the features of the DO-SCALDO concept with other split-rail techniques suggests that this approach offers low noise, regulated voltages and high differential output power. Also, the inductor-less architecture of this method may reduce EMI/RFI burden. Typical applications of the DO-SCALDO regulator will be the industrial devices, commercial devices, and auto accessories where the virtual ground potential is necessary with symmetrical outputs for circuit components that do not require a common mode range GND.

Chapter 7 Conclusions and Further Research

7.1 Outcomes of this research

The advanced analysis of the SCALDO regulator is performed based on two research questions as discussed in Section 2.8. Therefore, the research work was carried out with the following two objectives.

1. Evaluate the stability of the overall SCALDO regulator when the low-frequency SC switching network is added in front of the LDO regulator.
2. Design and implementation of SCALDO based dual-output regulator for split-rail applications to overcome the limitations of existing topologies.

The outcomes and the conclusions of this research are discussed based on the above two factors in Sections 7.1.1 and 7.1.2, respectively.

7.1.1 Outcomes and conclusions of the stability criterion

The stability analysis of the single-stage SCALDO topology is investigated using a discrete LDO regulator built with a p-channel MOSFET. The circuit averaging method is used to derive the small-signal model of the discrete SCALDO regulator considering the low-frequency supercapacitor circulation network. The significant findings of this analysis are listed as follows:

- The open-loop gain transfer function of the SCALDO regulator has three zeros and five poles all of which are independent of the capacitance of the supercapacitor.
- The equivalent series resistance of the input switching network affects the frequencies of some of the low-frequency poles. It also creates two high-frequency zeros and one pole. One of the high-frequency zeros is a right-hand-plane zero.
- Two techniques have been identified to frequency compensate the basic SCALDO topology built with a PMOS LDO regulator. The first method is the use of the output capacitor ESR as with the conventional PMOS LDO regulators. The second method is the application of feedforward compensation by adding a feedforward capacitor to the feedback resistor network. The simulated and experimental

results obtained from a 12 V to 5 V discrete SCALDO regulator show how the output capacitor ESR can be utilised to stabilise the control loop.

- The calculated and simulated results further show that the frequencies of the poles and zeros due to the SC circulation network occur at relatively high frequencies and their effect on the phase margin is minimal.

From the above observations, the following conclusions are made.

1. The ESR of the output capacitor can be effectively used to stabilise the control loop of a basic SCALDO configuration.
2. When the capacitance of the supercapacitor is significantly larger than the input and output capacitors, its effect on the open-loop poles and zeros are negligible.
3. If the sum of the resistances of the switches and the ESR of the supercapacitor is very low (typically less than 0.5 Ω), its influence on the phase margin is minimal and doesn't affect the stability of the SCALDO regulator.

7.1.2 Outcomes and conclusions of the dual-output SCALDO regulator Implementation

A split-rail DC-DC converter is designed and developed by extending the fundamentals of the SCALDO regulator. The significant findings related to this work are listed below.

- The cascade connection of the positive and negative LDO regulators with a virtual ground creates the dual-polarity voltages at the output. The differential load current is controlled with the aid of the charge balance of a supercapacitor, and the circuit operation can be derived from the single-stage SCALDO topology.
- The switching frequency of the proposed dual-output DC-DC converter is very low as with the SCALDO method, and it depends on the capacitance and the ESR of the SC, the power supply voltage, the minimum voltage of the LDO regulators, the differential load current and the resistance of the switches.
- The power losses of this dual-output SCALDO regulator are similar to the losses inherent in a basic SCALDO design. The ohmic losses due to the resistance of the switches and the ESR of the SC add a significant contribution to the loss factor along with the power consumption of the control circuit.

- The maximum achievable ETEE of the DO-SCALDO regulator at steady state is the ratio of the sum of the absolute values of output voltages of the LDO regulators to the source voltage.
- The steady-state observations of a 12 V to ± 5 V proof-of-concept prototype show that the voltage regulation of the output rails is maintained with respect to the virtual ground throughout the switching cycles. The switching frequency varies with the differential load current, and the maximum frequency of this prototype is less than 0.4 Hz.
- The theoretical achievable ETEE is 83.3 %, while the maximum working efficiency is about 81 % for the rated input voltage and 15 W of output load. The ETEE can be increased up to 86 % if the power supply voltage is reduced by 5 % from its rated value.
- The transient results indicate that the output load enjoys the same quality voltage regulation of a linear regulator.
- The comparison of the features of the DO-SCALDO concept with other split-rail techniques suggests that this approach offers low noise, regulated voltages and high differential output power.
- The inductor-less architecture of this method might lead to low EMI/RFI issues.

The conclusions of the DO-SCALDO research approach are listed below.

1. The SCALDO regulator can be developed to generate dual outputs using two LDO regulators of opposite polarity with the low-frequency energy circulation of a supercapacitor.
2. The same useful characteristics such as high efficiency, low noise, fast dynamic response and voltage regulation of the original SCALDO concept are achieved in the dual-output version.
3. The inductor-less architecture and low-frequency operation of the proposed dual-output DC-DC converter provide some potential advantages over switch-mode or charge pump converters especially for noise sensitive applications.

7.2 The significance of the findings of this research

The flowchart in Figure 7-1 demonstrates where the SCALDO research fits in the field of modern DC-DC converters. This study contributes to the SCALDO research

by developing a dual-output DC-DC converter and analysing the stability of the basic topology.

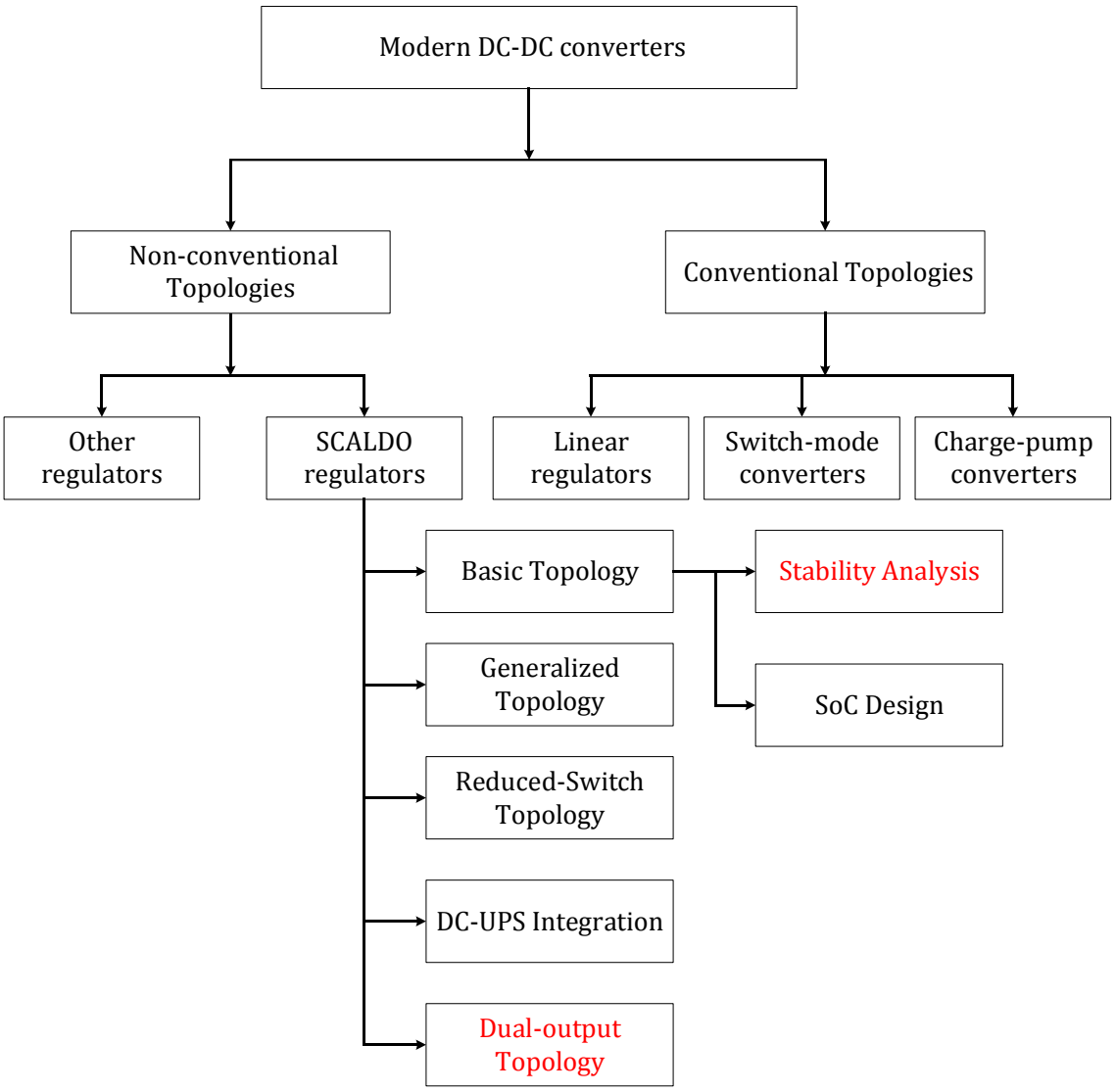


Figure 7-1: The contribution as a part of SCALDO research.

The findings of this study have several important implications for future practice. As an example, the results of the stability analysis will help designers select the appropriate circuit parameters to ensure the stability of the SCALDO regulator. Similarly, this work can be used to optimise the process parameters of the IC version of the SCALDO regulator. Also, the DO-SCALDO regulator brings some competitive advantages over conventional dual-output or split-rail converters, especially for noise sensitive applications. Since the DO-SCALDO concept is validated in this thesis, a compact version of this design such as an IC will be an advantage for commercialisation.

7.3 Recommendations for further research

The work presented in this thesis could be further developed and extended in a number of directions. Since the stability analysis is done with respect to a discrete SCALDO regulator, a possible further extension would be the investigation of the stability of a SoC design. Also, it will be useful to analyse the stability related to the optimisation of the loop parameters during the design process. It is also required to investigate the stability of the other topologies of the SCALDO regulator such as the generalised concept and the reduced-switched method.

In terms of the DO-SCALDO regulator, further research could explore the stability of the overall circuit design. The outcomes of the stability analysis of the single-stage SCALDO topology may be used to derive the stability of the dual-output version. In addition, the proposed DO-SCALDO regulator might eliminate the EMI/RFI issues due to its inductor-less architecture and low-frequency operation. Nevertheless, further research needs to be done in the direction of the EMI testing, and such work would be useful in developing the DO-SCALDO regulator for a specific low-EMI application. Moreover, the power density of the converter can be increased if the two LDOs and the switches are combined in a single IC. In this scenario, the supercapacitor and the input/output capacitors are the only components external to the IC; this leads to a large decrease in PCB space. Also, the development of an adjustable voltage version of the DO-SCALDO regulator might expand its applications to a wider scope.

Another practically useful study might explore the power supply ripple and its influence on the output voltage of a SCALDO regulator. The effect of the input source ripple together with the switching noise should be evaluated in a SCALDO regulator. Also, this kind of study will make an important contribution to low noise power supply design using the SCALDO technique.

Appendix A: Small-Signal Model of the Error Amplifier

The small-signal model of the BJT differential pair (previously shown in Figure 3-3) is constructed in Figure A-1[49]. The two transistors are displayed as Q_1 and Q_2, and their base, collector and emitter terminals are denoted as B, C, and E, respectively with the subscript of the transistor number. The base-collector and base-emitter parasitic capacitances of Q_1 are shown as C_{BC1} and C_{BE1}, respectively. The term R_{B1} represents the junction resistance of the base terminal of Q_1. The output resistance of Q_1 for small signals is displayed as r_{o1}. Also, $r_{\pi 1}$ denotes the small-signal input resistor between the base and the emitter. Since the collector and the emitter junction resistances are very small compared to R_{C1}, r_{o1}, and R_E, they are ignored in this model. The current-controlled voltage source of Q_1 is the product of the transconductance (g_{m1}) and the base-emitter small-signal voltage ($v_{\pi 1}$). The output voltage at the collector terminal of Q_1 is shown as V_{oe1}. Since the two transistors are identical, the same notation is used for the small-signal parameters of Q_2.

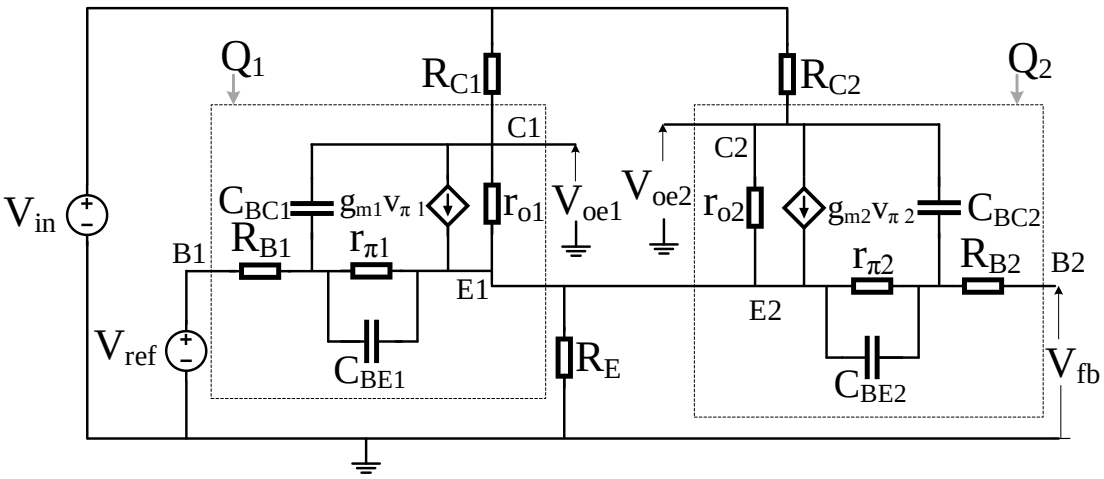


Figure A-1: The small-signal model of the NPN BJT differential pair.

The small-signal voltage gain is obtained by applying the half-circuit analysis [80]. The half-circuit of Q_2 is constructed in Figure A-2. Since the two BJTs have identical properties, the terms R_B, R_C, r_π, g_{mb}, r_o, C_{BE}, C_{BC} and R_o in this diagram are applied to an equivalent single BJT transistor. In addition, v_{diff}, v_{cm}, and v_{oe} are the small-signal quantities for the input differential signal, the common-mode voltage across r_π, and the output voltage, respectively. Similarly, R_{sig} is the resistance of the input differential signal.

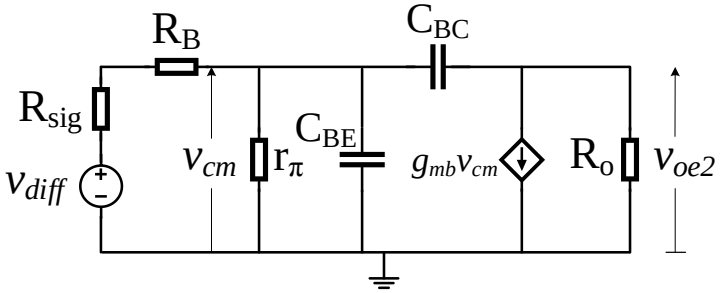


Figure A-2: The half-circuit of the differential amplifier (considering the Q_2 transistor).

The voltage of the input differential signal is defined in (a-1).

$$v_{diff} = \left(v_{fb} - v_{ref}\right)/2 \tag{a-1}$$

Where; v_{ref} and v_{fb} are the small-signal quantities of the reference voltage and the feedback voltage of the SCALDO regulator, respectively.

Because the base of Q_1 is connected to the reference voltage source (which is considered as the ground for ac signals), the impedance of the input differential signal is the impedance seen through the feedback resistor network (refer Figure 3-1 for SCALDO circuit diagram). If the impedance across the P-channel MOSFET of the LDO regulator is considered to be very small compared to the resistance of the feedback network, the resistance of the input differential signal can be approximated as (a-2).

$$R_{sig} \approx R_1 // R_2 \tag{a-2}$$

Where; R_1 and R_2 are the resistances of the feedback resistors of the LDO regulator.

The output resistance of this half-circuit model is approximated in (a-3). This approximation is done by neglecting the effect of R_E since it is larger than the small-signal resistance between the base and the emitter (looking into the emitter) of a BJT so that the input differential signal is divided equally between the two emitter junctions. More details are available in [49].

$$R_0 \approx R_C // r_o \tag{a-3}$$

Where; $R_C = R_{C1} = R_{C2}$.

The half-circuit in Figure A-2 can be further simplified by applying Thevenin's theorem to the input side. The Thevenin's equivalent circuit of this half-circuit model is displayed in Figure A-3.

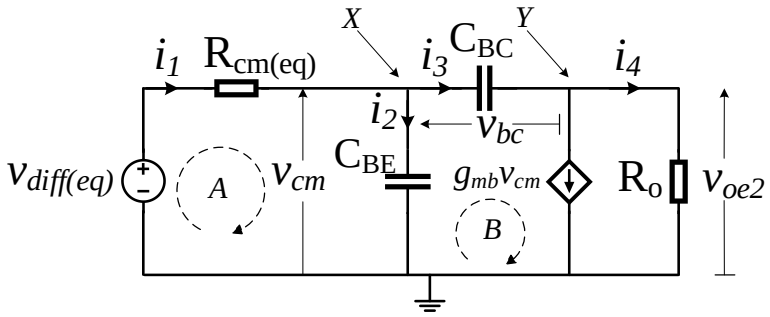


Figure A-3: Thevenin's equivalent half-circuit of the NPN BJT differential amplifier.

The Thevenin's equivalent input voltage ($v_{diff(eq)}$) and the equivalent resistance ($R_{cm(eq)}$) of this circuit are defined in (a-4) and (a-5), respectively.

$$v_{diff(eq)} = \frac{r_\pi}{\left(r_\pi + R_B + R_{sig}\right)} v_{diff} \tag{a-4}$$

$$R_{cm(eq)} = \left(R_B + R_{sig}\right) // r_\pi \tag{a-5}$$

The following two relationships can be obtained by applying KCL to the nodes X and Y in Figure A-3.

$$i_1 - i_2 - i_3 = 0 \tag{a-6}$$

$$i_3 - i_4 - g_{mb} v_{cm} = 0 \tag{a-7}$$

Similarly, KVL can be applied to loops A and B to derive (a-8) and (a-9).

A$\curvearrowright$
$$v_{diff(eq)} - i_1 R_{cm(eq)} - v_{cm} = 0 \tag{a-8}$$

B$\curvearrowright$
$$v_{cm} - v_{bc} - v_{oe2} = 0 \tag{a-9}$$

Also, the two currents that flow through C_{BE} and C_{BC} capacitors are defined in s-domain as follows:

$$i_2 = s v_{cm} C_{BE} \tag{a-10}$$

$$i_3 = sv_{bc}C_{BC} \tag{a-11}$$

The ratio of the output voltage (v_{oe2}) to the input voltage ($v_{diff(eq)}$) can be obtained by using the relationships from (a-4) to (a-11). This ratio is given in (a-12).

$$\frac{v_{oe2}}{v_{diff(eq)}} = \frac{-R_o(g_{mb} - sC_{BC})}{R_{cm(eq)}R_oC_{BE}C_{BC}s^2 + \left(R_{cm(eq)}(C_{BE} + C_{BC} + R_oC_{BC}g_{mb}) + R_oC_{BC}\right)s + 1} \tag{a-12}$$

The poles of (a-12) can be obtained by factorising the denominator assuming that they are widely separated. Therefore, the factorised gain transfer function is given in (a-13).

$$\frac{v_{oe2}}{v_{diff(eq)}} \approx \frac{-R_o g_{mb}(1 - s/\omega_{z(ea)})}{(1 + s/\omega_{p1(ea)})(1 + s/\omega_{p2(ea)})} \tag{a-13}$$

Where; $\omega_{z(ea)}$, $\omega_{p1(ea)}$ and $\omega_{p2(ea)}$ are the zero, the first pole and the second pole of the gain transfer function of the error amplifier.

The frequencies of these poles and the zero are approximated as follows:

$$\omega_{z(ea)} = -\frac{g_{mb}}{C_{BC}} \tag{a-14}$$

$$\omega_{p1(ea)} = -\frac{1}{R_{cm(eq)}C_{BE} + (R_{cm(eq)} + R_o(1 + R_{cm(eq)}g_{mb}))C_{BC}} \tag{a-15}$$

$$\omega_{p2(ea)} = -\frac{R_{cm(eq)}R_oC_{BE}C_{BC}}{R_{cm(eq)}C_{BE} + (R_{cm(eq)} + R_o(1 + R_{cm(eq)}g_{mb}))C_{BC}} \tag{a-16}$$

The ratio of the output voltage of the Q_2 transistor to the input differential signal can be redefined as (a-17) by using (a-1), (a-4), and (a-13).

$$\frac{v_{oe2}}{(v_{fb} - v_{ref})} = \frac{-0.5(r_\pi/(r_\pi + R_B + R_{sig}))R_o g_{mb}(1 - s/\omega_{z(ea)})}{(1 + s/\omega_{p1(ea)})(1 + s/\omega_{p2(ea)})} = \frac{-G_{ea}(1 - s/\omega_{z(ea)})}{(1 + s/\omega_{p1(ea)})(1 + s/\omega_{p2(ea)})} \tag{a-17}$$

G_{ea} is the gain of this error amplifier as per (a-18).

$$G_{ea} = 0.5(r_\pi/(r_\pi + R_B + R_{sig}))R_o g_{mb} \tag{a-18}$$

According to the operation principle of the BJT differential pair [49], the mirror output voltage at Q_1 should be negative with respect to the output voltage of Q_2 (v_{oe1}= - v_{oe2}). Since the PMOS pass device of the SCALDO regulator is fed from Q_1, the output signal of Q_1 to the differential input signal is defined as per (a-19). For the simplicity of notation, the output voltage the error amplifier is denoted as v_{oe}, where; v_{oe}= v_{oe1}= -v_{oe2}.

$$\frac{v_{oe}}{\left(v_{fb}-v_{ref}\right)}=\frac{0.5(r_{\pi}/(r_{\pi}+R_B+R_{sig}))R_o g_{mb}(1-s/\omega_{z(ea)})}{\left(1+s/\omega_{p1(ea)}\right)\left(1+s/\omega_{p2(ea)}\right)}=\frac{G_{ea}(1-s/\omega_{z(ea)})}{\left(1+s/\omega_{p1(ea)}\right)\left(1+s/\omega_{p2(ea)}\right)} \quad \text{(a-19)}$$

If the high-frequency pole ($\omega_{p2(ea)}$) and zero ($\omega_{z2(ea)}$) are neglected, the error amplifier first-order model for the small-signal quantities can be approximated as (a-20).

$$\frac{v_{oe}}{\left(v_{fb}-v_{ref}\right)}\approx\frac{G_{ea}}{\left(1+s/\omega_{p1(ea)}\right)} \quad \text{(a-20)}$$

Appendix B: Schematic and PCB design of the 12 V to 5 V Discrete SCALDO Regulator

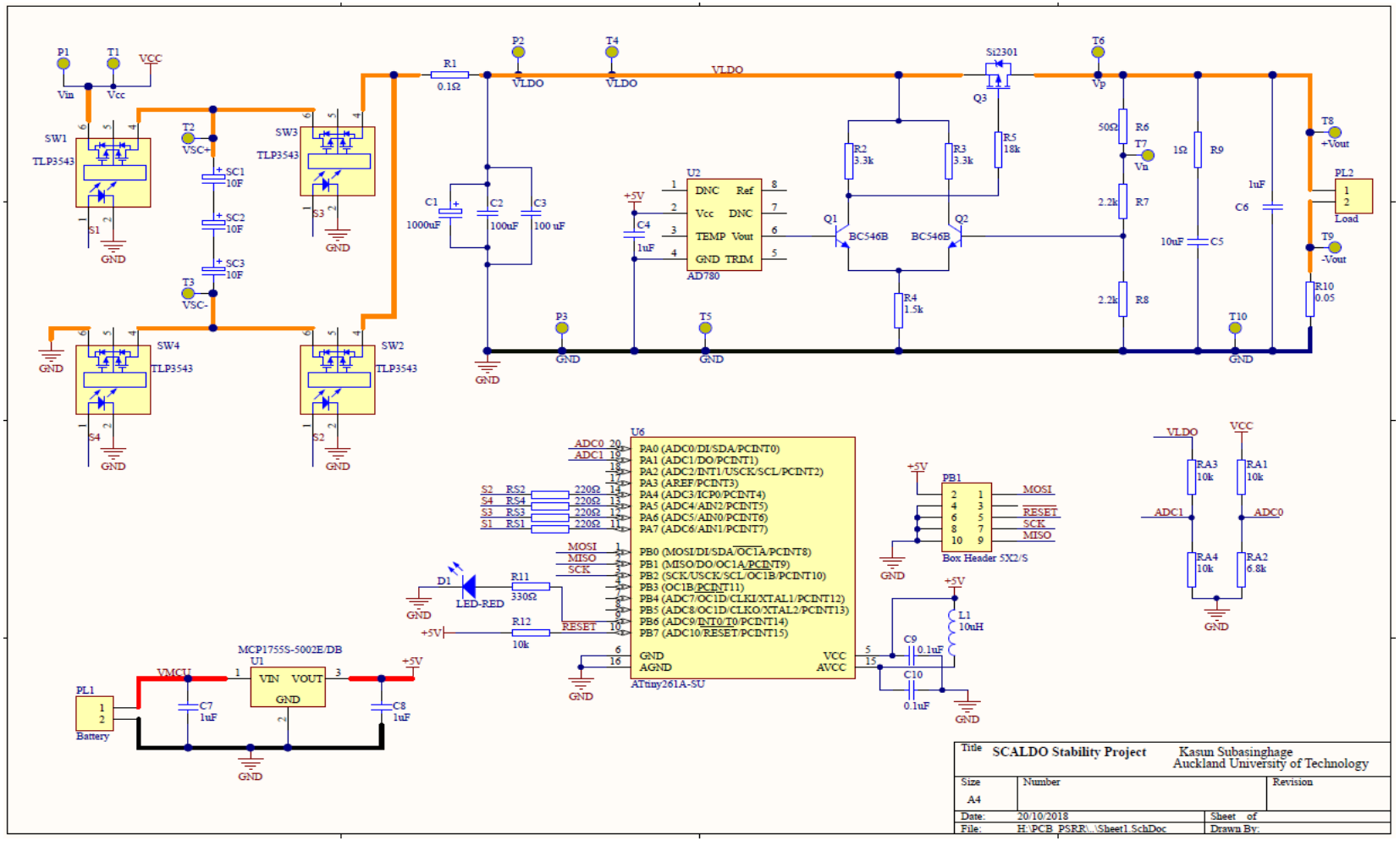


Figure B1: The schematic of the 12 V to 5 V discrete SCALDO regulator.

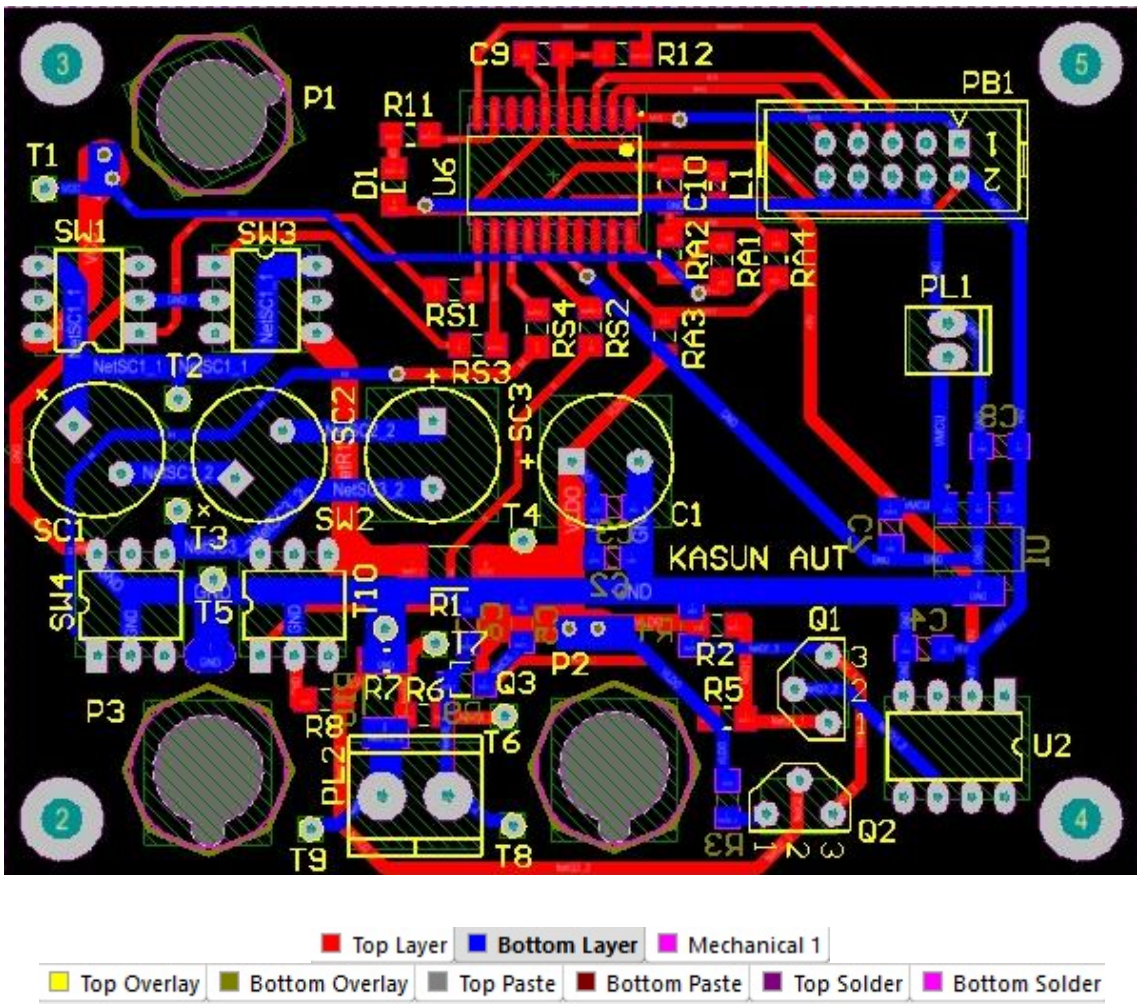
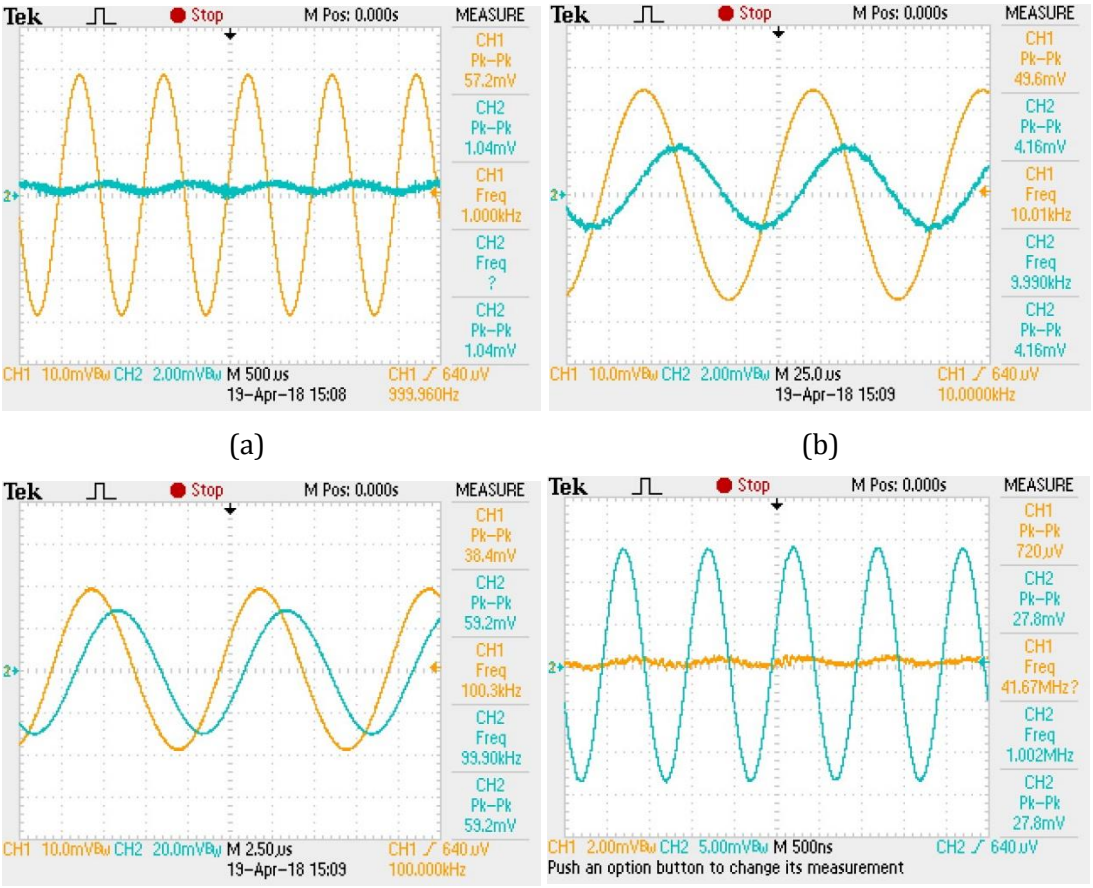


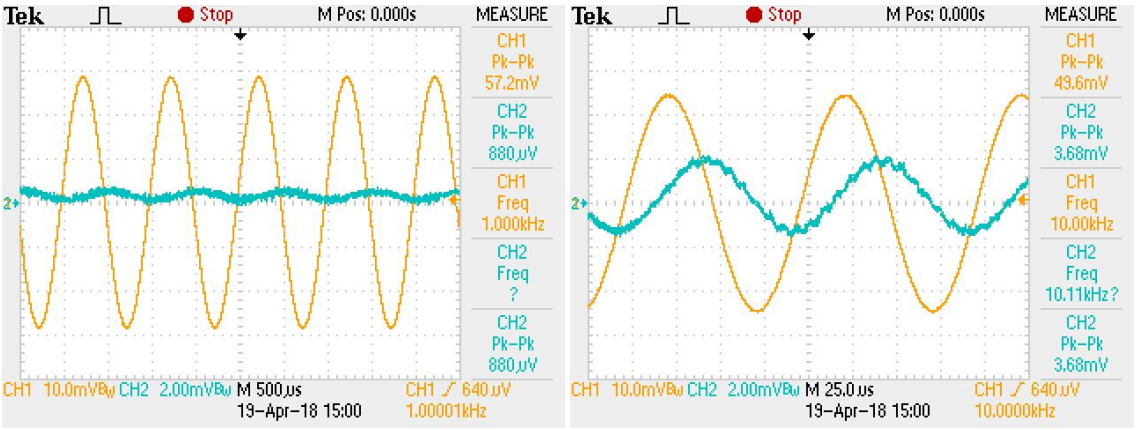
Figure B2: The PCB Layout of the 12 V to 5 V discrete SCALDO regulator.

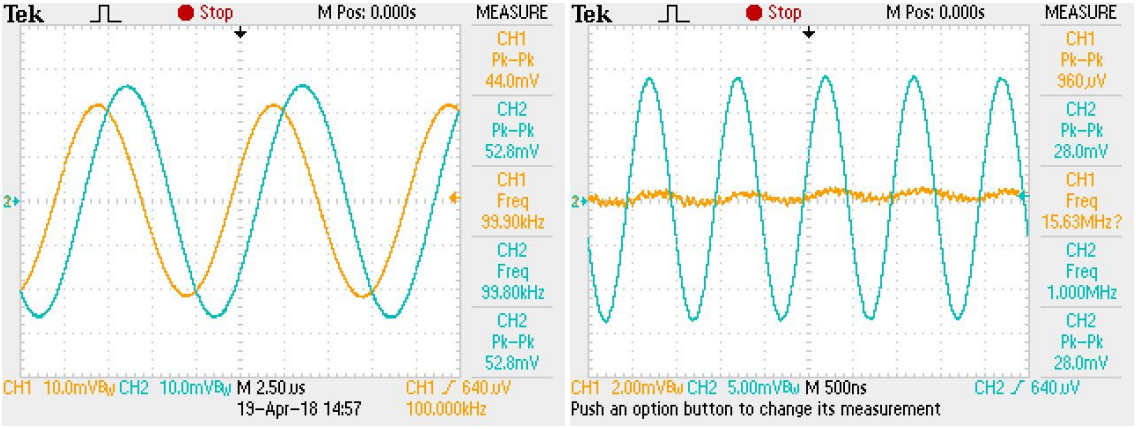
Appendix C: Oscilloscope Traces of the Open-Loop Frequency Measurements



Scope settings: CH1= $V_{P(sig)}$, CH2= $V_{N(sig)}$

Figure C1: The open-loop measurements for 100 mA of load current: (a) 1 kHz, (b) 10 kHz, (c) 100 kHz, (d) 1 MHz.





(c) (d)

Scope settings: CH1= $V_{P(sig)}$, CH2= $V_{N(sig)}$

Figure C2: The open-loop measurements for 200 mA of load current: (a) 1 kHz, (b) 10 kHz, (c) 100 kHz, (d) 1 MHz.

Appendix D: Schematics and PCB design of the 12 V to ±5 V DO-SCALDO Regulator

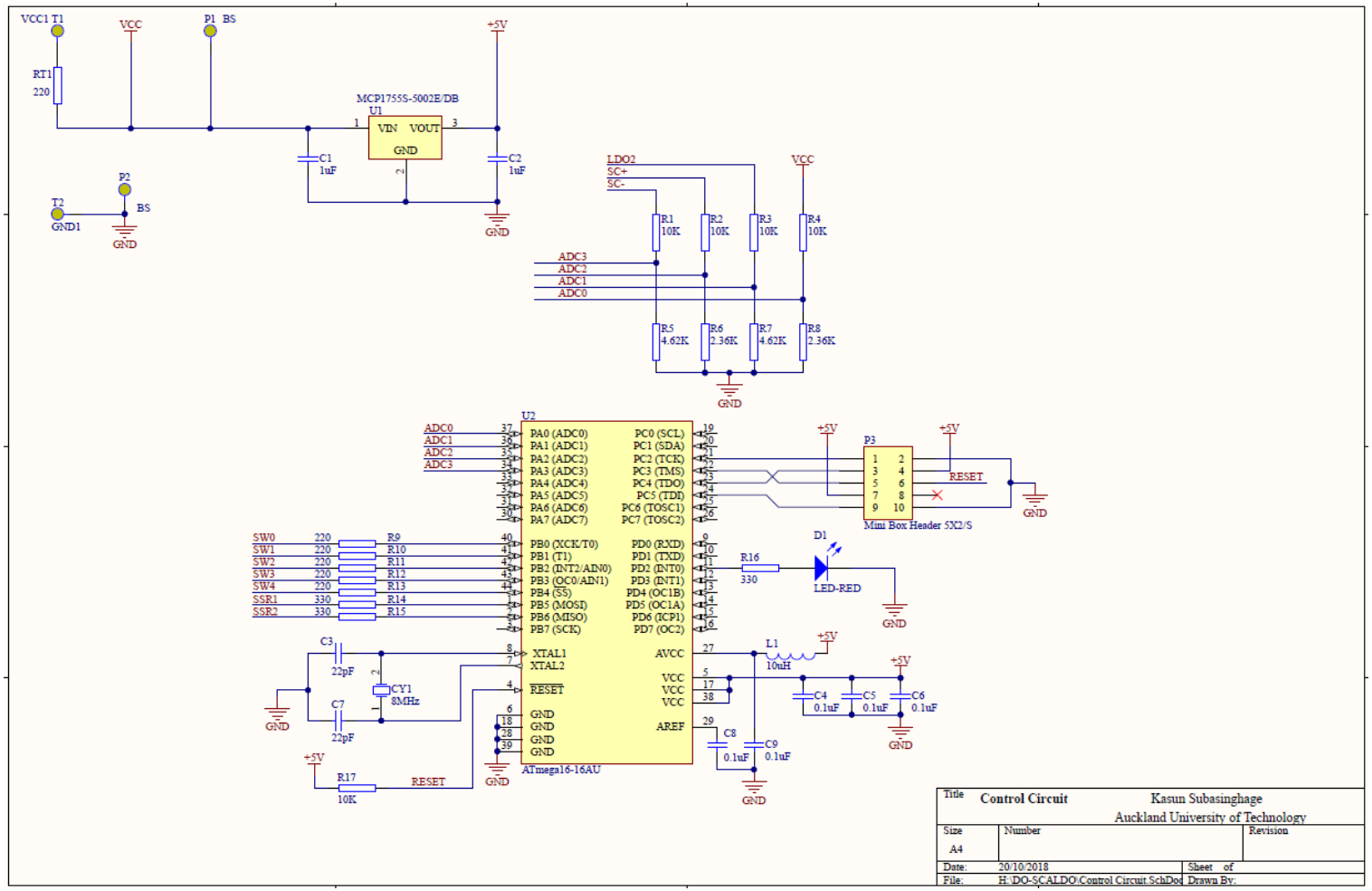


Figure D1: The schematic of the control circuit.

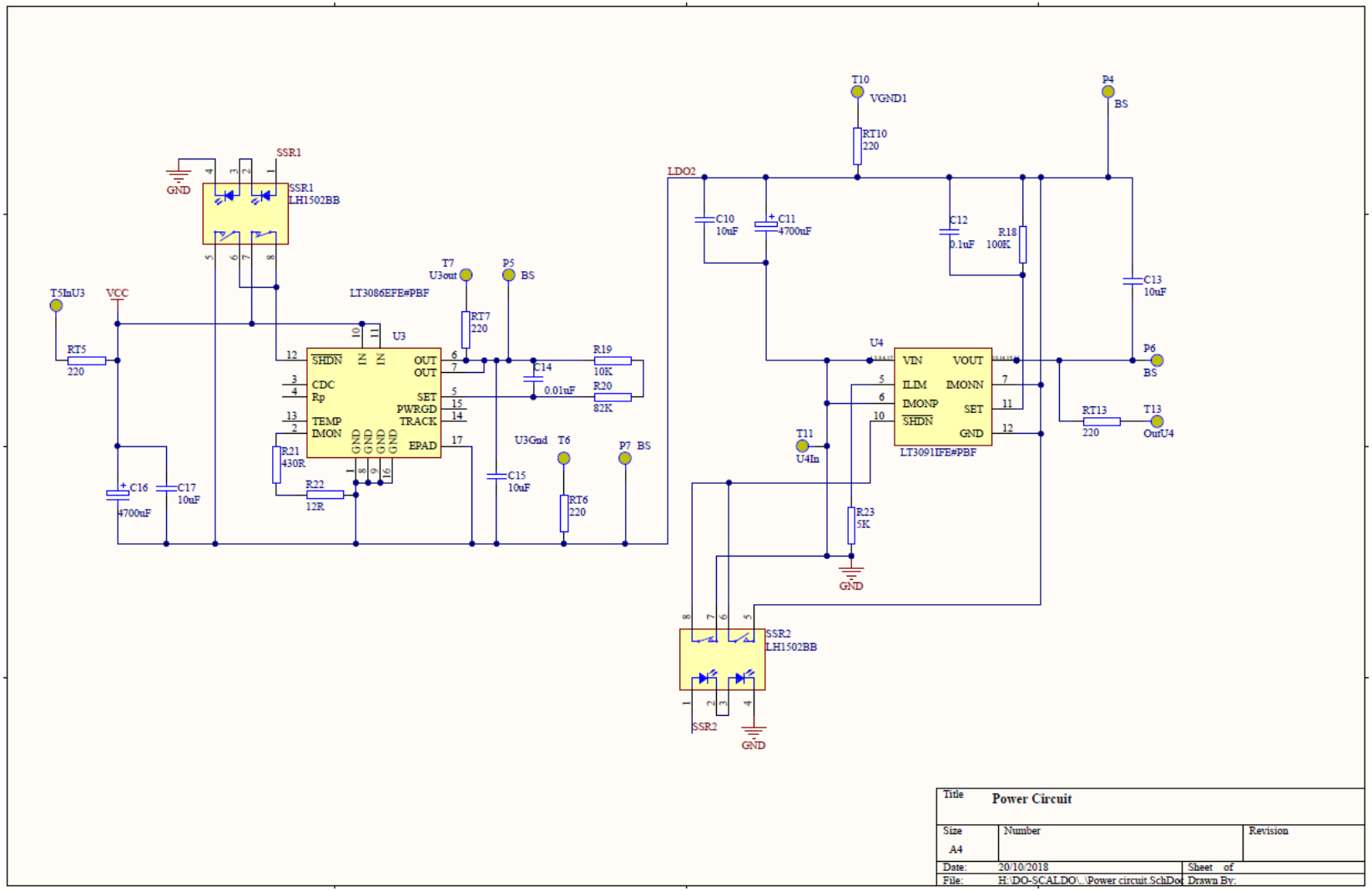


Figure D2: The schematic of the power circuit.

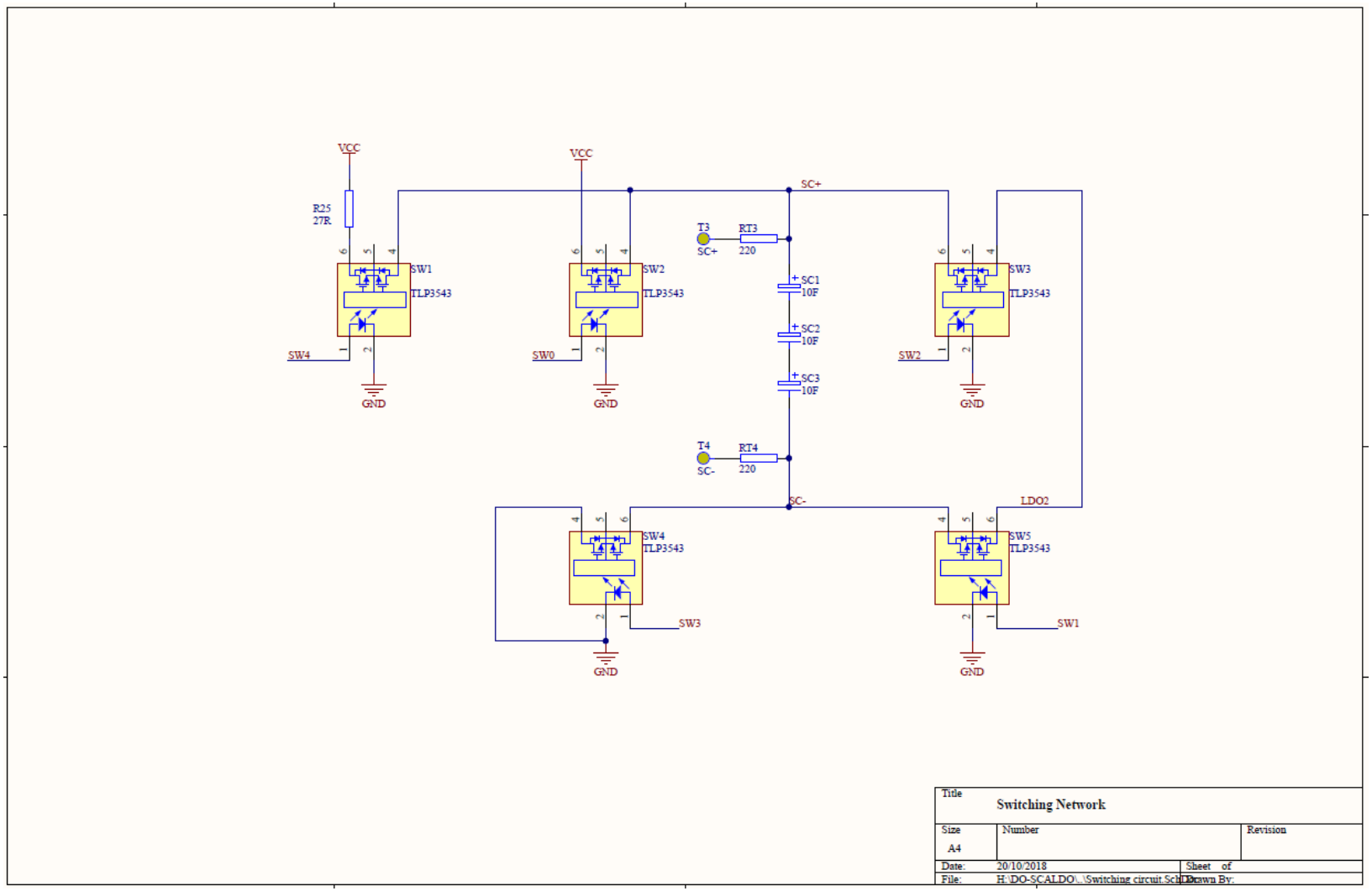


Figure D3: The schematic of the switching circuit.

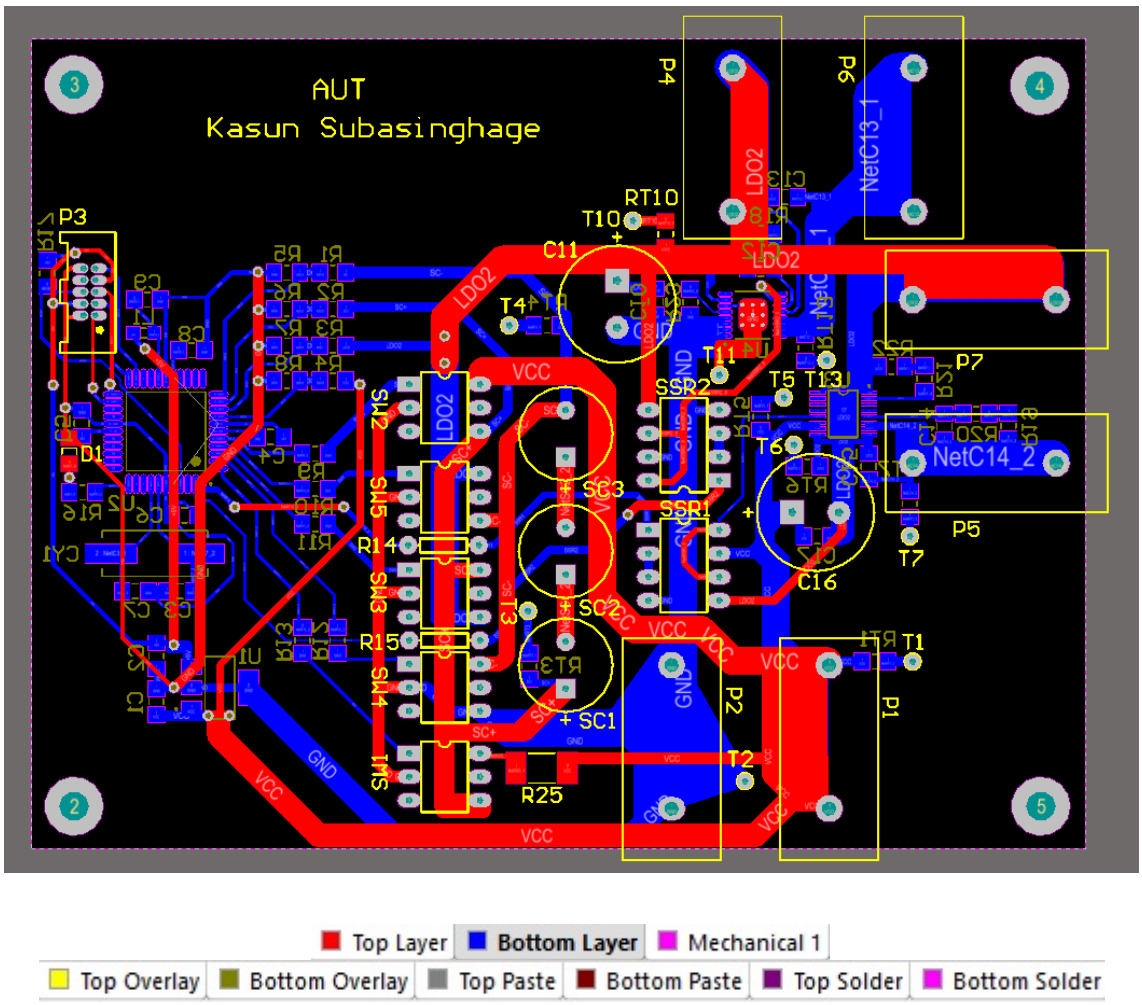


Figure D4: The PCB design of the 12 V to ±5 V DO-SCALDO regulator.

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