DESIGN OF RECONFIGURABLE MULTIBAND LOW NOISE AMPLIFIERS FOR SOFTWARE DEFINED RADIOS

A THESIS SUBMITTED TO AUCKLAND UNIVERSITY OF TECHNOLOGY
IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

Aayush Aneja
School of Engineering, Computer and Mathematical Sciences

September 2020

Attestation of Authorship

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material which to a substantial extent has been accepted for the qualification of any other degree or diploma of a university or other institution of higher learning.

Signature of candidate

Acknowledgements

I hereby express my gratitude to all those who have supported me during my time in Auckland University of Technology. The entire time span from receiving my enrolment letter to the time of writing the thesis and submitting it has been a roller coaster. Sometimes it's grappling with the circuits for the precision in my results during the experiments or dealing with the crescendo of emotions regarding other significant aspects of my life. But some people stood by me like a solid rock during the ups and downs. They are the pillars over which I could lay my foundation because I know they would never let me fall.

First and foremost, I would like to sincerely thank my primary supervisor Dr. Xue Jun Li for giving me the opportunity to do my research under his supervision and for mentoring me throughout my PhD. He has always been keen to guide me and provide me with his valuable suggestions regarding any aspect of my PhD. He nurtured my knowledge and pushed me ahead to grow and learn more. His experience has made it possible for me to achieve better results. He has always answered my queries and handled my doubts like a true mentor.

I express my sincere appreciation and gratitude towards my secondary supervisor Associate Professor Tom Moir for being very supportive during my PhD tenure. My heartiest thanks to Mr Jian Huang who just didn't help me but also guided me with his in-depth knowledge.

I express my gratitude to Professor Peter Chong, head of the department for not only

providing the required resources but also supporting me to be financially stable by providing an opportunity of teaching assistanceship. I also thank Ms Josephine Prasad, for being so supportive and taking care of me as her own family member.

I would also like to thank my parents for making all the sacrifices in their life for enabling me to achieve great heights in my life. Without them, I would be nothing.

Love and thanks to my brother, Aditya Aneja for being there for me whenever I sought someone to talk while I was stressed. My father, brother and mother-in-law for appreciating my efforts and believing in me.

I would like to thank my friends for making the journey even more memorable.

Last but not the least, to the love of my life, my dearest wife, Sheena Bassi Aneja for being there for me during the major phase of my PhD. She not only took care of me but also motivated me during my downs. She was the one I could lean on when I wanted a firm emotional support.

Aayush Aneja

September 2020

Abstract

The rapid proliferation of wireless communications necessitates software defined radios (SDRs). In an SDR receiver, a multiband LNA is the first active element, which should provide good impedance matching, adequate gain, low noise figure (NF) and low power consumption. Multiband LNAs for SDRs include Concurrent LNAs, Non-Concurrent LNAs and Reconfigurable LNAs. Existing LNA designs for SDRs have poor stopband rejection ratio, gain imbalance, low interference rejection, increased NF, degraded linearity and reduced operational bandwidth.

To fill these research gaps, firstly we propose a step-wise impedance scaling method to design concurrent multiband matching networks for LNAs. Subsequently, we design a dual band LNA (1.1GHz and 2.4GHz) that substantially reduces the in-band interference, stopband rejection ratio and gain imbalance between bands.

Thereafter, we propose the design of a continuously tunable LNA using a transformer-based input matching network for dynamic frequency tuning. The designed LNA has a wide tuning range (2.2 GHz$\sim$2.8 GHz) and the input impedance is dynamically tuned by controlling the bias voltage of the tuning transistor.

Next, we propose the design of a multimode LNA with a tunable input matching network that provides a wide tuning and operating range (0.9 GHz$\sim$2.5 GHz). By varying the biasing condition of the varactors, the designed LNA operates in six different modes. The LNA achieves a high gain, low noise, high interference rejection along with linear and stable operation in all modes.

Finally, we propose the design of a reconfigurable LNA with the continuous tuning of operational bandwidth and frequency in two separate switchable bands. The LNA implements a PIN diode in the input matching stage to reconfigure between the low band (0.2$\sim$1.5 GHz) and the high band (2.2$\sim$3.2 GHz). A varactor diode is added to the output load network of the LNA. The reverse bias voltage of varactor diode is varied to achieve continuous bandwidth tuning within each band.

This research proposes the design of multiband concurrent and reconfigurable LNAs for SDRs to achieve (i) wide tunable/switchable operational bandwidth with continuous tuning, (ii) high interference rejection, (iii) good linearity-gain trade-off, (iv) wide operating range, (v) improved stop band rejection ratio. Starting from mathematical derivation and modelling, we perform extensive simulation studies, and then fabricate the designed LNAs as microwave integrated circuits on printed circuit boards to obtain measurement results. Finally, we compare the analytical results, simulation results with measurement results in terms of gain, noise, linearity, and impedance matching. For future work, switchable LNAs together with field programmable grate arrays (FPGAs) can be investigated.

Publications

C1: **Aayush Aneja**, Xue Jun Li, Brandt Erfeng Li, “Design of a continuously tunable low noise amplifier for multiband radio," in Proc. of *IEEE Mediterranean Microwave Symposium*, Marseilles, France, pp. 1–4, 28-30 November 2017.

C2: **Aayush Aneja**, Xue Jun Li, “A 1.2 and 2.4 GHz variable gain concurrent dual band low noise amplifier," in Proc. of *IEEE Asia Pacific Microwave Conference*, Kuala Lumpur, Malaysia, pp. 1258–1261, 13-16 November 2017.

J1: **Aayush Aneja**, Xue Jun Li, “Multiband LNAs for Software-Defined Radios: Recent Advances in the Design of Multiband Reconfigurable LNAs for SDRs in CMOS, Microwave Integrated Circuits Technology," *IEEE Microwave Magazine*, vol.21, no. 7, pp. 37–53, 2020.

J2: **Aayush Aneja**, Xue Jun Li, “Design and Analysis of a Continuously Tunable Low Noise Amplifier for Software Defined Radio," *Sensors*, vol. 19, no. 6, pp. 1273–1286, 2019.

J3: **Aayush Aneja**, Xue Jun Li, “Design of a multimode tunable low noise amplifier for software defined radios," *Electronics Letters*, vol. 56, no. 16, pp. 808–810, 2020.

J4: **Aayush Aneja**, Xue Jun Li, Peter Han Joo Chong, “Design and Analysis of a 1.1 and 2.4 GHz Concurrent Dual-band Low Noise Amplifier for Multiband Radios," *AEU - International Journal of Electronics and Communication*, 2021.

J5: **Aayush Aneja**, Xue Jun Li, Adnan Ghaffar, “Design of concurrent multiband matching networks for low noise amplifiers in software defined radio, **under review**, *Circuits, Systems and Signal Processing*, 2021.

J6: **Aayush Aneja**, Xue Jun Li, “Design and analysis of a reconfigurable wideband LNA for software defined radio," **under review**, in *IEEE Microwave and Wireless Component Letters*, 2020.

Contents

List of Tables

List of Figures

Glossary and Notations

Glossary

ADC	Analog to Digital Converter
ADS	Advanced Design System
APS	Active Phase Shifter
ASIC	Analog Semiconductor Integrated Circuit
BPF	Bandpass filter
BW	Bandwidth
CA	Carrier Aggregation
CG	Common Gate
CMOS	Complementary Metal-Oxide Semiconductor
CRLNA	Common Resistive Low Noise Amplifier
CS	Common Source
CTLNA	Continuously Tunable Low Noise Amplifier
dB	Decibels
DBIMN	Dualband Input Matching Network
DBLNA	Dualband Low Noise Amplifier
DC	Direct Current
DSP	Digital Signal Processing
EM	Electromagnetic

FIR	Finite Impluse Response
FOM	Figure-of-Merit
FPGA	Field Programmable Gate Arrays
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHz	Giga Hertz
GI	Gain Imbalance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
Hz	Hertz
I/Q	In-Phase Quadrature
IDCS	Inductively Degenerated Common Source
IDE	Integrated Design Environment
IF	Intermediate Frequency
IFTT	Impedance and Frequency Transformation Technique
IMN	Input Matching Network
IR	Interference Rejection
IRL	Input Return Loss
JFET	Junction Field Effect Transistor
LNA	Low Noise Amplifier
LTE	Long-term Evolution
MBIMN	Multiband Input Matching Network
MBLNA	Multiband Low Noise Amplifier
MEMS	Micro-Electromechanical Systems
MIC	Microwave Integrated Circuit
MIT	Multiband Impedance Transformer

MMIC	Monolithic Microwave Integrated Circuits
mmWave	Millimeter Wave
mW	Milliwatt
NF	Noise Figure
NMOS	N-Type Metal-Oxide Semiconductor
OMN	Output Matching Network
ORL	Output Return Loss
PA	Power Amplifier
PCB	Printed Circuit Board
PCRF	Phase Change Radio Frequency
PHEMT	Pseudomorphic High Electron Mobility Transistor
PI	Phase Imbalance
PIN	Positive-Intrinsic-Negative
PMOS	P-Type Metal-Oxide Semiconductor
Q**-Factor**	Quality Factor
RF	Radio Frequency
RFLNA	Resistive Feedback Low Noise Amplifier
SBRR	Stopband Rejection Ratio
SDR	Software Defined Radio
Si-Ge	Silicon-Germanium
SISL	Substrate Integrated Suspended Line
SMA	SubMiniature Version A
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SP	Scattering Parameters
SR	Software Radio

TBIMN	Triband Input Matching Network
TGLNA	Tunable Gain Low Noise Amplifier
TL	Transmission Line
USRP	Universal Software Radio Peripheral
UWB	Ultra Wideband
VGA	Variable Gain Amplifier
WLAN	Wireless Local Area Network

Notations

α	Ratio of currents
α_M	Ratio of Transcondutance to Collector Conductance
β	Propagation Constant
Δ	Stability Constant
ϵ_r	Dielectric Constant
Γ_{in}	Input Reflection Coefficient
Γ_{out}	Output Reflection Coefficient
λ	Wavelength
μ	Stability Criterion
ω	Angular Frequency in radians/s
Ω	Ohms
ϕ	Phase Shift
θ	Angle
A_p	Power Gain
A_v	Voltage Gain
C	Capacitor
C_{gs}	Gate-Source Capacitance
C_{be}	Base-Emitter Capacitance
f	Frequency
F	Noise Factor
f_{op}	Operating Frequency
g_m	Transconductance
h	Height of Substrate
I_{in}	Input Current

I_{out}	Output Current
P_{1dB}	1-dB Gain Compression Point
K	Stability Factor
P_{DC}	DC Power Dissipation
P_{in}	Input RF Power
P_{out}	Output RF Power
S_{11}	Input Return Loss
S_{21}	Transmission Coefficient
S_{12}	Reverse Transmission Coefficient
S_{21}	Output Return Loss
V_{DD}	Supply Voltage
V_{DS}	Drain Source Voltage
V_{GS}	Gate Source Voltage
V_{in}	RF Input Voltage
$V_{n,s}$	Noise Voltage due to Source
V_{out}	RF Output Voltage
X	Reactance
Z_{in}	Input Impedance
Z_L	Load Impedance
Z_{out}	Output Impedance
Z_s	Source Impedance
Z_0	Characteristic Impedance

Chapter 1

Introduction

1.1 Background

The history of wireless radio communication dates back to 1864, when James Clark Maxwell showed mathematically that electromagnetic (EM) waves could propagate through free space. This led to the development of first fully operational radio transceiver by Marconi in the year 1894. Since then, a number of radios were developed that could operate from few Kilo Hertz (KHz) to several Giga Hertz (GHz) [1]. Further research led to the development of conventional digital radio that could digitally modulate or demodulate the information signal.

Subsequent advancement in communication systems led to the development of wireless standards for cellular, mobile and personal area communication such as 2G, 3G, long-term evolution (LTE), wireless local area network (WLAN), Bluetooth, ultra wideband (UWB), etc. A traditional radio adopts a radio frequency (RF) signal to transmit or receive information. However, it usually features a bulky device. Additionally, it is usually costly and has high power consumption

With technology advancement in analog semiconductor integrated circuit (ASIC) design processes, it is now possible to design a fully functional radio transceiver front-end

on a tiny chip. Additionally, a complete radio system can be accomplished on a small printed circuit board (PCB). Nevertheless, their operation in specialised applications still require additional bulky and complex circuits to operate with multiple frequency channels, RF power modes and modulation schemes. Due to surge in the demand for high data rates and increasing wireless standards, multiband operation, reconfigurable modes and intelligent modulation techniques were still required to solve major radio communication problems. This led to the development of software defined radios (SDRs) and cognitive radio.

1.2 SDRs

The last decade has witnessed an increasing number of wireless standards for civil, military and astronomical communications. Along with advance of integrated circuit (IC) technologies and ever-growing requirements of high data rates, next-generation radios are expected to operate over multiple frequency bands in a single system. For example, carrier aggregation (CA) is used in LTE - Advanced in order to increase the bandwidth. It is challenging for traditional radios to operate over multiple frequency bands. Contrary to traditional radios, SDRs can handle multiple wireless standards (at different frequency bands or at the same frequency band) simultaneously or discretely, with a sole reconfigurable hardware system [2]. SDRs can - (i) work at different channels, (ii) adapt to multiple disparate carrier frequencies, (iii) fix a software bug during operation and (iv) cancellation of interfering bands through software.

In general, SDR is an umbrella term for Software Based Radio (SBR) or Software Radio (SR) [3]. Nevertheless, some researchers argue that SDR is an advanced version of SBR, while SR is in its conceptual stage.

SDRs were originally proposed for military communications, especially when military

personnel had to use multiple and bulky traditional radios for communication in battle-ground and patrolling [4]. Recently, the focus of SDRs has been shifted to commercial civil communications.

1.2.1 Why SDR?

The motivation behind extensive research in SDR technology originated from the fact that legacy communication systems are approaching their capability limits. For example, they usually operate on single band and require a dedicated hardware. However, customers require devices that can provide ubiquitous seamless connectivity through network interoperability of various wireless standards, as well as reduced cost [5]. SDR is a propitious radio technology that offers a cost effective solution to increase the radio system capabilities with minimum hardware requirement, small size and ultra low power.

As shown in Figure 1.1, an SDR can be viewed as a radio that implements a specified range of capabilities through elements that are software-reconfigurable [6]. An SDR front-end supports multiband operation. For reception, antenna and low noise amplifier (LNA) are required to capture and amplify the signal, respectively, followed by digitisation using analog-to-digital converter (ADC) and modification in field programmable gate arrays (FPGAs) and digital signal processing (DSP) modules [7]. For transmission, antenna and power amplifier (PA) are required [4].

Modern digital radios include DSP, while SDR is an enhanced version of digital radios in the sense that SDR is capable of configuring operational parameters through software [8]. In the analog domain, SDRs adopt hardware, such as antennas, LNAs, PAs with reconfigurability to support multiband operations. In the digital domain, SDRs implement DSP algorithms running in the host computer. Therefore, various configurations can be achieved by modifying the DSP algorithms. These configurations

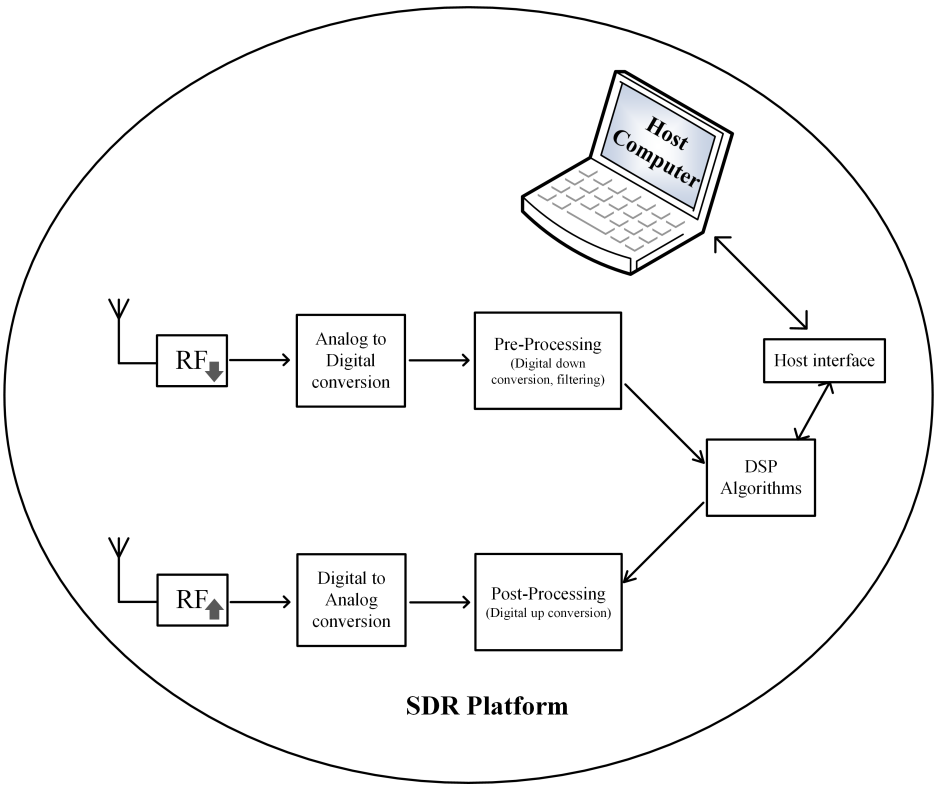


Figure 1.1: Typical structure of a software defined radio platform

include modulation/ de-modulation, multiple access schemes, encryption/decryption and frequency spreading. For example, SDRs may use system–on–chip (SoC) like DM644x for digital baseband processing. This is contrary to the conventional analog radios, in which changes in hardware are necessary in order to alter their fundamental characteristics [9].

1.2.2 Requirements in SDR

One of the major advantages of SDRs is that it allows implementation of radio functionality in software, which was previously challenging or even impossible to achieve by changing hardware for traditional analog radios. Current researches in this area have focused on the flexibility of SDR [10]. An ideal SDR may adopt 2 - 3 analog channel filters to provide switchable band configuration. However, this leads to reduced

flexibility. A flexible SDR requires minimum analog components, maximum software capabilities and minimum power consumption. Additionally, modern handheld and compact SDR systems require sufficient cooling to handle increasing currents due to high processing values.

1.2.3 SDR Hardware

Mobile technology demands for hardware miniaturization and SDR offers a promising way to replace most hardware in a transceiver by its software counterpart. Recent researches on SDRs [11] focus on employing FPGAs as hardware accelerator to overcome the host computer's processing bottleneck to support complex algorithms. A popular example of SDR employing a reconfigurable hardware is Reconfigurable Hardware Interface for Computing and Radio (RHINO) project that has an open source interface, which is used for educational purposes. It has an ARM Cortex A8 processor for digital baseband and signal processing. Figure 1.2 shows the receiver front-end circuit of a modern SDR. Nevertheless, there exist significant obstacles that prevent the full implementation of SDRs. Take a receiver for example, it is still challenging to design antennas [12], LNAs [13] and mixers [14] for SDRs.

In particular, the design of LNA for SDR poses several challenges. These challenges include designing LNAs which operate at multiple frequency bands and must achieve minimum desirable performance metrics in each band. SDRs require that the LNAs must be flexible and must have a wide operating range. In most cases, it is required that LNA be switchable or tunable and hence it is challenging for the microwave design engineer to achieve dynamic switching/tuning while suppressing noise, interfering signals and gain imbalance at all bands. These challenges are aggravated due to parasitic impedances, substrate losses and different load impedances. Furthermore, specific trade-offs such as the gain-linearity trade-off, are required to be overcome for all operational bands.

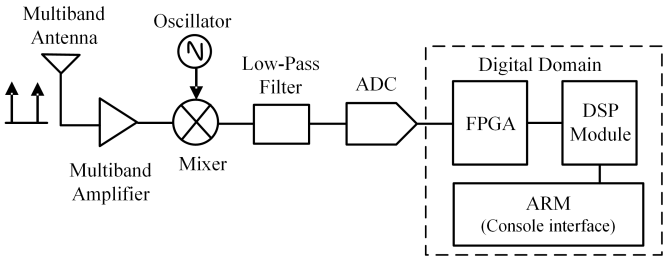


Figure 1.2: A general multiband SDR receiver architecture

1.3 Research Questions

The following four research questions are considered in this thesis.

- Question 1: How can we propose a step-wise impedance scaling method for designing concurrent multiband matching networks for SDR LNAs?
- Question 2: How can we design a concurrent dual band LNA with high performance metrics while minimising the interference between bands and gain imbalance at the same time?
- Question 3: How can we design a continuously tunable LNA with dynamic tuning of operating frequency?
- Question 4: How can we improve the operating range of a multiband reconfigurable LNA?

1.4 Objectives

The objective of this research is to design, develop and analyse novel concurrent and reconfigurable multiband LNA circuits for SDRs with a high Figure of Merit (FOM). Recent works on reconfigurable LNA reveal that improving the LNA operating range, minimising interference and wide tunable bandwidth is an immediate necessity to make the SDR platforms more flexible. An ideal SDR requires a flexible RF front-end

that must not only support both wideband transmission at a high operating frequency, and a large centre frequency range, but also be able to adjust its operating frequency and/or transmission bandwidth so as to avoid interference with other wireless services. Additionally, it must consume low power for optimum performance, for extending battery life in portable devices and for reducing interference.
This research aims to design and fabricate LNAs for SDR receivers that attempt to address the specific design challenges.

1.5 Research Contributions

This thesis makes the following contributions to the development of reconfigurable LNAs for SDRs.

1. We propose a methodology for designing novel dual band and triband impedance matching networks using impedance and frequency transformation technique.

2. We propose the design and analysis of a novel concurrent dual band LNA with a high gain, high interference and stopband rejection ratios, less gain imbalance and very low NF.

3. We perform the design and analysis of a novel continuously tunable LNA with a transformer based impedance matching network and dynamic frequency tuning.

4. We propose the design and analysis of a novel multi mode LNA for SDR that implements an input tunable matching network to increase the operating range of LNA.

5. We propose the design and analysis of a novel reconfigurable dual band LNA with continuous tuning of operational bandwidth/frequency range in each wide band.

Noteworthily, the designed LNAs follow the hierarchical categorisation of LNAs for SDRs. The LNA proposed in research contribution 2 is a concurrent dualband LNA that uses the impedance matching scheme proposed in contribution 1. The proposed SDR LNAs in research contribution 3 and 4 are input tunable LNAs. The tunable LNA design in contribution 4 has a wider operating range and shows multiple operation modes. Finally, the reconfigurable LNA proposed in contribution 5 demonstrates switchable and output tunable configuration. Furthermore, tunability in contribution 4 and 5 in the input matching and output matching stage, respectively is achieved using the same varactor diode to obtain desired results.

1.6 Thesis Organisation

The thesis is organised in eight chapters.

Chapter 1 explains the background of the SDR, research gaps, motivations and the objectives of this research.

Chapter 2 gives a comprehensive review of the LNA designs for SDR.

Chapter 3 presents the design of dual band and triband matching networks for concurrent multiband LNAs.

Chapter 4 presents the design of a two-stage concurrent dual band LNA with state-of-the art performance metrics including high gain and high interference rejection ratio. The LNA's input matching network is constructed using the design equations proposed in Chapter 3.

Chapter 5 presents the design of a continuously tunable LNA using a transformer based matching network for dynamic frequency tuning.

Chapter 6 presents the design of a multimode LNA with a novel tunable input matching network to increase the operating range of SDR LNA.

Chapter 7 presents the design of a wideband reconfigurable LNA with a switchable

input matching network and continuously tunable output matching network. The LNA operates in two separate bands and provides continuous bandwidth tuning in each band. Finally, Chapter 8 concludes the whole research, and provides recommendations for future research on this topic.

Chapter 2

Literature Review

2.1 SDR Receiver Architectures

To fully comprehend the concept of LNA, it is important to review fundamental SDR receiver architectures. In traditional radios, receiver front-ends are mainly categorised into two main types, namely heterodyne receivers and homodyne receivers. Heterodyne receivers have been primarily used for narrowband applications [15], which is due to their high receiver sensitivity and selectivity. With the advancement of complementary metal-oxide semiconductor (CMOS) technologies, the problems associated with heterodyne receivers such as image rejection and third order intermodulation disorders have aggravated. On the other hand, homodyne receivers are resistant to problems related to image-rejection. Nevertheless, the overall performance of the homodyne receiver circuits can be corrupted by flicker noise and DC offsets. The noise constraint in homodyne receivers can be extenuated by adopting weaver architecture [16] or image reject topology [17].

Likewise, to overcome the linearity constraint of heterodyne receivers, inductively degenerated common source (IDCS) topology and cascode parallel feedback in LNAs and mixers have been adopted in the literature, but these topologies have associated

drawbacks such as reduced receiver gain.

The key difference between SDR and traditional radio lies in its reconfigurability—SDR can adapt its communication protocols through software, while it is difficult or impossible for traditional radio to achieve this. SDR implements software-based modulations, demodulations, signal processing, and encoding. As such, front-end hardware components for SDR must be reconfigurable [18].

The three well known configurations for SDR receiver front-ends are - (i) Superheterodyne receiver (ii) Zero-intermediate frequency (IF) receiver (iii) Bandpass sampling receiver [2]. Figure 2.1 (a), (b) and (c) show the architecture of all three configurations. Superheterodyne reciever configuration is primarily used for high frequency microwave and millimeter wave (mmWave) communication [19]. It uses an image-reject filter in the mixer stage. This configuration is not a popular choice for SDR receivers because of single channel restriction, difficult integration, limited bandwidth and complex multiband reception. The Zero-IF configuration [20] is a simpler yet highly efficient version of superheterodyne receiver. This receiver deploys an in-phase quadrature (I/Q) mixer and an anlog filtering stage. I/Q mixers have minimum on-chip integration requirements as compared to image-reject mixers. Thus, Zero-IF configuration is a popular choice for multiband and SDR receivers. However, the baseband signal output at the mixer is vulnerable to corruption due to flicker noise in Zero-IF configuration.

Finally, the bandpass sampling receiver [21] overcomes the aforesaid shortcomings by using a tunable filter or LNA and digitally processing the sampled signal. Due to reduced components, integration is easy, which currently makes it a popular choice for SDR receivers. The associated drawback is phase - gain mismatch that can be overcome by gain control technique.

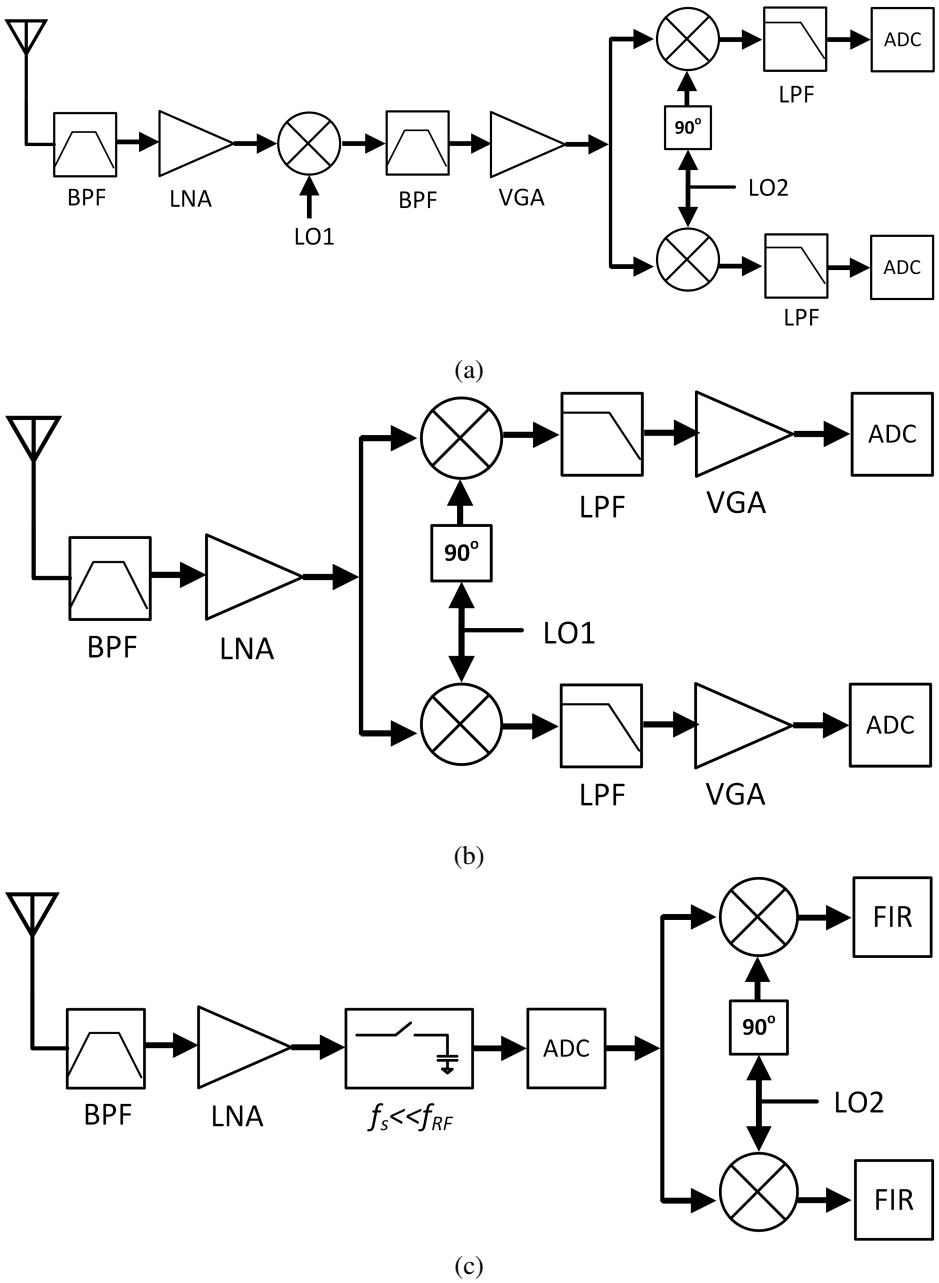


Figure 2.1: (a) Superheterodyne receiver architecture (b) Zero-IF receiver architecture (c) Bandpass sampling receiver [2]

2.2 Low Noise Amplifier

The LNA is the first active element in a radio receiver chain. The primary purpose of LNA is to amplify a very low power signal present at its input without significantly degrading its signal-to-noise ratio (SNR). Contrary to regular amplifiers, LNAs consider

the presence of larger signals and minimise intermodulation distortion.

2.2.1 LNA Basics

Important performance metrics for LNAs that are summarised as follows.

a. Gain The ability of the LNA to amplify the radio signal is known as LNA gain. It can be mathematically expressed as

$$A_p = \frac{P_{out}}{P_{in}} \tag{2.1}$$

where A_p is the power gain, P_{out} and P_{in} are the output and input power, respectively. In the Scattering-matrix (S-matrix), the magnitude of S_{21} represents the LNA gain.

The LNA gain is usually expressed in decibels (dB) as

$$A_p(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \tag{2.2}$$

b. Noise Figure Noise figure (NF) is defined as the degradation in SNR level of the signal due to noise introduced by sources present in the circuit. In general, NF is the dB value of noise factor which is defined as the ratio of input SNR (SNR_i) to output SNR (SNR_o) of the LNA. NF is mathematically defined as

$$NF(dB) = 10\log_{10}\frac{SNR_i}{SNR_o} = 10\log_{10}\frac{P_{s_i}/P_{n_i}}{P_{s_o}/P_{n_o}} \tag{2.3}$$

where P_{s_o} and P_{s_i} are the available signal power and P_{n_o} and P_{n_i} are the available noise power at the output and input of LNA, respectively.

c. Linearity It refers to the ability of the LNA to maintain the proportionality of the input and output of the signal by augmenting power levels without transforming

signal content. Problems arising due to non-linear behaviour are second and third order intermodulation and gain compression. The linearity of LNA is measured by determining the 1-dB compression point (P_{1dB}) and third order intercept point (IP_3). P_{1dB} is the output power level at which the gain drops by 1dB from its constant value. IIP_3 is the input power level at which the power of third order components reaches the same level of the fundamental component's power.

d. Stability The LNA stability measures its tendency to oscillate at any frequency. An LNA generally operates with (i) unconditional stability or (ii) conditional stability. For a device to be unconditionally stable, the input and output port impedance must not have any negative real part. This means that $|\Gamma_{in}|$<1 and $|\Gamma_{out}|$<1 for all arbitrary source and load impedances.

Stability of the LNA can be determined by evaluating the stability factor K and stability constant Δ. The values of K and Δ can be calculated as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{21}S_{12}|} \tag{2.4}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.5}$$

The necessary stipulation for unconditional stability of an LNA is K>1 and Δ<1.

e. Input and Output Return Loss Input return loss (IRL) is defined as the power loss in a signal reflected at the input port due to discontinuity. Likewise, Output return loss (ORL) is power loss in the signal reflected at the output port of LNA. Input and output return loss are characterised by the terms S_{11} and S_{22} of the S-matrix. IRL and ORL can be mathematically calculated as

$$IRL = 10\log\frac{P_{in}}{P_r} \tag{2.6a}$$

$$ORL = 10\log\frac{P_{out}}{P_r} \tag{2.6b}$$

where P_r is the reflected power. To achieve a high return loss (RL), it is desired that the LNA input and output impedances are matched to the source and load, respectively.

f. Power Dissipation It measures the power drawn by the device from the DC power supply. Due to advancements in IC design techniques and low power technologies, it is required that LNA must have a very low power dissipation. It is commonly measured in milliwatts (mW).

Like traditional radios, SDRs rely on several key hardware components, such as an antenna, an LNA, a mixer and a PA. As shown in Table 2.1, the LNA should provide wideband impedance matching, adequate gain, low NF and low power consumption [22]. Furthermore, stable and linear operation is also desired as the performance of the LNA will significantly affect that of the whole receiver chain. Figure 2.2 shows the schematic of a typical single band LNA, which consists of an input matching network (IMN), a biasing network, a gain stage and finally an output matching network (OMN).

2.3 LNAs for SDRs

Conventional LNAs are designed to amplify desired RF signals while rejecting undesired out–of–band interfering signals. Front-end circuits in SDRs are required to handle multiple frequency bands either simultaneously or discretely. Therefore, LNAs for SDRs must possess the ability to handle multiple frequency bands. Designing an LNA for SDR at least requires a performance that meets general design specifications as indicated in Table 2.1. Moreover, LNAs for SDRs must possess additional custom requirements that are summarised in Table 2.2. LNAs for SDRs can be classified as either wideband LNAs or multiband LNAs (MBLNA). Wideband LNAs simply cover multiple frequency bands simultaneously via their wideband IMNs and OMNs. They do not selectively attenuate undesired interference signals. This may lead to stringent

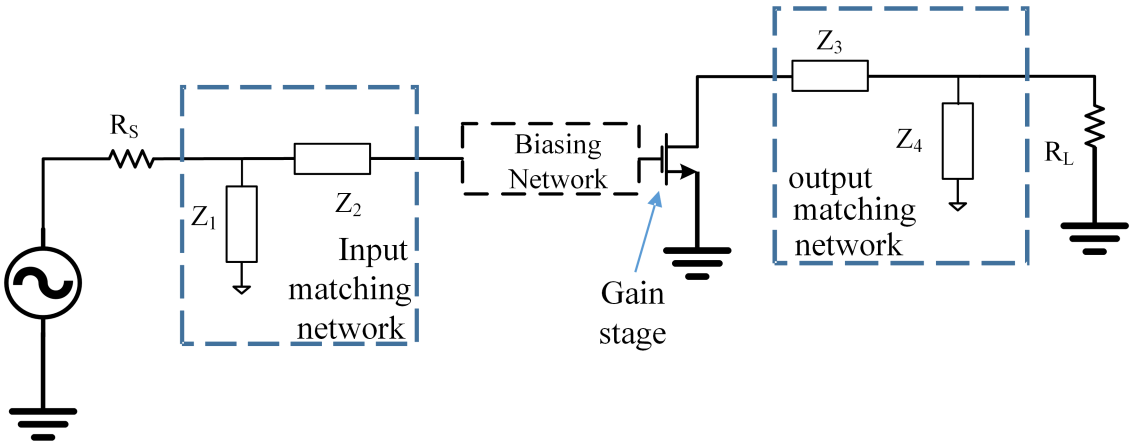


Figure 2.2: A typical single band LNA with stub matching

Table 2.1: Typical LNA design specifications

LNA Attributes	**Description**	**Typical value**
Gain	ratio of output power to input power	S_{21}>10 dB
Return Loss	losses from reflection from the ports	S_{11}<–10 dB , S_{22}<–10 dB
Noise Figure	measure of introduced noise by LNA	NF<3.5 dB
Linearity	output must be proportional to input	$IIP_3 \geqslant 0$ dBm
Stability	unconditional stability in the desired frequency range.	K >1, |Δ|<1
Power consumption	DC power drawn from the power supply	P_{DC} <20 mW
Reverse isolation	isolation from the other port	S_{12}<–30 dB

linearity requirements on the mixer and subsequent RF stages. Consequently, an LNA with multiple passbands is preferred for SDRs.

A straightforward solution to realize multiple passbands is to integrate multiple, separate narrowband LNAs in parallel [23]. However, this approach suffers from high power consumption, large circuit area, and complicated signal routing. Consequently, a single LNA with a concurrent or reconfigurable multiband operation is desired. Figure 2.3 summarizes LNA types for SDRs.

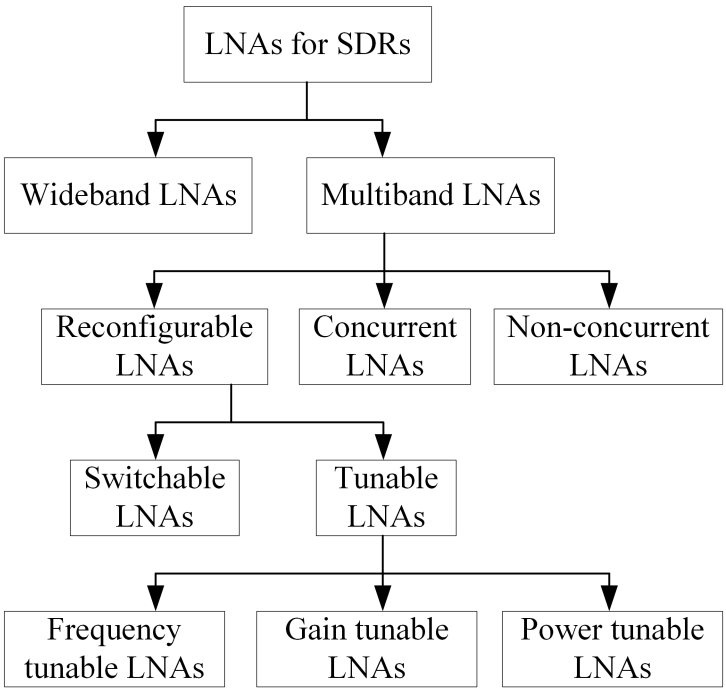


Figure 2.3: Types of LNAs for SDRs

Table 2.2: SDR LNA design specifications

Attributes	Description	Expected value
Wide spectrum	operate in wide spectrum	BW >500 MHz
Reconfigurable frequency	adjustable operating frequency	2 or more bands
Tunable gain	continuous / discrete gain variation	Tuning range >5dB
Adjustable power	switchable power operating modes	P_{DC}(min) <5mW
Stopband rejection ratio (SBRR)	difference between passband gain and stopband attenuation	SBRR>10/10
Low passband gain imbalance (GI)	difference between peak gains at different centre frequencies.	GI <2 dB
Low passband phase imbalance (PI)	difference in phase of signal at different centre frequency	PI <10°
High interference rejection ratio (IRR)	rejection of interference from adjacent bands.	IRR >20dB

BW: Bandwidth

2.3.1 Wideband LNAs

Wideband LNAs provide a flat gain response across a wide range of frequencies for certain applications [24]. For these LNAs, frequency reconfiguration requires frequency synthesizer circuits and filtering circuits (e.g., tunable bandpass filter or digital

platforms). Popular circuit topologies for wideband LNAs include: common source (CS)-common gate (CG) differential cascode topology [25], resistive shunt feedback topology, [26] inductive peaking topology [27] and distributed amplifier topology [28]. Figures. 2.4–2.6 show the typical topologies for a wideband SDR LNA.

A CS-CG cascode topology is illustrated in Figure 2.4 (a). It has high reverse isolation because of high-output impedance at the drain terminal. However, it suffers from a larger DC voltage requirement than a normal CS stage [29]. Figure 2.4 (b) shows the resistive shunt feedback topology [26], which is employed in CS LNAs to achieve a flat gain across a wide bandwidth. However, this topology results in trade-off between the NF, linearity and bandwidth of LNA. This is because the feedback resistance (R_F) is of the order of few hundred Ω so as to achieve the 50 Ω impedance match across a wide bandwidth. A low value R_F may results in high NF and low linearity, while a high value R_F may result in reduced bandwidth.

A conventional inductive or shunt peaking technique uses an inductor in parallel with the load to increase the small signal bandwidth by improving the rise time [30]. Figure 2.5 (a) shows the inverter stage with inductive peaking technique. The peaking inductor at the input of the inverter cell augments the 3-dB bandwidth. However, gain flatness is a concern for this topology. Figure 2.5 (b) shows the split-load inductive peaking technique, which is an improved version of inductive peaking. This technique can be applied at the gate of an N-type metal-oxide semiconductor (NMOS) in inversion to enhance the 3-dB bandwidth and improve rise time [27].

Figure 2.6 shows a cascaded LNA with a CG stage, followed by a CS stage with a series-shunt loading network to obtain a wideband response [31, 32]. This technique can be combined with transformer-coupling techniques to improve the noise performance of the circuit, and for gain enhancement and neutralization. However, transformer coupling may result in distortions as third order intermodulation products, leading to degraded linearity.

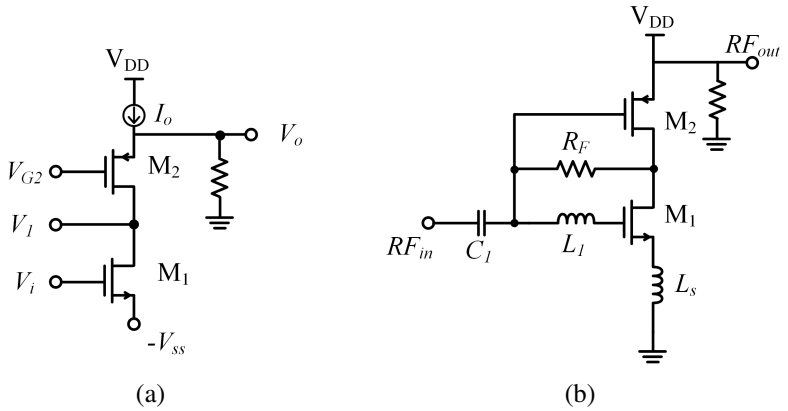


Figure 2.4: (a) CG-CS cascode topology (b) Resistive shunt feedback

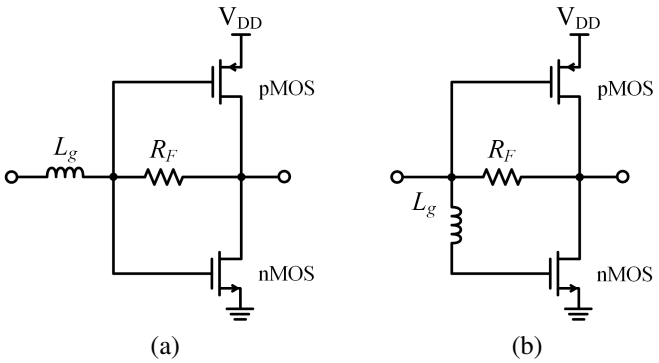


Figure 2.5: (a) Inverter stage inductive peaking (b) Split load inductive peaking [27]

Current research in wideband SDR LNA design focuses on inductorless architectures in order to reduce chip size, reduce power consumption, and improve linearity. For example, reported inductorless architectures for wideband LNA design include active shunt feedback [22, 33, 34], active inductors [35], and differential circuits [36].

For wideband SDR LNAs, capacitive parasitics associated with CMOS transistors require extra attention as they reduce the effective gain and increase the NF, especially for LNAs with distributed topology. While, these parasitics can be tuned out using inductors for a narrowband LNA design [37], the concern still remains and needs to be addressed for wideband SDR LNAs.

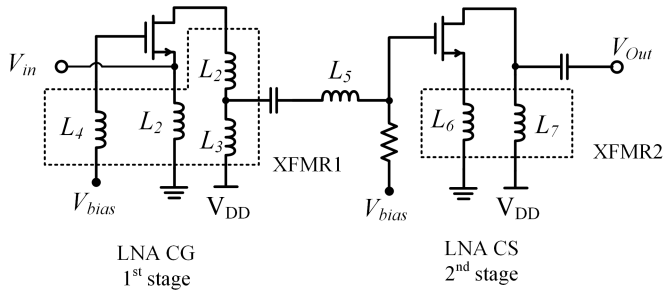


Figure 2.6: Cascaded LNA stages with transformer coupling for wideband response [31]

2.4 Multiband LNAs

MBLNAs can handle multiple bands concurrently, or switch to a particular band in a continuous or discrete manner. MBLNAs are divided into three major categories:

Concurrent MBLNAs Concurrent MBLNAs provide concurrent reception of amplified signal in multiple frequency bands, which is achieved by either manipulating the operation condition of active devices, or configuring input/output matching networks and output loads [38]. Concurrent MBLNAs can handle multiple frequency bands simultaneously. They reject the stopband signals and amplify the passband signals. In addition, they can improve the system efficiency by reducing power consumption because the same transconductance element is used for multiple bands [39].

Non-Concurrent MBLNAs Non-concurrent MBLNAs can operate at multiple frequency bands, but cannot handle them concurrently. They adopt passive matching networks for band selection [38].

Reconfigurable MBLNAs Reconfigurable MBLNAs are similar to non-concurrent MBLNAs, but with reconfiguration of matching components / bias voltages in the input or output matching stage.

2.4.1 Concurrent MBLNAs

Concurrent MBLNAs have the capability to handle multiple frequency bands simultaneously. They are preferred over wideband LNAs for multiband radios because of their capability to reject the stopband signals and amplify the passband signals. In addition, they can improve the system efficiency by reducing power consumption because the same transconductance element is used for multiple bands [39]. To design a concurrent MBLNA, it is required that the input and output impedance matching is achieved at the desired operating frequencies. Moreover, a multiband load is needed to get the desired S_{21} response at the output.

The first concurrent MBLNA was a dual band LNA (DBLNA) implemented in 0.35μm CMOS technology in 2002 [40]. Since then, several concurrent MBLNA architectures have been proposed to improve the SBRR, reduce noise, improve linearity, increase output power, and minimize GI. Figure 2.7 (a) shows the design of a conventional concurrent DBLNA that consists of a wideband IMN and a dual band load. Its input impedance can be expressed as

$$Z_{in} = j\omega L_1 + \left(j\omega L_2 \| \frac{1}{j\omega C_1} \right) \| R_1 \| \left(\frac{1}{j\omega(C_{gs1} + C_{ex})} + j\omega L_s + \frac{g_m L_s}{C_{gs1} + C_{ex}} \right) \tag{2.7}$$

where g_m, C_{gs1} are the transconductance, gate-source capacitance, respectively of transistor M_1 and L_s is the source inductance. The wideband input matching implies additional filtering and cautious frequency planning to deal with interference. Consequently, a multiband IMN (MBIMN) is desired.

Multiband impedance transformer (MIT) [41] is widely adopted to provide multiband input matching, out-of-band interference suppression, and noise reduction. However, this technique increases on board circuit area and power consumption. Another technique is to implement transmission line stubs with coupled lines as impedance transformers

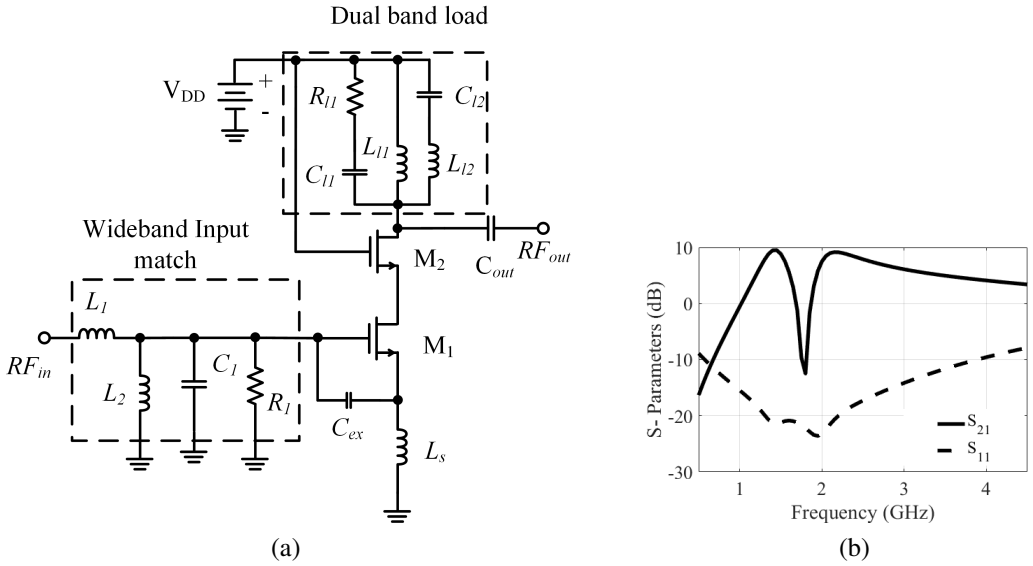


Figure 2.7: (a) Conventional DBLNA architecture [40] (b) Gain and IRL for conventional DBLNA

[42]. This technique provides a concurrent impedance matching at all frequencies and inherent DC blocking at the input. It is suitable for frequency-dependent complex loads. However, it results in larger on-chip/ on-board area and does not provide a compact design.

Multi-resonant circuits were considered to design multiband impedance matching in [43, 44]. In [44], analytical synthesis of the matching network using multi-resonant circuits as switches was proposed. The design employed a large number of passives, leading to an increased NF.

As illustrated in Figure 2.8, an alternative approach for multiband matching is to implement frequency transformation techniques [45, 46]. This requires mapping the frequencies and transforming the network from a single band IMN to a dual band or multiband IMN. However, a frequency transformation technique employs a large number of passives, leading to increased noise. Additionally, multiple spiral inductors increase the overall cricuit size and their low quality (Q) factor affects the overall LNA's FOM.

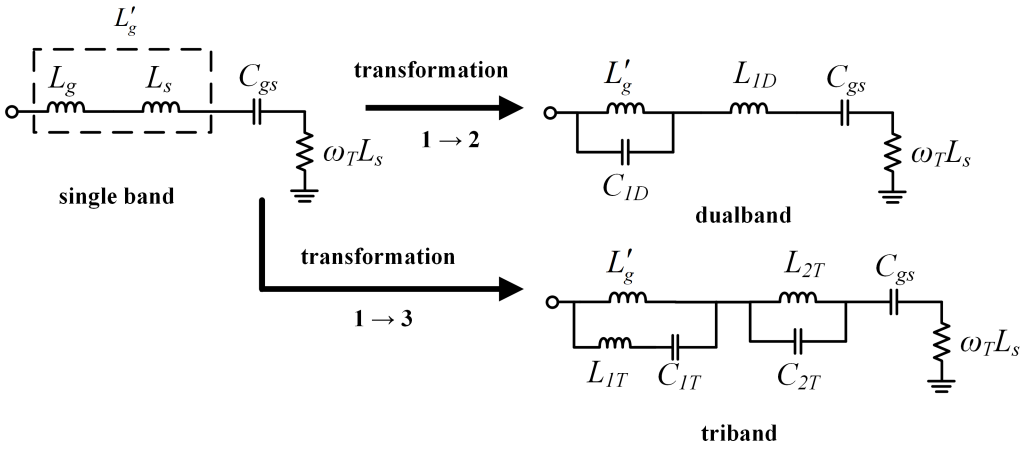


Figure 2.8: Concept of frequency transformation proposed in [45]

For the conventional dual band load shown in Figure 2.7 (a), its impedance can be derived as

$$Z_L = \frac{(1 + s^2 L_{l1} C_{l1})(1 + s^2 L_{l2} C_{l2})}{s\left[s^2 (L_{l1} + L_{l2}) C_{l1} C_{l2} + (C_{l1} + C_{l2})\right]} \tag{2.8}$$

The L_{l1}–C_{l1} pair and L_{l2}–C_{l2} pair form a bandpass filter and a bandstop filter, respectively. These filters generate two passbands [47] as shown in Figure 2.7 (b). Similarly, to design a conventional tri-band load, an additional series L_{l3}–C_{l3} pair can be added in parallel to the existing dual band load.

The conventional load design has a poor SBRR, unbalanced gain, low IRR and sharp roll-off at n^{th} band. Therefore, recent research has focused on modifying the conventional multiband load by implementing feedback notches [48], suspended inductors [49], load-pull technique [50], and eliminating the bandstop filter from the multiband load [51]. However, these modifications suffer from issues like lack of optimum passband and stopband rejection, poor output match, low linearity, and uncontrolled out-of-band impedances that may lead to instability.

2.4.2 Non-Concurrent MBLNAs

Non-concurrent LNAs achieve band-selection through switchable passive matching networks without complex reconfiguration circuits. They are often mistaken for reconfigurable LNAs and are not popular for designing MBLNAs. The reconfiguration in non-concurrent LNAs is done through a band-selection stage with passive matching networks that occurs before the amplification stage.

The non-concurrent LNA proposed in [52] provides an interchangeable band selection between 2.1 GHz – 2.3 GHz and 5.1 GHz – 5.9 GHz by changing the characteristics of a passive matching network through a switched inductor and a switched capacitor. As shown in Figure 2.9, switched inductor matching network (SIMN) was formulated by adding a switch in parallel to an inductor in front of the existing IMN.

2.4.3 Reconfigurable LNAs

Reconfigurable LNAs can support different operating frequencies by varying the input and/or output matching stage of the LNA. The simplest way to design a reconfigurable LNAs is to integrate multiple narrowband LNAs in parallel, and each of the narrowband LNAs will operate at a particular frequency [53]. These type of reconfigurable LNAs are known parallel LNAs. They usually accommodate 2–3 frequency bands and require additional switches for reconfiguration. However, parallel LNAs consume a large on-chip/ on-board area and high power, limiting their usage for reconfiguration purposes. Reconfigurable LNAs can be broadly categorised as switchable LNAs and tunable LNAs.

2.4.3.1 Switchable LNAs

Switchable LNAs adopt switches in the input matching stage and/or complex load stage to shift the operating frequency. Figure 2.10 shows the basic implementation of

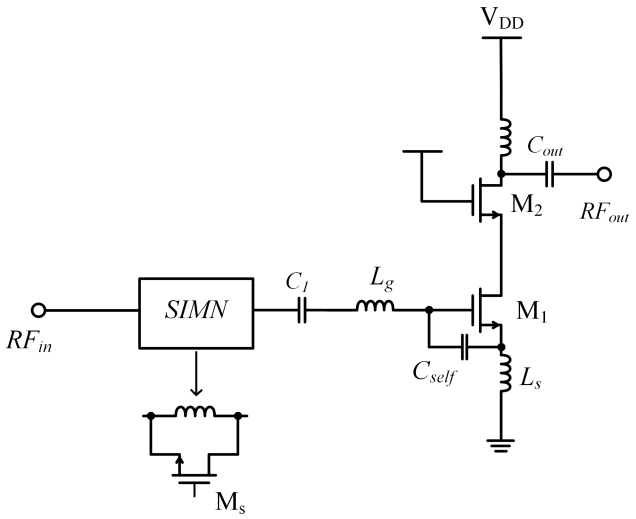


Figure 2.9: Non-concurrent LNA [52]

a switchable LNA [54]. The complex loading network consists of a capacitor bank in parallel with an inductive load. Capacitors C_1 to C_4 have different values and the circuit uses switches connected to the capacitors to vary the impedance of the loading network. The resonant frequency is given by

$$f_{load} = \frac{1}{2\pi\sqrt{LC_{total}}} \tag{2.9}$$

where C_{total} is the effective capacitance due to the bank capacitors (C_1 to C_4), and the parasitic capacitances due to all transistors; L is the load inductance. FETs can be used as switches to control effective capacitance to resonate with L [54], at the expense of increased NF.

Switchable CMOS LNAs adopt switches to tune the operating frequency. They are popular due to thier low cost structure and large-scale integration of multiple baseband and IF blocks on the same die. Additionally, Switchable CMOS LNAs have advantages like low power consumption, small on-chip area and stable manufacturing process [55]. Solid-state switches are typically implemented for monolithic microwave integrated circuit (MMIC) and microwave integrated circuit (MIC) LNAs. Solid-state switches

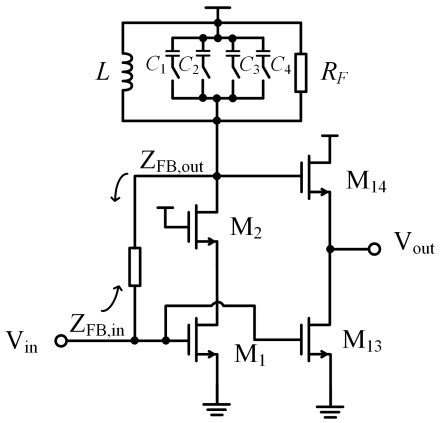


Figure 2.10: Switchable LNA for SDR [54]

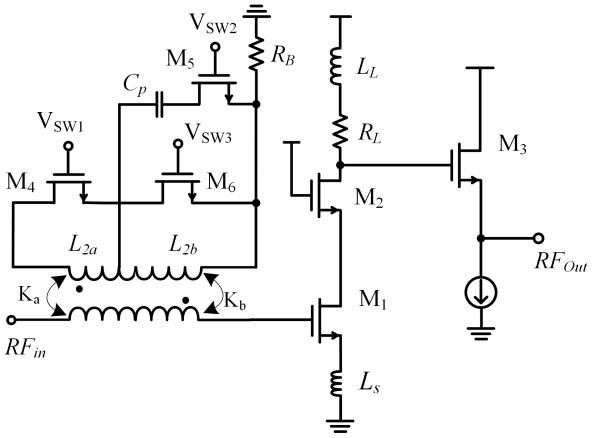


Figure 2.11: Switchable LNA with CMOS switches [56]

use positive-intrinsic-negative (PIN) diodes, FETs/ high electron mobility transistors (HEMTs) or Heterojunction-bipolar transistors (HBTs) that are fabricated in Gallium Arsenide (GaAs) or Gallium Nitride (GaN) technology.

Figure 2.11 shows the design of a highly reconfigurable LNA that adopts CMOS switches. The configuration of three CMOS switches can be varied with an asymmetrically segmented secondary inductor to achieve five different modes of operation [56]. Although CMOS switchable LNAs have low power consumption and small on-chip area [55], the parasitic capacitance of transistor switches causes a significant frequency shift in nearly all modes of operation.

Micro-electromechanical systems (MEMS) switches were proposed to tackle the performance degradation factors associated with extra passive components in CMOS switchable LNAs [57, 58]. MEMS switches have proven advantages in designing reconfigurable MMIC LNAs as they possess very low static power dissipation [59]. However, their switching speed is relatively lower than that of CMOS switches. Furthermore, due to integration, packaging, and reliability challenges, MEMS switches are not yet popular in the design of switchable LNAs [55].

2.4.3.2 Tunable LNAs

Unlike switchable LNAs, the operating frequency of tunable LNAs can be tuned continuously or discretely within a certain bandwidth. Discrete tuning may require switchable reconfiguration with more passive/active elements, leading to high power consumption, increased noise, and increased circuit complexity. Contrary to continuous tuning, discrete tuning is achieved by tuning one more elements in the IMN or OMN to achieve reconfiguration between two or more disparate bands.

Tunable LNAs can be further divided into input tuning LNAs and output tuning LNAs.

Input Tuning LNAs: Input tuning LNAs achieve reconfiguration by changing one or more elements in the input matching stage. As illustrated in Figure 2.12, one can replace the input inductor in a conventional narrowband LNA with a variable inductor. However, such an LNA would not have optimal performance. Furthermore, practical implementation of a tunable series inductor may be challenging. Therefore, the IMN should employ other techniques such as replacing the passive tunable inductor L_g with an active inductor [60], implementing a transformer-based variable inductor [61], tunable floating inductors [62] or an active shunt feedback [22]. The first technique for input tuning LNAs was proposed in [62], where scaling of L_g was done by adding an amplifier in the feedback loop of the

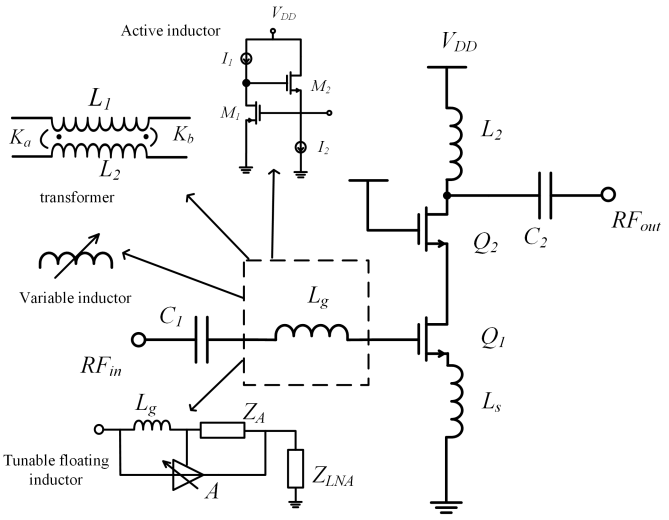


Figure 2.12: General concept of implementing an input tuning LNA

input matching stage.

Active inductor circuits are used to design inductorless reconfigurable LNAs for bandwidth expansion [35] and small chip size [63, 64]. However, active inductors can result in higher NF, reduced linearity, and higher power consumption.

Impedance transformer based variable inductors [61] can provide a wide tuning range by controlling the currents through primary and secondary windings of the transformer. However, this technique requires complex design and implementation of a transformer, leading to hysteresis loss at high frequency and reduced linearity.

Other techniques for input-tuning LNAs include: (1) Miller capacitance in the feedback path and a CMOS switch [65], (2) high-Q inductors and switches [66], (3) a tapped gate inductor and phase change switches [67]. In [65], the authors vary the bias currents to discretely tune between two disparate bands. The bias voltage V_{ctrl} is tuned to switch between two bias currents $I_{c1} = 3.8$ mA and $I_{c1} = 3$ mA. When I_c1 is 3 mA, the LNA operates at 5.2 GHz. On the other hand, when I_c1 is 3.8 mA, the LNA operates at 2.4 GHz.

Output Tuning LNAs: Output tuning is referred to as the capability to reconfigure

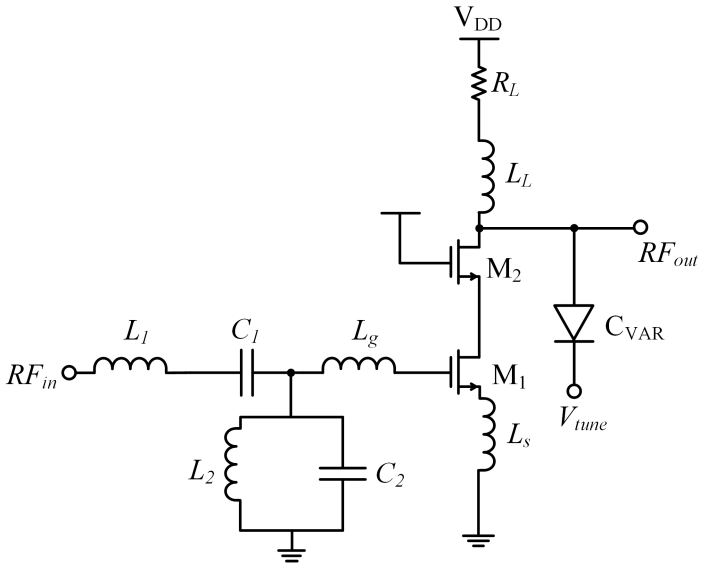


Figure 2.13: Output tuning LNA [70]

the frequency response of the output impedance. Several techniques for output tuning LNAs have been proposed [68, 69], and they generally include a tunable $L - C$ tank circuit. As shown in Figure 2.13, the reconfiguration is achieved by varying C_{VAR} from 0.46 pF to 1.46 pF up to a range of 82 per cent. As a result, the loading network $L_L - C_{VAR}$ resonates at different frequencies from 6 GHz and 10 GHz [70].

In [71], the LNA design employs a GaN HEMT-based switched inductive matching network in the output and input stages to obtain reconfiguration between the S band and the X band. These matching networks minimize the impact of parasitic capacitance when the FET switch is in the OFF state. However, the technique suffers from poor linearity-gain trade-off.

The output tuning LNA proposed in [72] adopted band selective filtering, which is provided by an $L-C$ resonant tank consisting of a multitapped switched inductor and two on-chip varactors. Moreover, the LNA also provides a controllable output DC level by providing a separate bias to the inverter amplifier. However, the linearity and noise performance of the LNA is degraded by the low Q-factor of

the implemented switched inductor.

Other techniques for output tuning LNA include variation of drain voltage [46], variable inductors [73], and variable capacitors [74].

2.4.3.3 Tunable Gain LNAs

Besides frequency, reconfigurable LNAs for SDRs can adapt other specifications such as gain, output power, etc. Tunable gain LNAs (TGLNA) provide gain variation in a particular bandwidth or even in multiple bands. Typical applications for TGLNAs include communication systems, radar, and remote sensing. The most common ways of achieving tunable gain are by varying the output impedance or by controlling the effective transconductance of the input transistor. Other techniques include current steering techniques [75], switchable passives [23], attenuators [76], and voltage variable attenuators [77]. However, the parasitics in current steering circuit limit the bandwidth of LNAs as well as the gain steps. Likewise, switchable passives affect the performance of CMOS TGLNAs, and attenuators require additional power for operation, especially when working with the minimum gain.

For a flexible SDR LNA, both frequency and gain may be concurrently tunable in the same design as proposed in [78, 79]. In [79], frequency tunability was achieved by changing the response of an L–C network in the output load through a variable capacitance. Likewise, the LNA implements active CMOS resistors in the negative feedback path to achieve a continuously tunable gain from 3 dB to 23 dB. However, the non-linearity of the feedback loop may degrade the overall linearity [79].

The LNA design in [77] proposed a TGLNA for SDR that combines variable voltage attenuator to avoid the strong signal compression. The LNA output has two balun circuits to achieve variable gain at the output. Turning off one balun will provide the maximum gain while turning on both baluns will provide the minimum gain. To achieve such reconfiguration the signals at the output of balun stages must have 180° phase

shift. The proposed TGLNA was able to achieve a variable gain from –25 dB to 10 dB. However, this technique resulted in significantly high NF due to multiple noise sources and high power consumption, especially when working with the minimum gain with both baluns on.

2.4.3.4 Reconfigurable Power-consumption LNA

In [34], a gyrator-based reconfigurable LNA is implemented to achieve three switchable power modes—low power mode, moderate performance mode, and high power mode. The LNA exploits the gyrator-C effect [80] to achieve wideband input matching, current reuse topology for low power operation, and shunt feedback topology for linearity improvement. The LNA features very small chip size (0.07 mm^2) and low power consumption (1.52 – 7.0 mW).

2.5 Design Techniques for SDR MBLNAs

This section discusses the design techniques implemented in literature for high performance SDR MBLNAs. We focus on common topologies for SDR MBLNAs, reconfiguration techniques, impedance matching techniques and Process technologies.

2.5.1 Common LNA Topologies for SDR MBLNAs

Commonly implemented LNA topologies have been utilised distinctively in the literature to implement MBLNAs and improve their performance.

2.5.1.1 Inductively Degenerated Common Source Topology

By far, IDCS is the most commonly implemented topology for MBLNAs [81, 82, 83]. Figure 2.14 (a) shows the IDCS topology, where an inductor is added to the source of

the transistor before it is grounded. Source degeneration introduces negative feedback in LNAs that helps to provide a broadband response. Additionally, implementing a source inductor increases the real part of input impedance that helps in providing a better input matching at a desired frequency. For the conventional narrowband LNA shown in Figure 2.12, the input impedance is given as

$$Z_{in} = \frac{g_{m1}L_s}{C_{gs1}} + j\left(\omega L_s + \omega L_g - \frac{1}{\omega C_{gs1}}\right) \tag{2.10}$$

The real part of input impedance depends on: (1) the fixed transconductance g_{m1}, (2) the fixed gate source capacitance C_{gs1} of the transistor M_1, and (3) the degenerated inductor L_s, which is variable. The operating frequency also depends on the value of gate inductor L_g and degenerated inductor L_s. Contrary to resistive degeneration that usually affects the noise performance of LNA, inductive degeneration does not seriously degrade the NF. However, it does reduce the overall gain of the LNA due to the introduced negative series feedback.

2.5.1.2 Common Gate (CG) Topology

CG topology is adopted in designing the wide operating range MBLNAs. As compared to IDCS topology, CG topology, shown in Figure 2.14 (b) has an obvious advantage of lower NF due to its smaller input impedance. In addition, CG topology is usually implemented with cascode configuration to achieve better reverse isolation and higher gain performance [84]. Moreover, in [85], CG topology has been employed for designing a triband LNA for SDR with the improved gain-bandwidth product.

2.5.1.3 Current Reuse Topology

The current reuse topology is a dual cascode stage topology that uses the same bias current for both transistors. Recent MBLNA designs focus on inductorless architectures

using active inductor that may lead to increased power consumption. As shown in Figure 2.14 (c), current reuse is used to reduce the power consumption of MBLNAs by nearly 50 $\%$ compared to conventional LNAs. This is achieved with two gain stages [86]. The two transistor M_1 and M_2 in the current reuse structure can be modelled as one transistor M', which comprises of a P-type metal-oxide semiconductor (PMOS) and an NMOS transistor connected in parallel. Therefore, by adding up the gate-source capacitances, gate-drain capacitances, drain-source capacitances and individual transconductance of two transistors, we have

$$\begin{aligned} C_{gs} &= C_{gs1} + C_{gs2} \\ C_{gd} &= C_{gd1} + C_{gd2} \\ C_{ds} &= C_{ds1} + C_{ds2} \\ g_m &= g_{m1} + g_{m2} \end{aligned} \tag{2.11}$$

where C_{gs}, C_{gd}, C_{ds} are the effective gate-source capacitance, gate-drain capacitance and drain-source capacitance, respectively and g_m is the effective transconductance of the modelled transistor M' [34]. As a result, the effective transconductance is increased, leading to high output impedance, high gain and reduced NF. However, the linearity of the LNAs is reduced.

2.5.1.4 Source Follower

The source follower circuit also known as the common drain configuration is often used as a voltage buffer in MBLNAs. A source follower stage in LNAs will have a high input impedance and low output impedance. The low output impedance is due to the body effect. Therefore, it is used with a low impedance load. Figure 2.14 (d) shows the configuration of source follower. In MBLNAs, source follower is implemented for a wideband output impedance match and measurement purposes. In [87], a source follower circuit was adopted in a reconfigurable LNA to reduce power consumption. The transconductance of source follower is varied by a switchable current source bank.

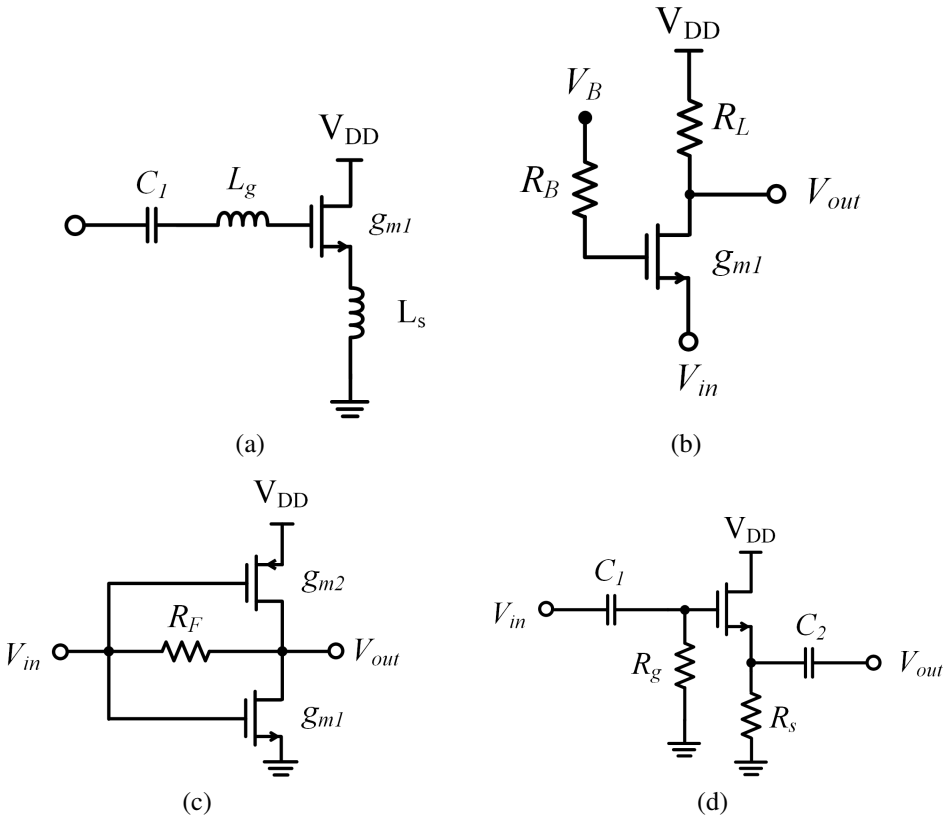


Figure 2.14: (a) IDCS (b) CG topology (c) Current reuse (d) Source follower

A source follower improves reverse isolation and can be implemented for DC voltage shift [77]. The drawbacks of source follower circuit are large output swing, poor driving ability and nonlinearity due to body effect.

2.5.2 Reconfiguration Techniques

Reconfigurable frequency response is one of pivotal requirements for the design of SDR LNAs. In general, reconfiguration in SDR can be achieved in two ways—digital reconfiguration and analog reconfiguration.

2.5.2.1 Digital Reconfiguration

Digitally tunable SDR receivers typically employ wideband or concurrent MBLNAs to cover a broad range of frequencies. Detection of waveforms and channelization [88] can be done through frequency hopping and multiple encoding schemes that involve FPGA and DSP algorithms. For example, an SDR frequency tuning algorithm was proposed in [89] that used a test bed comprising a Universal Software Radio Peripheral (USRP-N210) paired with an RFX2400 daughter board.

2.5.2.2 Analog Reconfiguration

An SDR device usually conflates a programmable DSP System-on-Chip (SoC) and a reconfigurable MBLNA for the radio front-end [66]. Analog reconfiguration can be achieved either by implementing tunable passive devices or by varying associated bias voltage of tuning circuitry. For example, the SDR receiver in [90] adopted two wideband LNAs operating in two bands, 0.1 GHz – 1.5 GHz and 1.5 GHz – 5 GHz. A switch was implemented to select the operating LNA. Further, frequency tunability was realized by feedback resistors in a reconfigurable mixer and a tunable capacitor bank in a voltage controlled oscillator. Other analog reconfiguration techniques involve switchable multi-tap transformers [83], tunable impedance transformers [91] and switched passives [81].

2.5.3 Matching Techniques

Impedance matching plays an important role in the design of LNAs. For a narrowband LNA, impedance matching serves two purposes: (1) maximum power transfer and (2) minimum noise factor [92]. In case of MBLNAs for SDR applications, impedance matching can be designed to achieve concurrent or discrete frequency reconfiguration. This section revisits prevalent impedance matching techniques for concurrent and

reconfigurable MBLNAs.

2.5.3.1 Transformer Based Matching Networks

Transformer based matching networks have been extensively utilized in the input matching stage to design MBLNAs for SDRs. For example, in [93], dual-band input matching was achieved by transformer-based resonators with capacitive termination. The primary winding of the transformer was used as the gate inductance, while the secondary was terminated with a capacitor. Likewise in [25, 56, 94, 95, 96], transformers were utilized to vary the response of input matching to get a reconfigurable response. Figure 2.15 (a) shows the architecture of an LNA with a transformer network for input impedance matching from 3 GHz to 5 GHz. A transformer-based matching network provides high reconfigurability and easy implementation in the CMOS process. Nevertheless, the foremost concerns with the use of transformer-based matching include: insertion loss, bandwidth compression, hysteresis, and its large on-chip/on-board area requirement that increases the circuit size and hence the implementation cost.

2.5.3.2 Microstrip Line Based Matching Networks

Microstrip line-based matching has been explored as a potential technique for designing concurrent MBLNAs [99]. As shown in Figure 2.15 (b), multisection impedance transformers [41, 82, 100] are popular for designing concurrent MBLNAs. These transformers are composed of microstrip lines with series connection in either T-shape [101] or π-shape [98]. They can be used to simultaneously match complex load impedance at two or more disparate frequencies. However, the use of microstrip line based matching networks is limited to MIC technology.

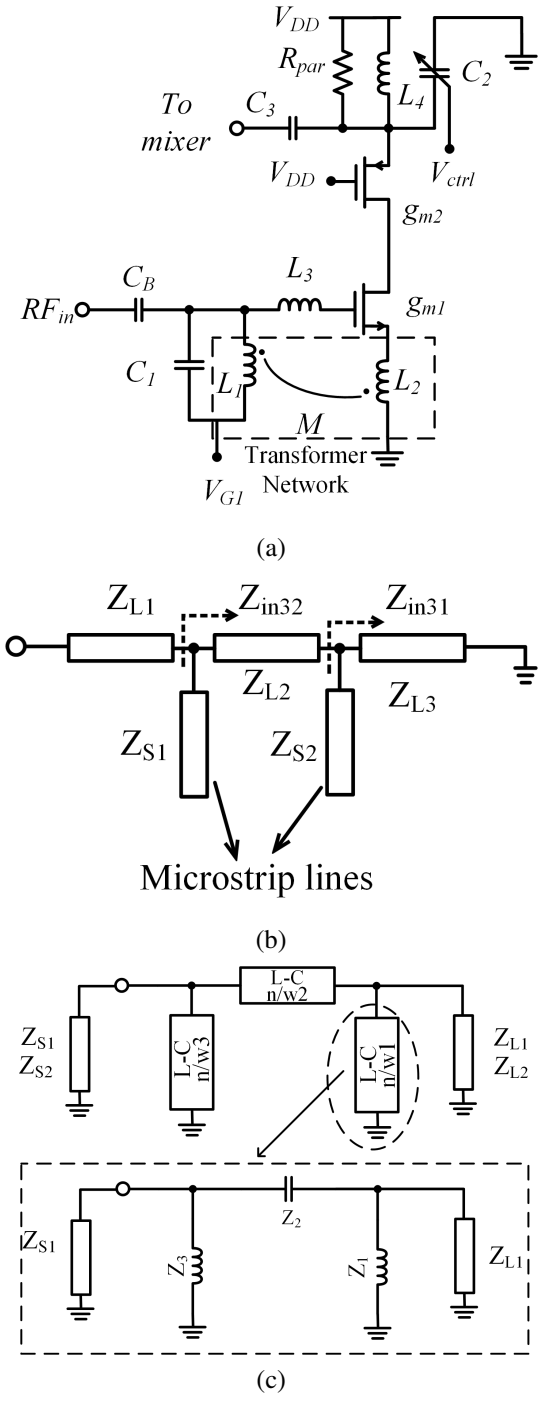


Figure 2.15: (a) LNA schematic implementing a transformer based IMN [74] (b) Multiband impedance transformer [97] (c) Lumped element based impedance matching [98]

2.5.3.3 Lumped Element Approach

Lumped element based matching is a common technique in LNA design. It usually adopts $L-$type, T-type, or π-type networks. As shown in Figure 2.15 (c), a lumped element based matching network for concurrent DBLNA was proposed in [98]. The technique allows concurrent matching of two arbitrary loads to two different sources at 25.5 GHz and 37 GHz. For reconfigurable LNAs, an $L-$type matching network is preferred as it uses only two reactive components to match the desired load impedance. The objective is to realize reconfiguration through the implementation of variable inductors/capacitors [74, 102] or discrete switches [66, 81] in series with inductors/capacitors by changing the frequency response. However, recent designs tend to reduce lumped elements in matching stages due to associated losses with lumped elements for MBLNAs.

2.5.4 Process Technologies

Common process technologies for designing MBLNAs for SDR include CMOS processes (0.35 μm, 0.18 μm, 0.13 μm, 90 nm, 65 nm, 25 nm), 0.13 μm and 90 nm SiGe-BiCMOS process, 0.25 μm, 0.15μm, 0.1 μm MMIC/Pseudomorphic HEMT (PHEMT) process and MIC technology. Besides these, other process technologies are derived from the above-mentioned techniques, and have been investigated to improve the design of MBLNAs for SDRs operating at microwave as well as mmWave range.

2.5.4.1 MMIC on Quartz Substrate

An LNA circuit was realised into a DBLNA by using a single-pole-double-through (SPDT) switch fabricated over a quartz substrate [57]. The LNA was fabricated in GaAs MMIC. As shown in Figure 2.16 (a), this technique is applicable when switching between two different LNAs is required. It also helps to reduce the NF of the circuit.

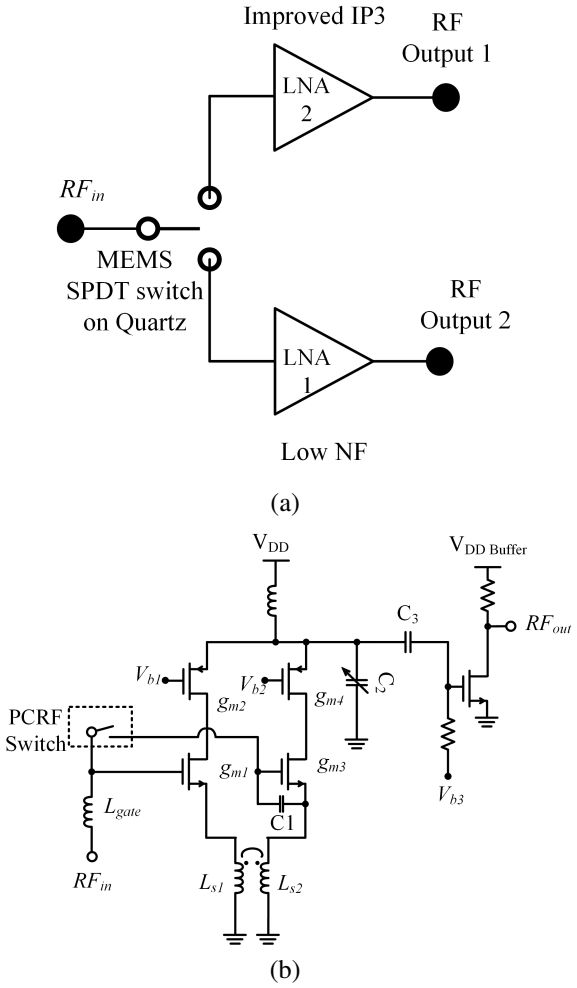


Figure 2.16: (a) Schematic of proposed technique using MEMS switch on quartz substrate for dualband LNA [57] (b) Schematic of customised PCRF switch + 3/5 GHz CMOS LNA proposed in [67]

Moreover, implementing MEMS switches and LNA circuits in same branch reduces the power consumption. Nevertheless, the technique resulted in a significant frequency shift from the desired 20 GHz band by almost 3 GHz, which was primarily due to the load capacitance of different air bridges on transmission lines.

2.5.4.2 Flip-Chip Integration Process

In [67], a reconfigurable DBLNA was reported using phase-change RF (PCRF) switches. These were integrated with LNAs fabricated in 0.13μm CMOS process. The objective

of designing PCRF switches in flip-chip integration was to allow reconfiguration of narrowband LNAs without sacrificing their performance. The PCRF switches were fabricated in-house using a customised process and then added switching pads to the 3/5 GHz DBLNA circuit as shown in Figure 2.16 (b). However, the integration resulted in variation of input matching at desired frequency, leading to increased RL.

2.5.5 Comparison of Reviewed Techniques

Table 2.3 compares the proposed techniques for the design of MBLNAs for SDRs.

Table 2.3: Summary of design techniques for SDR LNAs

Refs.	**LNA Type**	**Proposed Technique**	**Pros**	**Cons**
[29]	wideband	differential cascode topology	high output power, high PAE	large DC voltage requirement
[26]	wideband	resistive shunt feedback	flat gain, wide bandwidth	affects noise performance
[30]	wideband	inductive series/ shunt peaking	increased small signal bandwidth, improved rise time	gain variation across wide bandwidth
[35, 60] [63, 64]	wideband / multiband	active inductors (load/ i/p match)	less chip area, high Q of circuit	high power consumption, slower design process.
[41, 82], [97, 100]	concurrent multiband	multiband impedance transformers (i/p matching)	low noise due to fewer passives	large on-chip area, high power consumption
[28, 103]	concurrent multiband	transmission line stubs (varying impedance)	low noise, inherent DC block	large chip/board area
[45, 46]	concurrent multiband	frequency transformation (i/p match)	agile, simplified and provides good impedance match	low Q of multiple passives
[50]	concurrent multiband	load pull technique (o/p match)	better output impedance match, fast tuning	uncontrolled out of band impedance, stability issue
[95]	concurrent multiband	single-ended to differential output with transformer f/b	low GI, high IRR	poor IRL and ORL, high NF
[56]	reconfigurable	multitap transformer with CMOS switches	multimode operation, highly flexible reconfiguration	frequency deviation due to parasitic capacitance
[57, 59], [58]	reconfigurable	MEMS switches/ MEMS varactors	low static power dissipation, wide tuning range	low switching speed reliability issue, complex packaging
[61, 104]	reconfigurable	impedance transformer based variable inductor	wide continuous tuning range, allow switchable configuration	hysteresis loss at high frequency, reduced linearity of LNA
[67]	reconfigurable	PCRF switches	easy reconfiguration of existing narrowband systems	significant shift in operational frequency, poor IRL and ORL
[71]	reconfigurable	switched inductive matching	minimized impact of parasitics in off state	poor linearity-gain tradeoff
[79]	tunable gain	negative feedback path	wide tuning range	non-linearity of feedback path affects total linearity
[77]	tunable gain	voltage variable attenuators	strong signal compression, improved receiver sensitivity	high NF, high power consumption

PAE: power-added efficiency; i/p: input; o/p: output; f/b: feedback.

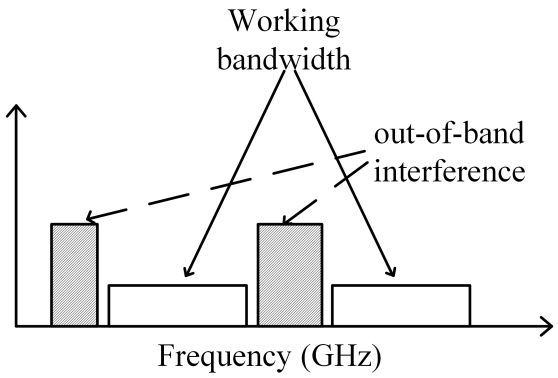


Figure 2.17: Concept of out-of-band interference [108]

2.6 Major Design Challenges and Proposed Techniques

The design of MBLNAs involves complex circuitry and a large number of passives. Therefore, it is common for conventional MBLNA designs to incur noise degradation, interference, harmonics, low passband and stopband rejection ratios, frequency shifts, and high implementation cost. This section summarizes major challenges in the design of MBLNAs, along with recently proposed techniques to overcome them.

2.6.1 Out-of-band Interference

As shown in Figure 2.17, out-of-band interference arises from undesired signals in frequency bands adjacent to the desired operating frequencies. They cause saturation and degrade the sensitivity. A single-ended input to differential output concurrent DBLNA was proposed to mitigate this issue. The differential signals at the output of LNA would improve the SDR receiver's power supply rejection ratio (PSRR), harmonic rejection, and intereference rejection [95]. Other techniques for out-of-band interference rejection include bandpass filter (BPF)-LNA co-design [105], input-band selection via $L - C$ load tank coupled with differential topology [106], and interference rejection active BPF [107]. These techniques are able to achieve an IRR of more than 35 dB.

2.6.2 Limitation of CMOS Switches at mmWave

CMOS switches are capable of providing low cost and fast switching design for reconfigurable LNAs. The performance of CMOS and PIN diode switches are competitive till the operating frequency reaches X band. However, in mmWave, these switches result in poor reverse isolation and high insertion loss [109]. RF MEMS devices are expected to achieve superior performance in mmWave frequencies. The insertion loss performance of such switches can be as low as 1 dB and the reverse isolation can be better than 15 dB, providing better performance than CMOS switches [110].

2.6.3 High Cost Due to Large On-chip Area in CMOS

Many reconfigurable LNAs implement transformers that occupy an on-chip area of about 500 μm^2 or more. This is much higher than their narrowband counterparts. Their low Q-factor also poses a challenge and creates obstacles in incorporating other components on the microchip, leading to increased common-mode noise and cost. MEMS-based switches and varactors were proposed in switchable LNAs [58, 109], replacing conventional transformers. MEMS varactors have lower losses but a limited tuning range. However, the tuning range can be improved by adding a switched shunt capacitor.

Active inductor circuits were explored to design inductorless reconfigurable LNAs [64, 86, 111] to reduce the chip size. In [111], the LNA consumed an on-chip area of 0.165 mm^2 (including pads) and NF was 1.9 dB to 3.4 dB. However, drawbacks associated with use of an active inductor are reduced linearity and high power consumption. An inductorless design using a gyrator was achieved for a reconfigurable LNA in [34]. The proposed design operates in different operating power modes and accounts for a very small chip size of 0.07 mm^2.

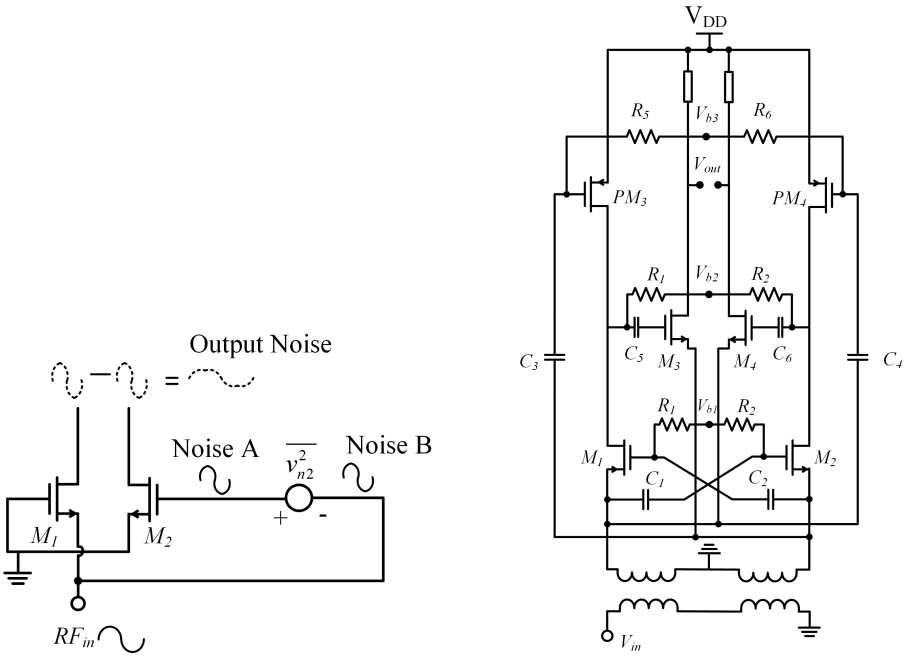
2.6.4 In-band Common Mode Noise

Reconfigurable LNAs face high thermal noise and in-band common mode noise, along with additional noise from switching and tuning transistors. For example, MITs, active phase shifters, and CMOS transistor switches for reconfigurable input matching induce high noise in reconfigurable LNA circuits. Moreover, the in-band common mode noise degrades an SDR receiver's sensitivity.

To overcome the common-mode noise, differential circuit topology is widely implemented. For example, [112] proposed an LNA that incorporates a cascode connection of a PMOS and an NMOS transistor in CG topology to reduce the noise due to the current buffer circuit.

The noise cancelling phenomenon in LNAs for SDRs was reviewed in [113]. The LNA proposed in [106] uses capacitive cross coupling with a gate resistor to cancel out the thermal noise. The current disturbance in the gate resistor generates the thermal noise. The two noises, Noise A and Noise B, generated at two ends of the resistor (modelled as $\overline{v_{n2}^2}$) will be contrary to each other. The CS amplifier with transistor M_2 amplifies and reverses the Noise A, while M_1 amplifies Noise B. The next stage in the circuit cancels out these noises. The noise cancellation concept proposed in [106] is shown in Figure 2.18 (a).

Similarly, a feed forward noise cancellation technique shown in Figure 2.18 (b) was implemented for a wideband LNA in [114]. The noise voltage (v_{noise}) at source and drain of M_1 has different polarity. v_{noise} at drain of M_1 is amplified by M_3 and v_{noise} at source of M_1 is amplified by M_4. Therefore, M_3 and M_4 have same polarity of v_{noise} at their drain terminals. This results in partial v_{noise} cancellation by M_1. Similarly, partial v_{noise} by M_2 is also cancelled.



(a) (b)

Figure 2.18: (a) Noise cancellation scheme proposed in [114] (b) Feed forward noise cancellation scheme implemented in [106]

2.6.5 Gain Imbalance

It is desired that MBLNAs exhibit nearly equal gain values for all operational bands. GI (see Figure 2.19) reduces their agility and flexibility. Many reported MBLNAs suffer from GIs of more than 5 dB between bands of operation. For example, DBLNA in [115] has a GI of more than 13 dB. Similarly, a difference of more than 7 dB between peak gain values at their respective operating frequencies was reported in [85, 93]. Few LNA designs were reported to specifically address GI. However, some topologies and technologies, like substrate integrated suspended line (SISL) [116], load pull, and current steering, can help reduce the GI to as low as 0.6 dB.

2.6.6 Stopband Rejection Ratio

SBRR is the difference between values of S_{21} at stopband centre frequencies and passband centre frequencies in a concurrent MBLNA. Figure 2.19 shows the difference between IRR and SBRR. A high SBRR is desired in concurrent MBLNAs to minimize interference, achieve stability and low noise in desired pass bands. SBRR improves the passband performance and removes the sharp roll-off in S_{21} that is achieved due to improper filtering at the load of concurrent MBLNA. LNA in [48, 95] have proposed a novel dual band load to improve the passband performance that eventually increases the SBRR of a concurrent triband LNA. However, the LNA in [48] implements a wideband IMN that places stringent requirements to minimise interference from stopbands.

2.6.7 Harmonics and Intermodulation Products

Conventionally, harmonic rejection is a requirement of the mixer that follows the MBLNA in an SDR. Third and fifth order harmonics cause intermodulation products, leading to signal distortions. For LNAs, those with $IP_3 > 0$ dBm are likely to have less harmonics and are capable of cancelling intermodulation products. However, third and fifth order harmonics may be high in one band while low in other bands in the case of MBLNAs for SDR [91]. Due to this issue, it is quite difficult for an MBLNA to achieve good linearity across the desired frequency bands. Although no technique exists for reducing harmonics precisely for MBLNAs, an N-path filtering was proposed to minimize third order intermodulation products in an LNA for SDR at the expense of increased power consumption and high NF [117]. Alternatively, a capacitive cross-coupled technique was adopted to improve the linearity of a wideband LNA in [35, 84, 106]. This technique can be well adopted to reduce intermodulation products in MBLNAs. Moreover, a complementary source follower technique was implemented in [84] to reject harmonics and overcome non-linearity limitations from active feedback.

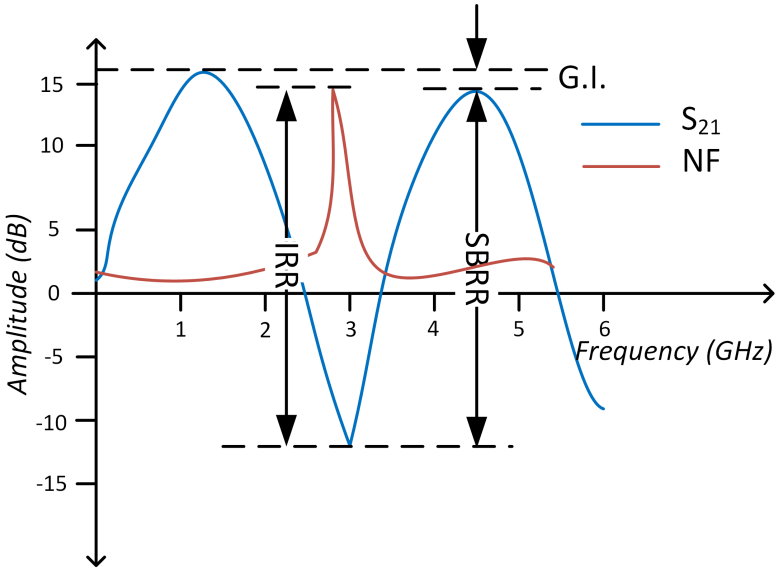


Figure 2.19: Concept of IRR, SBRR and GI

Other popular techniques include the derivative superposition method [118], in which the third-order derivatives of drain currents of the main and the auxiliary transistors are added to cancel distortion [119]. As shown in Figure 2.20, this technique is also known as the multiple gated transistor technique [120] because it utilizes multiple parallel transistors with their gates connected.

A brief summary of design challenges in MBLNA for SDRs is presented in Table 2.4

2.7 Conclusion

Different techniques have been developed for designing state-of-the-art MBLNAs for SDR receivers. To overcome the associated design challenges, novel techniques such as $L-C$ bandpass filtering, dual reactive feedback [125], active inductor circuits [86], and active notch filter [48] have been proposed. These have been coupled with circuit topologies like source follower feedback, IDCS, differential design and CG topology [126]. However, there are respective benefits and drawbacks associated with the use of every reviewed technique. Going forward, it is necessary to balance the trade-offs,

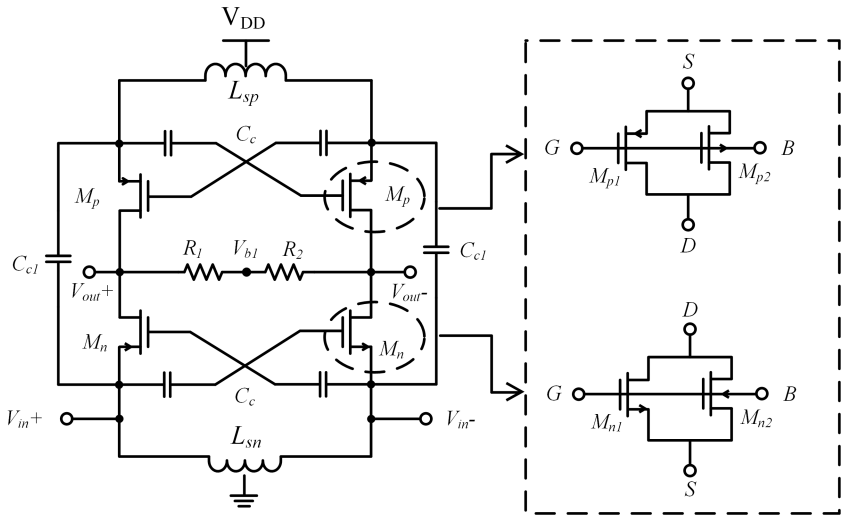


Figure 2.20: MGTR technique for linearity improvement implemented in [120]

minimize the drawbacks, and achieve optimal performance. Differential signalling design is a popular technique to overcome a number of design challenges, like thermal noise cancellation, harmonic rejection, interference rejection, and bandpass response. Likewise, IDCS with cascode topology is the most-used topology in the design of CMOS MBLNAs. Furthermore, it is worthy pointing out that most reconfigurable LNAs were proposed in CMOS, while few were proposed in MIC technology.

Challenges and trade-offs are common in the design of MBLNAs. This leaves a substantial opening for research. After a profound review of the literature, we attempt to provide some issues that are resolved in our research reported in this thesis.

- Most concurrent MBLNAs reported in literature have high GI especially the MBLNAs working at high microwave and mmWave frequencies.
- IRR and SBRR are important performance metrics in concurrent MBLNAs and very little has been reported to improve them.
- SDRs require a wide tuning range (>500 MHz) for most applications. However, most frequency tunable LNAs reported literature have a limited tuning range.

Table 2.4: A comparison of techniques to overcome challenges in SDR LNA design

Objective	Technique Proposed	Results	Other Techniques
Reducing out of band interference	Band-select with differential LNA topology [106]	3-dB BW = 150 MHz IRR >20 dB	- Frequency transformation - stepped impedance stubs
	IRR BPF [105]	3-dB BW = 5 GHz IRR >40 dB	
	Single-to-differential with transformer feedback [48]	3-dB BW >400 MHz IRR >42 dB	
Improving switching efficiency at mmWave frequencies	RF MEMS switches [109, 110]	S_{11} = –24 dB @ 24GHz ; S_{22} = –25 dB @ 74 GHz	FPGA-based programmable switches, memristor switches [121]
Minimizing on-chip area and design cost	Active inductor load [111]	Area $\leq$ 0.165 mm^2	Capacitive cross coupling with active shunt feedback [122]
	Gyrator circuit [34]	Area $\leq$ 0.07 mm^2	
Reducing in-band common-mode noise	Feed forward noise cancelling [114]	NF = 3.1 dB	Active noise cancelling using programmable FPGA in SDR receivers.
	Capacitive cross-coupling [106]	NF = 2.1 dB	
	Differential design [112]	NF = 3.1 dB	
Minimum GI	SISL [116]	GI $\leq$ 0.6 dB	Active gain control using buffer in differential design
	Current steering	GI $\leq$ 1dB	
Reducing IM products	N – path filtering [123]	IP3 = 8.2 dBm	Digital pre-distortion technique (DPD)[124]
	Derivative superposition [118]	IP3 = 18 dBm	

- Wideband LNAs and IMNs are still popular in practically implemented SDR receivers. Frequency and gain tuning is performed in a digital manner. Significant interference and noise may be observed in the signal reception

Table 2.5: A performance comparison of existing concurrent MBLNAs

Ref	**Freq (GHz)**	S_{21} **(dB)**	S_{11} **(dB)**	**NF (dB)**	IP_3 **(dBm)**	P_{DC} **(mW)**	**Area** (mm^2)	**Process**
[85]	2.4	10.6	–12.5	4.96	–7	3.6	0.64	0.18μm CMOS
	5.2	17.4	–22.7	5.16	–16			
	5.8	15.6	–25	5.57	–16			
[127]	23.5	21.9	–25	5.1	–10.4	-	0.19	0.18 μm SiGe BiCMOS
	35.7	16.6	–15	7.2	–8.3			
[49]	2.3	14.4	–12.8	2.5	-	11.9	0.29	0.35 μm SiGe BiCMOS
	4.5	14.3	–11.5	3.0	-			
[128]	1.217	16	–10.1	2.2	–12.5*	13.6	1.28	0.18 μm CMOS
	1.568	14.7	–11.4	2.35	–13.5*			
[129]	0.9	18	–20	2	–7.7	12	-	0.13 μm CMOS
	2.4	27	–12	3	–7.2			
[51]	2.4	–19.3	–16.8	3.2	–20.1	20	-	0.13 μm CMOS
	5.2	17.5	–19.4	3.3	–18.1			
[93]	2.45	9.4	–12.62	2.8	–4.3	2.79	0.36	0.13 μm CMOS
	6	18.9	–21	3.8	–5.6			
[39]	25.5	16	–28	3.5	–2	48	0.16	65 nm CMOS
	76.5	10	–25	8.2	–4			
[95]	21.5	–8	15.7	4.3	–14.9	73.8	0.69	0.18 μm SiGe BiCMOS
	36	–9	15.7	4.3	–16.8			
[47]	2.4	12.9	–13.1	3.7	–4	7.6	0.9	0.18 μm CMOS
	5.2	8.2	–10.5	3.7	–1			
[48]	13	22.3	–7$\sim$–9	3.7	–13.5	36	0.59	0.18 μm SiGe BiCMOS
	24	24.6		3.3	–17.1			
	35	22.2		4.3	–16.1			
[116]	2.45	28.4	–13	0.7	–6.6	36	850	SISL
	5.25	28.8	–20	1.1	–5.1			

* P_{1dB}, SiGe: Silicon Germanium

- There exists a stringent requirement for reconfigurable MBLNAs to provide simultaneous reconfiguration of input and output matching.

Table 2.5 and Table 2.6 summarize the performance of recently reported MBLNAs with novel techniques for performance improvement. Although some of them had excellent performances, most of them faced design challenges some of which are resolved in our research.

Table 2.6: Performance comparison of existing reconfigurable MBLNAs

Ref.	**Freq (GHz)**	S_{21} **(dB)**	S_{11} **(dB)**	**NF (dB)**	IP_3 **(dBm)**	P_{DC} **(mW)**	**Area** (mm^2)	**Process**
[54]	1.7 – 5.7	10 – 12	–16 – –10	2.9 – 7	–21.5 – –12	12.6	1.25	0.18 μm SiGe BiCMOS
[56]	2.8	16.1	–32.8	2.4	–4.0	6.4	0.73	0.13 μm CMOS
	3.3	14.2	–18.6	3.0	–2.0			
	4.6	14.2	–35.4	3.7	–3.2			
	2.05 5.65	14.9, 14.9	–8.6, –32.4	4.0, 4.8	–2.0, –4.2			
	4 – 7.8	15.6	<–10	4.0 – 5.3	–5.0 – –1.2			
[60]	0.9/1.5 1.9/2.4	17 – 21	–27 – –11	1.7 – 3.6	-	19.6	0.03	0.18 μm CMOS
[62]	1.9 – 2.4	10 – 14	–15 – –25	3.2 – 3.7	–6.7	17	0.083	0.13 μm CMOS
[79]	4.5 – 5.5	3 – 23	–6 – –8	2 – 6	–6.5 – 10	16	0.043	65 nm CMOS
[66]	2 – 5	14.8	<–10	5.8	–16.9	3.84	-	0.18 μm CMOS
	1.8	11.6	–19	8.5	–9.2			
	2.1	12.8	–14	8	–11.6			
	2.4	13.5	–11	8.5	–14.6	1.8		
	1.9, 5.2	18, 18	<–10	5.5, 7.8	–14.2, –17.2	3.84		
[67]	3	21.2	–9	2.5	–12.5	7.2	4	0.13 μm CMOS
	5	21.9	–10	2.7	–13.8	3.6		
[86]	1.8 – 2.4	20.6 – 22.1	–25 – –12	3.2 – 3.5	–16 – –11.8	9.6	0.05	0.13 μm CMOS
[87]	1.8	11	–12	2.8	–3.45	7.2	0.63	0.18 μm CMOS
	2.4	14.4	–13	3.3	–7.12			
	3.5	13	–14.4	3.8	–6.2			
	5.2	10	–10	4.3	–4.34			
[109]	51 – 60	18.7 – 21	–5	6.8 – 7.3	–18*	10.8	0.78	0.25 μm SiGe BiCMOS
	66 – 78	21.3 – 23	–5	7.6 – 8.4	–18*			
[72]	2.40	22.1	–14	2.8	–18.2	4.6	0.49	0.13 μm CMOS
	3.43	22.6	–30	2.2	–15.3			
	3.96	24.0	–28	2.4	–18.5			
	4.49	22.6	–18	2.5	–18.7			
	5.40	24.8	–17	3.1	20.4			
[130]	3.5	13	–14.8	3.9	–1.4	9.36	-	0.13 μm CMOS
	5.8	11	–13.1	4.2	–5.4			
[81]	2.4	20.7	–22.8	2.6	–6.2 $\sim$–5.1	19.8	-	0.18 μm CMOS
	3.5	21.08	–28.5	3.1				
[110]	24	22	–22	4.3	-	40	0.77	0.25 μm SiGe BiCMOS
	74	18	–20	8.5				
[112]	1.48	18.3	–11.9	3.1	–3.4	27.3	-	0.18 μm CMOS
	1.68	19	–12.2	3.2	–3			
	2.64	26	–11.3	3.3	–7			
[106]	0.8 $\sim$1.7	13 – 17.5	–18.3 – –41	2.17 – 3.4	7.36	8.96	-	0.18 μm CMOS

* P_{1dB}

Chapter 3

Design and Analysis of Concurrent Multiband Matching Networks for LNAs

3.1 Introduction

An LNA is an integral part of an SDR radio receiver. It should provide a multiband operation and must achieve perfect impedance matching at all desired frequencies while reducing maximum interference from adjacent undesired bands.

Wideband input matching is one of the most commonly implemented matching technique for designing MBLNAs. It provides a wide bandwidth and concurrent reception of desired operational frequencies. However, IRR requires vigilant frequency planning and additional filtering. Alternatively, a multiband matching network is thus preferred for concurrent MBLNAs.

Some widely adopted approches in MIC MBLNAs are (i) Multiband impedance transformers (MIT) [41] and (ii) transmission line (TL) based impedance matching [42]. TL based IMNs result in reduced noise in LNAs and provide efficient impedance matching.

However, they increase the chip size and are not suitable for RFIC LNAs. Multiresonant circuits [43, 44] have also been explored to design MBIMNs. In [44], analytical synthesis of IMN using multiresonant circuits as switches was proposed. The technique transforms switched dual band and triband IMN into switchless ones using foster resonant lumped networks. The design, however, included large number of passives that lead to higher losses at microwave frequencies. In [131], a tunable multiband impedance matching network was proposed that utilised a novel polynomial level synthesis based on real frequency technique. However, the design had no stopband rejection and both transmission and reflection coefficients indicated a wideband response.

In [45, 132], synthesis and transformation technique was utilised to design MBIMNs. In [132], the approach followed admittance de-normalisation to match the source with frequency-dependent complex loads. The topology, however, resulted in smaller operational bandwidths. Likewise in [45], transformational synthesis was utilised to design MBIMNs using 1 to n frequency mapping. The proposed method improved the efficiency of IMNs but resulted in higher losses and sharp roll-off of transmission coefficient at the n^{th} band. Impedance and frequency transformation technique (IFTT) proposed in this chapter is an efficient approach that requires mapping from an $L-$match to a bandpass match and subsequently to a dual band or multiband match [46].

In this chapter, we present a method to synthesise and design a dual band and a triple band IMN with distinct topologies. The method proposes the design of dual band IMN (DBIMN) and triple-band IMN (TBIMN) using inductive and capacitive elements through proposed frequency mapping which follows IFTT. Furthermore, the designed IMNs are converted to microstrip lines to minimise losses due to lumped passives. This chapter proposes a novel method and simplified concept of designing concurrent MBIMNs for SDR LNAs.

3.2 Types of IMNs for Multiband Circuits

3.2.1 Narowband Matching

In case of two-port networks, narrowband IMN involves matching of input impedance Z_{in} to the source impedance Z_s and output impedance Z_{out} to the load impedance Z_l at a single frequency or a small range of frequencies; i.e. for perfect impedance match $Z_{in} = Z_s^*$ and $Z_{out} = Z_l^*$. For a conventional narrowband CS LNA, source and load impedances for the transistor can be determined by plotting gain and noise circles on the smith chart. Thereafter, an inductive or capacitive IMN is designed to match impedance for maximum power transfer. Figure 3.1 (a) and (b) show the input matching stage of a conventional narrowband CS LNA and its equivalent small signal model. Inductor L_g and gate-source capacitance C_{gs} form an $L-$match to achieve input matching with complex impedance. Applying Kirchhoff's voltage law (KVL) in Figure 3.1 (b), the input voltage V_{in} in the network is given as.

$$V_{in} = j\omega L_g I_{in} + \frac{I_{in}}{j\omega C_{gs}} + g_m V_{gs} Z_s + Z_s I_{in} \tag{3.1}$$

$$\frac{V_{in}}{I_{in}} = j\omega L_g + \frac{1}{j\omega C_{gs}} + \frac{g_m V_{gs} Z_s}{I_{in}} + Z_s I_{in} \tag{3.2}$$

$$V_{gs} = \frac{I_{in}}{j\omega C_{gs}} \tag{3.3}$$

Substituting (3.3) in (3.2) $Z_{in}(j\omega)$ for LNA can be written as

$$Z_{in}(j\omega) = j\omega L_g + \frac{1}{j\omega C_{gs}} + \frac{g_m Z_s}{j\omega C_{gs}} + Z_s \tag{3.4}$$

where g_m is the transconductance of Q_1. Since, C_{gs} and Z_s are fixed, L_g can be made variable by replacing it with a tunable inductor L_g' to achieve an input tunable matching. Figure 3.2 (a) and (b) show possible configurations in $L-$match.

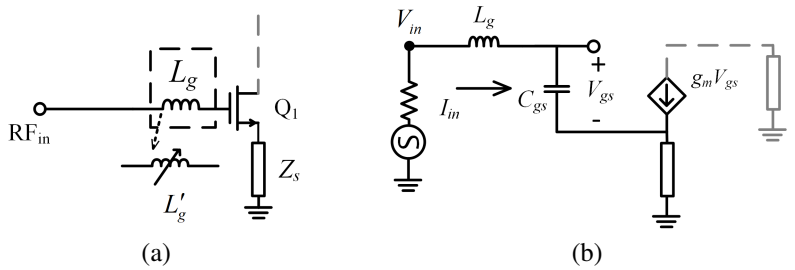


Figure 3.1: (a) Input stage of a narrowband LNA (b) Small-signal equivalent circuit

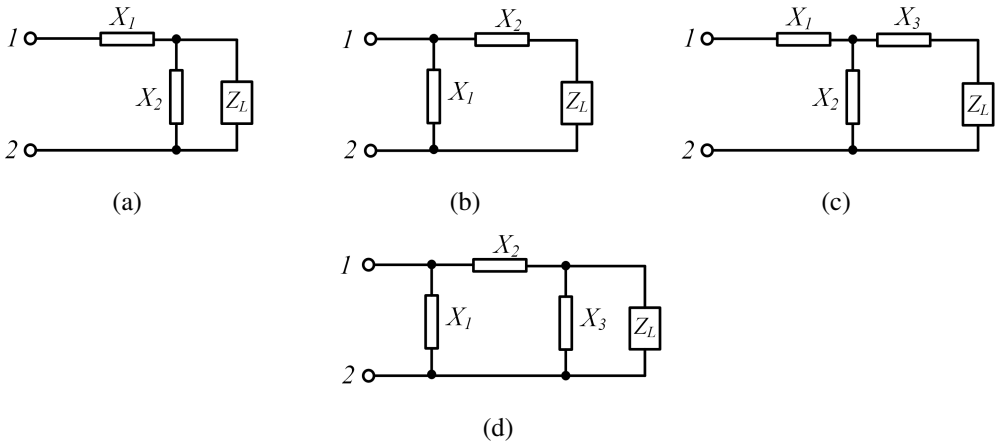


Figure 3.2: Possible configurations of (a) $L-$match with series first (b) $L-$match with shunt first (c) T-matching network (d) π matching network. (Here X_1, X_2 can be either an inductor or capacitor in alternate configuration and X_3 must be same element as X_1)

T and π based narrowband IMNs have back-to-back two $L-$matching networks. In general, these are two stage $L-$networks that can increase the $Q-$factor of the IMN. Figure 3.2 (c) and (d) show possible configurations in T and π networks. These IMNs offer low bandwidth but a higher Q value. Values of L and C for π and T networks can be calculated using $Q-$based method proposed in [133]. The parallel element in T-network (X_2) or in π network ($X_1 - X_3$) can be made either switchable or tunable to achieve multiband reconfigurable operation.

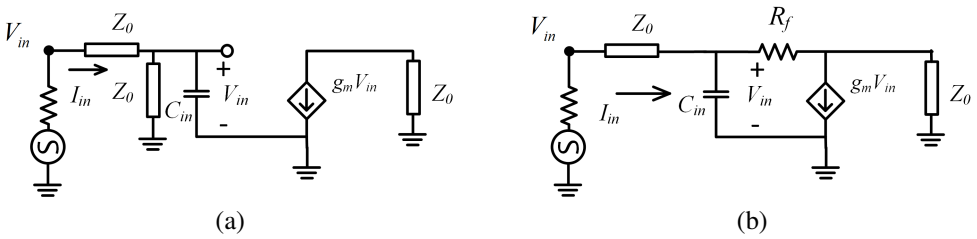


Figure 3.3: (a) Small signal model for CRLNA and (b) RFLNA

3.2.2 Wideband Matching

Wideband matching networks cover a wide range of frequencies concurrently and are therefore a popular choice for MBLNA design. In multiband SDR receivers, the frequency reconfiguration is done (i) digitally through frequency hopping schemes that involve FPGA algorithms and (ii) in analog domain using tunable filters. Wideband matching in LNAs can be simply achieved through CG configuration. This is because the Z_{in} for CG configuration remains resistive for a large frequency range. The input impedance of CG input stage is given as

$$Z_{in}\left(j\omega\right) \approx \frac{1}{j\omega C_{gs}} \Bigg\| \frac{1}{g_m + g_{mb}} \tag{3.5}$$

where g_{mb} is the back gate transconductance. Other commonly implemented wideband matching techniques are: resistive feedback [134] and reactive feedback [135] in CS LNA, $L-C$ ladder matching network [136] and bandpass filter based matching network [137]. In resistive feedback LNAs, the input capacitance C_{in} of the active device is directly proportional to effective transconductance $g_{m_{eff}}$. Since, resistive feedback reduces $g_{m_{eff}}$, thus C_{in} reduces and that leads to large bandwidth. Equations (3.6)–(3.13) present the bandwidth analysis of a resistive feedback LNA (RFLNA). Figure 3.3 (a) and (b) show the small signal model of a conventional resistive LNA (CRLNA) and RFLNA, respectively. Gain bandwidth product f_T as a function of g_m is

given as

$$f_T = \frac{g_m}{2\pi C_{in}} \tag{3.6}$$

but transconductance for CRLNA $g_{m_{cr}}$ is given as[1]

$$g_{m_{cr}} = 2 \cdot A_v / Z_0 \tag{3.7}$$

and for RFLNA is [1]

$$g_{m_{rf}} = \frac{1 + A_v}{Z_0} \tag{3.8}$$

where A_v is the voltage gain of the LNA. Substituting (3.7) in (3.6), C_{in} for CRLNA is

$$C_{in} = \frac{A_v}{\pi f_T Z_0} \tag{3.9}$$

and C_{in} for RFLNA is

$$C_{in_{rf}} = \frac{(1 + A_v)}{2\pi f_T Z_0} \tag{3.10}$$

The 3-dB bandwidth f_{3dB} for CRLNA and RFLNA is given as

$$f_{3dB} = \frac{1}{2\pi C_{in} \left(Z_0/2\right)} \tag{3.11}$$

From (3.9) and (3.11), f_{3dB} for CRLNA is given as

$$f_{3dB} = \frac{f_T}{A_v} \tag{3.12}$$

and for RFLNA is given as

$$f_{3dB_{rf}} = f_T \frac{2}{1 + A_v} \tag{3.13}$$

Thus, it is evident from (3.12) and (3.13) that $f_{3dB_{rf}} \gg f_{3dB}$ and hence, RFLNAs

[1] See Appendix 1 for derivation of $g_{m_{cr}}$ and $g_{m_{rf}}$

provide an efficient matching technique to design wideband LNAs. Further, in this chapter, our discussion for wideband matching is limited to the design of bandpass IMN.

3.2.3 Multiband Matching

MBIMN provides impedance matching at multiple bands simultaneously or discretely by eliminating interference from other bands. Depending upon the application, MBIMNs can either be reconfigurable or concurrent. Reconfigurable matching can be achieved in two ways: (i) by using PIN diodes, transistors as switches or MEMS switches; (ii) by using tunable elements such as varactor diodes, tunable inductors and impedance transformers, in the IMN or OMN stage of an LNA. On the other hand, concurrent MBIMNs can achieve simultaneous matching at multiple frequency bands while rejecting the interfering bands. Contrary to reconfigurable IMN, concurrent IMN provides the desired multiband response without the requirement of additional tuning/switching circuitry. Designing an MBIMN requires a perfect impedance match at multiple frequencies. A comprehensive and fathomable design procedure can ease the process to obtain highly accurate results.

3.3 Broadband IMN Design

Broadband IMN design can be achieved using a bandpass filter design technique. Figure 3.4 shows the concept of bandpass IMN design using frequency transformation. A second order bandpass network can be achieved from an $L-$match. However, impedance and frequency scaling is required to design a bandpass network from an $L-$match. The frequency scaling for a low pass prototype is accomplished by multiplying the

frequency ω by a factor $1/\omega_c$ [138].

$$\omega \leftarrow \frac{\omega}{\omega_c} \tag{3.14}$$

where ω_c is the low pass cutoff frequency. For impedance scaling, we first need to determine the element values for a maximally flat type prototype. For an $n^{th}-$order prototype. The element values are calculated as

$$g_k = 2\sin\left[\frac{(2k-1)\,\pi}{2n}\right] \qquad k = 0, 1, 2...n \tag{3.15}$$

Since, $L-$match is a second order low pass network therefore, $n = 2$. From (3.15), the values of prototype elements g_1 and g_2 are 1.41 each [138]. If Z_0 is the source impedance, then element values can be transformed as

$$L = \frac{Z_0 g_1}{\omega_c} \tag{3.16a}$$

$$C = \frac{g_2}{Z_0 \omega_c} \tag{3.16b}$$

For scaling the low pass frequency to bandpass, consider ω_{p1} and ω_{p2} are passband edges. Then, frequency transformation follows[138]

$$\omega \leftarrow \frac{1}{\delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{3.17}$$

where

$$\delta = \frac{\omega_{p2} - \omega_{p1}}{\omega_0} \tag{3.18a}$$

$$\omega_0 = \sqrt{\omega_{p1}\omega_{p2}} \tag{3.18b}$$

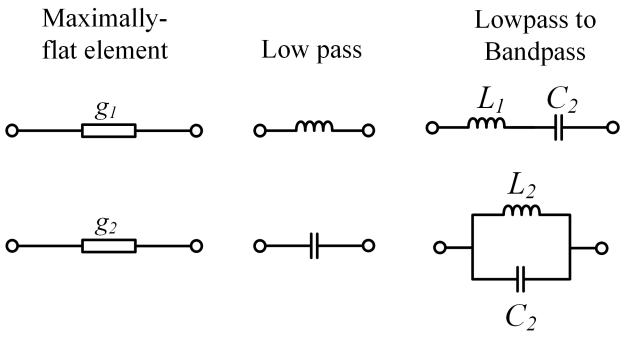


Figure 3.4: Transformation of source elements to low pass and further to bandpass network

δ is the fractional bandwidth and ω_0 is the centre frequency of the passband. For transformation from low pass to band pass, the condition must follow that $\omega_0 = \omega_c$. As shown in Figure 3.4, impedance transformation from low pass to bandpass prototype occurs after inductor L is transformed into a series connection of inductor L_1 and capacitor C_1. Alternatively, capacitor C is modelled as a parallel connection of inductor L_2 and capacitor C_2. Impedance scaling can be achieved through the following set of equations [138]

$$L_1 = \frac{L}{\delta} \tag{3.19a}$$

$$C_1 = \frac{\delta}{L\omega_0^2} \tag{3.19b}$$

$$L_2 = \frac{1}{C\omega_0^2} \tag{3.19c}$$

$$C_2 = \frac{C}{\delta} \tag{3.19d}$$

Design Example A: The objective is to design a wideband bandpass match to an arbitrary resistive load Z_0 = 100 Ω. The operating bandwidth is from 0.5 GHz to 1.5 GHz and hence $\omega_{p1} = 0.5$ GHz and $\omega_{p2} = 1.5$ GHz. Using the bandpass transformation analysis presented in (3.14) – (3.19), a bandpass filter based wideband IMN can be designed as shown in Figure 3.5 (a). The simulated response of the designed wideband

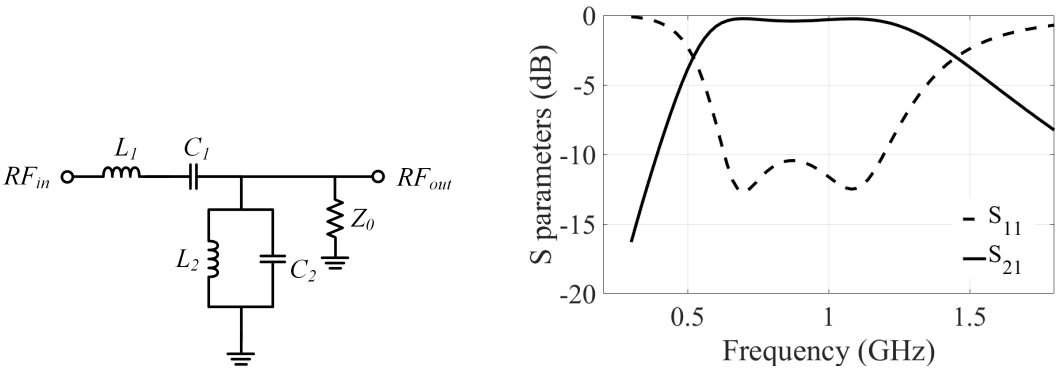


Figure 3.5: (a) A 0.5 to 1.5 GHz wideband IMN matched to 100 Ω (b) Simulated S-parameter response of designed wideband IMN

IMN is shown in Figure 3.5 (b). The bandpass match is achieved from the calculated values of L_1, C_1, L_2 and C_2. The achieved operational return loss bandwidth is 800 MHz (500 MHz – 1.3 GHz) and 3-dB insertion loss bandwidth is 1 GHz (500 MHz – 1.5 GHz).

Based on this technique, a wideband LNA operating from 0.5 GHz to 1.5 GHz can be designed with flat and wideband gain. However, in this case, impedance is matched to a complex load. The active device used in this example is ATF34143 from Avago Technologies. Using the Smith Chart tool and S-probe pair in Keysight Advanced Design System (ADS), impedances Z_s and Z_L towards the gate and drain of the transistor, respectively can be evaluated. At ω_0 = 868 MHz, $Z_s = 53.2 - j37.3\Omega$, which means that Z_s is capacitive. Likewise, $Z_L = 2.35 + j6.85\Omega$ and it is inductive. Since Z_s is complex, an intermediate wideband IMN can be designed to match Z_{in} with Z_s if, $|Z_{in}|$ = $|Z_s^*|$. Using equations (3.15) to (3.19), a second order broadband IMN can be designed for the LNA. The designed broadband LNA using bandpass IMN is shown in Figure 3.6 (a). Input impedance Z_{in_B} for designed broadband LNA is derived as

$$Z_{in_B} = \left(j\omega L_1 + \frac{1}{j\omega C_1}\right) + \left(j\omega L_2 \| \frac{1}{j\omega C_2}\right) \| R_b \| \left(j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}\right) \tag{3.20}$$

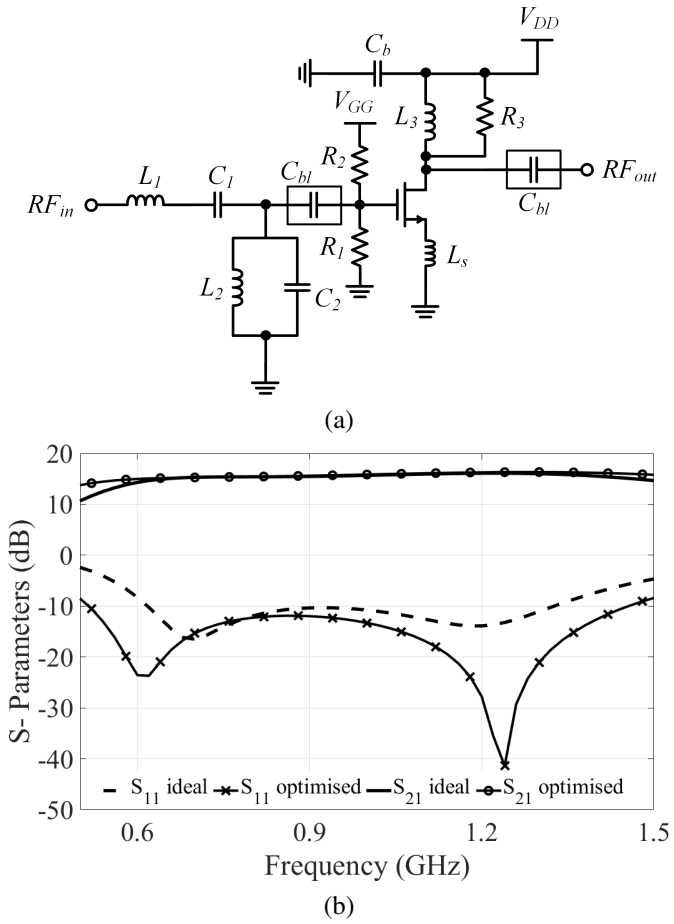


Figure 3.6: (a) A 0.5 to 1.5 GHz wideband IMN matched to 100 Ω [L_1 = 9.5nH, C_1 = 3.5 pF, L_2 = 13.8 nH, C_2 = 0.28 pF, R_1 = 100 Ω, $R_2 = R_3$ = 400 Ω, L_3 = 12 nH, C_b = 2.1 pF] (b) Simulated S-parameter response of designed wideband IMN

where $R_b = R_1||R_2$.The LNA utilises the wideband property of input IMN to achieve a flat and wide gain. A source degenerated inductor L_s is added to the circuit to increase the real part of IMN and to improve the reverse isolation. A complex parallel $R - L$ load is added to the output of LNA to achieve high flat gain from 500 MHz to 1.5 GHz. Figure 3.6 (b) shows the simulated performance of the example broadband LNA. The LNA achieves a flat and wideband gain (S_{21}) of more than 15 dB in the entire bandwidth. The LNA gain has been optimised to increase the 3-dB bandwidth. The S_{11} ideal is less than –10 dB from 600 MHz to 1.35 GHz and is optimised to less than –14 dB from 500 MHz to 1.5 GHz.

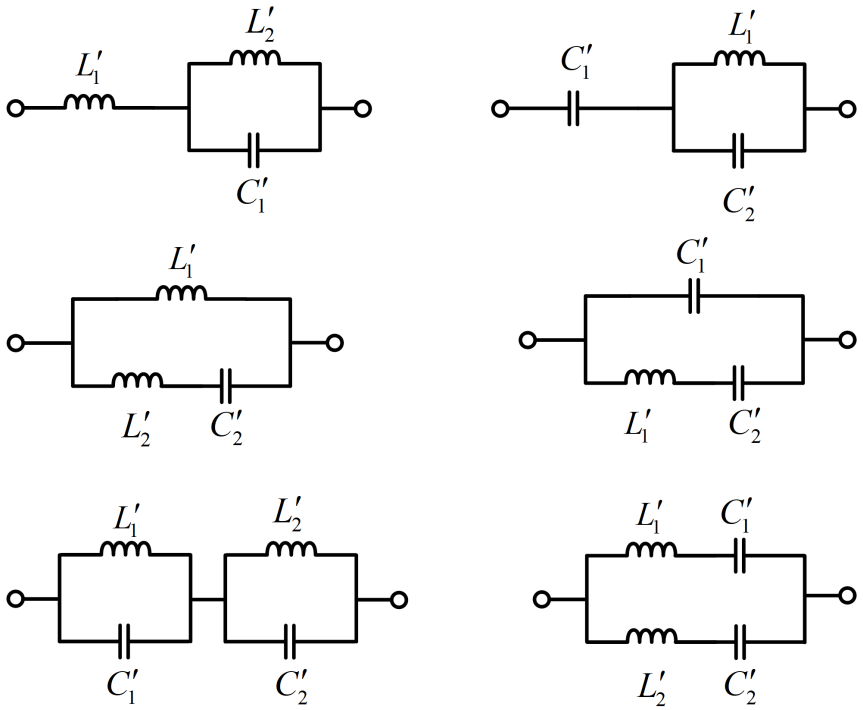


Figure 3.7: Possible configurations of first order DBIMN

3.4 Concurrent Multiband IMN Design

Concurrent MBIMNs for SDR LNAs require the input impedance to be matched to the source impedance at multiple frequencies, concurrently. In this section, we present the design and analysis of a concurrent dual band and a triband IMN. First order dual band resonators are commonly implemented technique for designing a DBIMN. Figure 3.7 shows possible first order DBIMN configurations. Conventional first order IMNs have lower efficiency and may result in reverse gain. In contrast, a high efficiency second-order dual band match results in a perfect impedance match, minimum losses at operational bands and high stopband loss between operating bands to reduce interference from other frequencies. This section discusses a step wise analytical approach for designing highly efficient second order DBIMN and TBIMN. Figure 3.8 shows the concept of impedance scaling and frequency transformation from an $L-$match to a dual band match and further to a triband match.

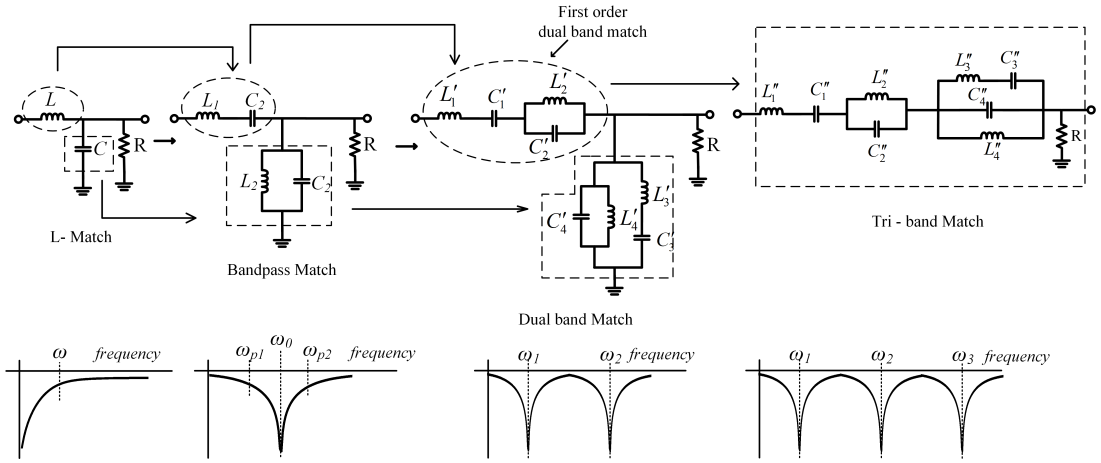


Figure 3.8: Concept of frequency mapping from $L-$match to dual band and triband match

3.4.1 Dual band IMN design

The aim is to design a DBIMN operating concurrently at two desired frequencies, say f_1 and f_2 where, $f_2 > f_1$. The first step is to transform a narrowband $L-$match into two single band bandpass networks, each operating at f_1 and f_2, respectively. The fractional bandwidth δ may be considered as 15% of the original bandwidth for each band. Additionally, ω_0 will be equal to the operating frequency for each network. The technique may follow the analysis proposed in section 3.3. The next step is to transform the two designed bandpass networks centered at f_1 and f_2 into a dual band network. The impedance scaling is achieved by mapping the series inductor L_1 into a series connection of L_1'–C_1' and the capacitor C_1 into a parallel connection of L_2'–C_2'. Likewise, the parallel inductor L_2 is transformed into a series connection of L_3'–C_3' to ground and the capacitor C_2 is transformed into a parallel L_4'–C_4' connection to ground.

$$L_1' = \frac{1}{2} \cdot \frac{\omega_2 L_{1,\omega 2}}{\omega_2 + \omega_1} \tag{3.21a}$$

$$C_1' = \frac{1}{\omega_1 \omega_2 L'_1} \tag{3.21b}$$

$$L_2' = \frac{(L_{1,\omega_1} - L_{1,\omega_2})}{2} \times \frac{\omega_2 - \omega_1}{\omega_2 + \omega_1} \tag{3.21c}$$

$$C_2' = \frac{1}{\omega_1 \omega_2 L'_2} \tag{3.21d}$$

where $\omega_1 = 2\pi f_1$, $\omega_2 = 2\pi f_2$, $L_{1,\omega 1}$, $L_{1,\omega 2}$ are the calculated values of inductor L_1 at f_1 and f_2, respectively. Furthermore, if $C_{1,\omega 1}$, $C_{1,\omega 2}$ are values of capacitor C_1; $C_{2,\omega 1}$, $C_{2,\omega 2}$ are the values of capacitor C_2 and $L_{2,\omega 1}$, $L_{2,\omega 2}$ are the values of inductor L_2 at two desired frequencies f_1 and f_2; then remaining element values in the DBIMN network can be calculated as

$$L_3' = \frac{1}{(\omega_2^2 - \omega_1^2) \cdot C_{1,\omega 1}} + L_{1,\omega 2} \tag{3.22a}$$

$$C_3' = \left(\frac{C_{1,\omega_1}}{1 + \omega_1^2 L_{2,\omega_1} C_{2,\omega_1}} \right) \times \frac{\omega_2^2 - \omega_1^2}{\omega_2^2 + \omega_1^2} \tag{3.22b}$$

$$L_4' = \left(\frac{L_{1,\omega_1}}{1 + \omega_1^2 L_{2,\omega_1} C_{2,\omega_2}} \right) \times \frac{\omega_2^2 - \omega_1^2}{\omega_2^2 + \omega_1^2} \tag{3.22c}$$

$$C_4' = \frac{1}{(\omega_2^2 - \omega_1^2)\, L_{1,\omega_1}} + C_{1,\omega_2} \tag{3.22d}$$

Design Example B: In this example, we propose the design of a DBIMN operating concurrently at 900 MHz and 2.0 GHz. Value of δ depends upon the bandwidth required. In this example, δ is 20% of the bandwidth in each band. We aim to design an IMN to match a 50 Ω resistive load. Now using equations (3.16) to (3.19), (3.21a) – (3.21d) and (3.22a) – (3.22d), a DBIMN can be designed as shown in Figure 3.9 (a). To verify its accuracy, the design was simulated in Keysight ADS. The simulated S_{11} and S_{21} of designed DBIMN are shown in Figure 3.9 (b). Equivalent impedance of designed DBIMN is

$$Z_{eq-DB} = \left(\frac{(\omega^2 L_1 C_1 - 1)(\omega^2 L_2 C_2 - 1) + \omega^2 C_1 C_2}{j\omega C_1 - j\omega^3 L_2 C_1 C_2} \right) + \left(\frac{j\omega C_4 - j\omega^3 L_3 C_3 C_4}{(1 - \omega^2 L_3 C_3)(1 - \omega^2 L_4 C_4) - \omega^2 C_3 C_4} \right) \tag{3.23}$$

3.4.2 Triband IMN Design

As shown in Figure 3.8, a conventional narrowband matching network can be transformed into a TBIMN by mapping its bandpass response into a triband response. The first step is to transform three low pass networks to three bandpass networks centered at three frequencies f_1, f_2 and f_3, respectively. The fractional bandwidth δ is considered as 15% of original bandwidth for each band. Thereafter, we design a first order dual band prototype that provides impedance match at f_1 and f_2. From the first-order dual band prototype, the series $L_1' - C_1'$ can be transformed to series $L_1'' - C_1''$ and parallel $L_2'' - C_2''$. The parallel $L_2' - C_2'$ can be transformed to series $L_3'' - C_3''$ and parallel $L_4'' - C_4''$ to form an indefinite triband prototype as shown in Figure 3.8. Considering that $f_3 > f_2 > f_1$, the values of inductors and capacitors can be calculated using the following analysis to design the desired TBIMN.

$$L_1'' = \frac{1}{2} \cdot \frac{\omega_1 \left(L_{1,\omega 1} + L_{1,\omega 2} + L_{1\omega 3}\right)}{\omega_3 + \omega_2 + \omega_1} \tag{3.24a}$$

$$C_1'' = \frac{1}{\omega_1 \omega_2 L''_1} \tag{3.24b}$$

$$L_2'' = \frac{\left(L_{1,\omega_1} - L_{1,\omega_2} - L_{1,\omega_3}\right)}{2} \times \frac{\omega_2 - \omega_1}{\omega_2 + \omega_1} \tag{3.24c}$$

$$C_2'' = \frac{1}{\omega_1 \omega_2 L''_2} \tag{3.24d}$$

where L_{1,ω_1}, L_{1,ω_2}, L_{1,ω_3} are the values of inductor L_1 (in Fig.3.8) at f_1, f_2, f_3, and $\omega_n = 2\pi f_n$, n= 1,2,3. The remaining element values in TBIMN are calculated as:

$$L_3'' = \frac{1}{2 \cdot \omega_2^2 C_{1,\omega 3}} \times U_x \tag{3.25a}$$

$$\frac{1}{C''_3} = \left(\frac{1}{C_{1,\omega 3}} + L_{2,\omega 2}\omega_2^2\right) \times \frac{1}{2U_x} \tag{3.25b}$$

$$\frac{1}{L''_4} = \left(\frac{1}{L_{2,\omega 1}} + C_{2,\omega 2}\omega_3^2\right) \times \frac{1}{2U_x} \tag{3.25c}$$

$$C_4'' = \frac{1}{2 \cdot \omega_3^2 L_{2,\omega 3}} \times U_x \tag{3.25d}$$

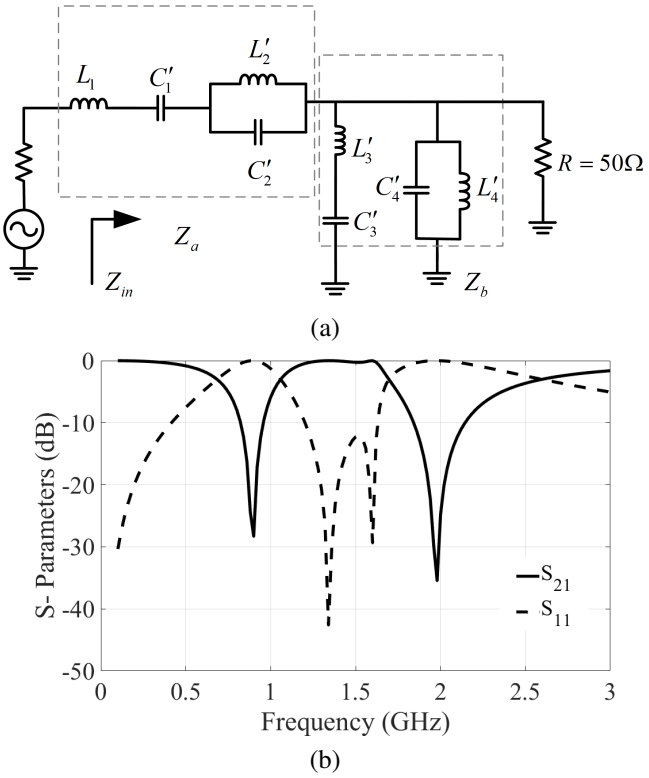


Figure 3.9: (a) DBIMN matched to 50 Ω (b) Simulated S-parameter response of designed DBIMN [Element values- L_1' = 12.89 nH, C_1' = 1.09 pF, L_2' = 8.66 nH, C_2' = 1.62 pF, L_3' = 58.5 nH, C_3' = 0.17 pF, L_4' = 38 nH, C_4' = 0.26 pF]

where $U_x = (\omega_3^2 - \omega_2^2 + \omega_1^2)/(\omega_3^2 + \omega_2^2 + \omega_1^2)$, $L_{2,\omega 2}$, $L_{2,\omega 3}$ are the values of inductor L_2 at f_2, f_3, respectively, $C_{1,\omega 3}$ and $C_{2,\omega 2}$ are the values of capacitors C_1 and C_2 at f_3 and f_2, respectively.

Design Example C: This example proposes the design of a concurrent TBIMN operating at 900 MHz, 2.4 GHz and 3.2 GHz. The load impedance is 50 Ω. A TBIMN with reactive elements can designed by scaling the frequencies and impedances shown in Figure 3.8. Thereafter, three bandpass networks centred at 900 MHz, 2.4 GHz and 3.2 GHz are designed using equations (3.16) to (3.19). Further, using the synthesis proposed in equations (3.24a) – (3.24d) and (3.25a) – (3.25d), element values for the triple band match are obtained. The designed TBIMN after transformation and synthesis is shown in Figure 3.10 (a). The designed circuit is then simulated in Keysight ADS to

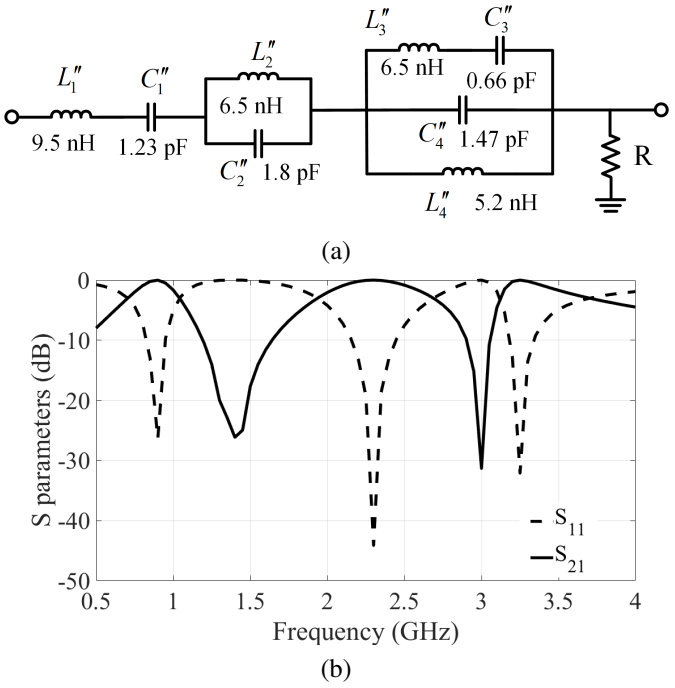


Figure 3.10: (a) TBIMN matched to 50 Ω (b) Simulated S-parameter response of designed TBIMN

verify the theoretical model. Figure 3.10 (b) shows the simulated S_{11} and S_{21} for the design TBIMN. Equivalent impedance of TBIMN Z_{eq-TB} is expressed as

$$Z_{eq-TB}(j\omega) = \left(\frac{1-\omega L''_1 C''_1}{j\omega C''_1} + \frac{j\omega C''_2}{1-\omega^2 L''_2 C''_2}\right) + \left(\frac{1-\omega^2 L''_3 C''_3}{j\omega C''_3} || \frac{j\omega C''_4}{1-\omega^2 L''_4 C''_4}\right) \quad (3.26)$$

3.5 Implementation and Results

3.5.1 DBIMN Implementation

The designed DBIMN in Section 3.4.1 is fabricated on (i) an FR-4 board (ε_r = 4.6, height (h) = 1.5 mm) with lumped components, and (ii) on a Roger's 5880 board (ε_r = 2.2, h = 0.254 mm) with microstrip lines (distributed elements). The transformation in

latter case is achieved by converting impedance of different IMN sections (Z_a and Z_b) into microstrip lines. Varying impedances in the IMN consisting of series and parallel components are converted into microstripline stubs of different lengths and widths. Figure 3.11 (a) – (g) shows equivalent distributed element models for lumped elements. Microstrip components designed in MIC/ microwave printed circuit board (MPCB) utilise the right configuration of lines and shapes to form passive elements. Some series inductors are implemented on the substrate using thin microstrip lines. Figure 3.12 (a) shows DBIMN implementation with lumped elements on FR-4 board and Figure 3.12 (b) shows DBIMN implementation with microstrip lines on Roger's 5880 board. Simulation has been carried out using Keysight ADS and MATLAB. Circuit analysis in both cases was done using EM simulation.

Figure 3.13 (a) shows the simulated and measured S_{11} for designed DBIMN with lumped components. Simulated and implemented element values are slightly different from the calculated values due to additional impedance induced from 0805 element pads and connecting microstrip lines. The simulated S_{11} is –15 dB and –20 dB at 1 GHz and 2.02 GHz, respectively. The measured S_{11} is –14 dB and –10 dB at 1 GHz and 2.02 GHz, respectively.

Figure 3.13 (b) shows the EM simulated and measured S_{11} and S_{21} for designed DBIMN with microstrip lines. The circuit achieves a minimum measured S_{11} of –20 dB at 850 MHz and –23 dB at 2 GHz. Additionally, measured S_{21} is –4 dB at 850 MHz and –3.5 dB at 2 GHz.

3.5.2 TBIMN Implementation

The TBIMN proposed in Section 4.2 has been implemented on an FR-4 board. Figure 3.14 shows the fabricated TBIMN. To improve the efficiency of the IMN, physical inductors are replaced with their microstrip equivalent model. The conversion was

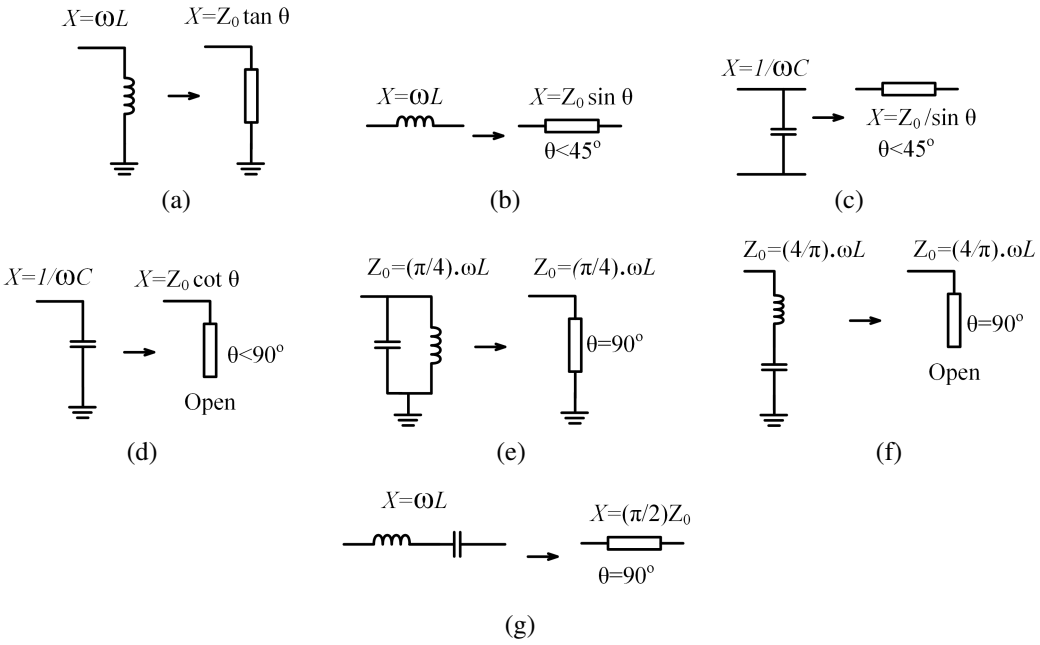


Figure 3.11: Lumped to distributed transmission line conversion (a) Inductor shunt to ground (b) Series inductor (c) Shunt capacitor (d) Capacitor shunted to ground (e) Parallel $L-C$ to ground (f) Series $L-C$ shunt to ground (g) Series $L-C$ in series

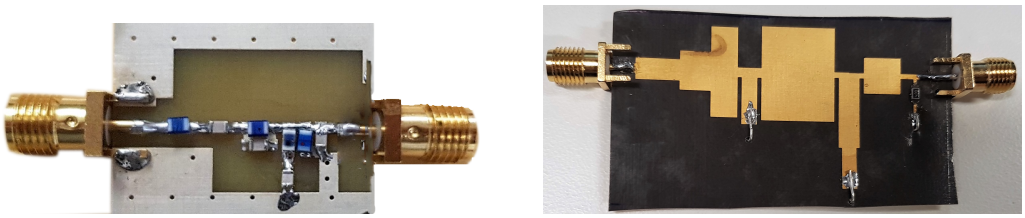
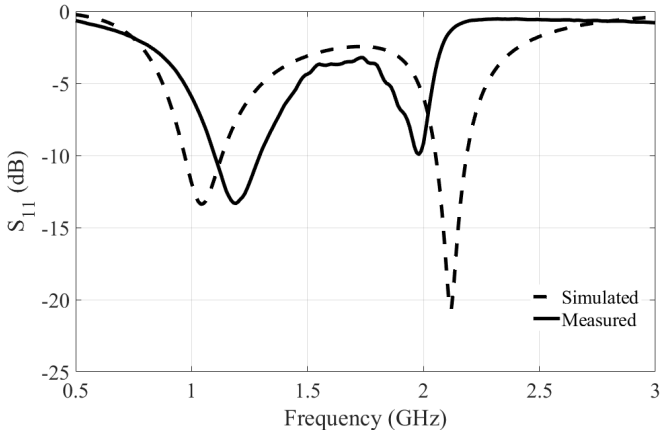


Figure 3.12: Fabricated DBIMN Prototype (a) with lumped elements (b) microstrip distributed elements

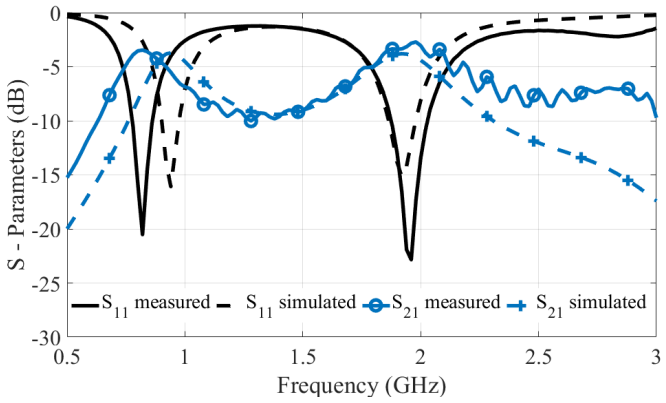
achieved from the analysis shown in Figure 3.11 (a) – (g). The equivalent inductance from lengths l and widths w of microstrip lines is calculated as [139]

$$L = 0.00508l\left[\ln\left(\frac{2l}{w+h}\right) + 0.5 + 0.2235\left(\frac{w+h}{l}\right)\right]\mu H \tag{3.27}$$

where h is the distance between the strip and the ground plane. The conversion leads to minimal losses due to high Q-factor of the fabricated TBIMN, thereby improving its efficiency and f_T. Additionally, high-Q 0603 capacitors are implemented on PCB to



(a)



(b)

Figure 3.13: Simulated and measured S-parameters of designed DBIMN with (a) lumped elements (b) microstrip distributed elements

reduce the chip size and achieve minimum return loss. Figure 3.15 (a) shows the EM simulated and measured S_{11} and S_{21} for the designed TBIMN. The measured S_{11} values are –44.6 dB, –14.7 dB and –33.9 dB; and S_{21} is –0.20 dB, –0.82 dB and –2.5 dB at 970 MHz, 2.41 GHz and 3.24 GHz, respectively. Figure 3.15 (b) shows the variation of Z_{in} for the designed triband IMN with frequency. The IMN achieves a perfect impedance match at all stipulated frequencies and measured Re(Z_{in}) is 50 Ω at 0.97 GHz, 2.4 GHz and 3.2 GHz.

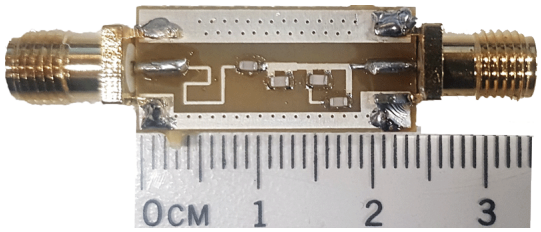
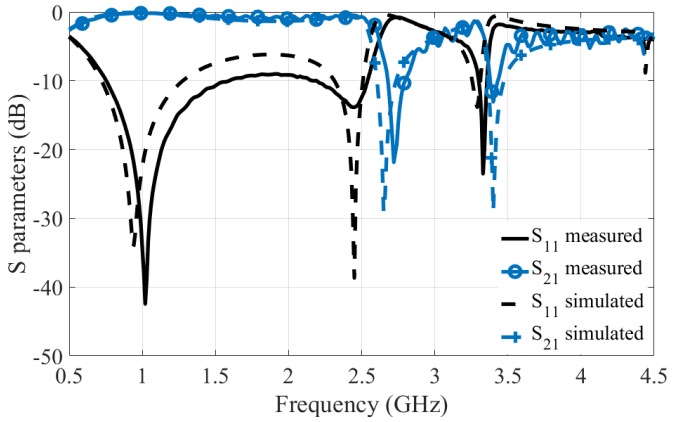
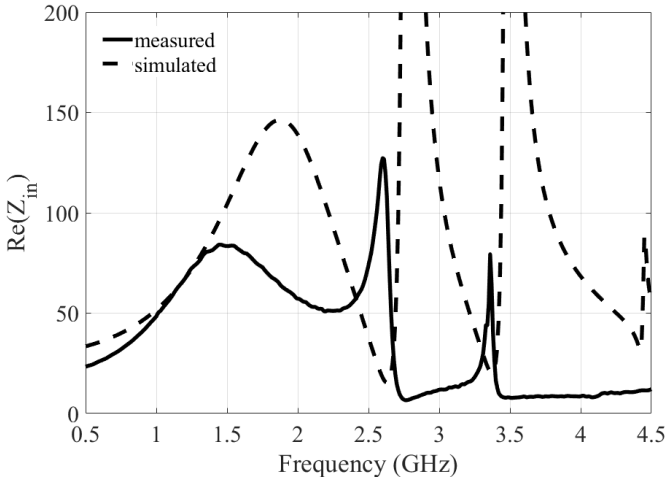


Figure 3.14: Fabricated TBIMN prototype



(a)



(b)

Figure 3.15: (a) Simulated and measured (a) S-parameters (b) Re(Z_{in}) of designed TBIMN Prototype

3.6 Conclusion

The design of concurrent multiband matching networks for LNAs in SDRs has been proposed. This chapter discusses wideband and multiband matching concepts with

mathematical analysis. A methodology for designing novel dual band and triband impedance matching networks using IFTT is presented. Novel design equations for deriving circuit elements are presented with comprehensible analysis. The equations formulated can be used to design a dual and a triple band matching network at any bands of operation. Design of a DBIMN operating at 900 MHz and 2.0 GHz, and a TBIMN operating concurrently at 900 MHz, 2.4 GHz and 3.2 GHz has been presented. The designed circuits are converted into their microstrip equivalents to improve matching efficiency. Thereafter, the dual band matching circuit is fabricated on a Roger's 5880 board using microstrip lines and on an FR-4 board using lumped components. The triband matching circuit is fabricated on an FR-4 substrate using microstrip lines and lumped capacitors. The designed IMNs achieve a very high measured IRL, high stopband attenuation and a perfect impedance matching at operational bands.

Chapter 4

Design and Analysis of a Concurrent Dual Band LNA

4.1 Introduction

The demand for multiband transceivers has proliferated substantially in communication systems involving cellular, defense and satellite communications. Multiband transceivers can accommodate different bands, ideally integrated into a compact circuit and efficient performance [140]. Among multiband transceivers, concurrent multiband transceivers are capable of handling multiple distinct standards with high precision and accuracy. Multiband transceivers require MBLNAs in receiver front-end since, each element in the chain must achieve multiband operation. The design of concurrent MBLNA involves major challenges like generation of multiple passbands, high gain, and high interference suppression.

Concurrent MBLNAs are the preferred choice for multiband transceivers over wideband LNAs and tunable LNAs. They do not require multiple parallel amplifiers for generating multiple passbands and thus consume less power [39]. Other associated benefits are interference suppression, efficient passband generation, and stopband rejection.

Existing DBLNA and MBLNA designs have implemented wideband IMNs for designing the input and output matching stages [48, 49, 85, 127]. IRR in these designs is achieved by increasing SBRR. A widely adopted technique is to use MITs [82, 141, 142] that consumes less power but increases the MIC size.

Other DBLNA and MBLNA designs reported in [128, 129, 143, 144] implemented multiband notches for designing the OMN and lacked ideal passband generation and stopband rejections. Thereafter, MBLNAs proposed in [48, 51, 95] implemented novel dual band and triband loads for optimum passband generation. However, the linearity was degraded and power consumption was high [48]. Alternative techniques for multiband IMN design include synthesis and transformation techniques [45, 98], resonant transformer [93] and transmission line stubs [103].

IFTT or frequency mapping proposed in chapter 3 allows synthesis of two single band matching networks to form a DBIMN. This technique facilitates achieving an optimum input matching, reduced power consumption of the circuit as well as reduced PCB or chip size.

Based on MBIMN design technique proposed in Chapter 3, this chapter aims to design and analyze a concurrent DBLNA operating at 1.1 and 2.4 GHz with perfect dual band impedance matching, sufficient SBRR, optimum passband generation, less GI and high IRR. The IMN is designed and analyzed using the frequency mapping technique proposed in Chapter 3 which follows the IFTT. The dual band operation is realized by employing dual bandpass load resonators at the output. The LNA is fabricated on an FR-4 substrate in MIC technology. The proposed DBLNA employs a cascaded stage to improve the total gain. In addition, it also provides a stable and linear operation without increasing the circuit size and power consumption.

4.2 Design of Concurrent DBLNA

The conventional DBLNA shown in Figure 2.7 (a), implements a wideband IMN and a conventional dual band load. Although wideband input matching could accommodate better operating frequency range, it requires additional filtering and a vigilant frequency planning because of interference. Therefore, a DBIMN is desired for a concurrent DBLNA. The wideband IMN in Figure 2.7 (a) can be converted into DBIMN by mapping its bandpass response into a dual band response. The conversion is done by performing a frequency transformation from low pass to bandpass network, and then from bandpass to dual band network.

4.2.1 Input Matching Network

The concept of frequency mapping from a low pass network to a dual band network is illustrated in Figure 3.8. The design procedure firstly involves mapping from a low pass $L-$matching network to a bandpass network and subsequently to a dual band network. The first step is to design two bandpass networks, each with centre frequencies f_1 and f_2, respectively. The low pass and bandpass element values at the two selected frequencies f_1 and f_2 can be determined using equations (3.14) to (3.19). In this case, the input impedance must be matched to a complex impedance Z_s at the input of transistor. Z_s at f_1 = 1.1 GHz is 24 + j15 Ω and at f_2 = 2.4 GHz is 14 + j30 Ω. To determine the ideal values of elements, we take the the magnitude of Z_s at f_1 and f_2 to design bandpass networks at these two frequencies.

Thereafter, the two individual bandpass networks are converted into a dual band network using the impedance scaling proposed in Figure 3.8. The design process follows the procedure outlined in section 3.4.1. Finally, the dual band element values at f_1 and f_2 are calculated using proposed equations (3.21a) – (3.21d) and (3.22a) – (3.22d).

Figure 4.1 (a) shows the proposed DBMIN design which follows the analysis outlined

in chapter 3. The values of inductances and capacitances are calculated at 1.1 GHz and 2.4 GHz. For simplicity, the network has been divided into two impedances Z_a and Z_b to write an explicable equation. The input impedance of the designed matching circuit can be expressed as:

$$Z_{in} = Z_a + Z_b \| R_b \| \left(j\omega L_s + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1} L_s}{C_{gs1}} \right) \tag{4.1}$$

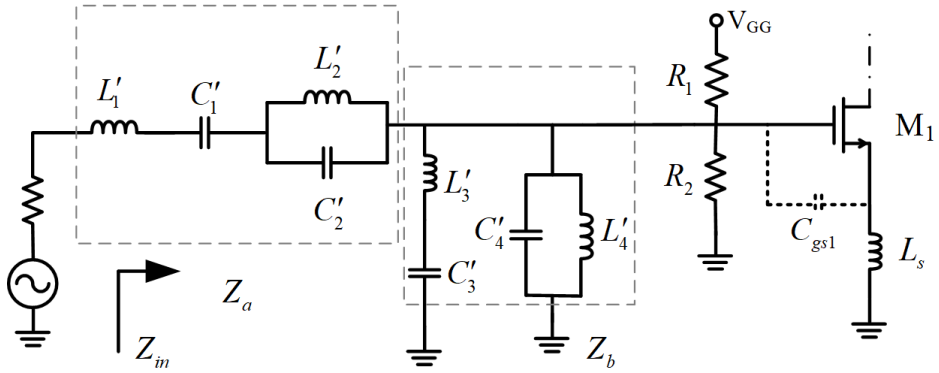
where $R_b = R_1 \| R_2$ is the equivalent of bias resistance and

$$Z_a = j \frac{(\omega^2 L'_1 C'_1 - 1)(\omega^2 L'_2 C'_2 - 1) + \omega^2 C'_1 C'_2}{\omega C'_1 - \omega^3 L'_2 C'_1 C'_2} \tag{4.2}$$

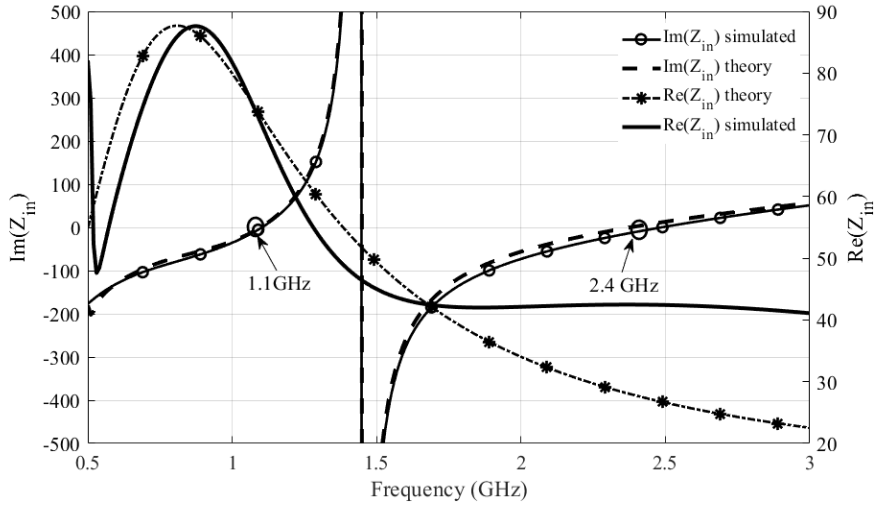
$$Z_b = j \frac{\omega C'_4 - \omega^3 L'_3 C'_3 C'_4}{(1 - \omega^2 L'_3 C'_3)(1 - \omega^2 L'_4 C'_4) - \omega^2 C'_3 C'_4} \tag{4.3}$$

Equation (4.1) can be solved to plot the frequency response of the designed IMN for a DBLNA. The complex impedance at the input of selected transistor is 24 + j15 Ω at 1.1 GHz, and 14 + j30 Ω at 2.4 GHz, g_m = 34 S and C_{gs}= 1.5 pF. Figure 4.1 (b) shows the simulated and theoretical frequency response of the designed DBIMN. It can be seen that a perfect input impedance match is achieved with Z_s for the designed DBIMN as Im(Z_{in}) is 0 Ω, while Re(Z_{in}) is matched to the the net real impedance at 1.1 GHz and 2.4 GHz, respectively.

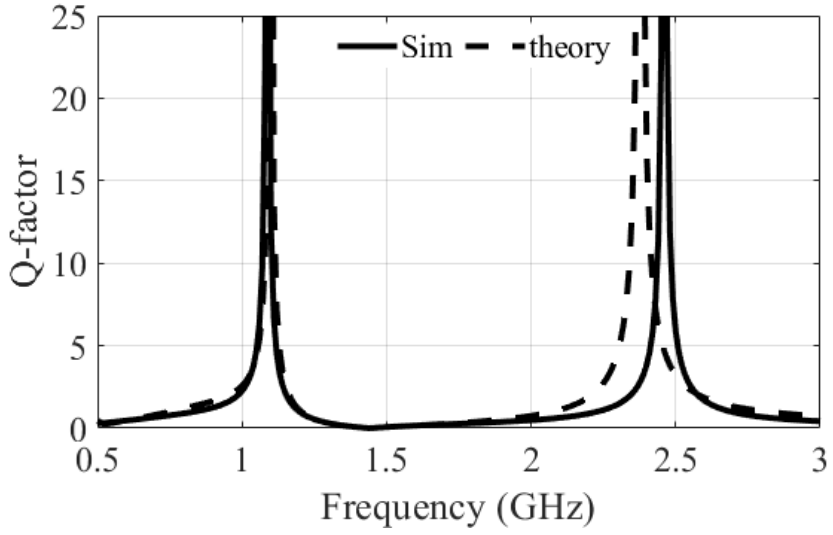
The Q-factor is the ratio of power stored to power dissipated in an IMN. Q of the circuit with passive matching components is required to be high at operating frequencies. Since the real part of impedance is parallel to the imaginary part, $Q = Re(Z_{in})/Im(Z_{in})$. Figure 4.1 (c) shows the theoretical and simulated frequency response of Q with ideal inductors and capacitors. In both cases, Q is greater than 25, indicating a minimal effect of Q-factor of passives on the IMN performance.



(a)



(b)



(c)

Figure 4.1: (a) IMN for the designed DBLNA (b) frequency response of IMN (c) $Q-$factor of the designed IMN

4.2.2 Design Strategy

The first step for designing the DBLNA is to consider the stipulated frequency bands. From the aforementioned analysis, we can calculate the component values for the IMN and design an optimal matching at desired operating frequencies. The second objective is to achieve an optimum passband gain with improved SBRR, minimum GI, high IRR between operating bands and most importantly, minimum noise matching. Generally, the IMN of LNA plays a role to achieve the desired noise matching in the operational bands. For a high IRR DBLNA, the noise matching is required to be achieved only for operational bands and NF must be high at stopbands. This is done by plotting gain and noise circles for the transistor. The 2 dB optimum NF circle is also plotted for a single stage amplifier. Thereafter, optimum reflection coefficient (Γ_{opt}) is plotted along with source reflection coefficient (Γ_s) for noise circles. The aim is to achieve the minimum difference between (Γ_{opt}) and (Γ_s), so that $F \approx F_{min}$. The circuit is then optimized to achieve minimum noise matching.

A conventional dual band load comprising a parallel $L_{l1} - C_{l1}$ pair and series $L_{l2} - C_{l2}$ pair, shown in Figure 2.7 (a), can be designed to get passbands and stopbands at desired frequencies. However, the passband at higher frequency does not provide a sharp roll-off characteristic and provides a wideband response as shown in Figure 2.7 (b). A modified dual band load is thus proposed for DBLNA. Figure 4.2 shows the schematic of the dual band load employing two bandpass notches and eliminating the stopband notch from conventional dual band load. These notches provide a parallel resonance at operating frequencies. Previous efforts to eliminate the stopband notch from dual band load lacked experimental validation [51]. The load impedance of the first stage is

$$Z_{load1} = \left(j\omega L_{l1} \| \frac{1}{j\omega C_{l1}} \right) + \left(j\omega L_{l2} \| \frac{1}{j\omega C_{l2}} \right) \tag{4.4}$$

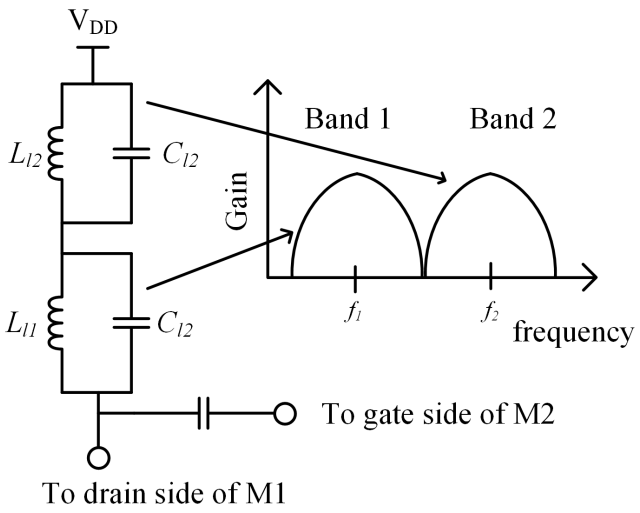


Figure 4.2: Implemented dual band load at the drain of M_1

The characteristic equation for Z_{load1} is

$$\omega^4 L_{l1} C_{l1} L_{l2} C_{l2} - \omega^2 \left(L_{l1} C_{l1} + L_{l2} C_{l2} \right) + 1 = 0 \tag{4.5}$$

Since, this is a fourth-order polynomial equation, calculating sum (S) and product (P) of roots would give the relationship between the operating frequencies and L_{l1}, C_{l1}, L_{l2} and C_{l2} .

$$S = \frac{L_{l1} C_{l1} + L_{l2} C_{l2}}{L_{l1} C_{l1} L_{l2} C_{l2}} = \omega_1^2 + \omega_2^2 \tag{4.6}$$

$$P = \frac{1}{L_{l1} C_{l1} L_{l2} C_{l2}} = \omega_1^2 \cdot \omega_2^2 \tag{4.7}$$

Solving (4.6) and (4.7) values of L_{l1}, C_{l1}, L_{l2} and C_{l2} can be determined by

$$\left(L_{l1} C_{l1} \right)^{-1} = \omega_1^2 \tag{4.8}$$

$$\left(L_{l2} C_{l2} \right)^{-1} = \omega_2^2 \tag{4.9}$$

Figure 4.3 shows the design of proposed DBLNA employing a second order $L - C$ based IMN and a modified dual band load at the output of each stage. The proposed

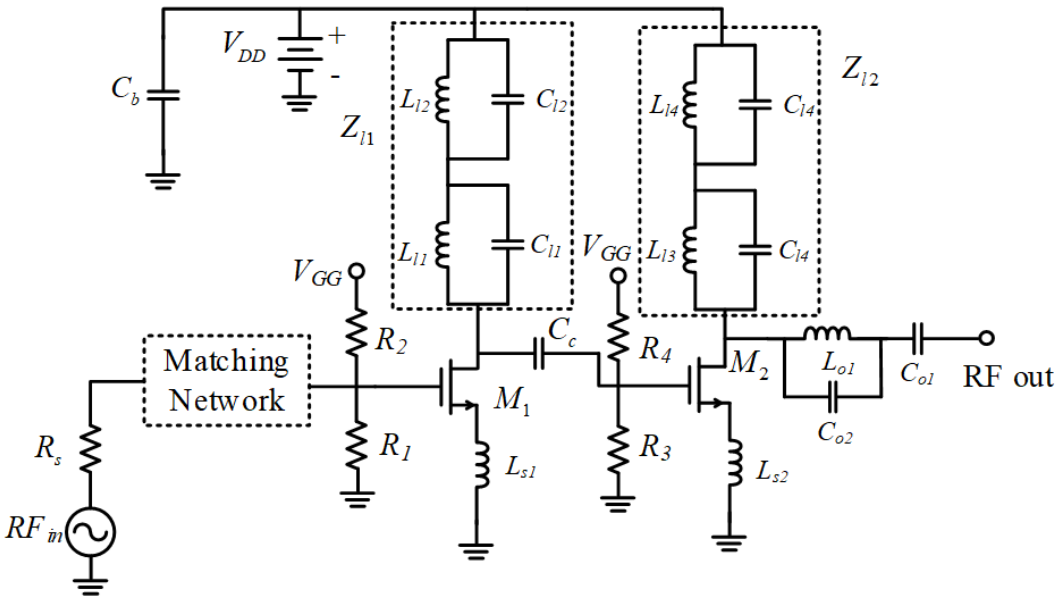


Figure 4.3: Schematic of 1.1 and 2.4 GHz DBLNA

circuit is a two-stage LNA with capacitive coupling between stages. Cascaded design improves the forward gain and reverse isolation. A source inductance of 0.24 nH is added to both transistors to improve the LNA stability and reverse isolation. Both transistors M_1 and M_2 in the DBLNA are identical. The design objective is to cover both operating frequency bands with optimized pass band performance, good gain-linearity balance, and adequate reverse isolation. The operating frequencies for passbands are centered at 1.1 GHz and 2.4 GHz. The circuit is designed to provide an efficient dual band matching and high gain. The IMN utilizes the dual band filter properties and two bandpass resonators in the load provide two distinct passbands each centered at stipulated frequencies. The dual band load does not reduce the voltage headroom of input stage and provides a desired wide and concurrent response in two bands. Bandpass notches in the output stage of LNA minimize GI and phase mismatch. The OMN is designed to match the load impedance to 50 Ω using conventional first-order matching that involves a parallel $L_{o1} - C_{o2}$ circuit with a series capacitor C_{o1} that also blocks the DC at the output.

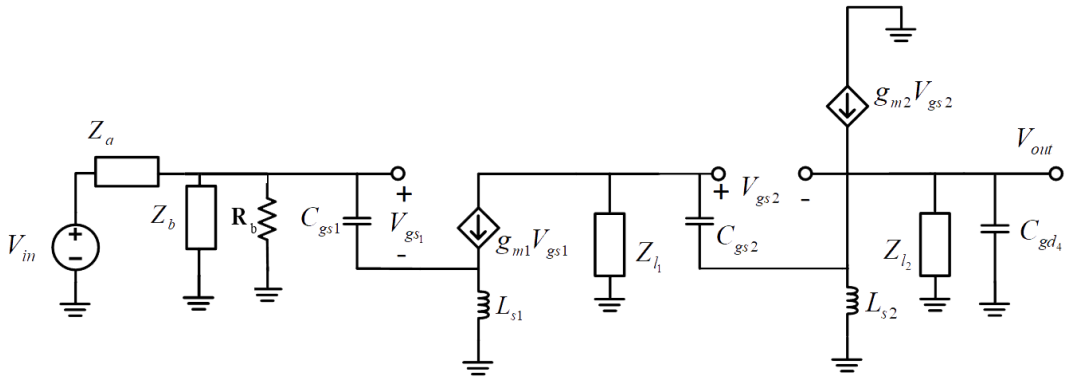


Figure 4.4: Small signal equivalent of the designed DBLNA

4.2.3 Gain

A single stage DBLNA can achieve good voltage gain. However, the cascaded stage of the LNA felicitates in achieving a higher gain in both bands of operation and suffices the required voltage gain for SDR. Figure 4.4 shows the small signal equivalent circuit of the designed DBLNA. The small signal transconductance parameters of M_1 and M_2 are $g_{m1}V_{gs1}$ and $g_{m2}V_{gs2}$. The output voltage (V_{out}) of the LNA is

$$V_{out} = g_{m2}V_{gs2} \cdot Z_{l2} \tag{4.10}$$

also,

$$V_{gs2} + V_{out} = -g_{m1}V_{gs1} \cdot Z_{l1} \tag{4.11}$$

where g_{m1} and g_{m2} are the transconductance, and V_{gs1} and V_{gs2} are the gate-source voltages of transistors M_1 and M_2, respectively. Z_{l2} is load impedance of second stage. The input voltage after applying KVL is

$$V_{in} = I_{in} \cdot Z_a + I_{in}\left(\frac{Z_b R_b \left(j\omega L_{s1} + 1/j\omega C_{gs1} + 1/g_m\right)}{Z_b + R_b + \left(j\omega L_{s1} + 1/j\omega C_{gs1} + 1/g_m\right)}\right) + g_m V_{gs}\left(j\omega L_{s1}\right) + V_{gs1} \tag{4.12}$$

where I_{in} is the input current from source V_{in}, and the current through C_{gs1}, $I_{cg} = V_{gs1}\,(jwC_{gs1}) \approx I_{in}$

$$V_{in} \;=\; V_{gs1} \cdot (j\omega C_{gs1}) \cdot \left(\left(\frac{1}{j\omega C_{gs1}} + \frac{g_{m1} L_{s1}}{C_{gs1}} + j\omega L_{s1} \right) \| R_b \, \| Z_a + Z_b \right) \quad (4.13)$$

where C_{gs_1} is the gate-source capacitance of M_1. Rearranging (4.13), we have

$$V_{gs1} = \frac{V_{in}}{(j\omega C_{gs1})\, Z_{in}} \quad (4.14)$$

From (4.11) and (4.14), we get

$$V_{gs2} = -g_{m1} Z_{l1} \cdot \frac{V_{in}}{j\omega C_{gs1} Z_{in}} - V_{out} \quad (4.15)$$

Substituting (4.15) in (4.10),

$$V_{out} = g_{m2} \left(-g_{m1} \frac{Z_{l1}}{j\omega C_{gs1} Z_{in}} . V_{in} - V_{out} \right) Z_{l2} \quad (4.16)$$

Solving (4.16), the voltage gain A_v is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-g_{m1} g_{m2} Z_{l1} Z_{l2}}{(j\omega C_{gs1} Z_{in})\,(1 + g_{m2} Z_{l2})} \quad (4.17)$$

Since both transistors M_1 and M_2 are same, therefore, $g_{m1} = g_{m2} = g_m$ and V_{gs1} = V_{gs2}; also, $L_{s1} = L_{s2} = L_s$. For the values of g_m = 34 S and V_{gs} = –0.53 V for the designed DBLNA, the derived theoretical dual band gain in (4.17) can be plotted with frequency as shown in Figure 4.5. The theoretical plot shows two distinct dual bands having a peak A_v at 1.1 and 2.4 GHz and IRR at 1.65 GHz.

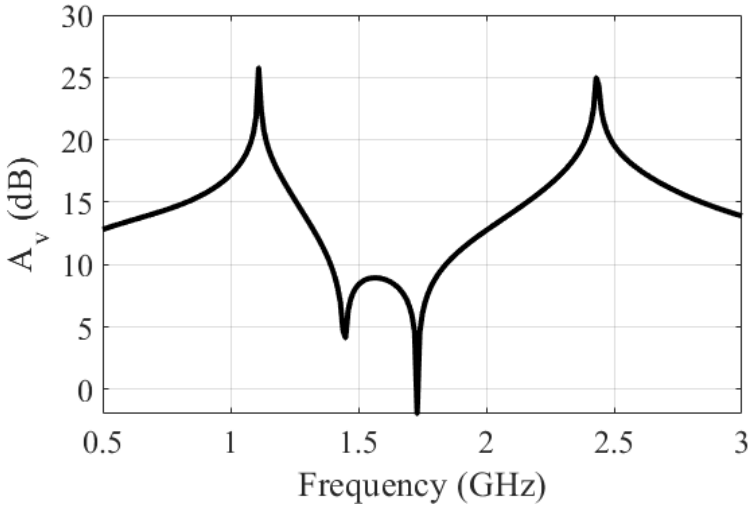


Figure 4.5: Theoretical gain for the designed DBLNA

4.2.4 Noise Analysis

The noise performance of the proposed DBLNA can be quantified by deriving its noise factor. Figure 4.6 (a) shows the noise equivalent model of the first stage. The main source of noise is thermal noise and all inductors and capacitors are considered to be ideal [96]. The primary thermal noise sources in the circuit are due to source $\overline{i^2_{n,s1}}$, induced gate $\overline{i^2_{n,g1}}$, drain $\overline{i^2_{n,d1}}$ and load $\overline{i^2_{n,rl1}}$. In the first stage of LNA, transistor M_1 contributes to more than 90 per cent of the noise in circuit. Therefore, the total short-circuit output noise current for first stage of designed DBLNA is derived below. The short-circuit noise current due to source is

$$i_{sc,R_s} = \frac{g_{m1} V_{n,s}}{sC_{gs1}\left(R_s + Z'_{in}\right)} \tag{4.18}$$

where $Z'_{in} = Z_a + Z_b \| \left(R_1 \| R_2\right)$. The short-circuit noise current due to induced gate and thermal drain noise of transistor M_1 is

$$i_{sc,g1} = \frac{g_{m1}\left(R_s + Z'_{in}\right) i_{n,g1}}{sC_{gs1}\left(R_s + Z'_{in} + g_{m1} L_s\right)} \tag{4.19}$$

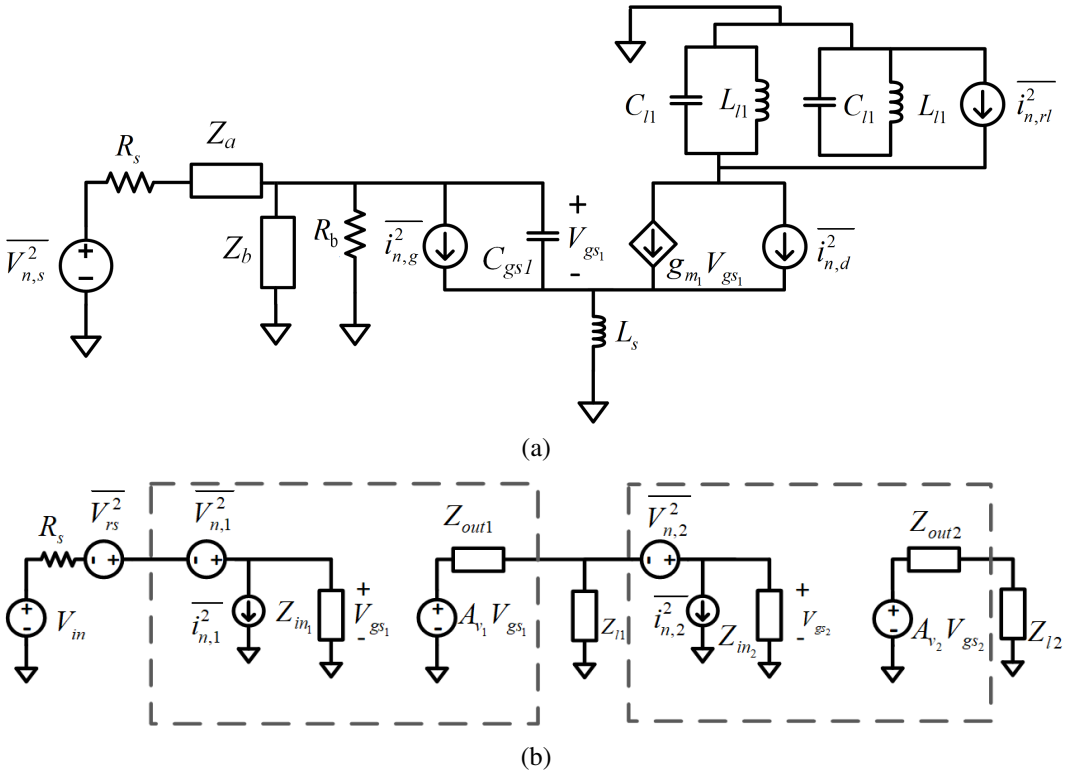


Figure 4.6: (a) Noise equivalent model of first stage of designed DBLNA (b) Two noise stages in cascade

$$i_{sc,d1} = i_{n,d1} - \frac{sg_{m1}L_s i_{n,d1}}{sC_{gs1}\left(R_s + Z'_{in} + g_{m1}L_s\right)} \tag{4.20}$$

Since gate and drain noise currents are related, thus from (4.19) and (4.20)

$$i_{sc,d1} = i_{n,d1}\left(1 - i_{sc,g1}\cdot\frac{sL_s}{i_{n,g1}\left(R_s + Z'_{in}\right)}\right) \tag{4.21}$$

$$i_{sc,rl1} = i_{n,rl1} \tag{4.22}$$

The total noise factor F_1 of the first stage is

$$F_1 = 1 + \frac{\overline{i^2_{sc,g1}} + \overline{i^2_{sc,d1}} + \overline{i^2_{sc,rl1}}}{\overline{i^2_{sc,R_s}}} \tag{4.23}$$

Substituting (4.18) to (4.20) and (4.22) in (4.23), expression for F_1 is

$$F_1 = 1 + \frac{\overline{i_{n,g1}^2}\left(\frac{g_{m1}(R_s+Z'_{in})}{sC_{gs1}X}\right)^2 + \overline{i_{n,d1}^2}\left(1-\frac{g_{m1}L_s}{C_{gs1}X}\right)^2 + \overline{i_{n,rl1}^2}}{\left(\frac{g_{m_1}V_{n,s}}{sC_{gs1}(R_s+Z'_{in})}\right)^2} \tag{4.24}$$

where, $X = R_s + Z'_{in} + g_{m_1}L_s$ According to the Friis equation, total noise factor F of the cascaded system is expressed as

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} \tag{4.25}$$

where G_{A1} is the power gain of the first stage of LNA and F_2 is the noise factor of the second stage. For simplicity, we consider a noise equivalent model of cascaded system shown in Figure 4.6 (b). The system consists of two noisy stages in cascade. The available power gain is the ratio of power available at output to power available at source [37]. In terms of noise sources, power gain of first stage in Figure 4.6 (b) can be derived to get the total noise factor. The power available at the output of the first stage is

$$P_{out1} = \frac{A_{v1}^2}{2Z_{out_1}} \times (V_{gs_1}/2)^2 \tag{4.26}$$

or

$$P_{out1} = \frac{A_{v1}^2}{8Z_{out1}} \times V_{in}^2\left(\frac{Z_{in1}}{R_s + Z_{in1}}\right)^2 \tag{4.27}$$

where A_{v1} is the unloaded voltage gain of first stage. Power available at source can be written as

$$P_{source} = \frac{(V_{in}/2)^2}{2R_s} = \frac{V_{in}^2}{8R_s} \tag{4.28}$$

From (4.26) and (4.28) we have,

$$G_{A1} = \frac{P_{out1}}{P_{source}} = A_{v1}^2\left(\frac{Z_{in1}}{R_s + Z_{in1}}\right)^2 \cdot \frac{R_s}{Z_{out1}} \tag{4.29}$$

In the second stage of LNA, the source impedance used for calculating the noise factor

depends on the source driving that stage. Considering $\overline{V_{n,2}^2}$ as the RMS noise voltage and $\overline{i_{n,2}^2}$ as the total thermal noise in the second stage, noise factor of second stage F_2 can be calculated as

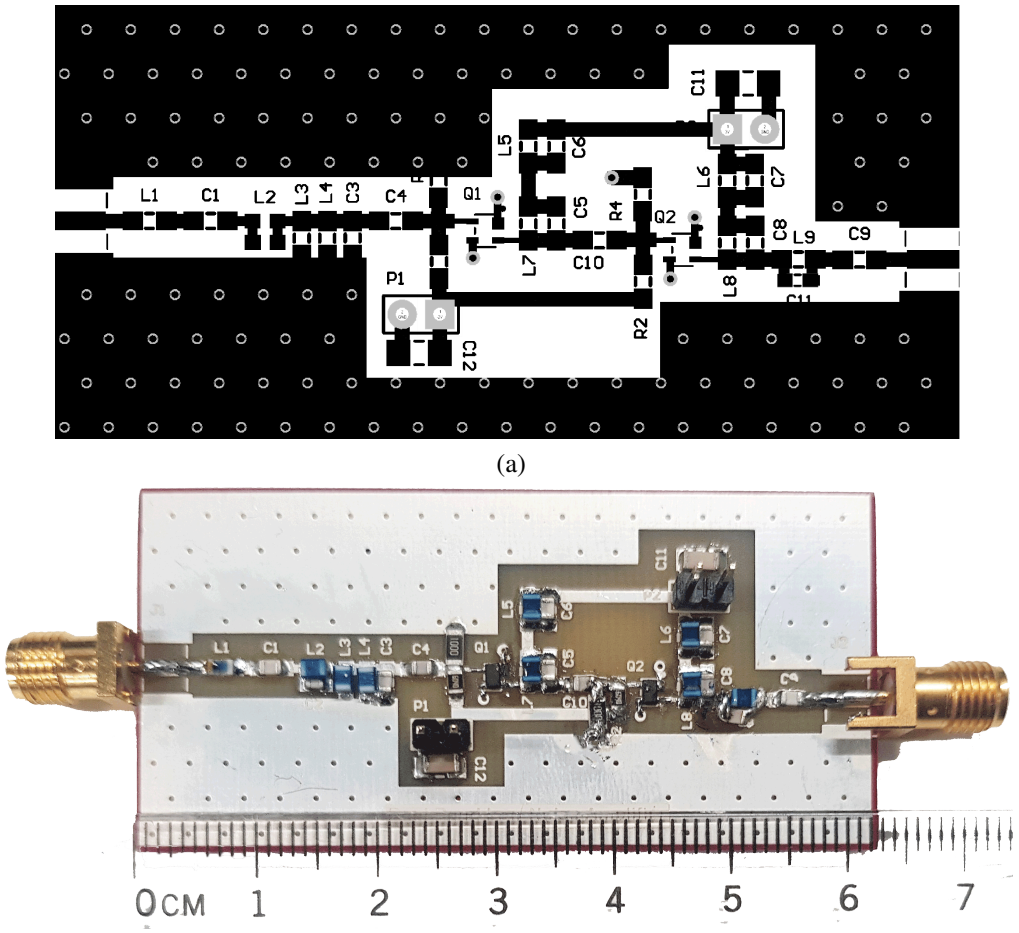
$$F_2 = \frac{\overline{\left|V_{n,2} + i_{n,2}Z_{out1}\right|^2}}{\overline{V_{R_s}^2}} \cdot \frac{R_s/Z_{out1}}{G_{A1}} \tag{4.30}$$

Substituting values from (4.24), (4.29) and (4.30) in (4.25), we can calculate the overall noise factor of the proposed DBLNA as

$$F = 1 + \frac{\overline{i_{n,g1}^2}\left(\frac{g_{m1}(R_s+Z'_{in})}{sC_{gs1}X}\right)^2 + \overline{i_{n,d1}^2}\left(1 - \frac{g_{m1}L_s}{C_{gs1}X}\right)^2 + \overline{i_{n,rl1}^2}}{\left(\frac{g_{m_1}V_{n,s}}{sC_{gs1}(R_s+Z'_{in})}\right)^2} + \frac{\left(\frac{\overline{|V_{n,2}+i_{n,2}Z_{out1}|^2}}{\overline{V_{R_s}^2}} \cdot \frac{R_s/Z_{out1}}{G_{A1}}\right) - 1}{A_{v1}^2\left(\frac{Z_{in1}}{R_s+Z_{in1}}\right)^2 \cdot \frac{R_s}{Z_{out1}}} \tag{4.31}$$

4.3 Circuit Implementation

The DBLNA circuit in Figure 4.3 is implemented with microstrip lines, passive components and RF junction field effect transistors (JFETs) on an FR-4 substrate (ϵ_r= 4.5, h = 1.5 mm, copper thickness = 35 μm). Implemented inductors and capacitors have slightly different values than ideal and simulated values due to the additional parasitic impedance from the surface mount (SMT) pads for 0805 components and microstrip lines. The source inductor has been modelled with microstrip line of size 0.508 mm $\times$ 0.508 mm on each source pin. Value of source inductance has been kept low to avoid gain peaking and subsequent oscillations. The microstrip components utilize the right configuration of lines and shapes to form passive elements. Via stitching and shielding has been proposed in the circuit to create a strong vertical ground connection through the MIC. This allows the designed LNA to maintain a low impedance and short return



(a)

(b)

Figure 4.7: (a) Layout and (b) Fabricated prototype of the designed DBLNA

loops. This also helps in reducing interference and return path impedance. Additionally, SMT inductors and capacitors have been used in the implementation of output loading network to reduce the circuit size and area. ATF34143 from Avago technologies is used as the active device to implement the circuit. The SMT inductors from Murata's LQW series and Coilcraft 0805-CS series are implemented as they have high-Q, low parasitics and minimal series resistances. Likewise, high-Q SMT capacitors from KEMET are implemented in the circuit.

Table II summarizes the component values calculated theoretically, implemented in EM simulation and on-board for the designed DBLNA. The traces have been properly isolated from DC and other signals. The ground plane layer usually provides a better

Table 4.1: Dual band matching network element values

Component	Calculated	Simulation	Implemented	Manufacturer
L'_1	2.1 nH	2 nH	1.8 nH	Coilcraft
C'_1	1.1 pF	1 pF	1 pF	KEMET
L'_2	9.2 nH	9 nH	8.2 nH	Murata
C'_2	0.97 pF	1 pF	1 pF	KEMET
L'_3	30 nH	33 nH	36 nH	Murata
C'_3	0.08 pF	0.05 pF	20 fF	Microstrip
L'_4	9.4 nH	10.9 nH	10 nH	Coilcraft
C'_4	1.44 pF	1.2 pF	1.2 pF	KEMET
L_s	0.3 nH	0.28 nH	20 mil*20 mil	Microstrip
R_1	50 Ω	100 Ω	100 Ω	Vishay
R_2	–	600 Ω	604 Ω	Vishay
L_{l1}	12 nH	8.2 nH	8.2 nH	Murata
C_{l1}	1.7 pF	1.2 pF	1.2 pF	KEMET
L_{l2}	3.6 nH	2.8 nH	2.8 nH	Murata
C_{l2}	1.22 pF	1 pF	1 pF	KEMET
L_{l3}	12 nH	8.2 nH	8.2 nH	Murata
C_{l3}	1.7 pF	1.8 pF	1.8 pF	Murata
L_{l4}	3.6 nH	2.8 nH	2.8 nH	Murata
C_{l4}	1.22 pF	1 pF	1 pF	KEMET
C_C	-	1 pF	1 pF	KEMET
L_{o1}	-	3 nH	2.8 nH	Murata
C_{o1}	-	1.2 pF	1.2 pF	Murata
C_{o2}	-	3.3 pF	3.3 pF	AVX

signal power and current at the output of the high frequency circuit. Therefore, ground inductance has been kept low and adequate ground has been provided. Figure 4.7 (a) and (b) show layout and fabricated prototype of implemented DBLNA, respectively.

4.4 Results and Discussions

The DBLNA circuit is biased by a 3 V supply and sinks 36 mA bias current. The DBLNA has been fabricated on an FR-4 substrate with microstrip lines and SMT passives using MIC/ MPCB fabrication process. The fabricated LNA dimensions are 60 mm $\times$ 30 mm $\times$ 1.5 mm. The designed DBLNA is suitable for SDR applications in

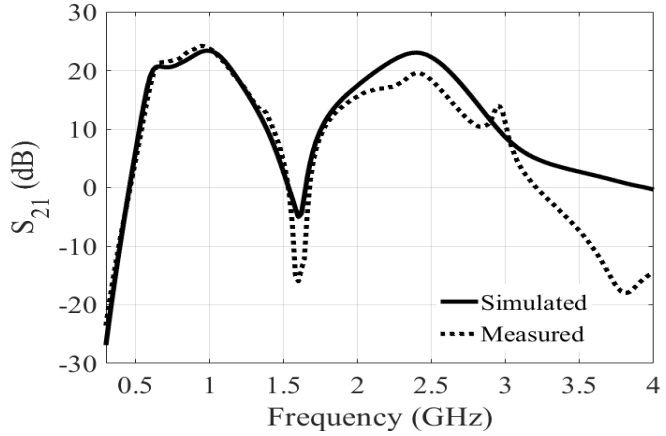
automotive and vehicular communications. Simulation analysis of the designed DBLNA circuit is carried out in Keysight ADS Momentum and integrated design environment (IDE).

The S-parameters of the fabricated DBLNA were measured using Agilent's PNA-L vector network analyzer (VNA). Simulated results were achieved using EM co-simulation in ADS for considering the effect of parasitic impedance from microstrip pads and lines. Passive components from vendor component libraries were implemented in simulation analysis. Figure 4.8 (a) shows the simulated and measured gain of implemented DBLNA. M_1 and M_2 are biased with V_{DS} = 3 V and V_{GS} = –0.53 V. The resulting drain current I_d = 36 mA. The two stage LNA achieves a very high measured gain of 24.3 dB at 1.1 GHz and nearly 20.1 dB at 2.4 GHz. The maximum simulated GI between the bands is 1 dB and measured GI is 4.2 dB. Measured 3-dB passbands are 530 MHz (670 MHz – 1.2 GHz) and 400 MHz (2.2 GHz – 2.6 GHz).

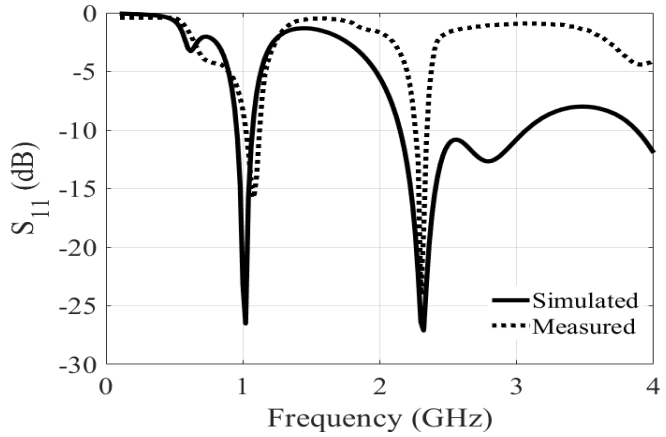
Measured results show two distinct concurrent dual bands centered at operating frequencies and loss at 1.6 GHz (stopband). In concurrent MBLNAs, SBRR is the difference between the values of S_{21} at stopband centre frequency and first passband centre frequency [48]. In this case, the measured SBRR from peak gain of 24.2 dB at 1.1 GHz to the attenuation loss of –16.2 dB at 1.6 GHz is 40.4 dB.

In addition, the cascaded stage of the LNA allows the simulated gain to increase significantly from 11 dB (single stage simulated gain) to 24 dB at 1.1 GHz and from 10 dB to 23 dB at 2.4 GHz. The two-stage design stabilizes the LNA and achieves higher output impedance.

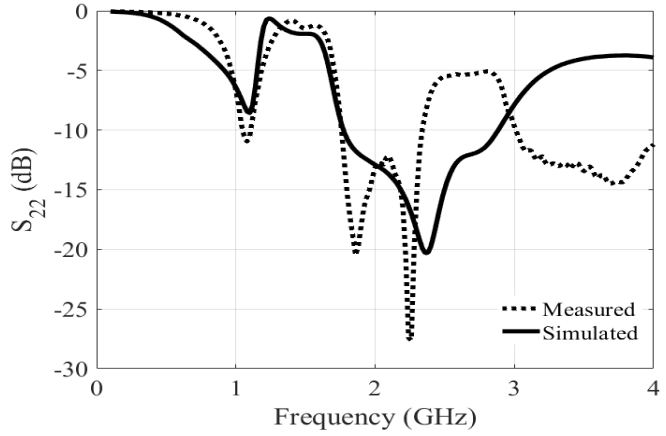
Figure 4.8 (b) shows simulated and measured S_{11} for the designed DBLNA. It achieves a simulated S_{11} of –26.5 dB and –27.1 dB at 1.1 GHz and 2.4 GHz, respectively and measured S_{11} of –15.8 dB and –24.1 dB at 1.1 GHz and 2.4 GHz, respectively. Figure 4.8 (c) shows output reflection coefficient S_{22} (dB) of designed DBLNA. The measured S_{22} achieves –10.9 dB and –11.6 dB at 1.1 GHz and 2.4 GHz, respectively. The reverse



(a)

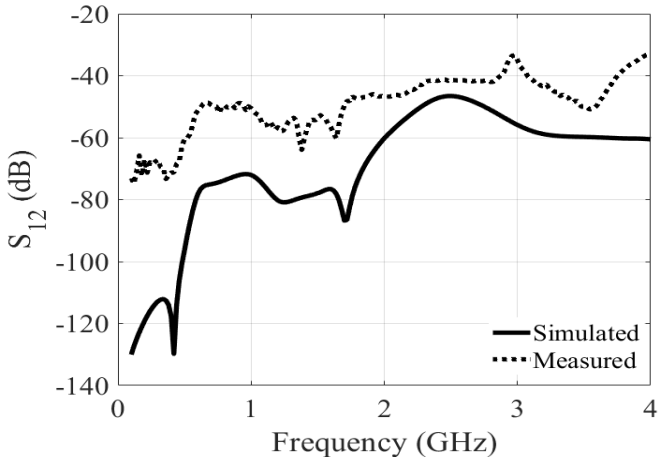


(b)



(c)

Figure 4.8: Simulated and measured (a) gain (S_{21}) (b) S_{11} (c) S_{22} of the designed DBLNA



(d)

Figure 4.8: (d) Simulated and measured S_{12} of the designed DBLNA (cont.)

isolation S_{12}, as shown in Figure 4.8 (d), is high and is measured to be –56 dB and –41.5 dB at 1.1 GHz and 2.4 GHz, respectively.

The NF of fabricated DBLNA MIC was measured with Keysight's PNA-X. The calibration for NF measurement was done using Keysight's power sensor module and RF noise source. The measurement was recorded over 201 points. The size and design of circuit is optimized for low NF during implementation. The measured NF of the designed DBLNA is 2.4 dB at 1.1 GHz and 3 dB at 2.4 GHz. Figure 4.9 shows the simulated and measured NF of the DBLNA.

The circuit also achieves a high IRR. In concurrent MBLNAs, IRR is the difference of LNA loss (S_{21} at 1.6 GHz) and NF of the LNA at stopband frequency (NF at 1.6 GHz) [107]. This stopband frequency is also the centre frequency of two operational bands. At 1.6 GHz, measured NF is 37.3 dB and the stopband loss is –16.2 dB. Thus, the total measured IRR is 53.2 dB.

Stability of the designed LNA has been determined by plotting the stability criterion μ versus frequency. Figure 4.10 shows that the LNA is unconditionally stable, as $\mu > 1$ in the whole frequency sweep range.

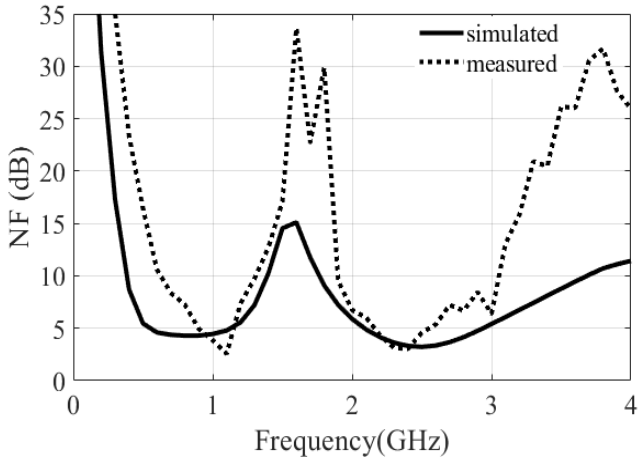


Figure 4.9: Simulated and measured NF of the designed DBLNA

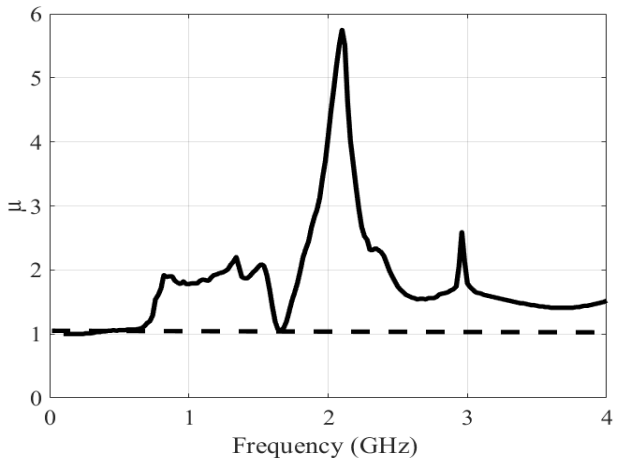


Figure 4.10: Variation of measured μ with frequency for the designed DBLNA

Linearity test was performed with P_{1dB} measurement. This measurement allows determination of compression points so that input levels can be controlled to prevent distortion. The instrument setup for P_{1dB} measurement is shown in Figure 4.11. The results were manually recorded by changing the input power from signal generator in steps of 1 dBm. Figure 4.12 (a) and (b) show output vs input power curve for estimation of 1 dB compression point for the fabricated DBLNA. Measured P_{1dB} is estimated to be –10 dBm at 1.1 GHz and –5.1 dBm at 2.4 GHz. Calculated IIP_3 from measured P_{1dB} for the designed DBLNA is 0 dBm and +4.7 dBm at 1.1 and 2.4 GHz, respectively [138].

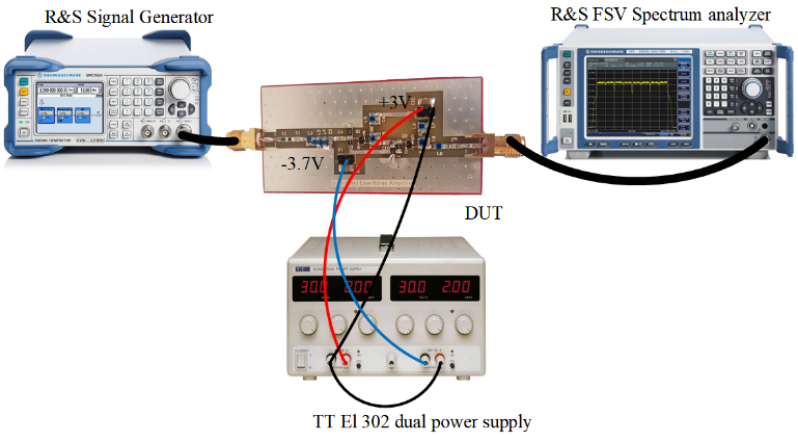


Figure 4.11: Bench setup for P_{1dB} measurement

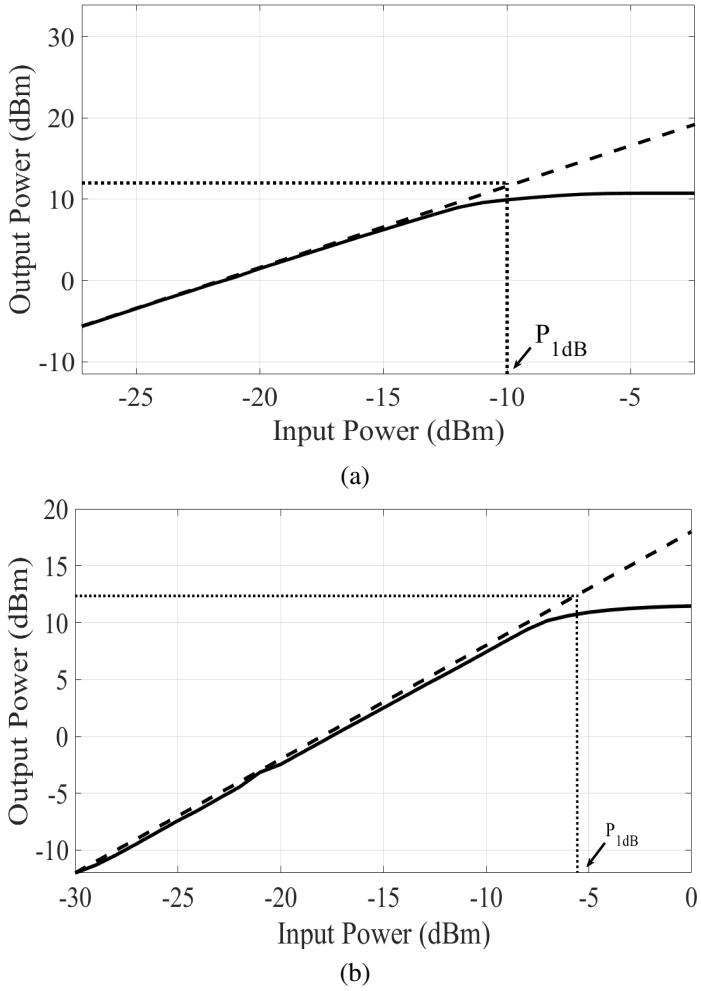


Figure 4.12: P_{1dB} performance of DBLNA at (a) 1.1 GHz (b) 2.4 GHz

4.5 Conclusion

This chapter presented a two-stage concurrent DBLNA architecture with a mathematically derived IMN and dual band load parameters. The chapter provided a fathomable analysis of the second-order dual band input matching stage designed using mathematical equations proposed in Chapter 3. We also presented the implementation and analysis of the modified dual band load that eliminates the need of band-reject filter from the conventional load. Analytical expressions for the design of IMN, output load, IFTT, theoretical gain and NF were presented. The LNA is implemented using microstrip lines and SMT passives on the FR-4 substrate. Simulation results of the designed circuit have been compared with measurement results. A high dual band gain, high IRR and improved SBRR was achieved with the fabricated DBLNA MIC. The proposed DBLNA is linear, unconditionally stable and has low NF at desired concurrent bands. A primary advantage of the designed DBLNA is that it provides a low-cost, power economic, high gain and a methodical design solution for amplification in a multiband front-end. Additionally, the LNA will suppress any common-mode noise and interference from the adjacent bands significantly. Table 4.2 compares the performance of the designed LNA with existing designs. The LNA outperforms the existing DBLNAs and MBLNAs at the expense of increased power consumption. To the authors' best knowledge, the proposed LNA is the first concurrent dual band MIC LNA explaining analytical step-wise mathematical approach for an economical on-board design and readily available passive components. Furthermore, the proposed LNA also achieves a state-of-art performance in all parameters which confirms its feasibility in the application of SDRs.

Table 4.2: Performance comparison of designed DBLNA with existing DBLNAs and MBLNAs

Ref.	**Freq**	S_{21} **(dB)**	S_{11} **(dB)**	**NF (dB)**	IP_3 **(dBm)**	**IRR (dB)**	**SBRR (dB)**	P_{DC} **(mW)**	**Process**
[85]	10.6 17.4 15.6	10.6 17.4 15.6	–12.5 –22.7 –25	4.96 5.16 5.57	–7 –16 –16	13.6	17	3.6	0.18 μm CMOS
[127]	23.5 35.7	21.9 16.6	–25 –15	5.1 7.2	–10.4 –8.3	27	21	–	0.18 μm SiGe BiCMOS
[49]	2.3 4.5	14.4 14.3	–12.8 –11.5	2.5 3.0	– –	18	27	11.9	0.35 μm SiGe BiCMOS
[128]	1.217 1.568	16 14.7	–10.1 –11.4	2.2 2.35	–12.5* –13.5*	–	12	13.6	0.18 μm CMOS
[51]^a	2.4 5.2	–19.3 17.5	–16.8 –19.4	3.2 3.3	–20.1 –18.1	51	43	20	0.13 μm CMOS
[95]	21.5 36	19.2 19.2	–8 –9	4 4.2	–14.1 –16.1	42	34.6	73.8	0.18 μm SiGe BiCMOS
[93]	2.45 6	9.4 18.9	–12.62 –21	2.8 3.8	–4.3 –5.6	–	38	2.79	0.13 μm CMOS
[116]	2.45 5.25	28.4 2.8.	–13 –20	0.7 1.1	–6.6 –5.1	16	36.4	36	SISL Avago
[41]	1.6–2.0 2.2 2.45	18 15 10	–24 –13 –11	1.9 2.6 5.0	4.1 6.2 14.7	6, 13	10, 11	108	MIC
[145]	2.4 3.5 5.5	22.4 21.1 20.7	–14.7 –16.2 –13.6	0.9 1.2 1.3	4.3 9.2 3.5	0, 0	2,2	40	MIC
[82]	0.9 1.8 2.45 3.5	10.7 9.1 9.0 7.2	–19 –11.3 –11 –14	0.9 0.9 1.1 1.2	–6 –8 –9 –7	20, 16, 20	26, 22, 21	40	MIC
[100]	0.95 1.85 2.65	18.9 12.8 10.2	–23 –24 –24	1.5 1.9 2.7	– – –	0, 0	12, 8	50	MIC
This	1.1 2.4	24.4 20.1	–15.8 –24.1	2.6 3.0	0 4.9	53.2	40.4	108	MIC

* P_{1dB} ^{a} simulated results .

Chapter 5

Design and Analysis of a Continuously Tunable LNA

5.1 Introduction

The number of wireless standards have increased rapidly in the last decade. Together with advancements in IC technologies, it has proliferated research in multiband radio systems. The recent trend is to increase the flexibility of SDR with specific attention on the front-end, particularly the LNA [8]. Improving the tuning range of LNAs is one way of achieving greater flexibility in radio systems. Continuously tunable LNAs (CTLNAs) accommodate large bandwidth and continuous reconfiguration. Therefore, these are a pliable alternative for improving the LNA tuning range.

Previous works on multiband CTLNAs have implemented both input and output tunable LNAs. For input tuning LNAs, it is primitive to select an appropriate topology for efficient design. CG topology was implemented in [106] to get the wideband response and stable operation. However, the topology is not efficient for designing an input tuning LNA due to low impedance at the source which results in low gain. The IDCS topology in LNA increases the real part of input impedance. It further improves the

overall gain and noise matching of the circuit. Figure 5.1 (a) illustrates the concept of input tuning LNA using a conventional source degenerated narrowband LNA.

It was briefly discussed in Section 3.1.1, that replacing the gate inductor L_g with a variable inductor L'_g provides reconfigurable input impedance matching. Implementing this in simulation model, we achieve a variable minimum input return loss (S_{11}) at different center frequencies as shown in Figure 5.1 (b). Nevertheless, implementing an LNA with L'_g will have (i) practical design aberrations, (ii) large on-chip/on-board area, and (iii) hysteresis due to the tunable inductor which would degrade the overall FOM of the LNA.

Output tuning LNAs have also been explored to achieve a wider continuous tuning range. Nevertheless, output tuning LNAs are more susceptible to process variations when compared to input tuning LNAs. They also require additional passives for designing a wideband IMN. Furthermore, less input tuning LNAs were reported in the literature as compared to output tuning LNAs [146].

Transformer based matching networks [56, 147] feature an interesting alternative with a wider tuning range and reduced power consumption. In this Chapter, we provide a comprehensive design and analysis of an input tuning LNA that implements a physical RF transformer to dynamically tune the input impedance. The LNA achieves a tunable input matching and a wideband output matching from 2.2 GHz to 2.8 GHz.

5.2 Motivation

A conventional narrowband LNA as shown in Figure 5.1 (a) consists of a gate inductor and a source inductor in its input matching stage. The input impedance of this LNA can be derived from the small signal equivalent circuit shown in Figure 5.1 (c). Applying

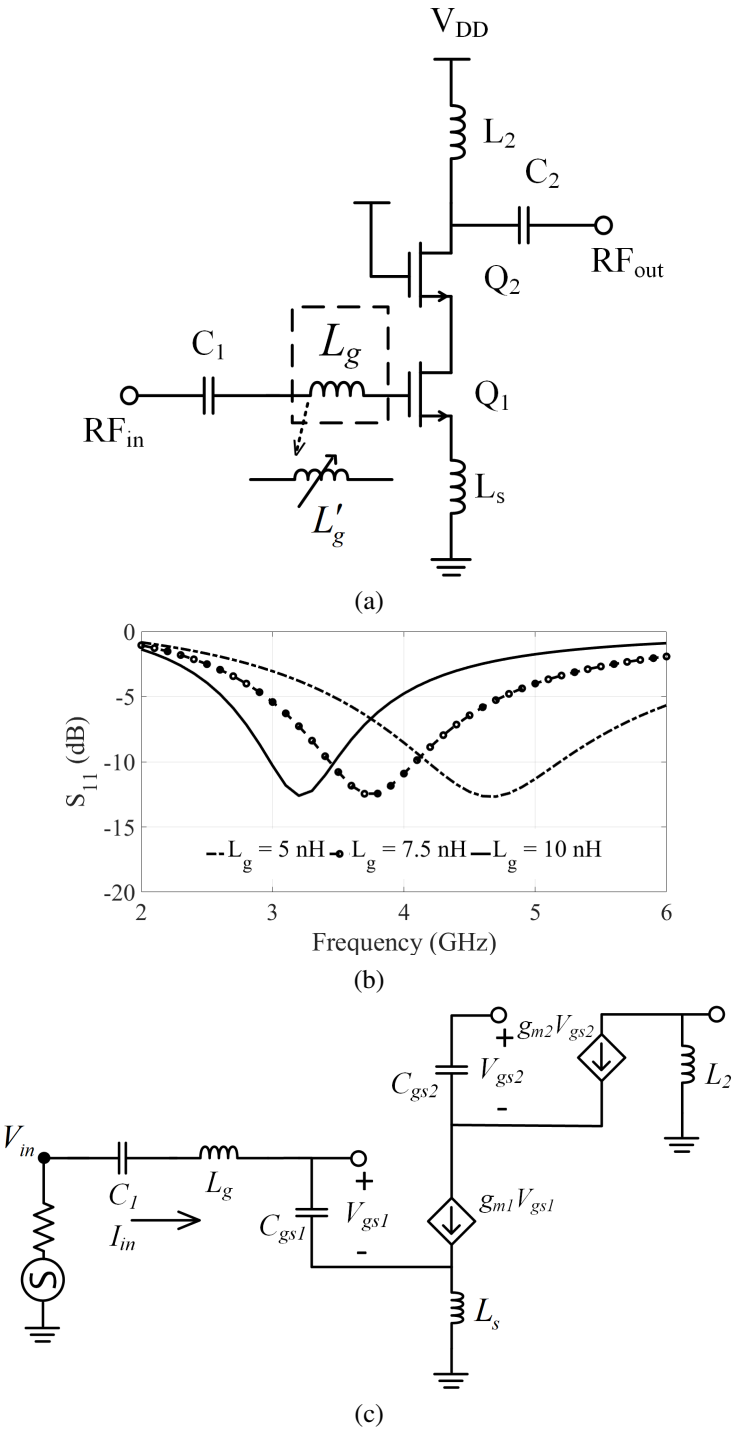


Figure 5.1: (a) Conceptual representation of a conventional input tuning LNA with L'_g (b) Corresponding varying S_{11} for different values of L_g (c) Small signal equivalent of conventional LNA

KVL to the circuit, the total input voltage V_{in} is

$$V_{in} = j\omega L_g I_{in} + \frac{I_{in}}{j\omega C_1} + \frac{I_{in}}{j\omega C_{gs1}} + (I_{in} + g_{m1} V_{gs1})\, j\omega L_s \tag{5.1}$$

$$\frac{V_{in}}{I_{in}} = j\omega\,(L_g + L_s) + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_{gs1}} + \frac{j\omega L_s g_{m1} V_{gs1}}{I_{in}} \tag{5.2}$$

$$V_{gs1} = \frac{I_{in}}{j\omega C_{gs1}} \tag{5.3}$$

From (5.2) and (5.3), input impedance of conventional narrowband LNA can be given as

$$Z_{in} = \left(j\omega\,(L_g + L_s) - j\left(\frac{1}{\omega C_{gs1}} + \frac{1}{\omega C_1}\right)\right) + \frac{g_{m1} L_s}{C_{gs1}} \tag{5.4}$$

where g_{m1},V_{gs1} and C_{gs1} are the transconductance, gate-source voltage, and gate-source capacitance of transistor Q_1, respectively. The resonant frequency of IMN f_0 depends on C_{gs1}, L_g and source inductor. The resonant frequency at which Z_{in} is real can be determined as

$$f_0 = \frac{1}{2\pi\sqrt{(L_s + L_g)\cdot C_x}} \tag{5.5}$$

where C_x is equivalent capacitance of C_{gs1} and C_1. It can be concluded from (5.4) and (5.5) that Z_{in} and f_0 can be made tunable by either varying L_s or L_g. Since, Re(Z_{in}) is directly proportional to L_s, replacing L_g with L_g' could be a viable solution. Nevertheless, an additional amplification stage is required to make L_g tunable or floating, which increases the circuit-area, implementation costs, NF and power consumption.

A feasible and efficient solution is to replace L_g with a physical RF impedance transformer, whose secondary winding can act as a variable inductor. The secondary inductance can be changed through an additional circuit connected to the primary winding of transformer network. Using switching circuits with primary winding and inductive-capacitive resonant networks would not provide continuous tuning. Moreover, additional switching circuits shall increase power consumption and NF of the circuit.

In this chapter, a CTLNA with tunable IMN is proposed with a physical RF impedance transformer network. Input impedance can be varied to achieve minimum S_{11} at each center frequency by changing the magnitude of current flowing through secondary winding of the transformer network. This can be achieved through magnetic coupling between primary and secondary windings of the transformer. Furthermore, the proposed LNA architecture comprises of an inductive load that provides a wideband response in the tuning range. This approach is expedient to maintain small area, continuous tuning and avoiding noise contributing elements in the signal path.

5.3 Proposed Circuit Topology

Figure 5.2 shows the block representation of the proposed CTLNA which consists of four different stages. The first stage is the IMN stage that consists of an input capacitor C_1 and a physical transformer. The second stage consists of a phase shifter network that comprises of two CG transistors connected in parallel to a CS transistor to get a relative 0° or 180° phase shift between the currents through primary and the secondary windings of the transformer. The third stage consists of a tuning transistor whose bias voltage V_{tune} can be varied to get the desired tunability. Finally, the fourth stage is the amplification stage that achieves a tunable wideband gain when V_{tune} is varied. For better understanding of the proposed circuit topology, design and synthesis of each stage is described as follows.

5.3.1 Transformer Network

The transformer in the input stage of the CTLNA is an RF impedance transformer. One end of its primary winding L_u is connected to the output of tuning transistor, while the other end is connected to the voltage supply V_{DD2} = 1.3 V. The secondary winding L_d is connected to the input transistor via a DC bias network. If L_d is considered

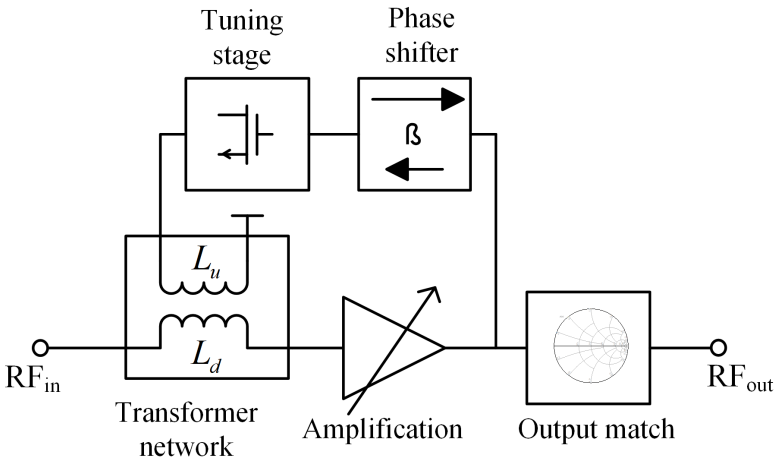


Figure 5.2: Conceptual block of proposed CTLNA

as a variable inductor as shown in Figure 5.2, then scaling its value will provide a 50Ω impedance matching at different center frequencies. The design utilizes a similar concept by implementing an RF impedance transformer in place of a variable inductor. Therefore, frequency reconfigurability can be achieved if current passing through L_d can be changed. The magnetism property of transformer can be utilized to change current through L_d. However, the currents i_1 and i_2 through L_u and L_d must have a relative phase shift ϕ of either 0° or 180° to allow continuous frequency tunability. This is because the RF impedance transformer circuit, shown in Figure 5.3 (a), provides a 50 Ω impedance match at a phase difference of 0° or 180° and the impedance is purely real at $\phi = 0^\circ$. This can be substantiated by deriving the relationship between transformer's input impedance $Z_{inT}(\omega)$ and ϕ. From the simplified transformer network shown in Figure 5.3 (b) and $Z_{inT}(\omega)$ can be given as

$$\frac{1}{Z_{inT}\left(s\right)} = \frac{1}{sL_1 + s\alpha M} + \frac{1}{R_c} + sC_t \tag{5.6}$$

$$\frac{1}{Z_{inT}(s)} = \frac{R_c + sL_{t1} + s\alpha M + s^2 C_{t1} L_{t1} R_c + s^2 \alpha M R_c C_{t1}}{R_c\left(sL_{t1} + \alpha M\right)} \tag{5.7}$$

Inverting equation (5.7) and substituting $s = j\omega$, $Z_{inT}(\omega)$ is

$$Z_{inT}(\omega) = \frac{j\omega R_c \left(L_{t1} + \alpha M\right)}{R_c \left(1 - \omega^2 C_t \left(L_{t1} - \alpha M\right)\right) + j\omega \left(L_{t1} + \alpha M\right)} \tag{5.8}$$

where $\alpha = i_2/i_1$ is the ratio of primary and secondary winding currents in the transformer network, M is the mutual inductance, L_{t1} is primary leakage, C_t is interwinding capacitance and R_c is core loss resistance. Inductances L_{t1} and L_{t2} correspond to inductances L_u and L_d in the implemented transformer network and given as.

$$L_{t1} = L_p \left(\frac{1}{k} - 1\right) \tag{5.9}$$

$$L_{t2} = \frac{L_{t1}}{N^2} \tag{5.10}$$

where k is the coefficient of coupling and N is the turns ratio. Due to phase difference between i_2 and i_1, $i_2 = \beta i_1 e^{-j\phi}$, where β is the gain and $\alpha = \beta e^{-j\phi}$. Therefore, (5.8) can be expanded as

$$Z_{inT}(\omega) = \frac{j\omega R_c \left(L_{t1} + \beta e^{-j\phi} M\right)}{R_c \left(1 - \omega^2 C_t \left(L_{t1} - \beta e^{-j\phi} M\right)\right) + j\omega \left(L_{t1} + \beta e^{-j\phi} M\right)} \tag{5.11}$$

Substituting values for variables in (5.11) as R_c = 0.91 Ω, $\beta = 1$, $\omega = 2\pi f$, $f = 1.5 - 3$ GHz, $L_{t1} = 3.37$ nH, $M = 0.5$ nH, $C = 995$ fF and plotting $\mathrm{Re}(Z_{in})$ vs ϕ from 0° to 360°, we can verify that $\mathrm{Re}(Z_{in})$ = 50 Ω at 0° and 180° as shown in Figure 5.4 (a). Additionally, $\mathrm{Im}\left(Z_{in}\right)$ is maximum at $\phi = 180^\circ$ (see Figure 5.4 (b)). This results in a phase mismatch between i_1 and i_2; however, the desired relative phase shift between i_1 and i_2 is 0° for continuous tuning. Moreover, the amplified signal is an inverted version of input signal. A possible solution is a phase shifter circuit that can provide a phase mismatch of 0° to ensure that currents and are in phase. The resonant frequency f_{Tr} of

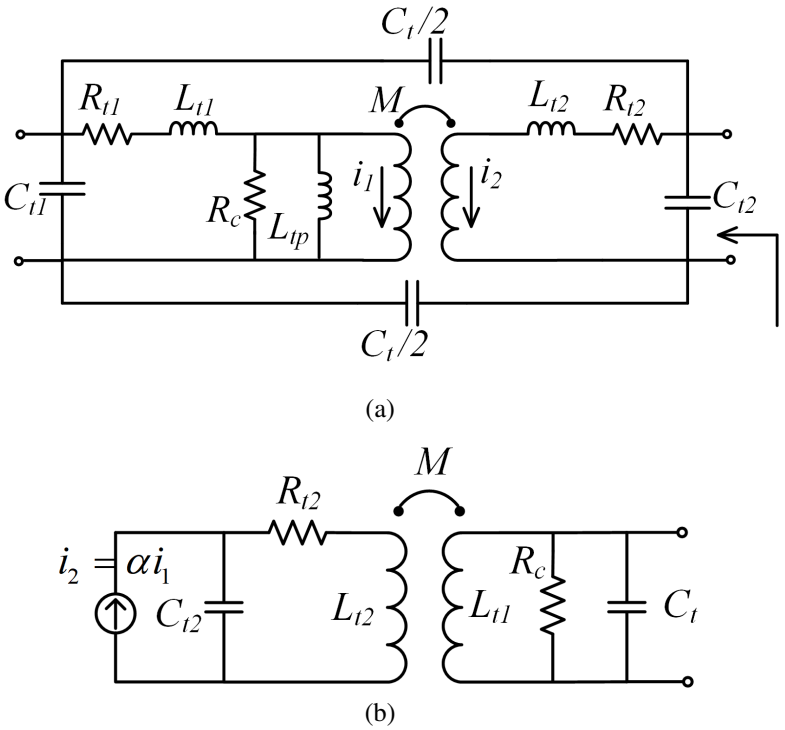


Figure 5.3: (a) Physical transformer equivalent circuit for designed CTLNA (b) Simplified transformer model for calculations

transformer can be determined as

$$f_{Tr} = \frac{1}{2\pi(L_{t1} \pm \alpha M)C_t} \tag{5.12}$$

The transformer's coefficient of coupling k is related to M as $M = k\sqrt{L_u L_d}$. A lower value of k would result in lower M and less sensitivity of transformer network to large frequency variation and current mismatch. Therefore, the value of k was kept low to achieve the desirable input match. Table 5.1 summarizes the design parameters for the transformer network.

5.3.2 Phase Shifter

The circuit implements a conventional active phase shifter (APS) [148] to shift the phase of the amplified signal. The APS receives the amplifier output and is applied

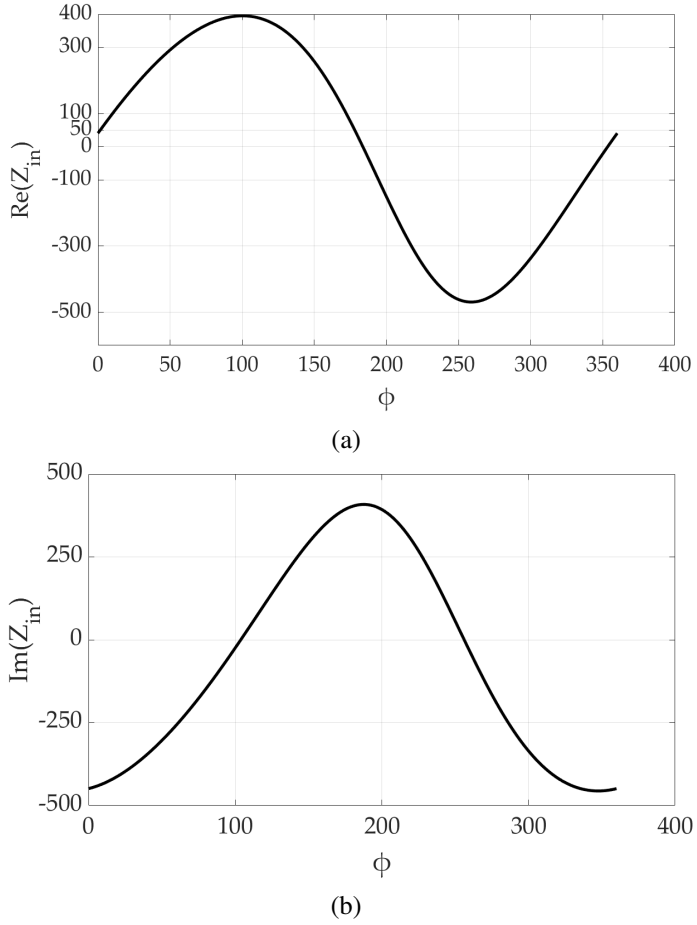


Figure 5.4: (a) $\mathrm{Re}(Z_{in})$ (b) $\mathrm{Im}\,(Z_{in})$ as a function of ϕ

Table 5.1: Transformer design parameters

Parameter	**Value**
Turns Ratio N	0.69
Magnetising Inductance L_{tp}	2.23 nH
Cross loss resistance R_c	1000 Ω
Coefficient of Coupling k	0.11
Primary loss resistance R_{t1}	0.91 Ω
Secondary loss resistance R_{t2}	4.47 Ω
Primary capacitance C_{t1}	924 fF
Secondary capacitance C_{t2}	150 fF
Interwinding capacitance C_t	340 fF

in the feedback path of the circuit. The circuit embeds two CG transistors in parallel to a CS transistor. Figure 5.5 (a) shows the schematic of the adapted APS circuit

with a conventional topology. The designed circuit is capable of providing a phase shift of more than 90° , thereby leading to elimination of phase mismatch between complex currents i_1 and i_2. A simplified small signal equivalent circuit to illustrate the conventional APS operation is shown in Figure 5.5 (b). According to [148], Y_{21} in admittance matrix for the APS is given as

$$Y_{21}(\omega) = \frac{i_2}{v_1} = -g_{m3} \cdot \left(\frac{\frac{1}{L_p(C_p+C_{gs4})} - j\omega \frac{1}{(C_p+C_{gs4})} \left(\frac{g_{m3}g_{m4}}{g_{m5}} - \frac{1}{R_p} \right) - \omega^2}{\frac{1}{L_p(C_p+C_{gs4})} + \frac{j\omega}{R_p(C_p+C_{gs4})} - \omega^2} \right) \tag{5.13}$$

Transformation of $Y_{21}(\omega)$ to $S_{21}(\omega)$ can be expressed as

$$S_{21}(\omega) = \left(\frac{\frac{2g_{m5}}{g_{m3}+g_{m5}} \sqrt{Z_{inPS} \cdot Z_{outPS}} - Z_{inPS} - \frac{j\omega Z_{inPS}}{\omega_T} Z_{outPS}}{\frac{1}{g_{m3}+g_{m5}} + Z_{inPS} + \frac{j\omega Z_{inPS}}{\omega_T} Z_{outPS}} \right) \cdot \left(\frac{\frac{1}{L_p(C_p+C_{gs4})} - \frac{j\omega}{R_p(C_p+C_{gs4})} - \omega^2}{\frac{1}{L_p(C_p+C_{gs4})} + \frac{j\omega}{R_p(C_p+C_{gs4})} - \omega^2} \right) \tag{5.14}$$

From (5.14), the phase of $S_{21}(\omega)$ can be derived as

$$\angle S_{21}(\omega) = -\tan^{-1} \left(\frac{\frac{\omega}{\omega_T} Z_{inPS}}{\frac{1}{g_{m3}+g_{m5}} + Z_{inPS}} \right) - 2\tan^{-1} \left(\frac{\omega}{R_p \left(\frac{1}{L_p} - (C_p + C_{gs4})\omega^2 \right)} \right) \tag{5.15}$$

where Z_{inPS} and Z_{outPS} are the input impedance and the output impedance of the APS, respectively. It can be concluded from (5.15) that $\angle S_{21}(\omega)$ depends upon inductor L_p and capacitor C_p. The shift in phase of the signal with constant signal amplitude is accomplished by variation in inductance or capacitance of the resonant circuit. The values of L_p and C_p for 2.2 to 2.8 GHz band are 17.5 nH and 10 pF, respectively. Figure 5.6 shows variation of $\angle S_{21}(\omega)$ of APS with V_X.

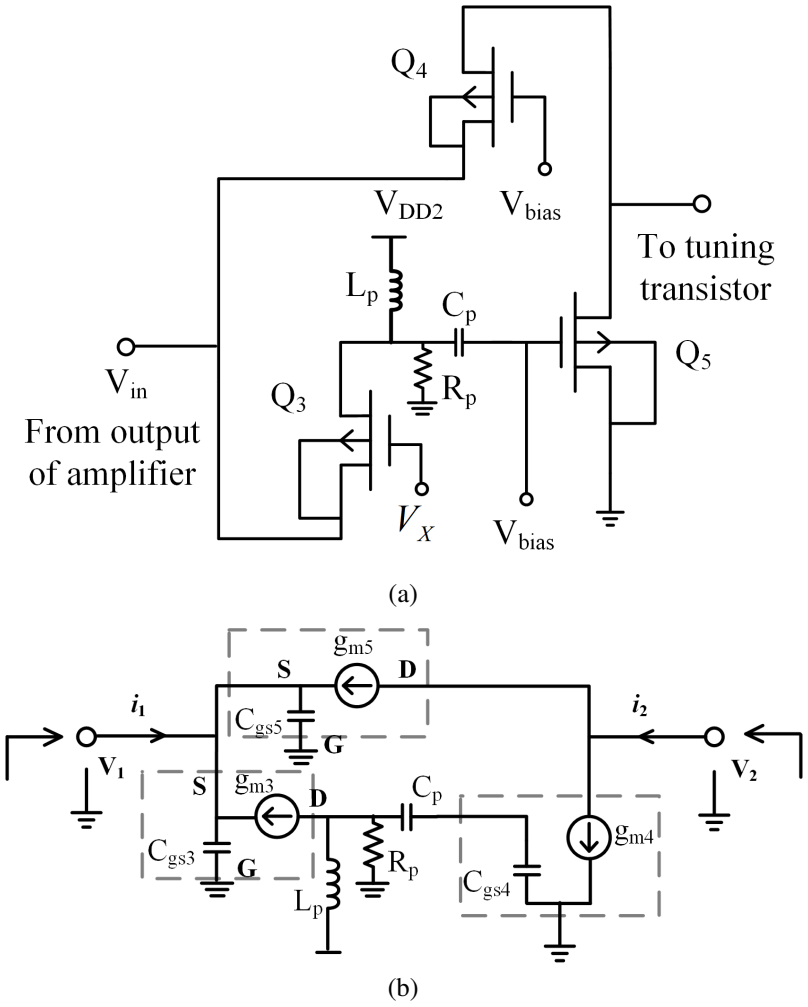


Figure 5.5: (a) Implemented PS circuit (b) Equivalent small signal model [148]

5.4 Tuning Stage

Figure 5.7 (a) shows the tuning stage of the designed CTLNA. It consists of a CS transistor biased with a positive gate voltage through a bias resistor. The CS transistor is placed in the feedback path and the input to its gate terminal is a phase shifted signal from the output of APS circuit. The output drain terminal is connected to one end of primary winding L_u of transformer network in the input stage. Varying the bias voltage (V_{tune}) of tuning transistor Q_6 continuously leads to incessant variation in its drain current I_{d6}. This further leads to variation in current i_1 flowing through L_u and resultantly in α and β. Figure 5.7 (b) shows the variation of I_{d6} with V_{tune}. The

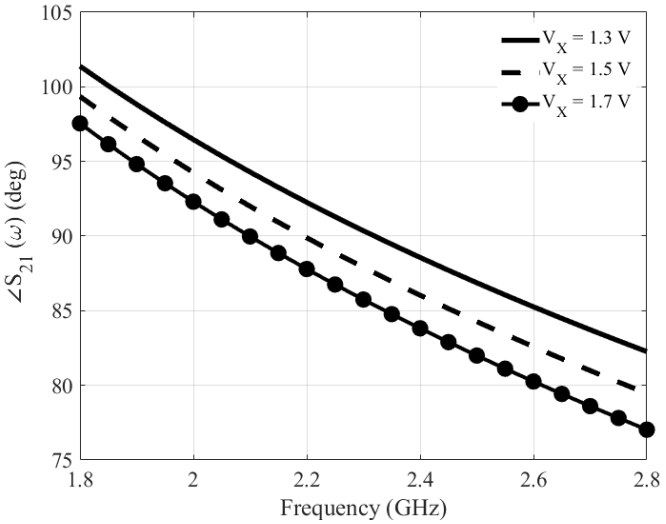


Figure 5.6: $\angle S_{21}\,(\omega)$ vs frequency at different values of V_x

resultant change in Z_{inT} (depends on β) varies the input impedance of CTLNA, leading to continuous tunability.

5.5 Circuit Analysis

Figure 5.8 shows the complete architecture of designed CTLNA with source degeneration and cascode topology. The cascode topology increases the circuit's AC resistance and aids in augmenting the gain. Inductive degeneration increases the real part of input impedance. The primary consideration while designing a CTLNA is to determine the band of operation. C_t, L_p and k values in transformer network are then selected to focus the desired operating band that ranges from 2.2 GHz to 2.8 GHz. One end of primary winding of the transformer in input stage is terminated with the output from the tuning transistor, while the other end is connected to voltage supply. Input capacitor C_1 and C_{gs1} resonate with L_d to achieve a continuously tunable impedance matching at different center frequencies. Continuous tuning shall only take place when i_1 and i_2 are in phase. The input of APS circuit is connected to the drain of Q_1 via $L_3 - C_3$ network. It provides a phase mismatch of 0° between the currents i_1 and i_2 through L_u and L_d.

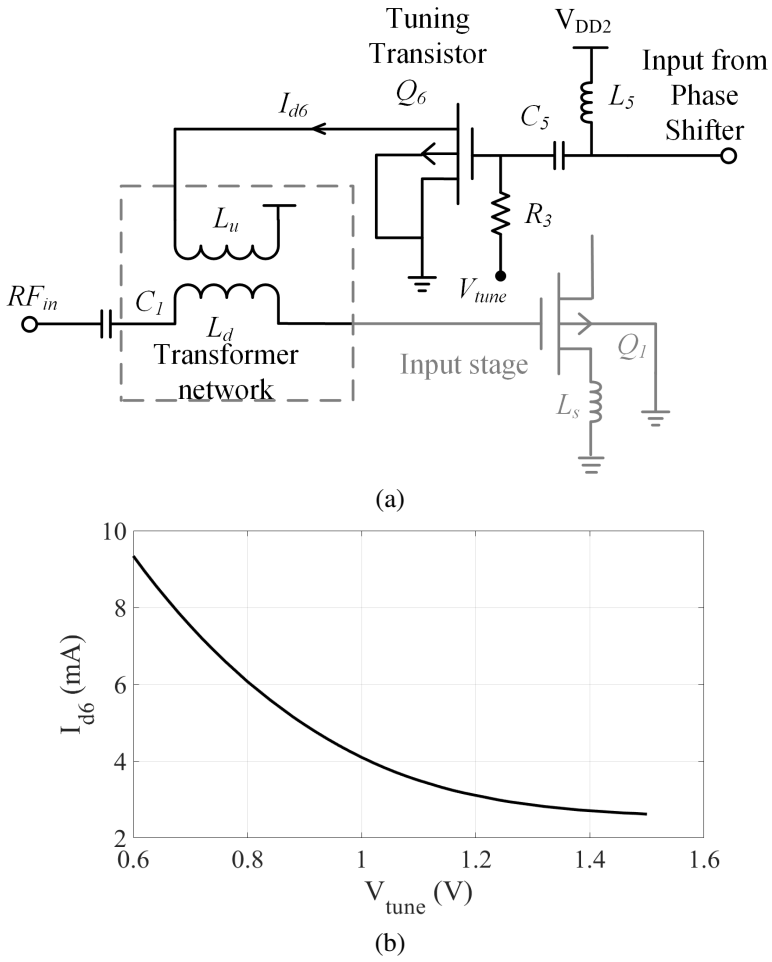


Figure 5.7: (a) Tuning stage of proposed CTLNA (b) Variation of I_{d6} with V_{tune}

The output of APS is fed to the gate of Q_6 whose drain terminal further connects to L_u to achieve tunable input matching.

A resistance R_b is also added for the purpose of providing DC bias to the input transistor Q_1. For simplicity, a fixed inductor L_2 was adopted in the output loading section of LNA to achieve a wideband gain. A large resistance R_1 is added in parallel to L_2 for improving LNA stability at different frequencies and increasing DC voltage gain.

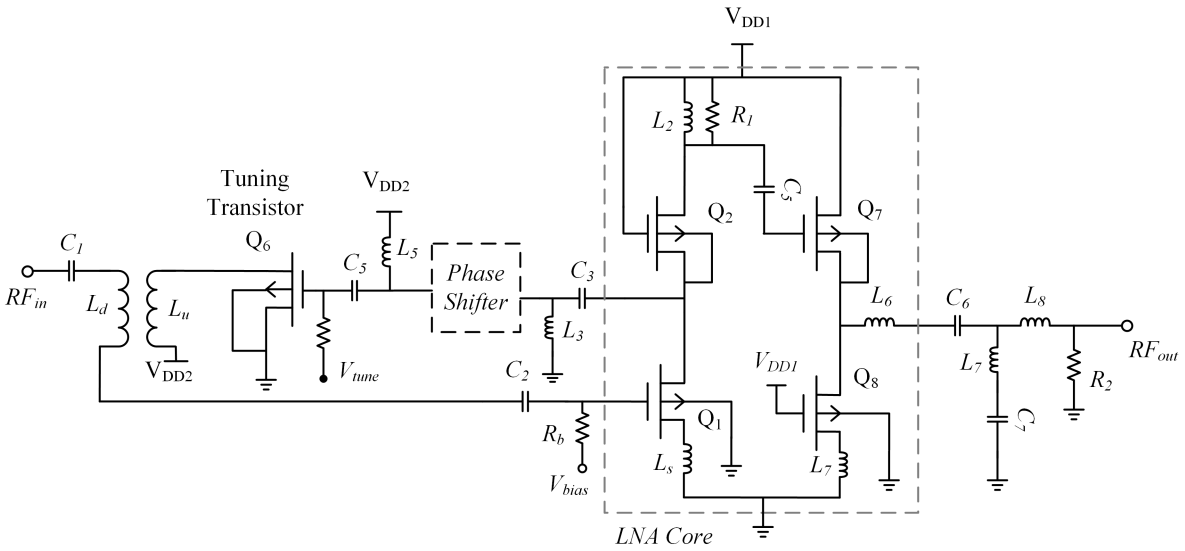


Figure 5.8: Complete CTLNA architecture

5.5.1 Input Impedance

The input stage of the proposed CTLNA consists of capacitor C_1 and the transformer network. Secondary inductor L_d can be considered as a tunable inductor L'_g that replaces L_g in Figure 5.1 to achieve tunable input impedance. As L_d cannot be directly varied, magnetic coupling can be utilized to vary the input impedance of LNA. Since $Z_{inT}(\omega)$ depends on α, the input impedance of the designed CTLNA $Z_{in}(\omega)$ is derived as

$$Z_{in}(\omega) = j\left(\omega L_s + \omega L_d \pm \omega\alpha M - \frac{1}{\omega C_{gs_1}} - \frac{1}{\omega C_1}\right) + \frac{g_{m_1} L_s}{C_{gs_1}} \tag{5.16}$$

and the frequency of operation is

$$f_{op} = \frac{1}{2\pi\sqrt{(L_s + L_d \pm \alpha M)C_x}} \tag{5.17}$$

Equation (5.17) shows that f_{op} depends on constants L_d, L_s, M, C_{gs1} and variable α. The value of α can be varied by changing V_{tune} that controls I_{d6} and eventually i_1. Note that the real part of input impedance depends on L_s and can be changed by varying

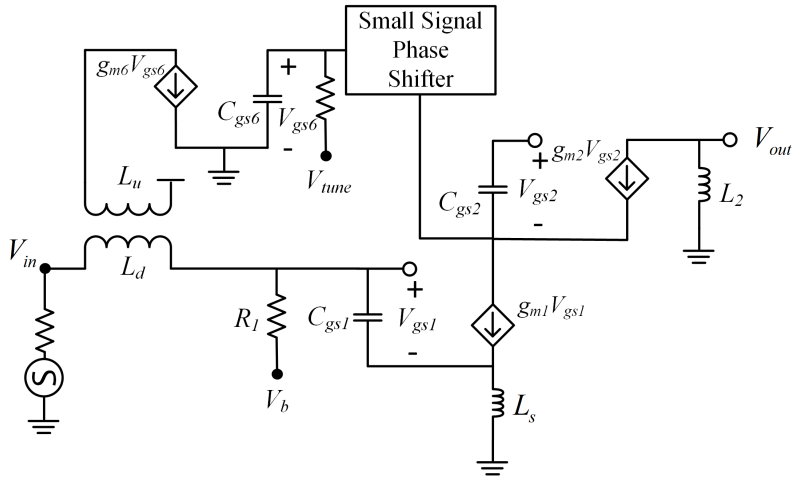


Figure 5.9: Simplified small signal model of CTLNA for gain analysis

L_s only. Its value has been selected to ensure that Z_{in} is matched to the source. The Q-factor of IMN (Q_{in}) is one of the primary elements used to determine the bandwidth of network. For the designed CTLNA, Q_{in} can be expressed as

$$Q_{in} = \frac{X_L}{R} = \frac{\omega L}{\mathrm{Re}\left(Z_{in}\right)} = \frac{\omega\left(L_s + L_d \pm \alpha M\right)}{\left(g_{m1}L_s/C_{gs1}\right)} \tag{5.18}$$

where $X_L$and R are imaginary and real part of input impedance, respectively. From (5.17) and (5.18), Q_{in} can be simplified as

$$Q_{in} = \frac{1}{\omega\left(g_{m1}L_s + C_{gs1}\right)} \tag{5.19}$$

It can be concluded from (5.19) that the bandwidth and f_{op} of CTLNA increases as Q_{in} becomes smaller.

5.5.2 Gain

Gain of the designed CTLNA can be derived similar to a narrowband LNA shown in Figure 5.1. However, in this case, the input gate inductor L_g is replaced with a

transformer based variable inductor L_d and its impedance $Z_{inT}(\omega)$ depends on M and α. The output loading network is similar to a conventional load. The low noise voltage gain for CTLNA can be derived from its small signal model of the input and amplification stage shown in Figure 5.9. For cascode LNAs, since all transistors are the same,

$$g_{m1} = g_{m2} = 2k_n \left(V_{gs} - V_T\right) \tag{5.20}$$

where is k_n conduction parameter, g_{m2} is the transconductance of the transistor Q_2 and V_T is the threshold voltage of implemented Philips MOS transistor. The small signal voltage gain A_v of an LNA is defined as

$$A_v = \frac{V_{out}}{V_{in}} \tag{5.21}$$

The V_{out} and V_{in} for the designed CTLNA are,

$$V_{out} = i_d Z_{out} = g_{m1} V_{gs1} \cdot Z_{out} \tag{5.22}$$

$$V_{in} = V_{gs1}(1 + Z_{in}) \tag{5.23}$$

Substituting (5.16) in (5.23), V_{in} expands to

$$V_{in} = V_{gs1}\left(1 + j\omega\left(L_s + L_d + \alpha M\right) + \frac{1}{j\omega C_x} + \frac{g_m L_s}{C_{gs1}}\right) \tag{5.24}$$

Also,

$$Z_{out} = \frac{g_{m2} L_2}{C_{gs2}} \tag{5.25}$$

From (5.22) and (5.25),

$$V_{out} = \frac{g_{m1} g_{m2} L_2}{C_{gs2}} . V_{gs1} \tag{5.26}$$

Finally, substituting (5.24) and (5.26) in (5.21), A_v can be derived as

$$A_v = \frac{V_{out}}{V_{in}} = \frac{j\omega g_{m1} g_{m2} L_2 C_x C_{gs1}}{\left(C_{gs1}\left(1 - \omega^2 C_x\left(L_d + L_s + \alpha M\right)\right) + j\omega C_x\left(1 + g_{m1} L_s\right)\right).\left(C_{gs2}\right)} \tag{5.27}$$

where C_{gs2} is the gate-source capacitance of the transistor Q_2. Equation (5.27) substantiates that A_v for the designed CTLNA depends on α and eventually on V_{tune}. Hence the gain can also be tuned continuously in the desired band by sweeping V_{tune} from 0.5 V to 1.5 V.

5.5.3 Noise Figure

Figure 5.10 shows the noise equivalent model for the designed circuit. NF for the proposed CTLNA can be quantified by deriving its noise factor F. The main noise source in the circuit is thermal noise and all passives in the circuit are considered as ideal. Considering that there are multiple noise sources in the circuit, it would be rather impractical to evaluate F without detailed noise model for all noise sources. Therefore, an expression for output noise current due to all noise sources is calculated. The short circuit noise current due to source is

$$i_{sc,R_s} = \frac{g_{m_1} V_{n,s}}{j\omega C_{gs1} R_s + Z'_{in}} \cdot \omega_z \tag{5.28}$$

and

$$Z'_{in} = 1 - \omega^2 C_{gs1}(L_s + L_d) + j\omega g_{m1} L_s \tag{5.29a}$$

$$\omega_z = \frac{g_{m2}}{g_{m\,Eq} + j\omega C_{Eq}} \tag{5.29b}$$

where $g_{m\,Eq} = g_{m2} + g_{m3} + g_{m4}$, $C_{Eq} = C_{gs2} + C_{gs3} + C_{gs4}$, ω_z is the zero introduced due to noise effect from other transistors Q_2, Q_3 and Q_4 in parallel and $V_{n,s}$ is the

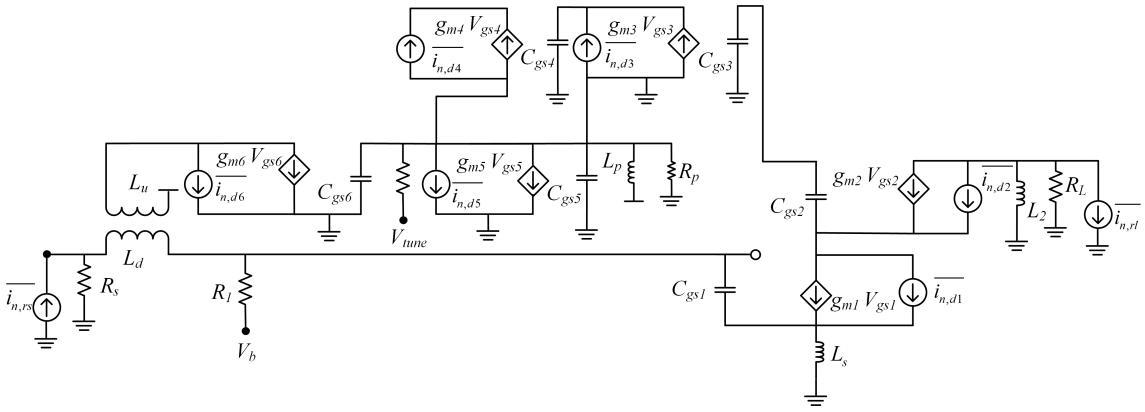


Figure 5.10: Noise equivalent model of designed CTLNA

noise voltage at source. The short circuit noise current due to thermal drain noise of transistors Q_1, Q_2 in the amplification stage is

$$i_{sc,d1} = \left(i_{n,d1} - \frac{j\omega g_{m_1} L_s i_{n,d1}}{j\omega C_{gs1} R_s + Z'_{in}} \right) \cdot (-\omega_z) \tag{5.30a}$$

$$i_{sc,d2} = i_{n,d2} \left(1 - \omega_z\right) \tag{5.30b}$$

where $i_{n,d1}$ and $i_{n,d2}$ are drain noise currents of Q_1 and Q_2. The transistors Q_3, Q_4 and Q_5 in the APS circuit also contribute to the overall NF of CTLNA. Therefore, short circuit noise current due to drain noise of Q_3, Q_4 and Q_5 is

$$i_{sc,d3} = i_{n,d3} \cdot (-\omega_z) \tag{5.31a}$$

$$i_{sc,d4} = i_{n,d4} \cdot (-\omega_z) \tag{5.31b}$$

$$i_{sc,d5} = i_{n,d5} \cdot \left(\frac{g_{m2}}{g_{m6}} \right) \tag{5.31c}$$

The short-circuit noise current due to drain noise of tuning transistor Q_6 is

$$i_{sc,d6} = \frac{j\omega g_{m1} i_{n,d6}}{j\omega C_{gs1} R_s + Z'_{in}} \cdot (-\omega_z) \tag{5.32}$$

and due to load is

$$i_{sc,rl} = i_{n,rl} \tag{5.33}$$

where $i_{n,d3}$, $i_{n,d4}$ $i_{n,d5}$, $i_{n,d6}$ are the drain noise currents of transistors Q_3, Q_4, Q_5 and Q_6 and $i_{n,rl}$ is the noise current of load resistance R_L. Using (5.28) to (5.33), F for the proposed LNA can be derived as

$$F = \frac{1 + \sum_{x=1}^{6} \overline{i_{n,dx}^2} + \overline{i_{sc,rl}^2}}{\overline{i_{sc,rs}^2}} \tag{5.34}$$

5.6 Results and Discussion

The proposed CTLNA is designed and simulated in MIC process. Keysight ADS and MATLAB are used as simulation tools for CTLNA analysis. The circuit is biased with 1.8 V supply and sinks 9 mA current. As can be seen in Figure 5.11 (a), S_{11} achieves a peak minimum for all different values of V_{tune} from 0.5 V to 1.5 V in steps of 0.2 V. It is below –10 dB at each center frequency for the entire tuning range and achieves as low as –40.4 dB at 2.57 GHz at V_{tune} = 1.2 V.

The LNA's IMN has been designed to match to 50 Ω at a particular centre frequency in the tuning range. The calculated 3-dB bandwidth at 2.2 GHz, 2.3 GHz, 2.41 GHz, 2.52 GHz and 2.65 GHz are 120 MHz, 100 MHz, 100 MHz, 110 MHz and 130 MHz, respectively. Figure 5.11 (b) shows the simulated gain for the designed CTLNA. The LNA gain directly depends on value of load inductor L_2. However, due to its dependency on α it can be tuned to different frequencies from 2.2 to 2.8 GHz. In addition, the CTLNA gain depends upon g_{m1} ,g_{m2}, C_{gs1}, C_{gs2}, source degeneration inductor L_s, and designed transformer parameters. The LNA achieves a maximum gain of 18 dB at 2.36 GHz in the stipulated tuning range. The minimum gain at 2.2 GHz center frequency is approximately 8 dB. Transistors Q_7 and Q_8 in the buffer stage are capable enough to

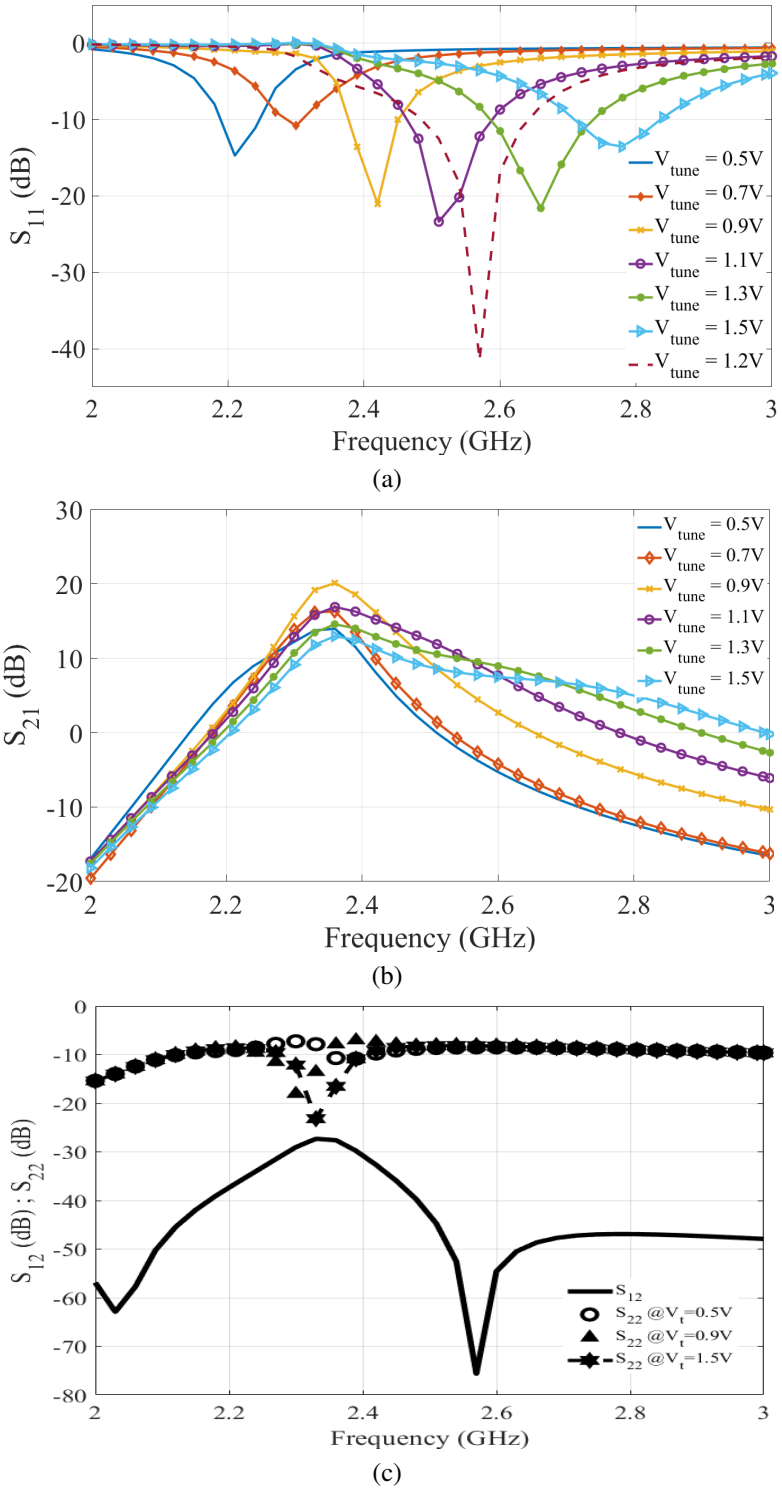


Figure 5.11: Simulated (a) Input return loss (S_{11}) (b) Gain (S_{21}) (c) Reverse isolation (S_{12}) and output return loss (S_{22})

stabilize the LNA and achieve high output impedance.

The output return loss S_{22} is less than –8 dB in the tuning range and achieves a peak minimum at center frequency of 2.35 GHz, which is the resonant frequency of output matching network. The reverse isolation S_{12} also remains more than 30 dB across the tuning range. Figure 5.11 (c) shows the variation of S_{12} and S_{22} with frequencies of the selected band.

Figure 5.12 (a) and (b) show the simulated NF for the designed CTLNA with tuning frequency and V_{tune}, respectively. It is clear from Figure 5.12 (b) that minimum NF at each center frequency varies between 1.4 dB to 4.8 dB. NF is a bit higher for 2.2 GHz and 2.3 GHz, which are initial frequencies in the tuning range. However, it is lower than 2 dB at center frequencies ranging from 2.4 GHz to 2.8 GHz.

The LNA stability depends upon the source and the load matching networks, which depends on the frequency of operation. Consequently, the designed CTLNA is supposed to be stable at a particular center frequency while it is unstable at other frequencies. Stability of LNA can be determined by calculating K and Δ for different values of V_{tune}. For the designed LNA, $K > 1$ and $|\Delta| < 1$ at all center frequencies within in the tuning range. Subsequently, the LNA is stable in the entire tuning range. Figure 5.13 shows variation of K with V_{tune} at different center frequencies.

Linearity of the designed CTLNA is measured by determining 1-dB compression point P_{1dB} and third-order intercept point IP_3. The P_{1dB} and IIP_3 calculations have been performed using 1-tone and 2-tone inputs, respectively. A non-linear model of the amplifier is analyzed with a frequency offset of 10 MHz between two tones. The source and load impedances are set to 50 Ω. IP_3 and P_{1dB} values for the designed CTLNA, range between –15 dBm to –31 dBm and –25 dBm to –42 dBm, respectively. Figure 5.14 shows the variation of P_{1dB} with V_{tune} in steps of 0.1 V for the proposed CTLNA.

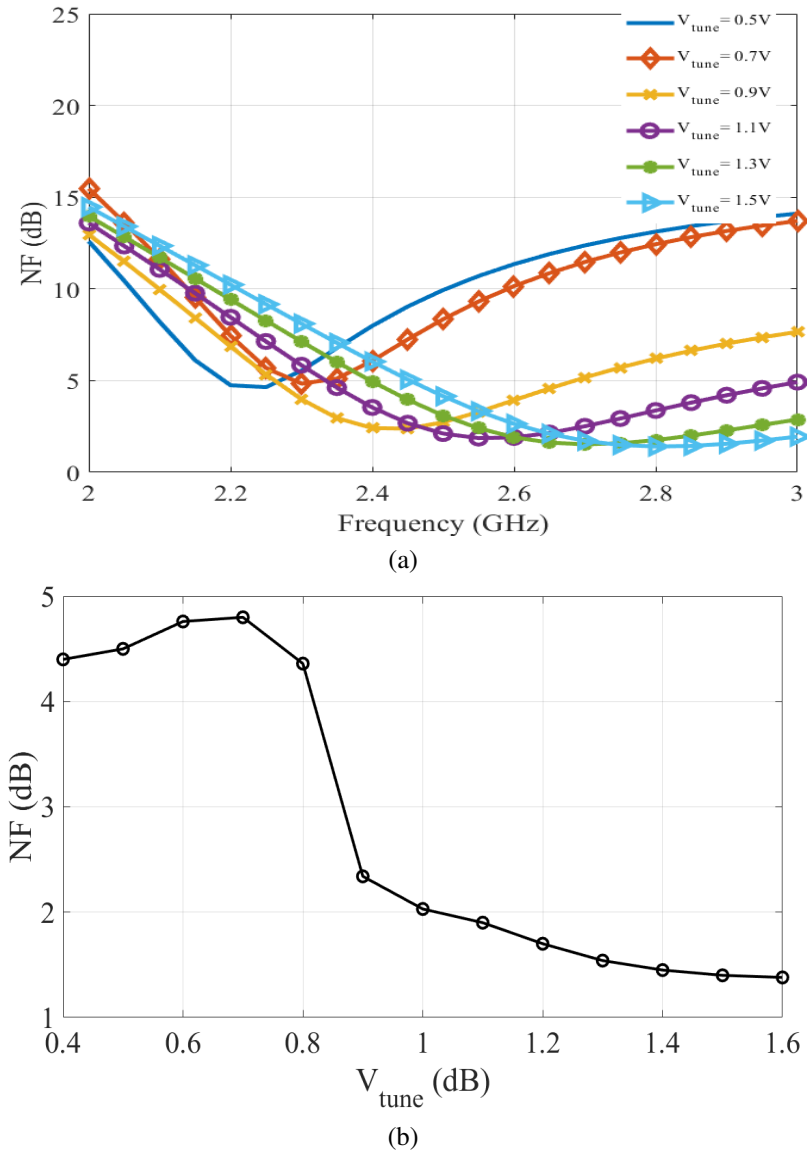


Figure 5.12: Simulated NF vs. (a) Frequency (b) V_{tune}

5.7 Conclusion

The design and analysis of an input tuning LNA with transformer based variable inductor matching is presented. The proposed CTLNA can be primarily used for SDR applications, such as green radio networks. The presented design takes advantage of continuous tuning due to magnetic coupling between primary and secondary windings of the transformer. This occurs by changing the ratio of currents through primary and

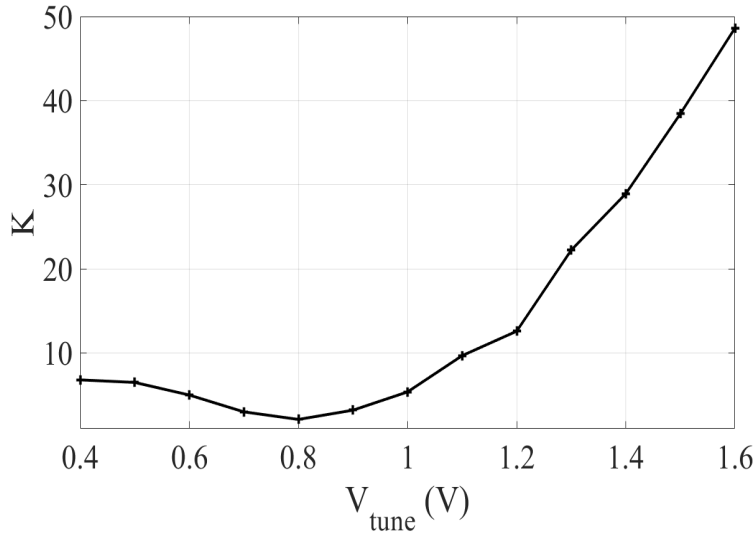


Figure 5.13: Variation of Stability factor K with V_{tune}

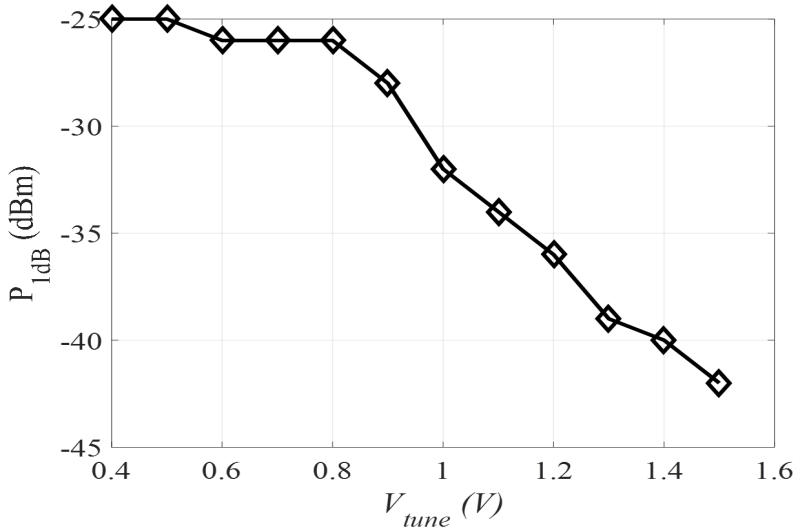


Figure 5.14: Variation of P_{1dB} with V_{tune}

secondary windings of the transformer network. To achieve tunability, the currents through transformer windings should be in phase. The circuit includes a phase shifter circuit to shift the phase of the input signal to achieve tunability through transformer. The methodology is used to further implement a tunable LNA in the frequency range of 2.2 to 2.8 GHz. The proposed design effectively integrates the transformer based matching network into an IDCS amplifier. The LNA achieves a wideband and tunable gain in the stipulated bandwidth. The tunable S_{11} is less than –10 dB in all operational

Table 5.2: CTLNA performance summary and comparison with previously published works

Ref.	**Freq. (GHz)**	S_{21} **(dB)**	S_{11} **(dB)**	**NF (dB)**	IP_3 **(dBm)**	V_{DD} **(V)**	**Tech.**	P_{DC} **(mW)**
This work	2.2 – 2.8	7 – 18	–40 – –11	1.4 – 4.8	–31 – –15	1.8	MIC	16.2
[149]	1 – 5	19 – 27	–18 – –5	2.4 – 3.8	–	1.2	65nm CMOS	12.1
[62]	1.9 – 2.4	10 – 14	–25 – – 12	3.2 – 3.7	–6.7	1.2	0.13μm CMOS	17
[72]	2.4 – 5.4	9.9 – 22	–14 – –30	2.4 – 4.9	–20 – –9	1	0.13μm CMOS	4.6
[60]	0.8 – 2.5	17 – 20	–27 – –11	3.1 – 3.6	–	1.8	0.18 μm CMOS	–

bands and achieves a minimum of –40.4 dB at 2.57 GHz. The NF ranges between 1.4 to 4.8 dB. In addition, mathematical analysis of transformer model, phase shifter and amplification stage are discussed. The proposed technique outlines an idea of continuous tuning that can be implemented to scale the input inductor value for any related application. Table 5.2 summarizes the simulated performance of the designed CTLNA and comparison with previously published works.

Chapter 6

Design and Analysis of a Multimode Tunable LNA

6.1 Introduction

A significant parameter of SDR receivers is the operating range. The ability to tune to different frequency operation modes improves the agility of SDR transceivers. Improving the operating range of LNA can help to realise an efficient SDR receiver [23]. The two popular ways of improving the operating frequency range of LNAs are (i) using a wideband matching network and (ii) using a reconfigurable matching network. The latter is preferred over the former to filter undesired bands [91].

Previous works to improve the bandwidth of matching network through filtering and reconfigurable matching achieved substantial results. Nevertheless, they suffered from several performance bottlenecks. The LNA proposed in [62] achieved an efficient tunable response from 1.9 to 2.4 GHz by tuning the gate inductor through feedback amplifier in the input stage. However, the LNA exhibited high gain imbalance in different bands, and low SBRR. Likewise, the design in [56] utilised a multitap transformer to replace the gate inductor to achieve a multimode reconfiguration. The aim was

to increase the operational bandwidth. However, multimode operation degraded the linearity in all bands. Variation of input impedance through transformer to achieve continuous tuning has also been proposed in [74, 96].

Additionally, varactor diodes were explored to achieve continuous frequency tuning in LNAs. In [150, 151] varactor diodes were implemented in the output stage of LNA to achieve reconfiguration. However, the frequency tuning range in both circuits was limited and FOM was low.

It would be interesting to see an LNA that could provide multiple operation modes [1] using varactor diode in the input matching stage by changing its bias conditions and bias voltages. This technique would enhance SDR's ability to select a particular frequency mode depending upon the application. In this chapter, we present the design of a tunable LNA that operates in multiple modes using a varactor diode in the input matching stage of the LNA. Multiple operation modes can be achieved by changing the diode bias voltage in both forward and reverse bias mode. Conventional double stub matching is implemented to first design a single band LNA and then modify it for a tunable response.

6.2 Circuit Design and Analysis

For a conventional stub matched LNA shown in Figure 6.1 (a), the frequency of operation depends on the distance of stub from the load. Likewise, in case of two-stub-matching, the frequency of operation f_{op} depends upon the distance between two stubs. For the LNA in Figure 6.1 (a), Z_{in} is given as

$$Z_{in} = Z_0 \frac{(R_s + jX_s) + jZ_0 \tan \beta d}{Z_0 + j(R_s + jX_s) \tan \beta d} \tag{6.1}$$

[1] Multiple operation modes refer to the frequency modes such as concurrent dual band/multiband mode, single band mode, frequency tunable mode, and/or wideband mode.

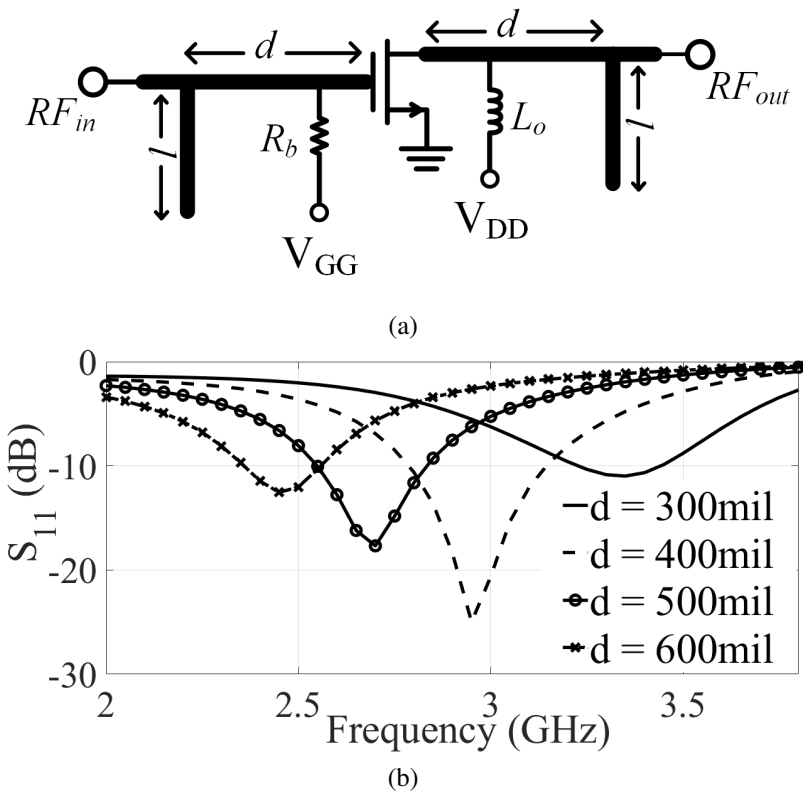


Figure 6.1: (a) Conventional single stub LNA design (b) variation of S_{11} with f_{op} at different values of d

where d is the distance of stub from the load, Z_0 is characteristic impedance and $Z_s = R_s + jX_s$ is the impedance at input of transistor. Variation in d would change Z_{in} and thus f_{op}. Figure 6.1 (b) shows the variation of S_{11} with f_{op} at different values of d. There is no practical way to directly alter the microstrip line of length d as it connects to the active device. Adding a parallel impedance can change the overall impedance of the circuit. Nevertheless, this technique would not reconfigurably achieve multiple tunable modes with different f_{op}.

6.2.1 Multimode Input Matching Network

It is possible to achieve a tunable multimode matching topology by varying the input impedance of the LNA circuit. The IMN consists of two stubs of lengths l_1, l_2 and

widths w_1 and w_2. Figure 6.2 (a) shows the design of the input matching network. The two stubs are separated by a distance d from each other. By modelling the transistor as a two-port network, a two–stub matching is designed to match Z_{in} with Z_S of the two-port network at a certain frequency f_1. Thereafter, two short microstrip line segments a and b are added in parallel to segment d. In reverse bias mode, segment a connects to the cathode of the varactor diode while segment b is short circuited. To achieve proper diode biasing, as shown in Figure 6.2 (b), the anode of the diode is connected to ground while the cathode is connected to the supply V_d through a DC feed inductor L_{d1}.

At this stage, we consider that that the V_d = 0 V. The resultant overall input impedance $Z_{in,T}$ of the circuit has a fixed value and is given as

$$\begin{aligned} Z_{in,T} = &\left(Z_{in} + jZ_0\left(\frac{\tan\beta l_1 \tan\beta l_2 \tan\beta l_3 - \tan\beta l_2 - \tan\beta l_1}{\tan\beta l_1 \tan\beta l_2}\right)\right) \\ &-j\left(\omega L_s - \frac{1}{\omega C_{gs}} - \frac{1}{\omega C_x}\right) + \frac{g_m L_s}{C_{gs}} \end{aligned} \tag{6.2}$$

where l_3 is the length of short-circuited stub b, L_s is the source inductance and C_x is the tunable capacitor to model the varactor diode. From (6.2), it is clear that $Z_{in,T}$ depends on C_x, which changes when the reverse bias voltage of diode V_{d-rb} is varied. This eventually results in variation of $Z_{in,T}$ as well as f_{op}. When the diode is forward biased (forward bias diode voltage V_{d-fb} > 0.7 V), the diode capacitance C_x changes and sets to a fixed value. Thus, variation in V_{d-fb} beyond 0.7 V does not vary $Z_{in,T}$.

$Z_{in,T}$ also depends on L_s. It increases the real part of input impedance and helps to achieve better reverse isolation. The input impedance in (6.2) can be plotted against frequency. Figure 6.3 (a) shows the theoretical plot of Im(Z_{in}) with frequency and Figure 6.3 (b) shows the theoretical plot of S_{11} of the designed IMN for multimode LNA. The input impedance is tuned to a different frequency particularly in the upper band when C_x is varied; thereby resulting in a multiband response.

Generally, the IMN of the circuit also serves for noise matching in LNA. The multiple

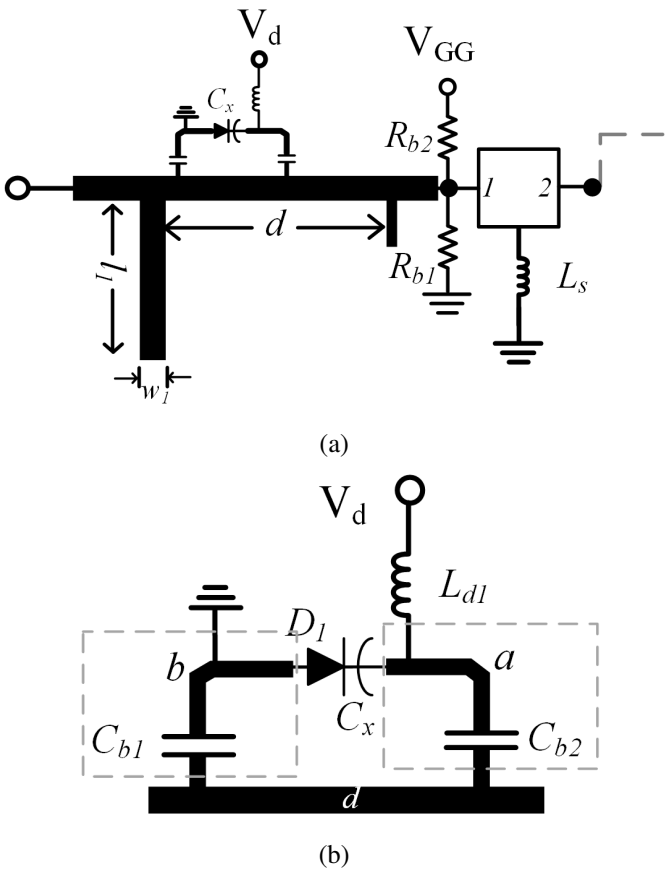


Figure 6.2: (a) Input matching network of the proposed tunable LNA (b) Biasing circuit for varactor diode in reverse bias mode

operation modes will lead to change in the input impedance. Circuit optimisation is required to achieve noise matching in all modes. This is done by plotting the gain and noise circles for the multimode LNA in Keysight ADS as shown in Figure 6.4. The aim is to achieve a NF of less than 2 dB in the all operation modes, particularly at f_{op} in each mode. The gain and noise circles are plotted to determine Z_s to match with Z_{in} for noise as well as impedance matching.

6.2.2 Design Methodology

Figure 6.5 shows the architecture of the proposed tunable multimode LNA. The design operates with the varactor diode in both forward and reverse bias modes. Table 6.1

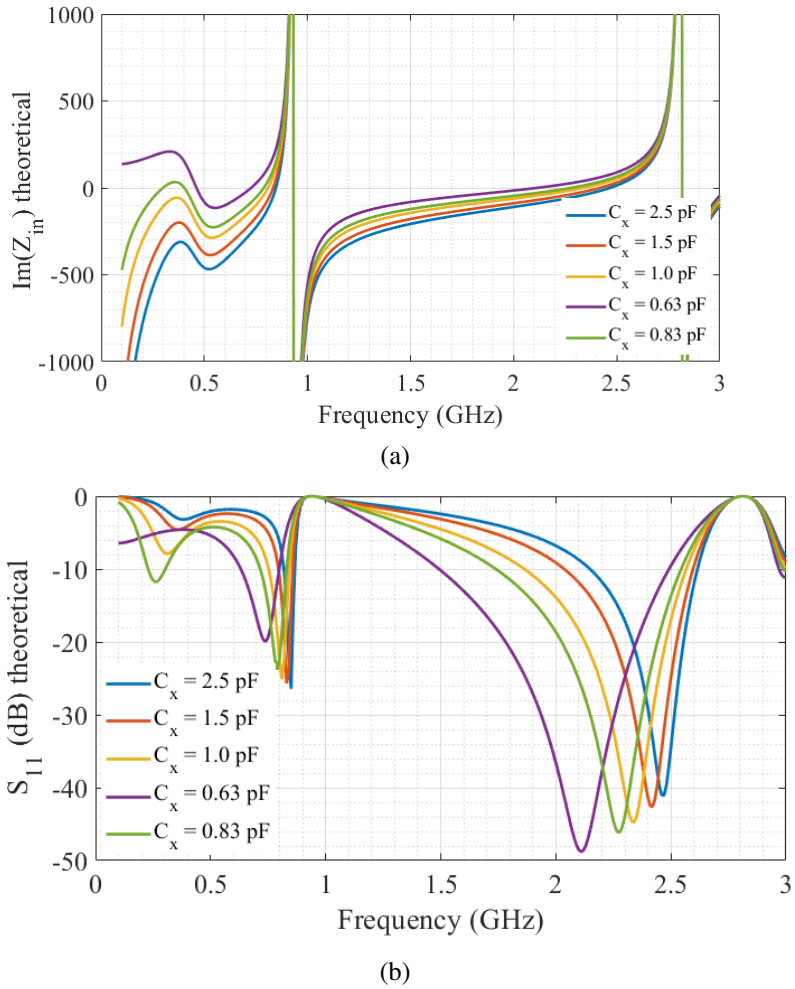


Figure 6.3: Theoretical (a) $Im(Z_{in})$ (b) S_{11} for the designed IMN

summarises the f_{op} of the designed LNA in all modes. In forward bias case, when V_{d-fb} > 0.7 V, the LNA achieves a wideband response. When no bias is applied, C_x is at its maximum, and the circuit operates in a dual band mode. When the diode is reverse biased, the LNA operates in dual band mode with a tunable upper band. The upper band is made tunable by continuously varying V_{d-rb}, starting from 0.5 V. When V_{d-rb} > 10 V, C_x is too low and LNA operates in single band mode.

The capacitors C_{b1} and C_{b2} in the input matching stage serve as DC blocking capacitors and form a part of the diode biasing circuitry. The input capacitor C_1 and ouput capacitor C_2 are high value capacitors that block the DC from the two SMA ports.

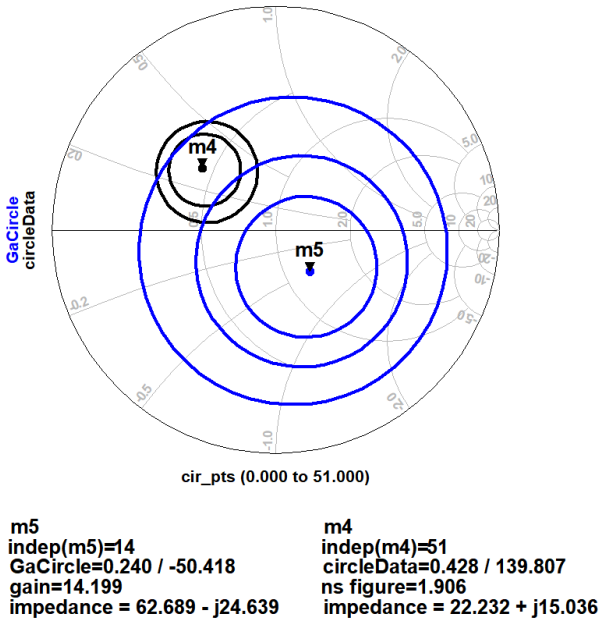


Figure 6.4: Gain and noise circles for noise matching of multimode LNA

Table 6.1: Bias and V_d configuration for multimode LNA design

Bias	V_d (V)	**Mode**	f_{op} (GHz)
Forward bias	0	dual band	0.9, 1.7 – 2.5 GHz
	>0.7	wide band	1.7 – 2.5
Reverse bias	1	dual band	0.9, 1.85 – 2.5
	3	dual band	1 , 2.0 – 2.5
	5	dual band	1 , 2.2 – 2.5
	>10	single band	0.95 – 1.1

The output matching network is designed using conventional stub matching and provides a 50 Ω impedance match at 2.4 GHz. The LNA implements a resistive - inductive load to achieve passbands and stopbands at desired frequencies. The resistor R_3 serves for biasing as well as output load resistance. Similarly, L_3 serves as a DC feed and output load. The aim is to achieve a good SBRR in dual band modes and a high IRR. The circuit uses CE3512K2 as the active device because of its high stability at higher frequencies. Additionally, Skyworks SMV1405-040LF is used as a varactor to achieve a wide capacitive range with smaller capacitance values at microwave frequencies. Table 6.2 shows the implemented component values.

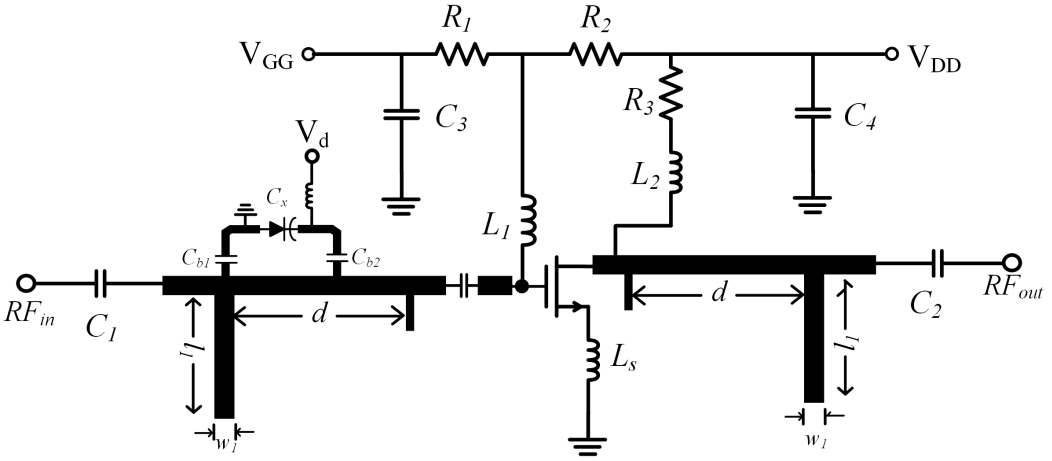


Figure 6.5: Multimode tunable LNA design

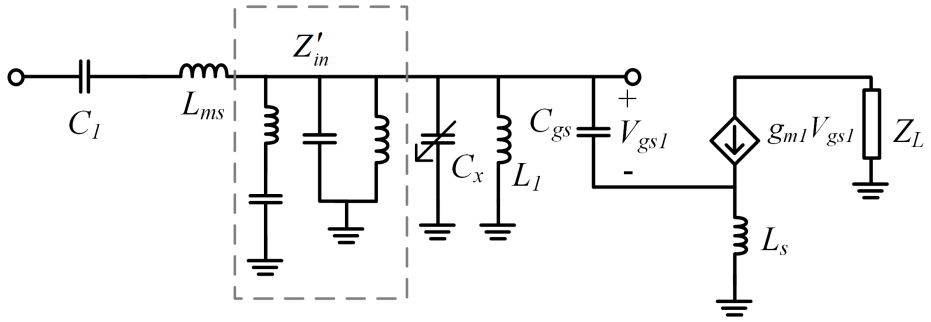
Table 6.2: SMT component values implemented in multimode LNA design

Component	**Implemented Value**	**Manufacturer**
C_1	10 pF	Murata
C_2	22 pF	Murata
C_{b1} , C_{b2}	10 nF	Murata
C_3, C_4	1 nF	Murata
L_1	8.2 nH	Coilcraft
L_2	15 nH	Coilcraft
L_{d1}	39 nH	Coilcraft
R_1, R_3	300 Ω	Vishay
R_2	1130 Ω	Vishay

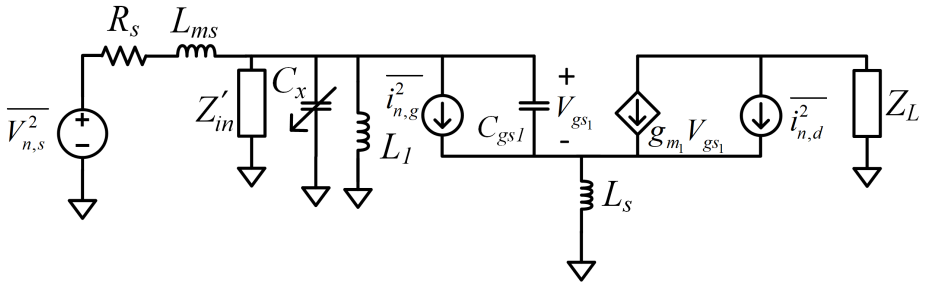
6.2.3 Gain Analysis

Figure 6.6 (a) shows the small signal equivalent of the multimode LNA circuit. Microstrip lines have been replaced with their lumped counterparts for the sake of convenience. Z'_{in} represents the equivalent impedance of the lumped section replaced from original distributed elements. L_{ms} is the inductance of microstrip line d with $\theta = 0°$. The small signal transconductance parameter of M_1 is $g_{m1}V_{gs1}$. The load impedance of LNA is given as

$$Z_l = R_3 + j\omega L_2 \tag{6.3}$$



(a)



(b)

Figure 6.6: (a) Small signal equivalent (b) Noise equivalent model of multimode LNA

The output voltage is given as

$$V_o = -(g_m V_{gs1}) Z_l \tag{6.4}$$

Applying KVL in the input side, the input voltage V_{in} is

$$V_{in} = I_{in}\left(\frac{1}{j\omega C_1} + j\omega L_{ms}\right) + I_{in}\left(Z'_{in} \,\|\, j\omega L_1 \|\, \frac{1}{j\omega(C_{gs}+C_X)} + j\omega L_s\right) + g_m V_{gs1}\left(j\omega L_s\right) \tag{6.5}$$

From (3.3), we have $V_{gs1} = \frac{I_{in}}{j\omega C_{gs}}$

$$V_{in} = V_{gs1}\left(j\omega C_{gs1}\right)\cdot\left[\frac{1}{j\omega C_1} + j\omega L_{ms} + Z'_{in} \,\|\, j\omega L_1 \|\, \frac{1}{j\omega(C_{gs1}+C_X)} + j\omega L_s + \frac{g_m L_s}{C_{gs}}\right] \tag{6.6}$$

$$V_{in} = V_{gs1}\left(j\omega C_{gs1}\right)\left(1 + Z''_{in}\right) \tag{6.7}$$

where $Z''_{in} = \frac{1}{j\omega C_1} + j\omega L_{ms} + \left(Z'_{in} \,\|\, j\omega L_1 \| \, \frac{1}{j\omega(C_{gs1}+C_X)} + j\omega L_s\right) + \frac{g_m L_s}{C_{gs}}$.
From (6.4) and (6.7) the voltage gain A_v is given as

$$A_v = \frac{V_o}{V_{in}} = \frac{-g_m Z_l}{j\omega C_{gs1}\left(1 + Z''_{in}\right)} \tag{6.8}$$

6.2.4 Noise Analysis

Figure 6.6 (b) shows the noise equivalent model of the designed multimode LNA. Since, the transistor M_1 contributes to maximum noise in the circuit, the primary sources of noise in the circuit would be due to source $\overline{i^2_{n,s1}}$, induced gate $\overline{i^2_{n,g1}}$, drain $\overline{i^2_{n,d1}}$ and load $\overline{i^2_{n,rl1}}$. Using the portion of short circuit noise current due to source, induced gate, thermal drain and load of LNA, the noise factor F can be derived as

$$F_1 = 1 + \frac{\overline{i^2_{n,g1}}\left(\frac{g_{m1}(R_s+Z''_{in})}{sC_{gs1}(R_s+Z''_{in})}\right)^2 + \overline{i^2_{n,d1}}\left(1 - \frac{g_{m1}L_s}{C_{gs1}(R_s+Z''_{in})}\right)^2 + \overline{i^2_{n,rl1}}}{\left(\frac{g_{m_1}V_{n,s}}{sC_{gs1}(R_s+Z''_{in})}\right)^2} \tag{6.9}$$

The derivation of this equation follows the derivation proposed in section 4.2.4.

6.3 Circuit Implementation

The tunable LNA in Figure 6.5 is implemented on an FR-4 board (ϵ_r = 4.5, h = 1.5 mm) using microstrip lines. The biasing is achieved using a potential divider bias and the measured power consumption of the LNA is 20 mW. The biasing was achieved at a gate-source voltage (V_{GS}) of - 0.5 V, V_{DS} = 2 V and I_d = 10 mA.

The 4-pin active device CE3512K2 requires good source pins connection to reduce overall power loss in transistor. Therefore, a wider custom microstrip pad is designed

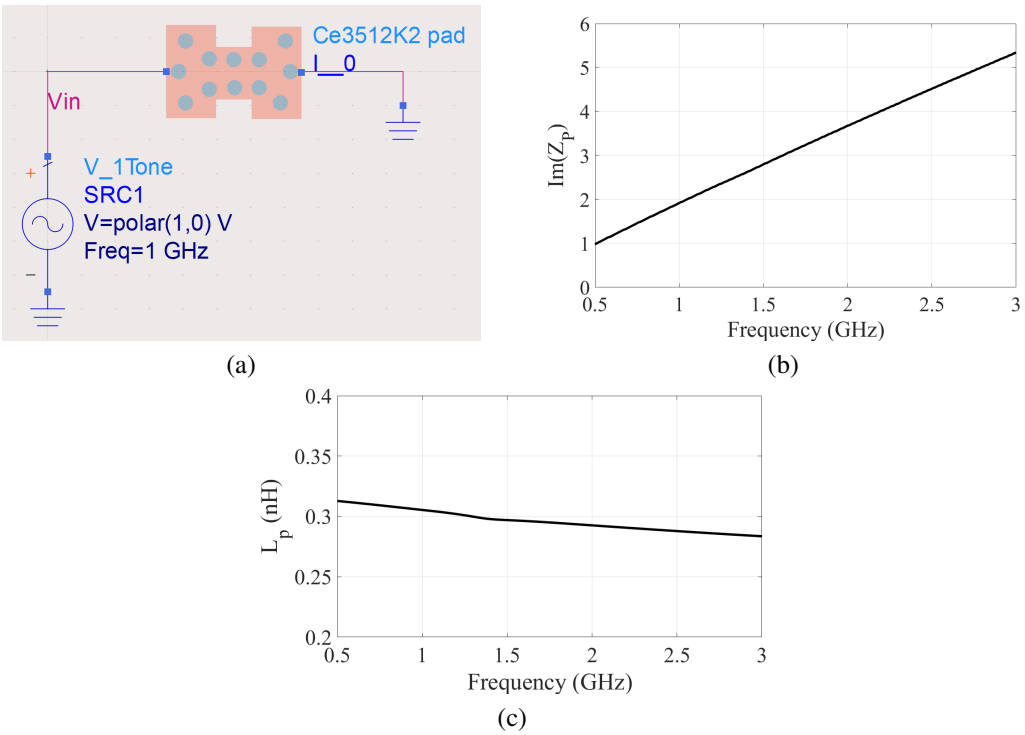


Figure 6.7: (a) CE3512K2 source pad modelling (b) Variation of Z_p with f_{op} (c) Variation of L_p with f_{op}

with pad and vias on both layers. This provides a robust source connection for the transistor. The impedance of microstrip pad Z_p depends on frequency and also affects the input impedance Z_{inT}. Figure 6.7 (a) shows the design of transistor pad and Figure 6.7 (b) shows the variation of Z_p with f_{op}. The resultant inductance of the pad L_p is approximately 0.3 nH and it varies from 0.28 nH to 0.32 nH from 500 MHz to 3 GHz, respectively as shown in Figure 6.7 (c). This eliminates the need of adding a separate source inductance as $L_p \approx L_s$.

A robust vertical ground connection has been created in the MPCB through via stitching. It not only allows easy ground path to SMT passive components and microstrip lines, but also helps in maintaining a low circuit impedance and short-return path loops. Figure 6.8 shows the fabricated multimode LNA for SDR applications.

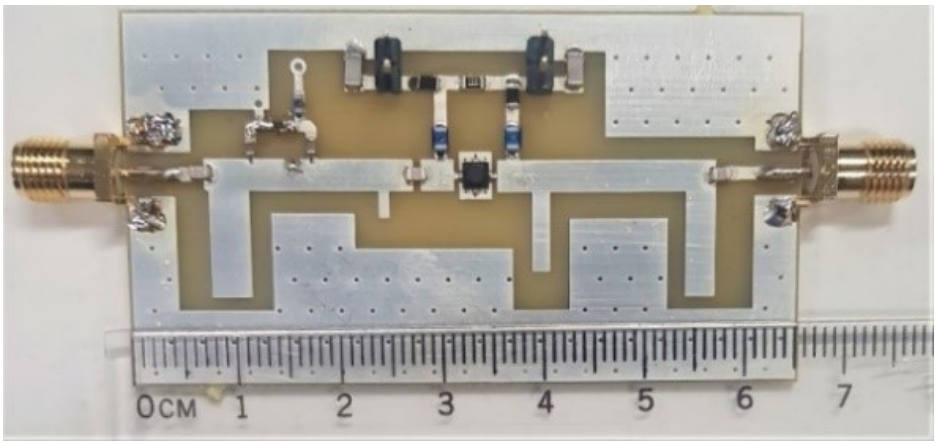


Figure 6.8: Fabricated multimode tunable LNA

6.4 Results

The LNA is fabricated in MIC process. The total PCB size is 65 mm $\times$ 35 mm. The simulation and EM analysis is carried out in Keysight ADS. MATLAB is used to carry out the mathematical analysis of multimode LNA. The LNA outperforms existing designs reported in [86, 150, 152, 153].

Figure 6.9 (a) and (b) show measured and simulated S_{11} and S_{21} of the LNA in no-bias and forward bias mode, respectively. When no bias is applied, the LNA operates in dual band mode and achieves a measured gain of 9.5 dB at 900 MHz and 8 – 15 dB at 1.7 – 2.5 GHz. The measured S_{11} is –10 dB at 900 MHz and <–9 dB from 1.7 – 2.5 GHz. When the diode is forward biased, the LNA operates in wideband mode and achieves a measured wideband gain of 7.5 – 14 dB from 1.7 – 2.5 GHz. The measured S_{11} is less than –8.5 dB in the bandwidth.

Figure 6.10 (a)–(d) show measured and simulated S_{11} and S_{21} of the LNA in reverse bias mode. At V_{d-rb} = 1 V, the LNA achieves a gain of 8.5 dB at 1 GHz and 8.5 – 14.7 dB at 1.8 – 2.5 GHz, while the S_{11} is –10 dB in lower band and –8 dB in upper band. When V_{d-rb} = 3 V, the measured S_{21} is 9.1 dB at 1 GHz and 10 – 14.7 dB at 2 – 2.5 GHz. The measured S_{11} is –11.3 dB at 1 GHz and less than –10 dB at 2 – 2.5 GHz. At

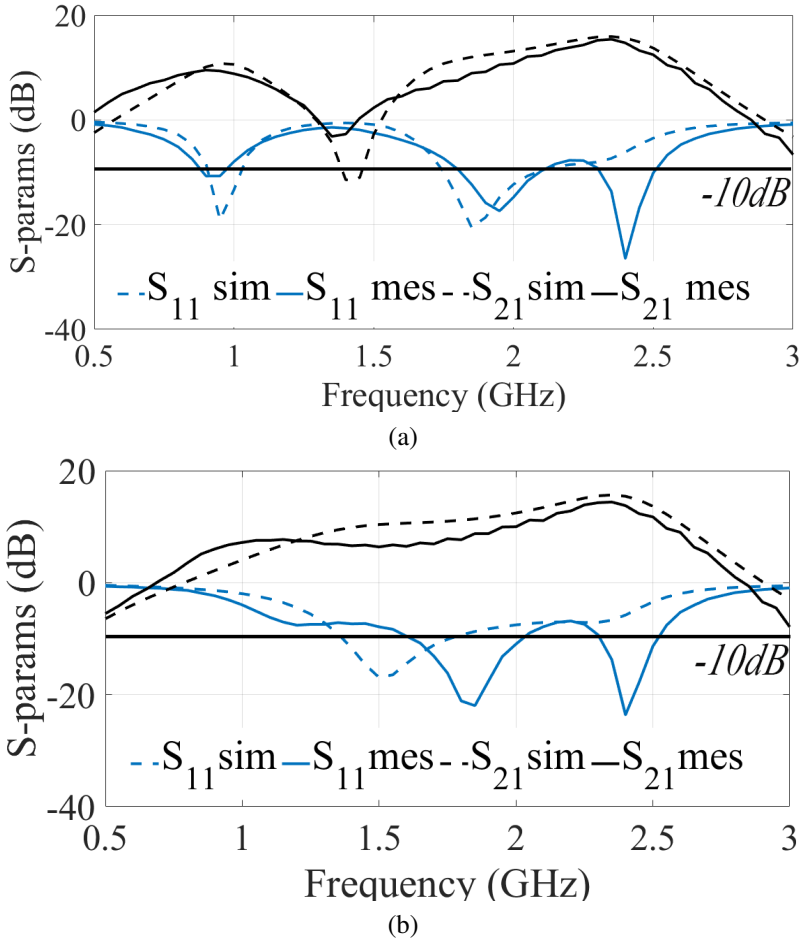
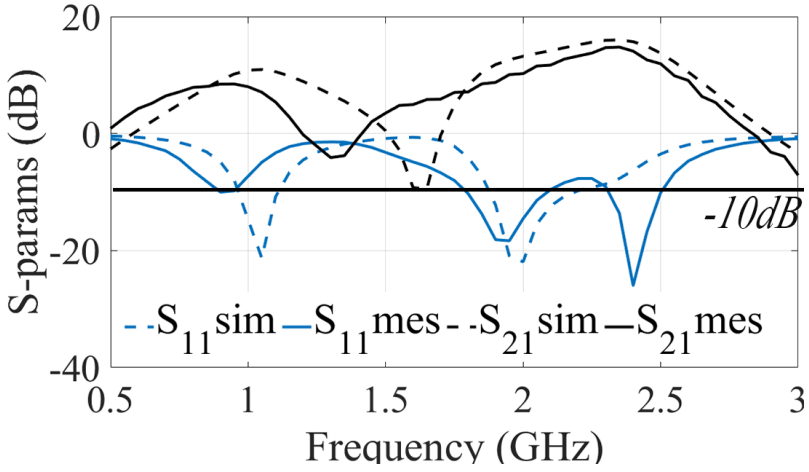


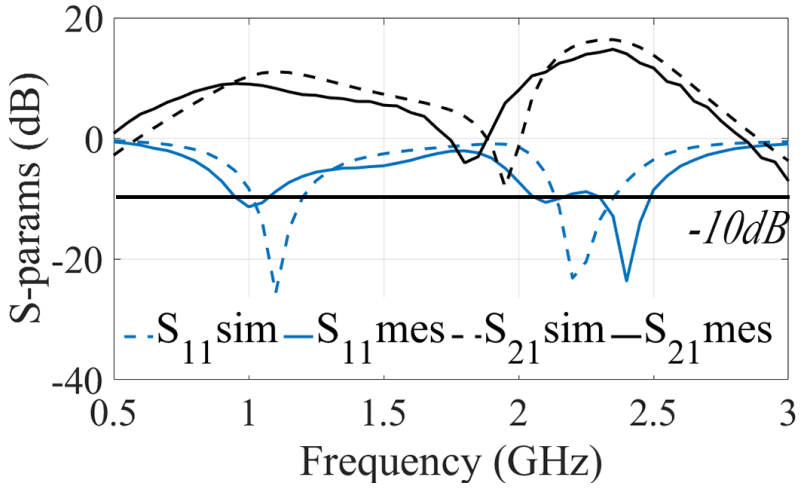
Figure 6.9: Simulated and measured S-parameters in (a) zero bias (b) forward bias mode

V_{d-rb} = 5 V, the LNA still operates in dual band mode while bandwidth of the second band narrows down to 300 MHz. The circuit achieves a gain of 9.2 dB at 1 GHz and measured peak gain of 14.7 dB from 2.2 – 2.5 GHz. When V_{d-rb} = 15 V, the LNA operates in single band with a measured S_{21} of 9 dB and S_{11} is –11.2 dB at 1 GHz. Figure 6.11 shows the simulated and measured S_{22} of the designed multimode LNA. The S_{22} is fixed and does not vary much with change in V_{d-rb}. Its measured value is –14 dB at 2.4 GHz.

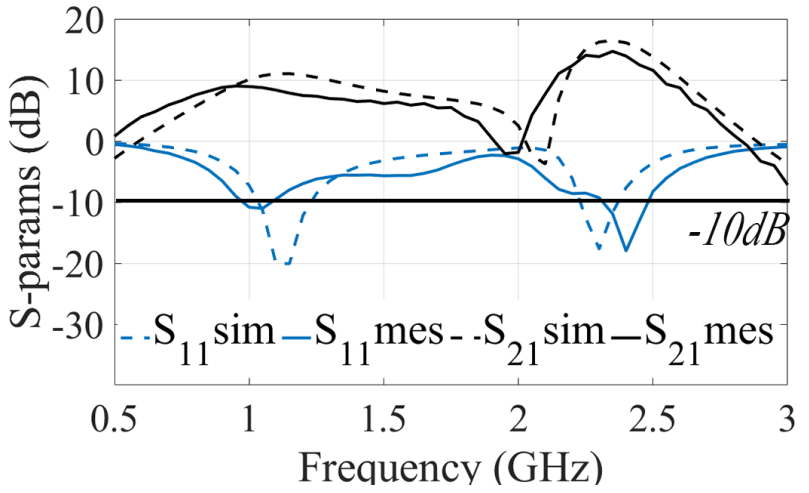
The NF of the LNA is measured using the Keysight's PNA-X network analyser. The circuit embeds minimum lumped components in the RF path and therefore achieves



(a)

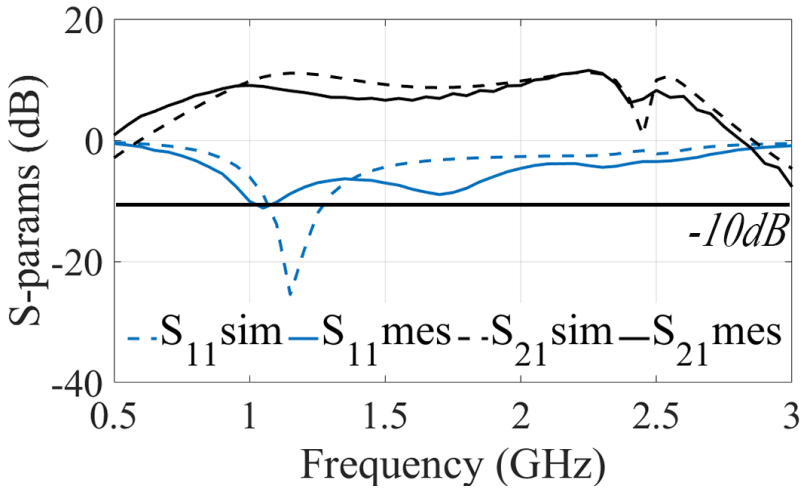


(b)



(c)

Figure 6.10: Simulated and measured S-parameters in reverse bias at (a) V_{d-rb} = 1 V (b) V_{d-rb} = 3 V (c) V_{d-rb} = 5 V



(d)

Figure 6.10: Simulated and measured S-parameters in reverse bias mode at (d) V_{d-rb} > 10 V

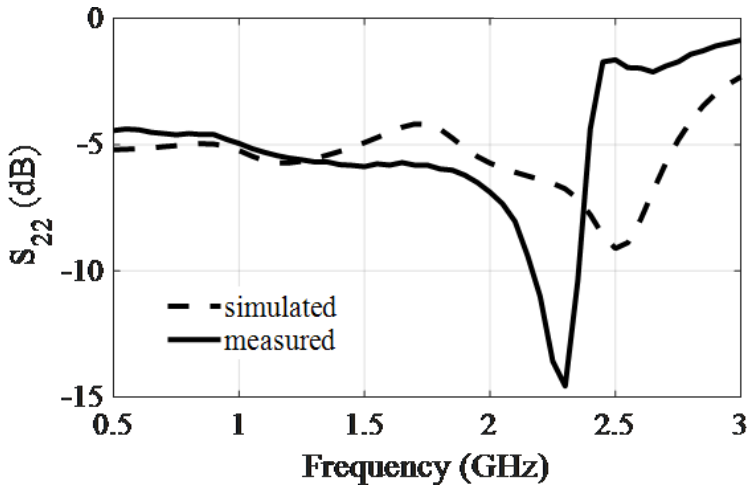


Figure 6.11: Simulated and measured S_{22} for multimode LNA

a low NF. The measured NF is similar in all modes of operation. Figure 6.12 shows the measured NF in zero bias case. It is 1.5 dB and 2 dB at 900 MHz and 2.4 GHz, respectively. The linearity of designed circuit is evaluated by measuring P_{1dB}. The amplifier achieves a good linearity and measured P_{1dB} is the similar in all modes of operation. The P_{1dB} is measured at discrete input power points using Rhode and Schwarz (R&S) FSV K30 spectrum analyser. Figure 6.13 (a), (b) show input vs output power curves for measurement of P_{1dB} at 900 MHz, 1.05 GHz and 2.4 GHz.

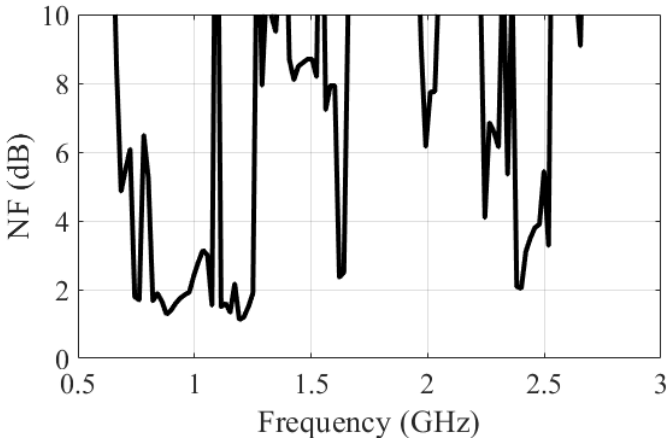
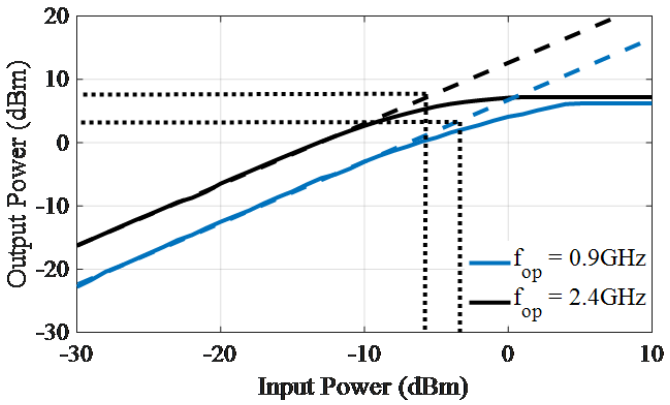
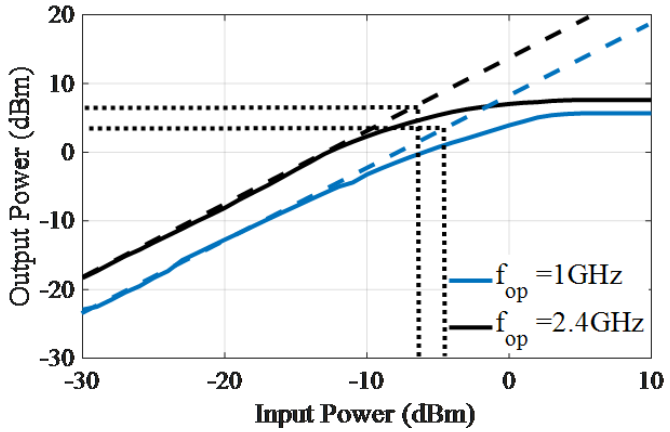


Figure 6.12: Measured NF for the designed LNA at in zero bias case



(a)



(b)

Figure 6.13: Measured P_{1dB} for designed LNA at (a) V_d = 0V (b) V_d = 5V

Measured P_{1dB} at 900 MHz with no bias is –4 dBm. Further, at 1 GHz with 5 V and 10 V reverse bias, P_{1dB} is –3 dBm. Finally, at 2.4 GHz with 0 V, 5 V and 10 V reverse

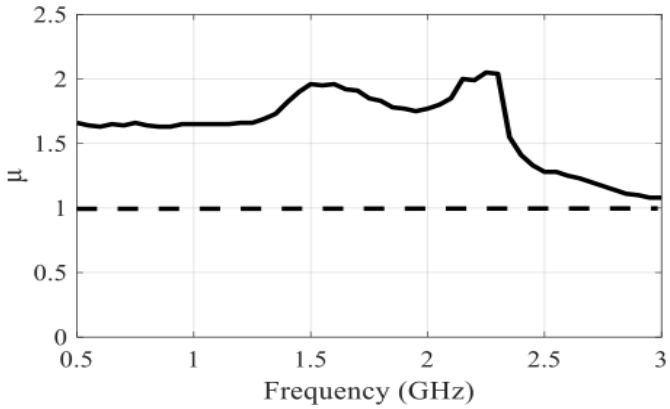


Figure 6.14: Stability criterion for designed LNA

bias, the measured P_{1dB} is –6 dBm.

The stability of the circuit is calculated using a single variable criterion μ at all values of V_d in reverse bias mode and in forward bias mode [154]. From calculations, μ >1 in all modes. As a result, the designed tunable LNA is unconditionally stable at all operating frequencies and in all modes of operation as shown in Figure 6.14.

6.5 Conclusion

A novel multimode LNA with continuously tunable IMN has been proposed in this chapter. The tunability and frequency reconfiguration in multiple modes is achieved by using a varactor diode in the input matching stage of the LNA. The circuit employs a modified open stub matching to achieve multiband tuning. The varactor diode is connected with an additional bias circuitry in parallel to the horizontal microstrip line. Multiple operational modes are achieved by varying the bias voltage of the varactor diode. The LNA achieves a good impedance matching, high gain, good linearity and unconditional stability in all modes of operation. To the authors' best knowledge, this is the first multimode LNA capable of achieving single band, concurrent dual band, wide band and continuously tunable upper band modes on MIC level. The proposed tunable LNA circuit provides a promising solution to the reconfigurable front-ends of SDRs.

Table 6.3: LNA performance summary and comparison with previous designs

-	f_{op}	S_{21}	S_{11}	NF	P_{1dB}	Mode
-	(GHz)	(dB)	(dB)	(dB)	(dBm)	-
This work	0.9, 1.7–2.5	9.5, 8–15	–10, <–9	1.5, 2	–4, –6	dual band
	1.7–2.5	7.5–14	<–8	2	–6	wide band
	1, 1.8–2.5	8.5, 8.5–14.7	–10, <–8	1.2, 2.2	–3, –6	dual band
	1, 2–2.5	9.1, 10–14.7	–10, <–8.5	1.2, 2.2	–3, –6	dual band
	1, 2.2 – 2.5	9.2, 10 – 14	–11.3, <-10	1.6, 2	–3, –6	dual band
	1	9.05	–11.2	1.5	–3	single band
[142]	0.9	10	<–18	2.3	-	fixed band
	1.5 – 2.4	8	<–18.7	3 – 4	-	tunable upper band
[74]	2.0 – 2.5	1.6 – 8	<–12	2.4 – 3.4	-	tunable lower band
	5	5.4	<–11	2.5	-	fixed band
[151]	1.8 – 2.4	20.6 – 22.1	<– 8	3.2 – 3.5	– 24.8, – 20.6 *	cont. tun.
[86]	0.7 – 1.5	5 – 10	–7 – –15	2.3 – 3.5	>–14.8*	cont. tun.
[153]	2 – 3	12 – 15	<–12	2.2 – 2.9	>–10.1*	cont. tun.

* Approximate P_{1dB} value, calculated from IP_3

Table 6.3 compares the performance of this work to that of related works.

Chapter 7

Design and Analysis of a Reconfigurable Wideband LNA

7.1 Introduction

SDRs require wide operational bandwidth for several applications. Wideband LNAs are used in conjunction with digital radio receivers that possess a high dynamic range. The frequency and bandwidth selection in this case requires digital reconfiguration through complex algorithms and channelisation. In such a scenario, the wideband receiver frond-end components are required to achieve a very high performance and interference rejection capabilities. This places stringent linearity and gain requirements on the LNA and mixer stages [155].

The two plausible ways of achieving a high reconfiguration are - using (i) switchable LNAs, and (ii) tunable LNAs. High reconfiguration in switchable LNAs is achieved in [56, 156]. Nevertheless, both the circuits implemented RF transformers in the IMN/ OMN stage that occupied a large circuit area. Additionally, use of multiple CMOS switches for reconfiguration leads to increased NF and reduced linearity. [57].

Tunable LNAs, on the other hand, can provide continuous narrowband tuning at multiple

frequencies. However, most input tunable LNAs implement tunable devices or networks that easily degrade the noise performance of the LNA and subsequently the receiver. Most works on wideband LNAs for SDRs implement conventional wideband LNA design approaches which are discussed in Chapter 2. However, recent works on wideband SDR–LNAs focus on achieving reconfiguration in power mode [34] , concurrent wide dual band operation [110] and reconfigurable wideband operation [157].

Apparently, no work has been presented that implements bandwidth tunability. It would be interesting see a fully integrated LNA that can achieve a broadband response with large 3-dB bandwidth and allows a continuous frequency and bandwidth tuning capability in more than one band.

In this chapter, we propose a dual band and bandwidth tunable LNA for SDR receivers. The LNA can be reconfigured between a high band and a low band using a switchable IMN. The proposed LNA is capable of switching from a narrowband operation to wideband operation in each band by varying the output impedance of the LNA. In other words, continuously tunable bandwidth in both high and low band, is achieved through a tunable OMN and load network.

7.2 Proposed Reconfigurable LNA

Figure 7.1 shows the schematic of the proposed reconfigurable LNA. The designed LNA employs an Si-Ge HBT as the active device. A series resistive-capacitive ($R-C$) feedback is added to achieve a wideband response in the lower band. The designed circuit is divided into three sections - (i) broadband amplifier, (ii) band reconfiguration by RF PIN diode and, (iii) frequency tuning by a tunable varactor. The design details of these sections are explained as follows.

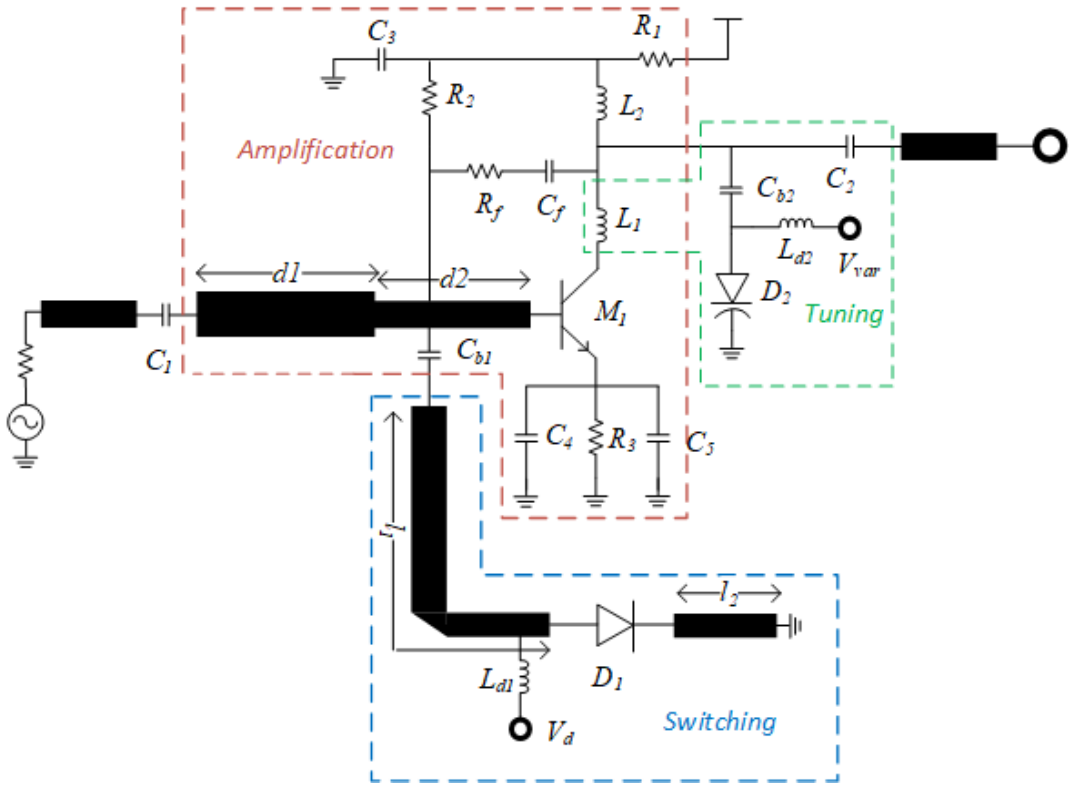


Figure 7.1: Schematic of proposed reconfigurable LNA

7.2.1 Broadband Resistive Feedback Amplifier

The amplification stage in the LNA provides a flat gain response across a wide bandwidth. The amplifier implements a microstrip line based IMN. The two microstrip lines of lengths d_1 and d_2 match the input impedance of the amplifier to the impedance at the input of transistor. The amplifier biasing is achieved through self biasing and potential divider biasing from a combination of resistors R_1, R_2 and R_3. The amplifier is in common emitter (CE) configuration with resistive degeneration. The resistor R_3 helps in increasing the real part of input impedance. The output side of the amplifier is connected to an inductive wideband load through inductances L_1 and L_2.

The resistor R_f is the feedback resistor which helps in providing a wide 3-dB bandwidth (see Section 3.2.2). The feedback capacitance C_f performs two functions (i) adds a reactive element to the feedback of amplifier (ii) blocks the DC from the collector side

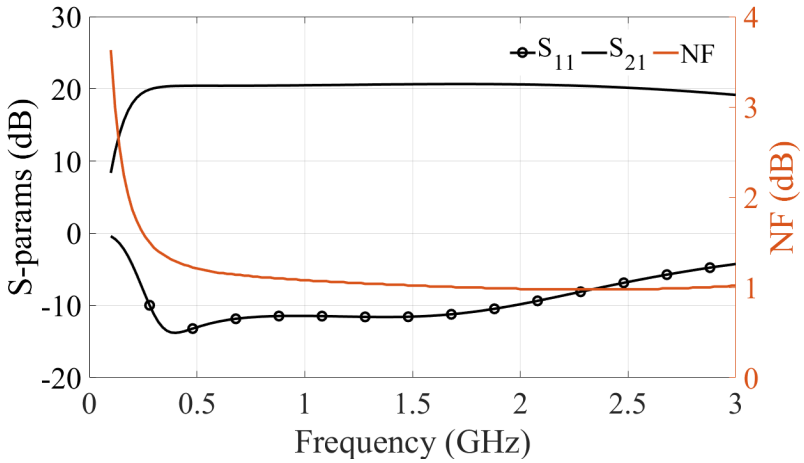


Figure 7.2: Simulated S_{21}, S_{11} and NF of the broadband amplification stage

of HBT.

Figure 7.2 shows the simulated S_{21}, S_{11} and NF of wideband amplification stage. In this case, the broadband amplifier stage is designed to cover a bandwidth from 0.2 – 2 GHz. The amplifier achieves a simulated wideband voltage gain of more than 20 dB across the bandwidth and S_{11} is also less than –10 dB. In the amplification stage, the value of inductor L_1 is kept low to achieve a wide operating range. Reducing the value of L_1 reduces the operating S_{11} bandwidth, thus narrowing the operating range of amplifier. The resistive feedback part in the broadband amplifier design facilitate impedance as well as noise matching thereby providing a simulated NF of less than 1.5 dB across the bandwidth.

7.2.2 Band Reconfiguration by PIN Diode

The reconfiguration in the existing resistive feedback broadband LNA is realised by a PIN diode. The aim is to perform reconfiguration between two separate wide bands. To achieve this, an open microstrip line stub of length l_1 and width w_1 is added to the input side of the amplifier. This open stub at $\theta = 90°$ is equivalent to a series $L - C$ network to ground (see Figure 3.11), the reactance of which is $\pi/4$ times the line reactance. A

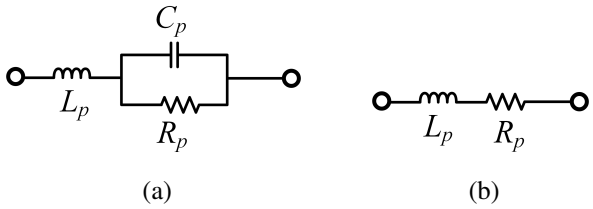


Figure 7.3: PIN diode equivalent circuit in (a) OFF mode (b) ON mode

short circuited line of length l_2 is connected to line l_1 through the PIN diode D_1. The diode D_1 is connected in forward bias configuration with its cathode connected to the ground. A high value inductor L_{d1} acts as DC feed to forward bias D_1. Figure 7.3 (a) and (b) show the equivalent circuits of D_1 in OFF and ON modes, respectively.

When D_1 is OFF, the parallel stub l_1 acts as an open stub. The line l_1 remains virtually disconnected from l_2 and the circuit operates in lower band that spans from 0.2 GHz to 1 GHz. In OFF mode, The package inductance L_p is connected in series with a parallel connection of the diode resistance R_p and junction capacitance C_p. The value of R_p is high ($\sim 5k\Omega$) in this mode and the diode blocks the RF signal.

On the other hand, when D_1 is ON, the stub l_1 is connected to stub l_2 and act as a short stub. The equivalent circuit is a parallel $L-C$ tank circuit shunted to ground, the impedance of which is $4/\pi$ times the total line impedance. In this case, the LNA operates in upper band that spans from 2.2 GHz to 3 GHz. In the ON mode, R_p is low, C_p is absent and the diode allows the flow of RF signal.

7.2.3 Frequency Tuning

After the band selection is achieved by the switching network, the next objective is to achieve reconfiguration in LNA bandwidth. One way to achieve this is by replacing load inductor L_1 with a transformer based variable inductor as shown in Chapter 5. However, this would result is increased circuit complexity, high NF, reduced linearity and large circuit area requirement.

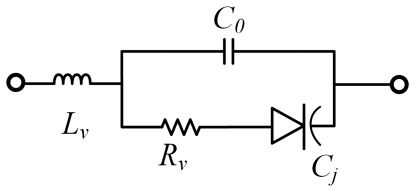


Figure 7.4: Equivalent circuit of varactor diode

Alternatively, a tunable varactor diode D_2 is added in parallel to L_1 to change the response of input and output matching network. The equivalent circuit for D_2 is shown in Figure 7.4. The varactor diode is placed in reverse bias configuration and positive bias to the cathode is provided through a DC feed inductor L_{d2}. The equivalent junction capacitance C_j of the diode D_2 changes when the reverse bias voltage V_{var} is varied. The relationship between C_j and V_{var} is given as

$$C_j(V_{\text{var}}) = \frac{C_0}{\left(1 - \left(V_{\text{var}}/V_0\right)\right)^p} \tag{7.1}$$

where, C_0 is the junction capacitance of D_2 with no bias, v_0, is the barrier potential for the implemented pin diode and p is the gradient coefficient. For the implemented diode, $V_0 = 0.79$ V and p = 0.5.

This circuit then behaves like an $L - C$ resonance tank that helps in achieving band selective tuning. When D_1 is OFF and V_{var} is varied, the circuit operates in the lower band and results in continuous change in operating bandwidth from 0.2 – 0.5 GHz to 0.2 – 1.4 GHz.

On the other hand, when D_1 is ON and V_{var} is varied, the circuit operates in the higher band and results in continuous change in operating bandwidth and centre frequencies from 2.2 to 3.2 GHz.

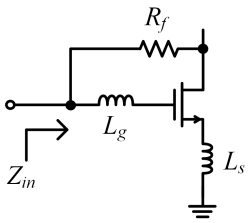


Figure 7.5: Input side of conventional RFLNA

7.3 Circuit Analysis

The designed reconfigurable LNA implements a discretely tunable IMN and a continuously tunable OMN. Diode D_1 provides reconfiguration between two widebands, while the diode D_2 provides continuous bandwidth tuning in each band. To maximise the bandwidth, a high value output capacitor C_2 is added to the circuit that also acts as a DC block.

7.3.1 Input Matching Network

Figure 7.5 shows the input side of a conventional IDCS RFLNA. Its input impedance is given as

$$Z_{in} = \frac{R_f}{1 + g_m r_o} \Bigg\| \left(j\omega \left(L_g + L_s \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \right) \tag{7.2}$$

where g_m and C_{gs} are the transconductance and gate source capacitance of transistor M, respectively and r_o is the output resistance. When (7.2) is compared with the Z_{in} of a conventional narrowband LNA (see equation (5.4)), it is concluded that at resonant frequency [1]

$$Z_{in} = \left(\frac{R_f}{1 + g_m r_o} \right) \Bigg\| \left(\frac{g_m L_s}{C_{gs}} \right) \tag{7.3}$$

This value is lower than the value of Re(Z_{in}) for narrowband LNA. Additionally, plotting Z_{in} for RFLNA with frequency shows that it achieves a wider bandwidth. Figure 7.6 shows the small signal equivalent of the proposed reconfigurable LNA.

[1] Since at resonance frequency, Im(Z_{in}) = 0

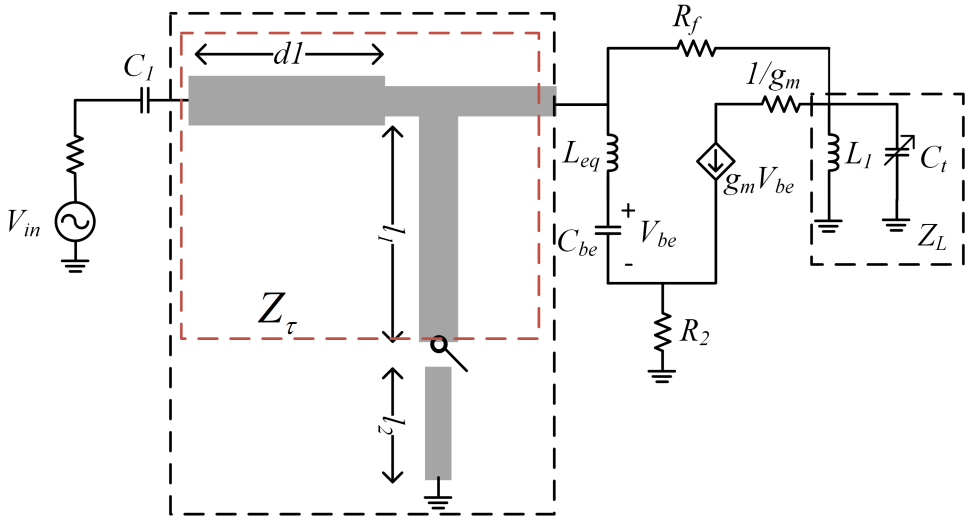


Figure 7.6: Small signal equivalent of proposed reconfigurable LNA

Applying KVL, the input impedance $Z_{in,T}$, is given as

$$Z_{inT} = Z_\tau + \left(\frac{1}{j\omega C_{be}} + j\omega L_{eq} + R_3 + \frac{g_m R_s}{j\omega C_{be}}\right) \| Z_{FB} \tag{7.4a}$$

when PIN diode is OFF and

$$Z_{inT} = Z_d + Z_\tau \| \left(\frac{1}{j\omega C_{be}} + j\omega L_{eq} + R_3 + \frac{g_m R_s}{j\omega C_{be}}\right) \| Z_{FB} \tag{7.4b}$$

when PIN diode is ON, and

$$Z_d = Z_0 \left(\frac{Z_s + jZ_0 \tan \beta d}{Z_0 + jZ_s \tan \beta d}\right) \tag{7.5}$$

where, $Z_\tau = Z_d - jZ_0 \cot \beta l_1$ when PIN diode is OFF, and $Z_\tau = Z_d + jZ_0 \tan \beta(l_1 + l_2)$ when PIN diode is ON. L_{eq} is the equivalent inductance of microstrip line d_2, Z_s is the impedance at input of transistor M, Z_0 is the characteristic impedance and

$$Z_{FB} = \frac{R_f + Z_L}{1 + g_m Z_L} \tag{7.6}$$

where Z_L is the load impedance of the tunable $L_1 - C_j$ tank circuit. A high value C_f is not included in the analysis as it does not affect $Z_{in,T}$ of the LNA. However, a low value C_f affects the bandwidth and operating frequency in the desired band.

7.3.2 Gain Analysis

Consider that D_1 is ON. Applying KVL in the circuit in Figure 7.6, the input voltage V_{in} is

$$V_{in} = I_{in}Z_\tau + I_{in}\left((j\omega L_{eq} + \frac{I_{in}}{j\omega C_{be}} + I_{in}R_3 + g_m V_{be}R_3)\,\|R_{FB}\right) + V_{be} \tag{7.7}$$

where V_{be} is the base-emitter voltage. Thus, from (7.2), input current I_{in} is

$$I_{in} = \frac{V_{in}}{Z_{in} + 1/j\omega C_{be}} \tag{7.8}$$

current in R_f is given as

$$I_{R_f} = \frac{V_{in} - V_{out}}{R_f} = V_{in}\frac{(1 + A_v)}{R_f} \tag{7.9}$$

Also,

$$I_{R_f} = I_{in} - \left(\frac{Z_{in}}{R_f + Z_{in}}\right) I_{in} = I_{in}\left(1 - \frac{Z_{in}}{R_f + Z_{in}}\right) \tag{7.10}$$

Since $|R_f| \gg |Z_{in}|$ for the operating bandwidth

$$I_{R_f} = I_{in}\left(1 - \frac{Z_{in}}{R_f}\right) \tag{7.11}$$

From (7.9) and (7.11)

$$V_{in}\left(\frac{1 + A_v}{R_f}\right) = I_{in}\left(1 - \frac{Z_{in}}{R_f}\right) \tag{7.12}$$

Substituting V_{in} from (7.8) in (7.12) and solving, we get

$$A_v = \frac{R_f - Z_{in} - (1/j\omega C_{be}) - 1}{Z_{in} + (1/j\omega C_{be})} \tag{7.13}$$

7.3.3 Noise Analysis

Figure 7.7 shows the noise equivalent model for the designed RFLNA. The noise factor F of the designed reconfigurable LNA is given as the sum of noise contributions by each stage. Let R_t be the loss resistance due to equivalent inductance of Z_τ and R_{leq} be the loss resistance due to L_{eq}. Then noise factor in this case is given as

$$F = \frac{\overline{\left|i_{o,T}^2\right|}}{\overline{|i_{so}^2|}} \tag{7.14}$$

where $\overline{\left|i_{o,T}^2\right|}$ and $\overline{|i_{so}^2|}$ are the total and source mean squared noise currents, respectively. The total noise factor is calculated as the ratio of the total output noise to the output noise due to source resistance R_s as follows

$$F = 1 + \frac{R_f + R_b + R_3}{R_s} + \frac{1}{R_s R_L g_m^2} + \frac{4\gamma R_s}{\alpha_M g_m}\left(\frac{-1}{1 + \frac{R_s(1+g_m R_L)}{R_f + R_L}}\right)^2 \tag{7.15}$$

where γ is the coefficient of channel noise and $\alpha_M = g_m/g_c$. Here g_c is the the HBT's collector conductance. The ratio of γ/α_M is generally assumed to be 1.33. The derivation of (7.15) is given in Appendix 2.

7.4 Circuit Design

The reconfigurable LNA circuit is designed as MIC on an FR-4 board ($\epsilon_r = 4.5$, h = 1.5 mm. The circuit uses BFP740F HBT as the active device in amplification stage, SMP1345-079LF PIN diode as RF switch in switching stage and SMV1405-040LF

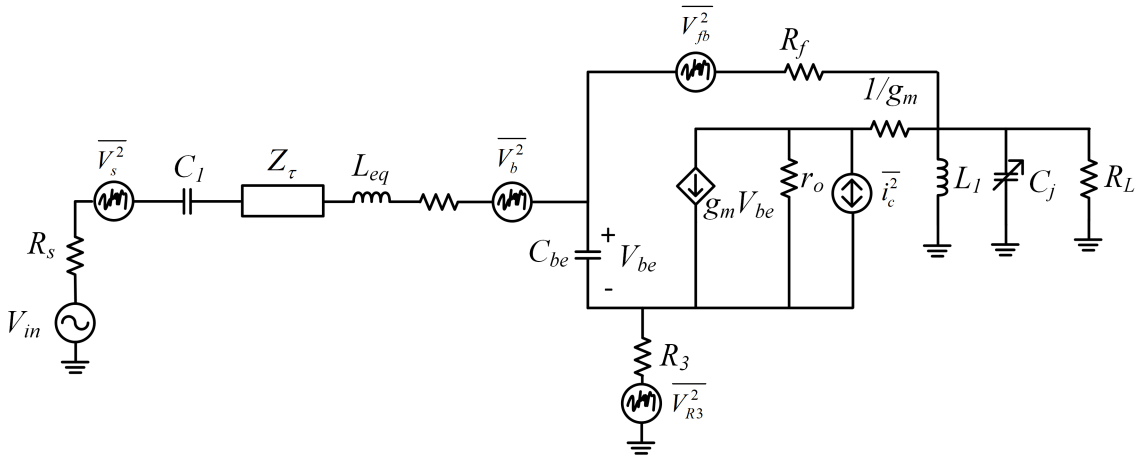


Figure 7.7: Noise equivalent model for design LNA

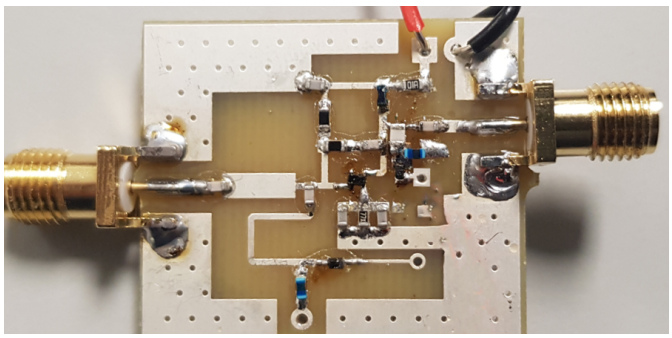


Figure 7.8: Fabricated reconfigurable wideband LNA

varactor diode in the tuning stage. Table 7.1 summarises the operating frequency range in both low band and high band mode. The circuit implements high - Q 0603 passive components form Murata and KEMET. The circuit only implements DC feed inductors to ensure low NF. The fabricated circuit is shown in Figure 7.8. A low value inductor L_1 is replaced with microstrip line of length and width 2 mm $\times$ 0.51 mm. Additionally, passive components are closely placed to minimise parasitic impedance due to microstrip lines. The total PCB size is 30 mm $\times$ 25 mm. An additional emitter inductance of 0.21 nH is introduced due to connecting microstrip lines. Table 7.2 shows the implemented component values in the designed circuit.

Table 7.1: Operating range for the designed reconfigurable LNA

Mode	V_{d-rb} **(V)**	**Frequency Range**	**Bandwidth**
Low band	0.5	0.2 – 0.5 GHz	300 MHz
	5	0.2 – 0.7 GHz	500 MHz
	30	0.3 – 1.5 GHz	1.2 GHz
High Band	0.5	2.2 – 2.6 GHz	400 MHz
	10	2.6 – 2.95 GHz	350 MHz
	30	2.7 – 3.15 GHz	450 MHz

Table 7.2: Implement component values for reconfigurable LNA

Component	**Value**	**Component**	**Value**
C_1	10 pF	L_1	1.5 nH *
C_2	100 pF	L_2	338 nH
C_3	1 nF	L_{d1}	100 nH
C_4	1 nF	L_{d2}	100 nH
C_5	1 nF	R_1	100 Ω
C_f	61 pF	R_2	16 kΩ
C_{b1}	100 pF	R_3	62 Ω
C_{b2}	100 pF	R_f	560 Ω

* Implemented as microstrip line on fabricated MIC

7.5 Results and Discussion

The circuit is designed to work with a 4 V supply an sinks 10 mA current. The measured V_{ce} for the LNA is 2.2 V. The net power consumption of the LNA is 40 mW. The circuit and EM simulation analysis is carried out in Keysight ADS IDE and Momentum, respectively. Reconfigurable LNA's S- parameters are measured with Anritsu S820E VNA. The LNA outperforms other reconfigurable LNAs reported in [60, 72, 102, 158]. Figure 7.9 (a) – (c) show the simulated and measured S_{11} and S_{21} when the D_1 is OFF. As shown in Figure 7.9 (a), the circuit achieves a simulated wideband gain of 14 dB – 17 dB and measured wideband gain of 9 dB – 14.5 dB from 0.2 GHz to 1 GHz. In this case, the reverse bias voltage V_{d-rb} of D_2 is 0.5 V. The measured S_{11} is less than –10 dB from 0.2 GHz to 0.5 GHz. Therefore, the operating bandwidth is 300 MHz.

When V_{d-rb} = 5 V, the simulated and measured S_{11} is less than –10 dB from 0.2 GHz to

0.7 GHz as shown in Figure 7.9 (b). The simulated and measured gain in this case is 10 – 15 dB and 9 – 14.5 dB, respectively. The operating bandwidth is 500 MHz.

When V_{d-rb} = 30 V, the LNA operates in wideband mode as shown in figure 7.9 (c). The simulated S_{11} in this case is less than –10 dB from 0.3 GHz to 1.8 GHz, while measured S_{11} is less than –10 dB from 0.3 GHz to 1.5 GHz. The operating bandwidth in this case 1.2 GHz. The simulated and measured S_{21} in the operating range is 9 - 15 dB and 8 - 14 dB, respectively.

Figure 7.10 (a) – (c) show the simulated and measured S-parameters when the D_1 is ON. When D_1 is ON and V_{d-rb} = 0.5 V, The LNA achieves a a simulated and measured S_{11} of –13.5 dB and –10 dB, respectively at 2.4 GHz. The measured operating bandwidth is 400 MHz from 2.2 GHz to 2.6 GHz as shown in Figure 7.10 (a). The LNA achieves a simulated and measured gain of 10 dB and $\sim$ 8 dB, respectively in the operating range. At V_{d-rb} = 10 V, the measured S_{11} is less than –10 dB from 2.6 to 2.95 GHz. The operating bandwidth in this case is 350 MHz. The measured gain in the operating range is 5 – 7 dB as shown in Figure 7.10 (b). The measured results have slight deviation in frequency from the simulated results due to resultant parasitic impedance from microstrip lines and additional package inductance offered by diodes D_1 and D_2.

At V_{d-rb} = 30 V, the simulated and measured S_{11} are –15 dB and –12.5 dB at 2.8 GHz. The operating frequency range is 450 MHz from 2.7 GHz to 3.15 GHz. The simulated and measured S_{21} in the operating range are 1 – 9 dB and 2 – 7 dB, respectively as shown in Figure 7.10 (c).

Figure 7.11 (a) and (b) show simulated and measured S_{22} of the designed LNA in D_1 ON and D_2 OFF mode, respectively. The LNA achieves a measured $S_{22} \leq$ –11 dB from 0.2 GHz to 1.8 GHz in D_1 OFF mode and less than –6 dB from 2.4 GHz to 3.2 GHz in D_1 ON mode.

Figure 7.12 (a) – (b) show the NF of the LNA in D_1 OFF and D_1 ON mode, respectively. The LNA achieves a low NF in both cases. In the former case, the LNA achieves a very

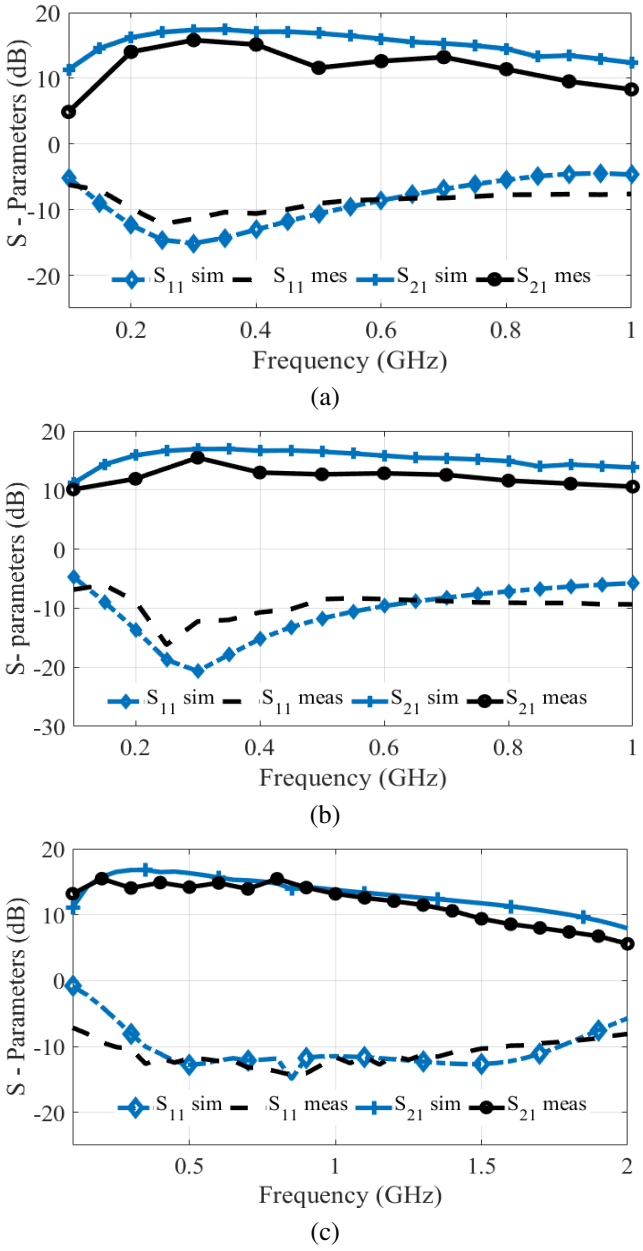


Figure 7.9: Simulated and measured S_{21} and S_{11} When D_1 is OFF and D_2 at (a) V_{d-rb} = 0.5 V (b) V_{d-rb} = 5 V (c) V_{d-rb} = 30 V

low and flat NF $\sim$ 1.2 dB from 0.1 to 1 GHz. Likewise, the LNA achieves a low NF of 1.8 dB – 2 dB from 1.8 GHz – 3.1 GHz in the latter case. It is important to note that in both cases, NF is recorded at V_{d-rb} = 25 V.

The LNA linearity is characterised with P_{1dB} measurement. P_{1dB} is measured using R&S FSV K30 spectrum analyzer and 1-tone input is given from R&S FSV Signal

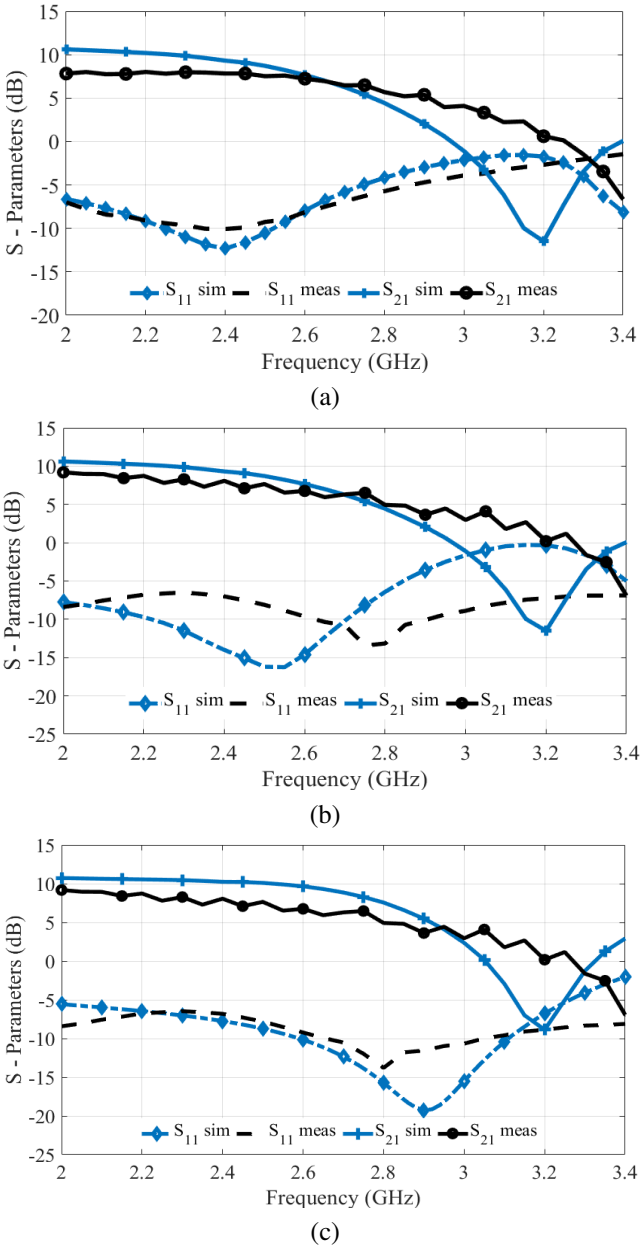


Figure 7.10: Simulated and measured S_{21} and S_{11} When D_1 is ON and D_2 at (a) V_{d-rb} = 0.5 V (b) V_{d-rb} = 10 V (c) V_{d-rb} = 30 V

generator. Gain compression points are identified and manually recorded for the frequency range from 0.2 GHz to 1.1 GHz and 2.2 GHz to 3 GHz; in steps of 100 MHz. Figure 7.13 (a) shows variation of P_{1dB} with frequency in D_1 OFF state. Measured P_{1dB} varies from –7 dBm to –1 dBm in the operating range at V_{d-rb} = 25 V. Figure 7.13 (b) shows P_{1dB} variation with frequency in D_1 ON state. The measured P_{1dB} varies

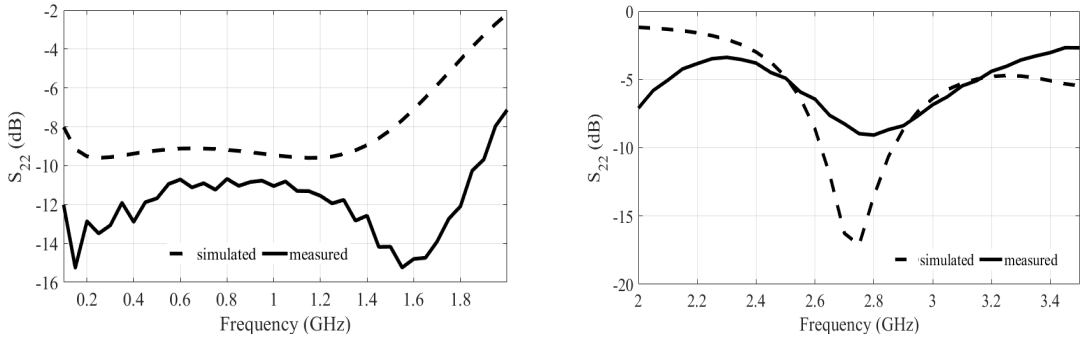


Figure 7.11: S_{22} of designed reconfigurable LNA (a) When D_1 is OFF (b) When D_1 is ON

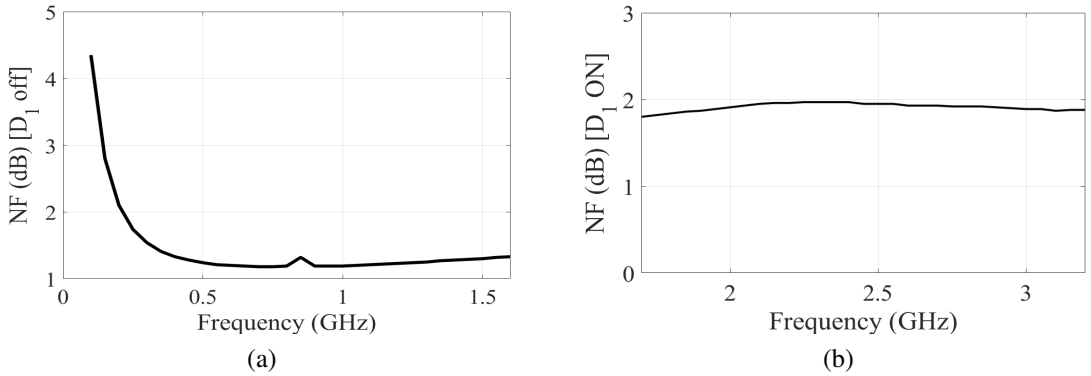


Figure 7.12: NF of designed reconfigurable LNA (a) When D_1 is OFF (b) When D_1 is ON

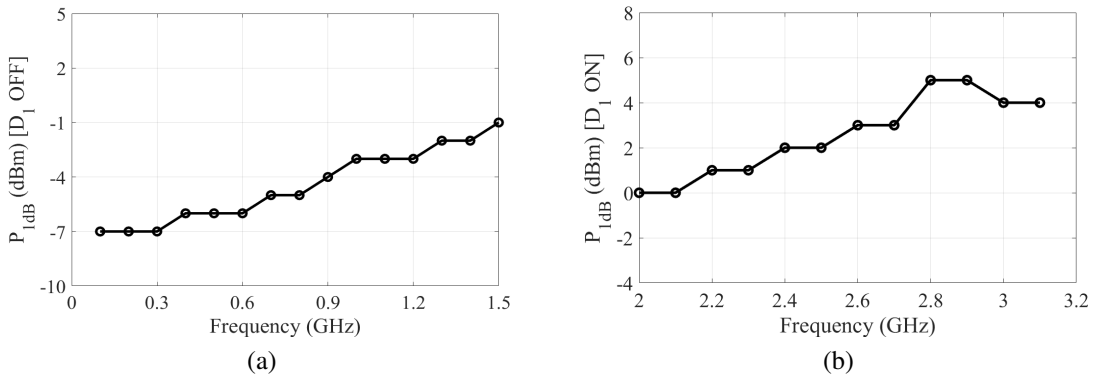


Figure 7.13: P_{1dB} vs frequency for designed reconfigurable LNA (a) When D_1 is OFF (b) When D_1 is ON

from 0 dBm to 5 dBm in the operating range at V_{d-rb} = 25 V.

7.6 Conclusion

A compact reconfigurable wideband LNA is reported in this chapter. The reconfigurable LNA is capable of achieving continuous bandwidth tuning in two separate bands where the lower band ranges from 0.2 GHz – 1.5 GHz and higher band ranges from 2.2 GHz – 3.2 GHz. The reconfiguration between low and high bands is achieved using PIN diode as an RF switch in the IMN of the LNA. Continuous tuning in each band is achieved using a varactor diode in the OMN. Wideband operation in each case is realised using resistive feedback topology. The designed reconfigurable LNA is fabricated as MIC and achieves high and flat gain in both bands. The circuit also achieves a very low NF along with linear and stable operation. The results indicate that the proposed design is suitable for low-cost and high performance reconfigurable LNAs for SDRs. Table 7.3 summarises the reconfigurable LNA results and compares it with other tunable LNAs.

Table 7.3: Designed reconfigurable LNA performance summary and comparison with related works

Ref	Freq range (GHz)	S_{11} (dB)	S_{21} (dB)	NF (dB)	IP_3 (dBm)	P_{DC} (mW)	Tech
This work (Band 1)	0.2 – 0.5	<-10	9 – 14.5	1.2 – 2	2	40	MIC
	0.3 – 1.5	<-10	8 – 15	1.2 – 2	2 - 8		
This work (Band 2)	2.2 – 2.6	<- 10	7 – 8	2	9 – 11		
	2.7 – 3.2	<- 10	2 – 7	2	11 – 14		
[72]	2.4 – 5.4	<- 10	22 – 24	2.2 – 3.1	-16 – -21	4.6	0.13 μm CMOS
[102]	2.9 – 3.5	<-5	6 – 12	3 – 5	-	18	0.18 μm CMOS
[158]	4.6 – 5.8	<-7	26 – 30	1.6 – 1.9	-6.5 – - 10.3	16	65nm CMOS
[60]	1 – 2.5	<-12	17 – 20	3.1 – 3.6	-	20	0.18 μm CMOS
[149]	1 – 5	<-5	19 – 27	1.8 – 3.4	-	12	65 nm CMOS

Chapter 8

Conclusion and Recommendation for Future Work

8.1 Conclusion

The thesis reports the design methodology and a detailed analysis of concurrent multiband and reconfigurable LNAs for SDRs. After a detailed analysis of multiband LNAs, the design issues specific to SDR LNAs are investigated to find solutions that can help in increasing SDR flexibility, achieving a high gain, high IRR and wide operating range in LNA designs.

Based on the identified problems, high performance LNAs are designed that are capable of overcoming the design issues to achieve exquisite results in all performance criteria for SDR LNAs.

Firstly, we propose the detailed design and analysis of the dual band and triband matching networks for concurrent multiband LNAs. The analysis explains the step-wise mathematical approach for the design. Thereafter, the mathematically derived values for passive components are implemented to design accurate dual band and triband matching networks. Theoretically derived results for Z_{in} and S_{11} are compared with

simulation and measurement results. The designed IMNs are converted into their microstrip equivalent circuits and fabricated results are compared with the simulation results.

Secondly, we propose the design and detailed analysis of a concurrent DBLNA with high IRR for SDR applications. The IMN is implemented using the proposed IFTT method and a modified dual band load is implemented to eliminate the sharp-roll off at the n^{th} band in the transmission curve. The two stage LNA design results in high gain in two operational bands with less GI, high IRR, high SBRR, low NF and high linearity.

Thirdly, a CTLNA with a transformer based IMN is proposed for SDR applications. The transformer's secondary winding acts as a tunable inductor whose inductance can be varied by changing the magnitude and phase of current flowing through primary winding of the transformer. This is done by adding an additional circuit in the feedback path of amplifier. This in turn would lead to change in magnitude and phase of the current in the secondary winding which leads to tunability. The proposed design overcomes the need of switches that require additional power for reconfiguration.

Thereafter, we propose the design of a multimode LNA that improves the operating range of the SDR LNA. The design incorporates a varactor diode in the input matching stage of the LNA. By changing the bias conditions and reverse bias voltage, six different operating modes can be obtained that include a wideband mode, single band mode, concurrent dual band mode and tunable upper band mode.

Finally, a reconfigurable wideband LNA with switchable dual bands is designed to achieve tunability in operational bandwidth of the LNA. The LNA implements a switching and a tuning circuit in the input and output stage of the LNA, respectively. The LNA achieves the desired performance metrics in both bands and results in continuous bandwidth tuning in each band.

To conclude, designed multiband LNAs, via the wideband or reconfigurable input and/or output impedance, can provide continuous as well as discrete frequency variation.

They can immanently reject undesired signals and out of band interferers, while adding minimum noise to the signal.

The designed concurrent DBLNA achieves a wide operating bandwidth in both bands. Additionally, all reconfigurable LNA design achieve a wide operating as well as tuning range which is greater than 500 MHz. Furthermore, the designed LNAs are linear, stable and suitable for many applications, including cognitive radios and SDRs. The proposed LNAs for SDRs are compared with the recent works and they outperform most of them at the expense increased power consumption.

8.2 Recommendation for Future work

Although four different LNA designs were presented in this thesis, there is still room to improve the design. The recommendations for future work are detailed as follows.

Promising inductorless architectures have been proposed for designing wideband, multiband and narrowband LNAs. However, there is a lack of significant research on design of highly reconfigurable inductorless LNA specially in MMIC and MIC processes. Inductorless design and reconfigurability in LNAs might seem as conflicting goals. However, they are not conflicting goals because some authors have proposed techniques such as active inductor technique, active notch filter and gyrator circuits for designing reconfigurable LNAs. These techniques are most commonly implemented in CMOS LNA and there are some limitations to these techniques due to the design process. For example, suffered linearity, high power consumption and higher noise because of large number of active devices in circuit. Moreover, there are very few frequency reconfigurable LNAs that implement inductorless architecture and scarcely any in MMIC/PHEMT process.

Some specific SDR applications require continuous tuning of gain and operational frequency. Moreover, specialised SDR applications required simultaneous gain and

frequency tuning. However, only limited research has been reported in this area. Along with smaller size and low power consumption, the performance of concurrent gain and frequency tunable LNAs can be improved.

Switchable LNAs require better reconfiguration techniques and switching circuits. Switching speed and efficiency of switches at high microwave and mm-wave frequencies is still a concern. Therefore, more research can be done to improve the switching efficiency. FPGA based programmable switches in conjunction with wideband LNA can be explored as a viable solution.

References

[1] A. M. Wyglinski, R. Getz, T. Collins, and D. Pu, *Software-Defined Radio for Engineers*. Artech House, 2018.

[2] P. Cruz, N. B. Carvalho, and K. A. Remley, "Designing and testing software-defined radios," *IEEE Microwave Magazine*, vol. 11, no. 4, pp. 83–94, 2010.

[3] H. Arslan, *Cognitive Radio, Software Defined Radio, and Adaptive Wireless Systems*. Springer, 2007.

[4] M. N. Sadiku and C. M. Akujuobi, "Software-defined radio: a brief overview," *IEEE Potentials*, vol. 23, no. 4, pp. 14–15, 2004.

[5] R. G. Machado and A. M. Wyglinski, "Software-defined radio: Bridging the analog–digital divide," *Proceedings of the IEEE*, vol. 103, no. 3, pp. 409–423, 2015.

[6] L. Mitola, "Technical challenges in the globalization of software radio," *IEEE Communications Magazine*, vol. 37, no. 2, pp. 84–89, 1999.

[7] W. H. Tuttlebee, *Software Defined Radio: Enabling Technologies*. John Wiley & Sons, 2003.

[8] A. Bazrafshan, M. Taherzadeh-Sani, and F. Nabki, "A 0.8-4-GHz software-defined radio receiver with improved harmonic rejection through non-overlapped clocking," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3186–3195, 2018.

[9] J. Wepman, "An overview of SDR and enabling technologies," *Institute for Telecommunication Sciences, National Telecommunications and Information Administration*, 2010.

[10] L. Qiu, K. Tang, Y. Zheng, L. Siek, Y. Zhu, and U. Seng-Pan, "A 16-mW 1-Gs/s with 49.6-dB sndr ti-sar ADC for software-defined radio in 65-nm CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 3, pp. 572–583, 2018.

[11] X. Cai, M. Zhou, and X. Huang, "Model-based design for software defined radio on an fpga," *IEEE Access*, vol. 5, pp. 8276–8283, 2017.

[12] P. S. Hall, P. Gardner, and A. Faraone, "Antenna requirements for software defined and cognitive radios," *Proceedings of the IEEE*, vol. 100, no. 7, pp. 2262–2270, 2012.

[13] S. Arshad, F. Zafar, R. Ramzan, and Q. Wahab, "Wideband and multiband CMOS LNAs: State-of-the-art and future prospects," *Microelectronics Journal*, vol. 44, no. 9, pp. 774–786, 2013.

[14] Y. Shen, H. Li, X. Chen, J. Liu, and H. Chen, "A 0.07-3GHz wideband front-end for SDR receiver with 2.3 dB NF and 12dbm IIP3 in 65nm CMOS," *IEICE Electronics Express*, pp. 16–23, 2019.

[15] R. A. Baki and M. N. El-Gamal, "RF CMOS fully-integrated heterodyne front-end receivers design technique for 5 GHz applications," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 1, 2004, pp. I–960.

[16] C.-C. Meng, T.-H. Wu, J.-S. Syu, S.-W. Yu, K.-C. Tsung, and Y.-H. Teng, "2.4/5.7-GHz CMOS dual-band low-IF architecture using weaver–hartley image-rejection techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 3, pp. 552–561, 2009.

[17] L. Der and B. Razavi, "A 2-GHz CMOS image-reject receiver with LMS calibration," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 167–175, 2003.

[18] A. Salleh, K. Yong, M. A. Aziz, M. H. Misran, and N. R. Mohamad, "Design of low power wideband low noise amplifier for software defined radio at 100MHz to 1GHz," *Procedia Engineering*, vol. 53, pp. 368–375, 2013.

[19] I. Madadi, M. Tohidian, K. Cornelissens, P. Vandenameele, and R. B. Staszewski, "A high IIP2 saw-less superheterodyne receiver with multistage harmonic rejection," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 332–347, 2016.

[20] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE Journal of solid-state circuits*, vol. 42, no. 5, pp. 954–966, 2007.

[21] A. Geis, J. Ryckaert, J. Borremans, G. Vandersteen, Y. Rolain, and J. Craninckx, "A compact low power SDR receiver with 0.5-20MHz baseband sampled filter," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*. IEEE, 2009, pp. 285–288.

[22] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1843–1853, 2016.

[23] A. Geis, Y. Rolain, G. Vandersteen, and J. Craninckx, "A 0.045 mm 2 0.1–6 GHz reconfigurable multi-band, multi-gain LNA for SDR," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2010, pp. 123–126.

[24] L. Wu, A. W. Ng, S. Zheng, H. F. Leung, Y. Chao, A. Li, and H. C. Luong, "A 0.9–5.8-GHz software-defined receiver RF front-end with transformer-based current-gain boosting and harmonic rejection calibration," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 8, pp. 2371–2382, 2017.

[25] X. Fan, H. Zhang, and E. Sánchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 588–599, 2008.

[26] K.-F. Cho and S. Wang, "A 0.4–5.3 GHz wideband LNA using resistive feedback topology," in *IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, 2016, pp. 1–2.

[27] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, "A DC-11.5 GHz low-power, wideband amplifier using splitting-load inductive peaking technique," *IEEE Microwave and wireless components letters*, vol. 18, no. 7, pp. 482–484, 2008.

[28] K. Mæland, K. G. Kjelgård, and T. S. Lande, "CMOS distributed amplifiers for UWB radar," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 1298–1301.

[29] R. Pierco, T. De Keulenaer, G. Torfs, and J. Bauwelinck, "Analysis and design of a high power, high gain SiGe BiCMOS output stage for use in a millimeter-wave power amplifier," in *10th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*, 2014, pp. 1–4.

[30] V. Singh, S. K. Arya, and M. Kumar, "G m-boosted current-reuse inductive-peaking common source LNA for 3.1–10.6 GHz UWB wireless applications in 32 nm CMOS," *Analog Integrated Circuits and Signal Processing*, pp. 1–13, 2018.

[31] S. Kundu and J. Paramesh, "A compact, supply-voltage scalable 45–66 GHz baseband-combining CMOS phased-array receiver," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 527–542, 2015.

[32] B. Afshar, Y. Wang, and A. M. Niknejad, "A robust 24mW 60GHz receiver in 90nm standard CMOS," in *IEEE International Solid-State Circuits Conference*, 2008, pp. 182–605.

[33] F. Belmas, F. Hameau, and J.-M. Fournier, "A 1.3 mW 20dB gain low power inductorless LNA with 4dB noise figure for 2.45 GHz ISM band," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011, pp. 1–4.

[34] M. De Souza, A. Mariano, and T. Taris, "Reconfigurable inductorless wideband CMOS LNA for wireless communications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2016.

[35] L. Ma, Z.-G. Wang, J. Xu, and N. M. Amin, "A high-linearity wideband common-gate LNA with a differential active inductor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 4, pp. 402–406, 2017.

[36] Z. Pan, C. Qin, Z. Ye, and Y. Wang, "A low power inductorless wideband LNA with g m enhancement and noise cancellation," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 58–60, 2017.

[37] B. Razavi, *RF microelectronics*. Prentice Hall New Jersey, 1998, vol. 2.

[38] A. Raffo and G. Crupi, *Microwave Wireless Communications: From Transistor to System Level*. Academic Press, 2016.

[39] M. Gamal, M. El-Nozahi, and H. El-Hennawy, "Concurrent dual-band LNA for automotive application," in *IEEE 58th Proc. of IEEE mWSCAS'15*, 2015, pp. 1–4.

[40] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 288–301, 2002.

[41] Y. Guan, Y. Wu, M. Li, W. Wang, and Y. Liu, "Generalised MIT in a tri-band LNA," *IET Microwaves, Antennas & Propagation*, vol. 11, no. 2, pp. 294–302, 2017.

[42] M.-L. Chuang, "Dual-band impedance transformer using two-section shunt stubs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1257–1263, 2010.

[43] C.-Y. Hsu, S.-C. Lin, and Z.-M. Tsai, "Quadband rectifier using resonant matching networks for enhanced harvesting capability," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 7, pp. 669–671, 2017.

[44] F. G. Silva, R. N. de Lima, R. C. S. Freire, and C. Plett, "A switchless multiband impedance matching technique based on multiresonant circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 7, pp. 417–421, 2013.

[45] N. Nallam and S. Chatterjee, "Multi-band frequency transformations, matching networks and amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 6, pp. 1635–1647, 2013.

[46] A. Aneja and X. J. Li, "A 1.2 and 2.4 GHz variable gain concurrent dual band low noise amplifier," in *IEEE Asia Pacific Microwave Conference (APMC)*, 2017, pp. 1258–1261.

[47] Y.-J. Hong, S.-F. Wang, P.-T. Chen, Y.-S. Hwang, and J.-J. Chen, "A concurrent dual-band 2.4/5.2 GHz low-noise amplifier using gain enhanced techniques," in *Proc. of APEMC'15*, 2015, pp. 231–234.

[48] J. Lee and C. Nguyen, "A concurrent tri-band low-noise amplifier with a novel tri-band load resonator employing feedback notches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4195–4208, 2013.

[49] Y.-T. Lin, T. Wang, and S.-S. Lu, "Fully integrated concurrent dual-band low noise amplifier with suspended inductors in SiGe 0.35 μm BiCMOS technology," *Electronics Letters*, vol. 44, no. 9, pp. 563–565, 2008.

[50] Ramya, T. Rama Rao, and R. Venkataraman, "Concurrent multi-band low-noise amplifier," *Journal of Circuits, Systems and Computers*, vol. 26, no. 06, p. 1750104, 2017.

[51] S. Sattar and T. Z. A. Zulkifli, "A 2.4/5.2-GHz concurrent dual-band CMOS low noise amplifier," *IEEE Access*, vol. 5, pp. 21 148–21 156, 2017.

[52] S.-S. Yoo and H.-J. Yoo, "A compact reconfigurable LNA for single path multistandard receiver," in *IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2007, pp. 461–464.

[53] T.-C. Chung, C.-W. Chen, O. T.-C. Chen, and R. Y. Tsen, "A multi-band RF front-end receiver for bluetooth, WCDMA, and GPS applications," in *IEEE 46th Midwest Symposium on Circuits and Systems*, vol. 3, 2003, pp. 1175–1178.

[54] R. Beare, C. Plett, and J. Rogers, "Highly reconfigurable single-ended low noise amplifier for software defined radio applications," in *IEEE 10th International New Circuits and Systems Conference (NEWCAS)*, 2012, pp. 549–552.

[55] X. J. Li and Y. P. Zhang, "Flipping the CMOS switch," *IEEE Microwave Magazine*, vol. 11, no. 1, pp. 86–96, 2010.

[56] X. Yu and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1236–1246, 2013.

[57] R. Malmqvist, C. Samuelsson, A. Gustafsson, P. Rantakari, S. Reyaz, T. Vähä-Heikkilä, A. Rydberg, J. Varis, D. Smith, and R. Baggen, "A K-band RF- MEMS-enabled reconfigurable and multifunctional low-noise amplifier hybrid circuit," *Active and Passive Electronic Components*, vol. 2011, 2011.

[58] A. Jajoo, L. Wang, and T. Mukherjee, "MEMS varactor enabled frequency-reconfigurable LNA and PA in the upper uhf band," in *IEEE MTT-S International Microwave Symposium Digest, 2009. MTT'09.*, 2009, pp. 1121–1124.

[59] J. Danson, C. Plett, and N. Tait, "Using MEMS capacitive switches in tunable RF amplifiers," *EURASIP Journal on Wireless Communications and Networking*, vol. 2006, no. 1, p. 016518, 2006.

[60] H. B. Kia, A. K. A'ain, I. Grout, and I. Kamisian, "A reconfigurable low-noise amplifier using a tunable active inductor for multistandard receivers," *Circuits, Systems, and Signal Processing*, vol. 32, no. 3, pp. 979–992, 2013.

[61] J. L. Brown and N. M. Neihart, "An analytical study of a magnetically tuned matching network," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012, pp. 1979–1982.

[62] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1054–1062, 2009.

[63] J. Manjula, P. S. Krishna, and D. Rubeena, "Design and performance analysis of active inductor based reconfigurable regulated cascode LNA for tunable RF front end," in *International Conference on Communication and Signal Processing (ICCSP)*, 2017, pp. 0222–0227.

[64] A. Slimane, M. T. Belaroussi, F. Haddad, S. Bourdel, and H. Barthélemy, "A reconfigurable inductor-less CMOS low noise amplifier for multi-standard applications," in *IEEE 10th International New Circuits and Systems Conference (NEWCAS)*, 2012, pp. 57–60.

[65] Y.-C. Yang, P.-W. Lee, H.-W. Chiu, Y.-S. Lin, G.-W. Huang, and S.-S. Lu, "Reconfigurable SiGe low-noise amplifiers with variable miller capacitance," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 12, pp. 2567–2577, 2006.

[66] A. A. Kumar, S. G. Singh, and A. Dutta, "Low power reconfigurable multi-mode LNA utilizing subthreshold bias and low-Q inductors," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 650–653.

[67] R. Singh, G. Slovin, M. Xu, T. Schlesinger, J. A. Bain, and J. Paramesh, "A reconfigurable dual-frequency narrowband CMOS LNA using phase-change RF switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4689–4702, 2017.

[68] N. Ahsan, A. Ouacha, J. Dabrowski, and C. Samuelsson, "Dual band tunable LNA for flexible RF front end," in *International Bhurban Conference on Applied Sciences & Technology*, 2007, pp. 19–22.

[69] J. Wilson and M. Ismail, "Input match and load tank digital calibration of an inductively degenerated CMOS LNA," *Integration, the VLSI Journal*, vol. 42, no. 1, pp. 3–9, 2009.

[70] Y.-C. Chen and C.-N. Kuo, "A 6-10-GHz ultra-wideband tunable LNA," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2005, pp. 5099–5102.

[71] K. W. Kobayashi, C. Campbell, C. Lee, J. Gallagher, J. Shust, and A. Botelho, "A reconfigurable S-/X-band gan cascode LNA MMIC," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2017, pp. 1–4.

[72] C.-T. Fu, C.-L. Ko, C.-N. Kuo, and Y.-Z. Juang, "A 2.4–5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 12, pp. 2754–2763, 2008.

[73] T. Yammouch, K. Okada, and K. Masu, "Physical modeling of MEMS variable inductor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 5, pp. 419–422, 2008.

[74] C.-R. Wu, H.-H. Hsieh, L.-S. Lai, and L.-H. Lu, "A 3–5 GHz frequency-tunable receiver frontend for multiband applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 9, pp. 638–640, 2008.

[75] S. Ray and M. M. Hella, "A 10 Gb/s inductorless AGC amplifier with 40 dB linear variable gain control in 0.13um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 440–456, 2016.

[76] F. D. Baumgratz, H. Li, S. Bampi, and C. E. Saavedra, "Wideband low noise variable gain amplifier," in *IEEE 28th Symposium on Integrated Circuits and Systems Design (SBCCI)*, 2015, pp. 1–6.

[77] F. D. Baumgratz, H. Li, F. Tavernier, S. Bampi, and C. E. Saavedra, "A 0.4–3.3 GHz low-noise variable gain amplifier with 35 dB tuning range, 4.9 dB nf, and 40 dbm IIP2," *Analog Integrated Circuits and Signal Processing*, vol. 94, no. 1, pp. 9–17, 2018.

[78] A. T. Phan and R. Farrell, "Reconfigurable multiband multimode LNA for LTE/GSM, WiMAX, and ieee 802.11. a/b/g/n," in *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2010, pp. 78–81.

[79] S. Popuri, V. S. R. Pasupureddi, and J. Sturm, "A tunable gain and tunable band active balun LNA for ieee 802.11 ac WLAN receivers," in *42nd European Solid-State Circuits Conference*, 2016, pp. 185–188.

[80] H. R. Sadr-MN, "A negative gyrator-c for purification of inductors in a differential lc-vco," *International Journal of Electronics Letters*, pp. 1–13, 2017.

[81] H. Eslahi, A. Jalali, S. Nateghi, and J. Mazloum, "A reconfigurable LNA with single switched input matching network for s-band (wimax/wlan) applications," *Microelectronics Journal*, vol. 46, no. 10, pp. 956–962, 2015.

[82] A. M. Gamal, H. N. Ahmed, and M. A. El-Kfafy, "A quad-band 0.9/1.8/2.45/3.5 GHz, multi-standard concurrent LNA using a dual-band impedance transformer," in *Proc. of IEEE APMC'15*, vol. 1, 2015, pp. 1–3.

[83] X. Yu and N. M. Neihart, "A 2–11 GHz reconfigurable multi-mode LNA in 0.13 μm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2012, pp. 475–478.

[84] B. Guo, J. Chen, and H. Jin, "A linearized common-gate low-noise amplifier using active cross-coupled feedback technique," *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 1, pp. 239–248, 2016.

[85] C.-C. Chen and Y.-C. Wang, "A 2.4/5.2/5.8 GHz triple-band common-gate cascode CMOS low-noise amplifier," *Circuits, Systems, and Signal Processing*, pp. 1–14, 2016.

[86] A. Slimane, F. Haddad, S. Bourdel, S. A. Tedjini-Baïliche, M. T. Belaroussi, T. Mohamed, and H. Barthélemy, "Compact inductorless CMOS low-noise amplifier for reconfigurable radio," *Electronics Letters*, vol. 50, no. 12, pp. 892–893, 2014.

[87] G. Adom-Bamfi and K. Entesari, "A multiband low noise amplifier with a switchable gm active shunt feedback for SDRs," in *IEEE Radio and Wireless Symposium (RWS)*, 2016, pp. 179–182.

[88] X. Liu, Z.-K. Wang, and Q.-X. Deng, "Design and fpga implementation of a reconfigurable 1024-channel channelization architecture for SDR application," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 7, pp. 2449–2461, 2016.

[89] M. Ibrahim and I. Galal, "Improved SDR frequency tuning algorithm for frequency hopping systems," *Etri Journal*, vol. 38, no. 3, pp. 455–462, 2016.

[90] V. Giannini, P. Nuzzo, C. Soens, K. Vengattaramane, J. Ryckaert, M. Goffioul, B. Debaillie, J. Borremans, J. Van Driessche, and J. Craninckx, "A 2-mm2 0.1–5 GHz software-defined radio receiver in 45-nm digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3486–3498, 2009.

[91] A. Aneja, X. J. Li, and B. E. Li, "Design of continuously tunable low noise amplifier for multiband radio," in *2017 Mediterranean Microwave Symposium (MMS)*, 2017, pp. 1–4.

[92] X. J. Li and Y.-P. Zhang, "CMOS low noise amplifier design for microwave and mmWave applications (invited review)," *Progress In Electromagnetics Research*, vol. 161, pp. 57–85, 2018.

[93] N. M. Neihart, J. Brown, and X. Yu, "A dual-band 2.45/6 GHz CMOS LNA utilizing a dual-resonant transformer-based matching network," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 8, pp. 1743–1751, 2012.

[94] A. W. Ng, S. Y. Zheng, H. Leung, Y. Chao, and H. C. Luong, "A 0.9 GHz–5.8 GHz SDR receiver front-end with transformer-based current-gain boosting and 81-dB 3rd-order-harmonic rejection ratio," in *Proceedings of ESSCIRC*, 2013, pp. 181–184.

[95] J. Lee and C. Nguyen, "A K-/Ka-band concurrent dual-band single-ended input to differential output low-noise amplifier employing a novel transformer feedback dual-band load," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2018.

[96] A. Aneja and X. J. Li, "Design and analysis of a continuously tunable low noise amplifier for software defined radio," *Sensors*, vol. 19, no. 6, p. 1273, 2019.

[97] L. Jiao, Y. Wu, Z. Zhuang, M. Li, and Y. Liu, "Multiband DC-block impedance transformer for extreme complex impedances," *Electronics Letters*, vol. 54, no. 2, pp. 105–107, 2017.

[98] C. Huynh, K. Kim, and C. Nguyen, "A new impedance-matching technique for dual-band RF circuits and antennas," in *Proc of IEEE ISAP & USNC/USRI NRC Meeting'15*, 2015, pp. 1398–1399.

[99] M. A. Maktoomi, M. S. Hashmi, and F. M. Ghannouchi, "Improving load range of dual-band impedance matching networks using load-healing concept," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 2, pp. 126–130, 2017.

[100] G. Wibisono and T. Firmansyah, "Concurrent multiband low noise amplifier with multisection impedance transformer," in *Asia-Pacific Microwave Conference Proceedings (APMC)*, 2012, pp. 914–916.

[101] P. Chen and K. Yang, "A novel T-type dual-band impedance transformer for frequency-relevant complex impedance load," in *Circuits, Devices and Systems (ICCDS), 2017 International Conference on*, 2017, pp. 59–62.

[102] C.-R. Wu and L.-H. Lu, "A 2.9-3.5-GHz tunable low-noise amplifier," in *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2006.

[103] M. A. Maktoomi, M. S. Hashmi, and F. M. Ghannouchi, "A T-section dual-band matching network for frequency-dependent complex loads incorporating coupled line with DC-block property suitable for dual-band transistor amplifiers," *Progress In Electromagnetics Research C*, vol. 54, pp. 75–84, 2014.

[104] J. Brown, "Design of a magnetically tunable low noise amplifier in 0.13 um CMOS technology," Thesis, 2012.

[105] H. Rezaei, E. Abiri, and M. R. Salehi, "Out-band interference rejection in UWB LNA receiver using coupled inductors in front end LNA," *Electrical and Electronic Engineering*, vol. 2, no. 4, pp. 177–182, 2012.

[106] J.-J. Wang, D.-Y. Chen, S.-F. Wang, and R.-S. Wei, "A multi-band low noise amplifier with wide-band interference rejection improvement," *AEU-International Journal of Electronics and Communications*, vol. 70, no. 3, pp. 320–325, 2016.

[107] W.-L. Chen, S.-F. Chang, G.-W. Huang, Y.-S. Jean, and T.-H. Yeh, "A ku-band interference-rejection CMOS low-noise amplifier using current-reused stacked common-gate topology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 10, pp. 718–720, 2007.

[108] H. Rezaei, E. Abiri, and M. Salehi, "Interference rejection in UWB LNA using front-end triode mosfet," in *IEEE International Conference on Electronics Design, Systems and Applications (ICEDSA)*, 2012, pp. 104–108.

[109] A. C. Ulusoy, M. Kaynak, T. Purtova, B. Tillack, and H. Schumacher, "A 60 to 77 GHz switchable LNA in an RF- MEMS embedded biCMOS technology," *IEEE Microwave and wireless components letters*, vol. 22, no. 8, pp. 430–432, 2012.

[110] A. Ulusoy, M. Kaynak, T. Purtova, B. Tillack, and H. Schumacher, "24 to 79 GHz frequency band reconfigurable LNA," *Electronics Letters*, vol. 48, no. 25, pp. 1598–1600, 2012.

[111] H. B. Kia, "Adaptive CMOS LNA using highly tunable active inductor," in *22nd Iranian Conference on Electrical Engineering (ICEE)*, 2014, pp. 1–6.

[112] Y.-S. Hwang, S.-F. Wang, and J.-J. Chen, "A differential multi-band CMOS low noise amplifier with noise cancellation and interference rejection," *AEU-International Journal of Electronics and Communications*, vol. 64, no. 10, pp. 897–903, 2010.

[113] E. A. Klumperink and B. Nauta, "Software defined radio receivers exploiting noise cancelling: a tutorial review," *IEEE communications magazine*, vol. 52, no. 10, pp. 111–117, 2014.

[114] Z. Li, L. Sun, and L. Huang, "0.4 mW wideband LNA with double g_m enhancement and feed-forward noise cancellation," *Electronics Letters*, vol. 50, no. 5, pp. 400–401, 2014.

[115] K.-A. Hsieh, H.-S. Wu, K.-H. Tsai, and C.-K. C. Tzuang, "A dual-band 10/24-GHz amplifier design incorporating dual-frequency complex load matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1649–1657, 2012.

[116] Z. Ke, S. Mou, K. Ma, and F. Meng, "A 0.7/1.1-dB ultra-low noise dual-band LNA based on SISL platform," *IEEE Transactions on Microwave Theory and Techniques*, no. 99, pp. 1–9, 2018.

[117] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly integrated and tunable RF front ends for reconfigurable multiband transceivers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 9, pp. 2038–2050, 2011.

[118] T. W. Kim, "A common-gate amplifier with transconductance nonlinearity cancellation and its high-frequency analysis using the volterra series," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 6, pp. 1461–1469, 2009.

[119] H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22–36, 2011.

[120] B. Guo, J. Chen, Y. Li, H. Jin, Y. Yang, and W. Chen, "A wideband common-gate LNA with enhanced linearity by using complementary mgtr technique," in *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016, pp. 1540–1542.

[121] M. Potrebić, D. Tošić, and A. Plazinić, "Reconfigurable multilayer dual-mode bandpass filter based on memristive switch," *AEU-International Journal of Electronics and Communications*, vol. 97, pp. 290–298, 2018.

[122] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with gm enhancement and noise-cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers, vol. PP*, no. 99, pp. 1–13, 2018.

[123] H. Darabi, P. Chang, H. Jensen, A. Zolfaghari, P. Lettieri, J. C. Leete, B. Mohammadi, J. Chiu, Q. Li, and S.-L. Chen, "A quad-band GSM/GPRS/EDGE SoC in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 870–882, 2011.

[124] P. Roblin, M. Rawat, and V. Ratnasamy, "RF front-end flexibility, self-calibration, and self-linearization: Characterizing and mitigating nonlinearities in SDR mimo systems for concurrent multiband operation," *IEEE Microwave Magazine*, vol. 19, no. 2, pp. 49–61, 2018.

[125] C.-T. Fu, C.-L. Ko, and C.-N. Kuo, "A 2.4 to 5.4 GHz low power CMOS reconfigurable LNA for multistandard wireless receiver," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2007*, 2007, pp. 65–68.

[126] M. T. Mustaffa, A. Zayegh, and T. Z. A. Zulkifli, "A reconfigurable LNA for multi-standard receiver using 0.18 μm CMOS technology," in *IEEE Student Conference on Research and Development (SCOReD)*, 2009, pp. 238–241.

[127] J. Lee and C. Nguyen, "A concurrent dual-band low-noise amplifier for K-and Ka-band applications in SiGe BiCMOS technology," in *Proc. of IEEE APMC'13*, 2013, pp. 258–260.

[128] J. Shen and X. Zhang, "Concurrent dual-band LNA for dual-system dual-band GNSS receiver," *Analog Integrated Circuits and Signal Processing*, vol. 78, no. 2, pp. 529–537, 2014.

[129] S. Datta, K. Datta, A. Dutta, and T. K. Bhattacharyya, "A concurrent low-area dual band 0.9/2.4 GHz LNA in 0.13 μm RF CMOS technology for multi-band wireless receiver," in *Proc. of IEEE APCCAS'10*, 2010, pp. 280–283.

[130] A. Zokaei and A. Amirabadi, "A dual-band common-gate LNA using active post distortion for mobile wimax," *Microelectronics Journal*, vol. 45, no. 7, pp. 921–929, 2014.

[131] O. H. Karabey, Y. Zheng, A. Gaebler, F. Goelden, and R. Jakoby, "A synthesis technique for multiband tunable impedance matching networks with optimized matching domain," in *2009 German Microwave Conference*, 2009, pp. 1–4.

[132] Y. Liu, "Synthesis techniques on multiband impedance matching networks for frequency-dependent complex loads," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 10, pp. 4507–4519, 2018.

[133] B. K. Chung, "Q-based design method for T network impedance matching," *Microelectronics journal*, vol. 37, no. 9, pp. 1007–1011, 2006.

[134] H.-K. Chen, Y.-S. Lin, and S.-S. Lu, "Analysis and design of a 1.6–28-GHz compact wideband LNA in 90-nm CMOS using a π-match input network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 8, pp. 2092–2104, 2010.

[135] Y.-S. Lin, C.-C. Wang, G.-L. Lee, and C.-C. Chen, "High-performance wideband low-noise amplifier using enhanced π-match input network," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 3, pp. 200–202, 2014.

[136] A. Ismail and A. A. Abidi, "A 3-10-GHz low-noise amplifier with wideband lc-ladder matching network," *IEEE Journal of solid-state circuits*, vol. 39, no. 12, pp. 2269–2277, 2004.

[137] B. Gowrish, K. Rawat, A. Basu, and S. K. Koul, "Broad-band matching network using band-pass filter with device parasitic absorption," in *82nd ARFTG Microwave Measurement Conference*, 2013, pp. 1–4.

[138] D. M. Pozar, "Microwave engineering," *Wiley*, 2012.

[139] C. A. Balanis, *Antenna theory: analysis and design*. John wiley & sons, 2016.

[140] T. Kaho, Y. Yamaguchi, T. Nakagawa, and S. Oshima, "Quad-band receiver front-end module using SiGe BiCMOS MMICs and ltcc triplexer," in *Proc of IEEE ISRFIT'15*, 2015, pp. 37–39.

[141] R. K. Barik, R. Siddiqui, K. P. Kumar, and S. Karthikeyan, "Design of a novel dual-band low noise amplifier incorporating dual-band impedance transformer," in *Proc. of IEEE SPCOM'16*, 2016, pp. 1–5.

[142] M. Amiri and M. Jalali, "A pseudo-concurrent multiband LNA using double tuned transformers," in *Proc. of 23rd ICEE'15*, 2015, pp. 1312–1315.

[143] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18-um muhboxm CMOS selective receiver front-end for UWB applications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1764–1771, 2006.

[144] C.-Y. Kao, Y.-T. Chiang, and J.-R. Yang, "A concurrent multi-band low-noise amplifier for wlan/wimax applications," in *Proc. of IEEE ICEIT'08*, 2008, pp. 514–517.

[145] G.-L. Ning, Z.-Y. Lei, L.-J. Zhang, R. Zou, and L. Shao, "Design of concurrent low-noise amplifier for multi-band applications," *Progress In Electromagnetics Research*, vol. 22, pp. 165–178, 2011.

[146] F. Akbar, M. Atarodi, and S. Saeedi, "Design method for a reconfigurable CMOS LNA with input tuning and active balun," *AEU-International Journal of Electronics and Communications*, vol. 69, no. 1, pp. 424–431, 2015.

[147] K. Kwon, S. Kim, and K. Y. Son, "A hybrid transformer-based CMOS duplexer with a single-ended notch-filtered LNA for highly integrated tunable RF front-ends," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 11, pp. 1032–1034, 2018.

[148] H. Hayashi and M. Mauraguchi, "An MMIC active phase shifter using a variable resonant circuit [and mesfets]," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 10, pp. 2021–2026, 1999.

[149] Z. Chen, X. Zhang, Z. Song, W. Jia, and B. Chi, "A 1.0–5.0 GHz tunable LNA with automatic frequency calibration in 65 nm CMOS," in *Radio-Frequency Integration Technology (RFIT), 2016 IEEE International Symposium on*, 2016, pp. 1–3.

[150] A. Kumar and N. P. Pathak, "Coupled stepped-impedance resonator (csir) based concurrent dual band filtering LNA for wireless applications," in *MTT-S International Microwave and RF Conference (IMaRC), 2015 IEEE*, 2015, pp. 262–265.

[151] T. Nesimoglu, "Design and analysis of frequency-tunable amplifiers using varactor diode topologies," *Circuits, Systems, and Signal Processing*, vol. 30, no. 4, pp. 705–720, 2011.

[152] Y. Itoh, W. Cao, T. Murata, and K. Sakurai, "An l-band gain and bandwidth tunable low-noise differential amplifier using varactor-tuned bias circuits and active loads," in *IEEE MTT-S International Microwave Symposium*, 2010, pp. 960–963.

[153] X. Xhafa and M. B. Yelten, "Design of a tunable LNA and its variability analysis through surrogate modeling," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, p. e2724, 2020.

[154] E. L. Tan, "A quasi-invariant single-parameter criterion for linear two-port unconditional stability," *IEEE microwave and wireless components letters*, vol. 14, no. 10, pp. 487–489, 2004.

[155] S. Sen, D. Banerjee, M. Verhelst, and A. Chatterjee, "A power-scalable channel-adaptive wireless receiver based on built-in orthogonally tunable LNA," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 5, pp. 946–957, 2012.

[156] S. Bagga, A. L. Mansano, W. A. Serdijn, J. R. Long, K. Van Hartingsveldt, and K. Philips, "A frequency-selective broadband low-noise amplifier with double-loop transformer feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1883–1891, 2014.

[157] J. Reinke, A. Jajoo, L. Wang, G. Fedder, and T. Mukherjee, "CMOS-MEMS variable capacitors with low parasitic capacitance for frequency-reconfigurable RF circuits," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*. IEEE, 2009, pp. 509–512.

[158] J. Sturm, S. Popuri, and X. Xiang, "A 65 nm CMOS resistive feedback noise canceling LNA with tunable bandpass from 4.6 to 5.8 GHz," *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 2, pp. 191–199, 2016.

Appendix A

Appendix 1

A.1 Derivation of $g_{m_{rf}}$ and$g_{m_{cr}}$

A.1.1 Derivation of $g_{m_{cr}}$

Figure A.1 (a) shows the small signal equivalent of a matched CRLNA. output voltage V_{out} is given as

$$V_{out} = -\left(g_m Z_0\right) V_{gs} \tag{A.1}$$

Applying KVL, the input Voltage v_{in} is derived as

$$V_{in} = I_{in} Z_0 + I_{in}\left(\frac{1}{j\omega C_{gs}}\right) + V_{gs} = I_{in}\frac{\left(Z_0 j\omega C_{gs} + 1\right)}{j\omega C_{gs}} + V_{gs} \tag{A.2}$$

But $V_{gs} = I_{in}/j\omega C_{gs}$, Therefore,

$$V_{in} = V_{gs}\left(2 + j\omega Z_0 C_{gs}\right) \tag{A.3}$$

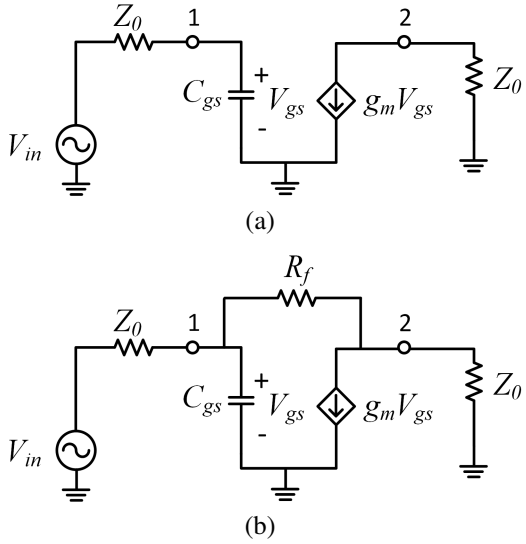


Figure A.1: Small signal equivalent of (a) CRLNA (b) RFLNA

The voltage gain A_v is given as

$$A_v = \left.\frac{V_{out}}{V_{in}}\right|_{Z_{in}=Z_0=Z_L} = \frac{-g_m Z_0}{2 + j\omega Z_0 C_{gs}} \tag{A.4}$$

Since the input impedance of CRLNA is matched to the source therefore,

$$Z_{in} = \frac{1}{j\omega C_{gs}} \tag{A.5}$$

From (A.4) and (A.5),

$$A_v = -\left.\frac{V_{out}}{V_{in}}\right|_{Z_{in}=Z_0=Z_L} = \frac{g_m Z_0}{2 + j\omega Z_0 C_{gs}} \tag{A.6}$$

or

$$g_m = \frac{2A_v}{Z_0} \tag{A.7}$$

A.1.2 Derivation of $g_{m_{rf}}$

Figure A.2 shows the small signal equivalent circuit of a conventional RFLNA. Considering the input impedance is matched and $Z_{in} = Z_0$, the input current I_{in} is given as

$$I_{in} = \frac{V_{in}}{Z_{in}} = \frac{V_{in}}{Z_0} \tag{A.8}$$

But current in R_f, $I_{R_f} = I_{in}$, Thus, $I_{R_f} = V_{in}/Z_0$.

Output current I_{out} is

$$I_{out} = \frac{V_{out}}{Z_0} = \frac{-V_{in}A_v}{Z_0} \tag{A.9}$$

Current in $1/g_m$ is $I_{g_m} = -g_m V_{in}$ Also,

$$I_{g_m} = I_{out} - I_{R_f} = \frac{-V_{in}(1 + A_v)}{Z_0} \tag{A.10}$$

From (A.9) and (A.10),

$$g_{m_{rf}} = \frac{1 + A_v}{Z_0} \tag{A.11}$$

Appendix B

Appendix 2

B.1 Derivation of noise figure of reconfigurable wide-band LNA

Current gain of a resistive feedback LNA is given as

$$i_o = g_m V_o = g_m \frac{v_{in}}{((R_s + R_b) \| R_{FB}) + \frac{1}{j\omega C_{be}}} \left(\frac{1}{j\omega C_{be}} \right) \tag{B.1}$$

$$i_o = \frac{g_m V_{in}}{\frac{1}{j\omega C_{be}} + \left(\frac{R_s R_{FB} + R_s R_{FB}}{R_s + R_b + R_{FB}} \right)} \left(\frac{1}{j\omega C_{be}} \right) \tag{B.2}$$

this can be re-written as

$$i_0 = G_m V_{in} \tag{B.3}$$

where

$$G_m = -j \frac{\omega_T}{\omega} \frac{1}{\frac{R_s R_{FB} + R_b R_{FB}}{R_s + R_b + R_{FB}}} \tag{B.4a}$$

and

$$\omega_T = \frac{g_m}{C_{be}} \tag{B.4b}$$

where ω_T is the unity current gain frequency. Total mean square noise current $\overline{i_{o,T}^2}$ is given as

$$\overline{i_{o,T}^2} = G_m^2 \left(\overline{V_b^2} + \overline{V_f^2} + \overline{V_{R_3}^2} + \overline{V_{g_m}^2} \right) + \overline{(i_c^2)} \tag{B.5}$$

where $\overline{(i_c^2)}$ is the mean source collector noise current. From equation (7.15) the noise factor F is given as

$$F = 1 + \frac{\overline{V_b^2}}{\overline{V_s^2}} + \frac{\overline{V_f^2}}{\overline{V_s^2}} + \frac{\overline{V_{R_3}^2}}{\overline{V_s^2}} + \frac{\overline{V_{1/g_m}^2}}{\overline{V_s^2}} + \frac{\overline{i_c^2}}{G_m^2 \overline{V_s^2}} \tag{B.6}$$

where $\overline{V_b^2}$, $\overline{V_f^2}$, $\overline{V_{R_3}^2}$, $\overline{V_{1/g_m}^2}$ and $\overline{V_s^2}$ are the mean squared noise voltages due to noise source from R_b, R_f, R_3, $(1/g_m)||R_L$ and R_s. Substituting various noise sources in (B.6) we get,

$$F = 1 + \frac{R_b + R_f + R_3}{R_s} + \frac{1}{R_s R_L g_m^2} + \frac{\overline{i_c^2}}{G_m^2 \overline{V_s^2}} \tag{B.7}$$

where $\left| \overline{i_c^2} \right| = 4kTg_m \left(\Delta f \right) \left(\gamma / \alpha \right)$; k is boltzmann constant, T is temperature and Δf is the bandwidth. Substituting equations (B.4a) and (7.7) in (B.7), we get

$$F = 1 + \frac{R_b + R_f + R_3}{R_s} + \frac{1}{R_s R_L g_m^2} + \frac{4\gamma g_m}{\alpha_M R_s} \left(\frac{\omega^2 C_{be}^2}{g_m^2} \right) \left(\frac{\frac{R_f + R_L}{1 + g_m R_L} \left(R_s + R_b \right)}{\left(R_s + R_b + \frac{R_f + R_L}{1 + g_m R_L} \right)} \right)^2 \tag{B.8}$$

Since $R_s \gg R_b$, solving (B.8), we get

$$F = 1 + \frac{R_f + R_b + R_3}{R_s} + \frac{1}{R_s R_L g_m^2} + \frac{4\gamma R_s}{\alpha_M g_m} \left(\frac{-1}{1 + \frac{R_s (1 + g_m R_L)}{R_f + R_L}} \right)^2 \tag{B.9}$$